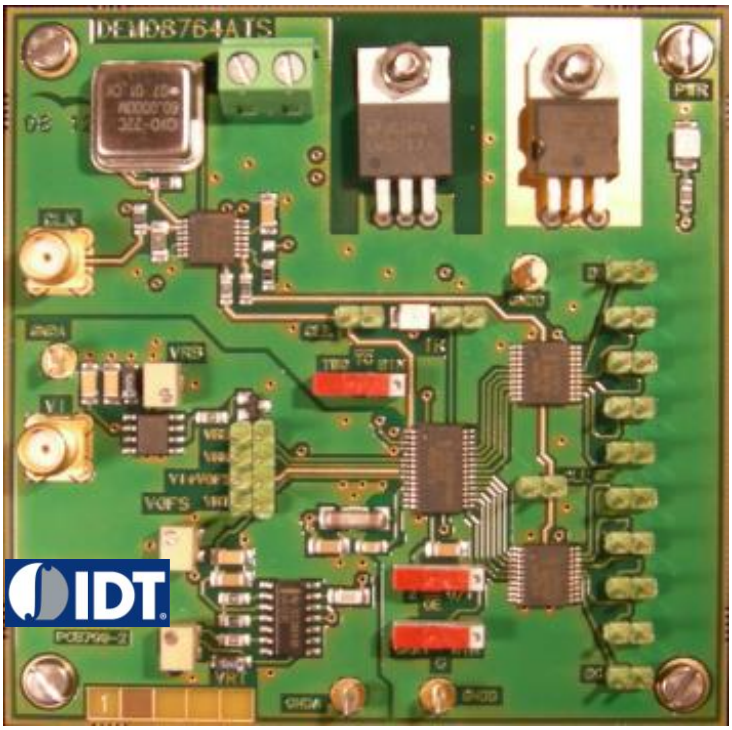
Quick Start

DEMO8764ATS Demonstration Board for ADC1005S060

Rev. 2.0 — 2 July 2012 **Quick Start**

Document information

Info	Content
Keywords	DEMO8764ATS, PCB709-2, Demonstration board, ADC, Converter, ADC1005S060
Abstract	This document describes how to use the demonstration board DEMO8764ATS for the analog-to-digital converter ADC1005S060.
Overview	

Revision history

Rev	Date	Description
2.0	20120702	Rebranded.
0.1	20080622	Initial version.

1. Quick start

1.1 Setup overview

Figure Fig 1 presents the connections to measure DEMO8764ATS.

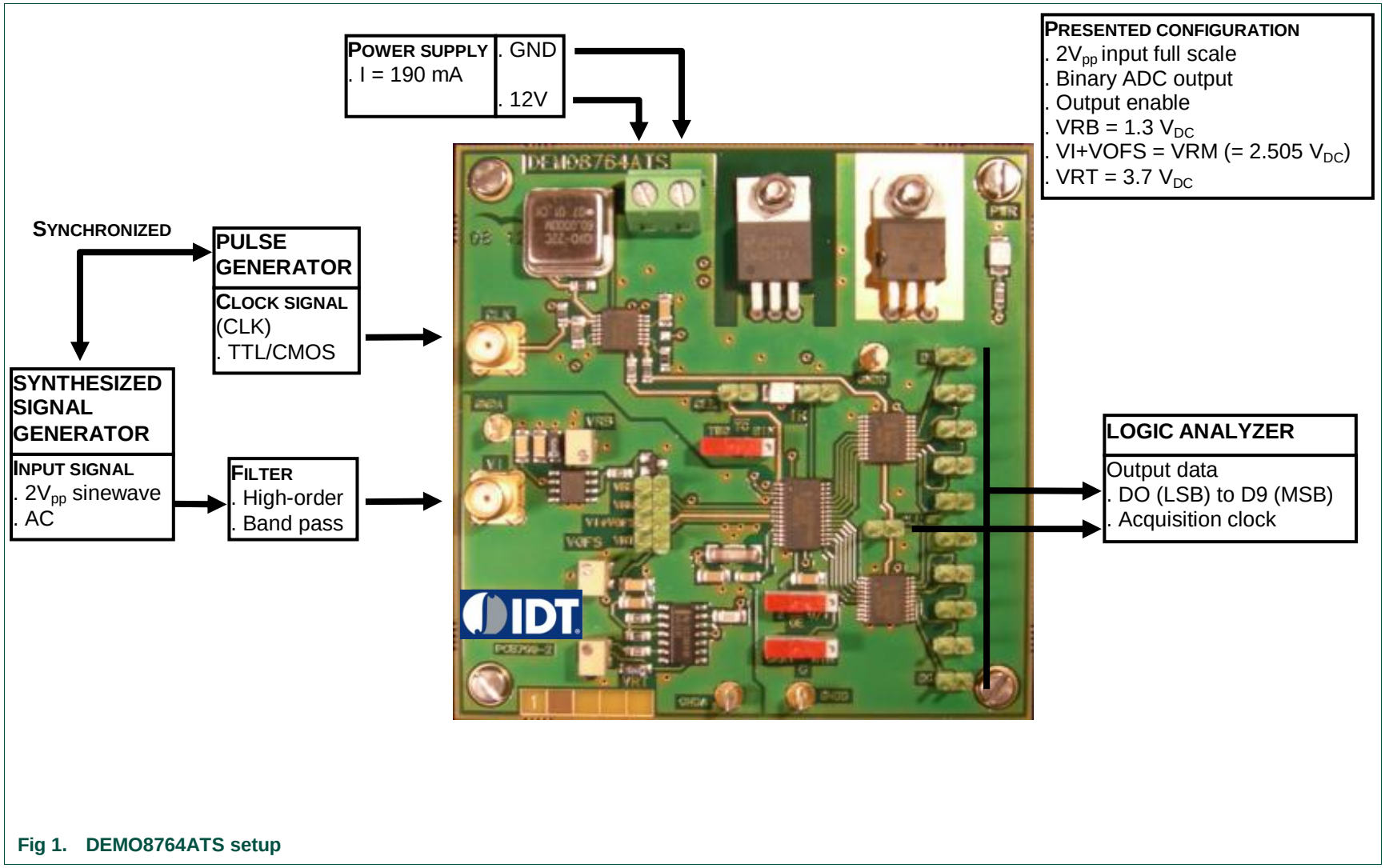
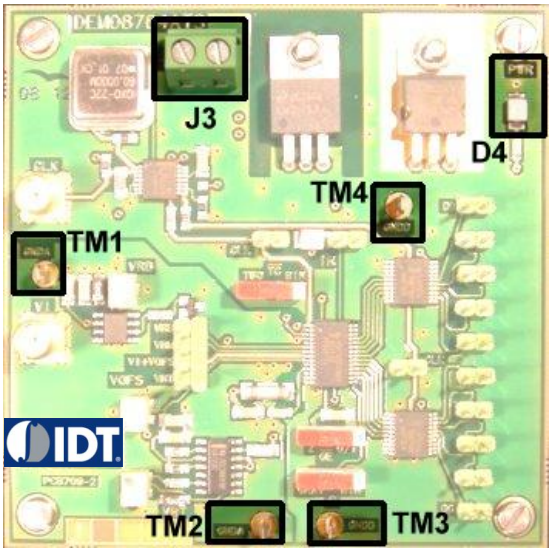


Fig 1. DEMO8764ATS setup

1.2 Power supply

The board is powered with a single 12 V_{DC} power supply. Two power supply regulators are used to supply all the 5V and 3.3V circuitry on the board.

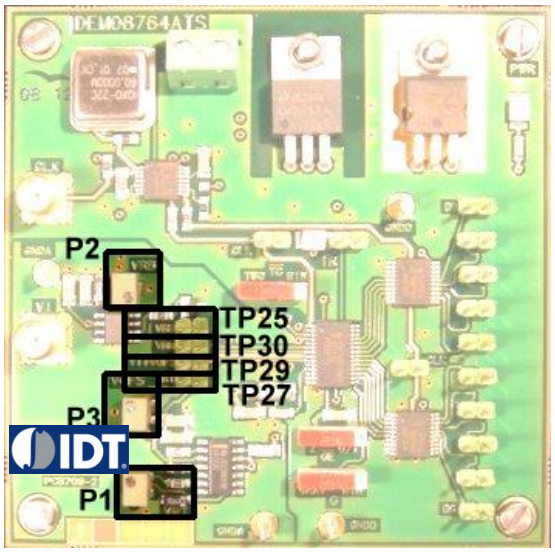
Table 1. General power supply

Name	Function	View
J3	Green connector – Power supply 12 V_{DC} / 190 mA.	
D4	PWR green light – It indicates the good supply plugging	
TM1, TM2	GNDA test point – Analog ground	
TM3, TM4	GNDD test point – Digital ground	

1.3 DC voltage adjustments

The ADC1005S060 allows to adjust the full scale input signal from 1.7 V to 2.5 V.

Table 2. DC voltage adjustments

Name	Function	View
P1	VRT trimmer – TOP reference adjustment	
TP27	VRT test point – TOP reference value (typ 3.7 V)	
P2	VRB trimmer – BOT reference adjustment	
TP25	VRB test point – BOT reference value (typ 1.3 V)	
P3	VOFS trimmer – Input signal DC offset adjustment	
TP29	VI+VOFS test point – Input signal DC offset (typ 2.505 V)	
TP30	VRM test point – MIDDLE reference value (typ 2.505 V)	

1.4 Input signals (VI, CLK)

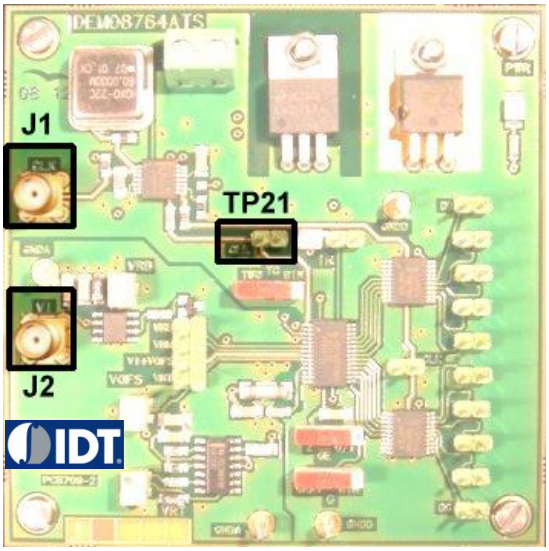
To ensure a good evaluation of the device, the input signal and the input clock must be synchronized together.

Moreover, the input frequency (Fi, MHz) and the clock frequency (Fclk, Msps) should follow the formula:

$$\frac{Fi}{Fclk} = \frac{M}{N}$$

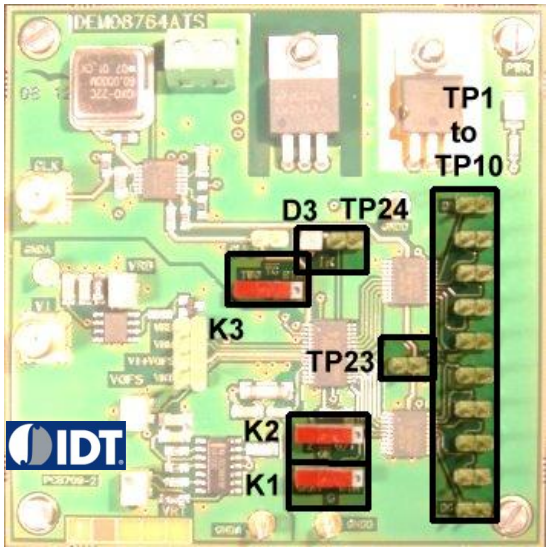
, where M is an odd number of period and N is the number of samples.

Table 3. Input signals

Name	Function	View
J2	VI connector – Analog input signal (50Ω matching)	
J1	CLK connector – Clock input signal (50Ω matching)	
TP21	CLK test point – Buffered clock signal for the IC . When J1 is open, the oscillator provides the clock. . When an external clock is provided on J1, the oscillator is off.	

1.5 Output signals (D0 to D9, IR)

Table 4. **Output signals**

Name	Function	View
TP1 to TP10	Array connector – ADC digital output (D0 to D9)	
D3, TP24	IR green light and test point – It indicates that the analog input signal is in the full scale range	
TP23	CLK connector – Clock output for data acquisition	
K1	G switch – Gray code selection  Binary  Gray	
K2	OEN switch – Output enable selection  Active output  High impedance output	
K3	TCN switch – 2's complement output selection  Binary  2's complement	

2. Example

2.1 Setup example

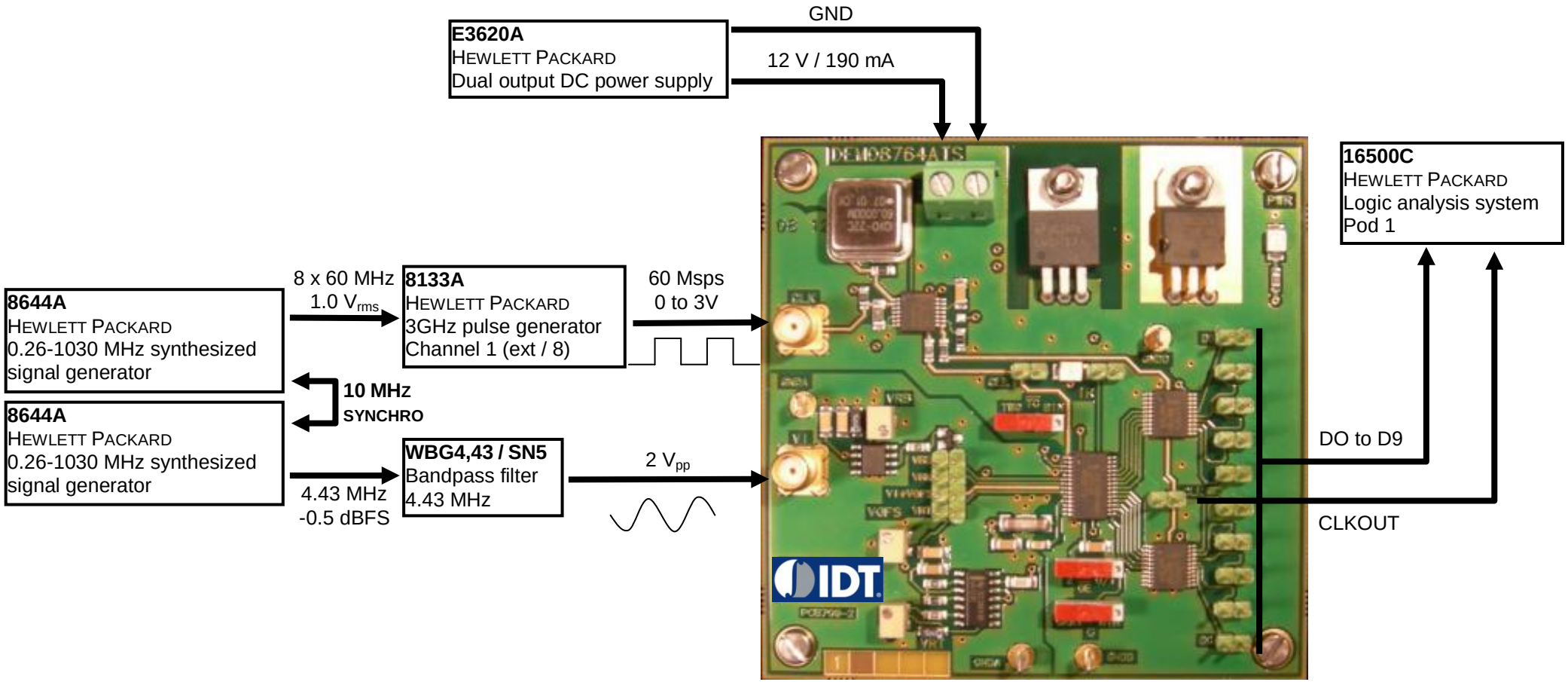


Fig 2. ADC1005S060 hardware setup