1. Introduction

The 9SQ440 Evaluation Board (EVB) is designed to help users evaluate the 9SQ440 PCIe Gen5 clock synthesizer. When the EVB is connected via USB to the user's computer running the Renesas 9SQ440 Timing Commander™ Software, the 9SQ440 can be configured to control frequencies with best-in-class performance. The 9SQ440 offers features of 7 pairs of 100MHz differential LP-HCSL outputs, 9 MXCLK pairs of differential outputs multiplexable between 100MHz/25MHz, and 3 pairs of 25MHz outputs. 9 selectable SMBus addresses available.
Board Overview

Figure 1. 9SQ440 EVB – Top View

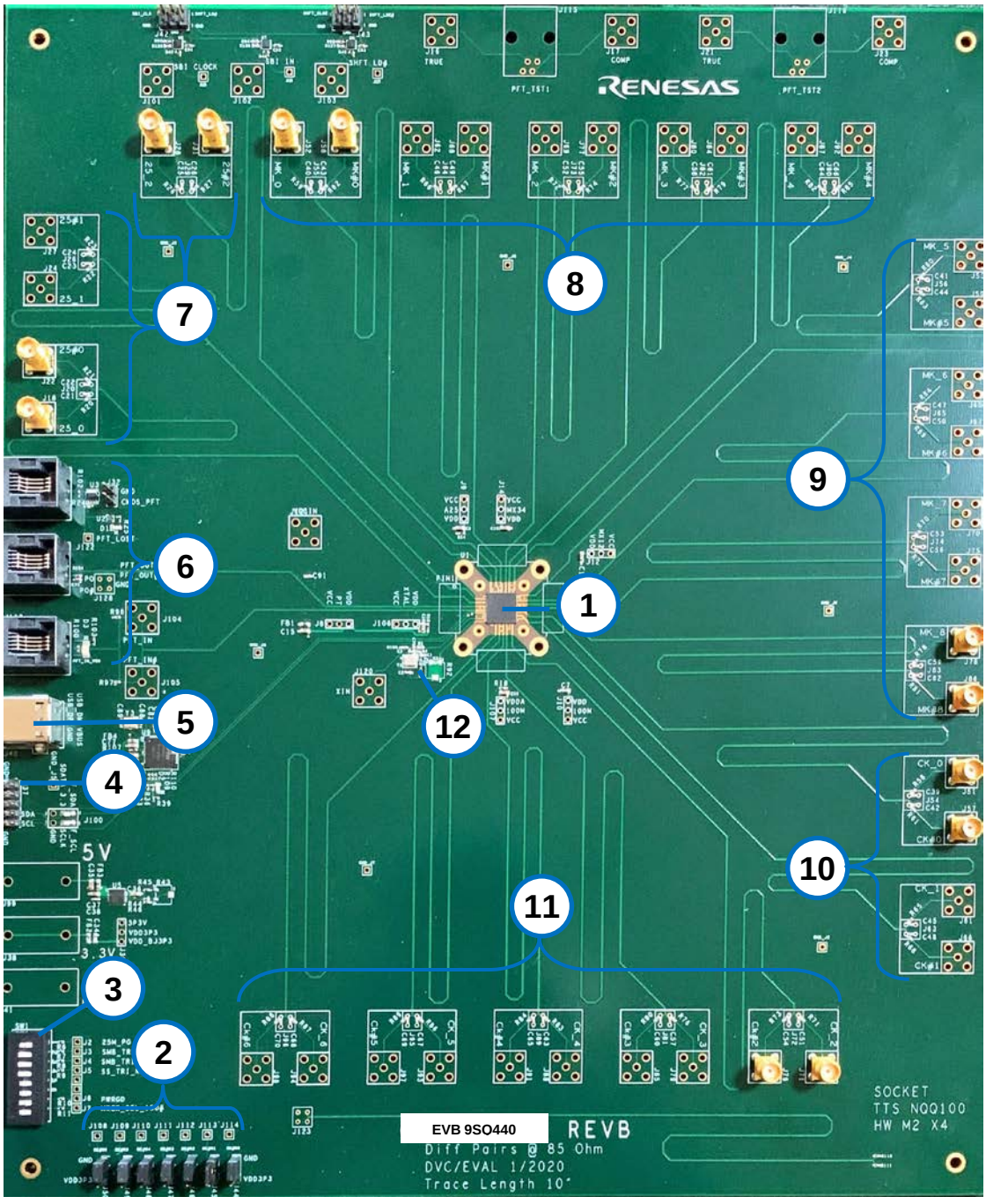

Table 1. 9SQ440 – EVB Pins and Functions

Note: See Figure 1 for reference numbers in the following table.

Ref.	Name	On-Board Connector Label	Function
1	9SQ440	U1	Evaluation device, 8 x 8 mm dual-row 100-pin QFN.
2	OE# Pins Control	J44, J45, J46, J47, J48, J49, J50	Hardware output enable/disable pins for 7 LP-HCSL 85Ω differential outputs. Active low on OE# pins for enabling 100M outputs. 1 = disable output; 0 = enable output.
3	DIP Switch	SW1	DIP switch device is used to setup 9SQ440 device condition. See Figure in below for detail.
4	SMBus Connector	J37	SMBus connector for SCLK and SDATA pins.
5	USB Interface	J40	USB type jack for connection with the user's computer and interaction with Renesas Timing Commander software.
6	RJ11 Connector	J117, J118, J119	RJ11 connectors for Platform Time input from another 9SQ440 clock synthesizer using ±0.7V 25MHz differential as input clock.
7	Test Points for 25M Outputs	J18, J22, J24, J27, J28, J31	SMA connectors for 25MHz differential outputs: J18, J22 for 25M0 (populated with a pairs of SMA connectors) J24, J27 for 25M1 J28, J31 for 25M2 (populated with a pairs of SMA connectors)
8	Test Points for MK Outputs	J52, J58, J62, J68, J69, J77, J80, J84, J87, J92	SMA connectors for MK differential outputs: J52, J58 for MK0 (populated with a pairs of SMA connectors) J62, J68 for MK1 J69, J77 for MK2 J80, J84 for MK3 J87, J92 for MK4
9	Test Points for MK Outputs	J53, J59, J60, J67, J70, J75, J78, J86	SMA connectors for MK differential outputs: J53, J59 for MK5 J60, J67 for MK6 J70, J75 for MK7 J78, J86 for MK8 (populated with a pairs of SMA connectors)
10	Test Points for CK Outputs	J51, J57, J61, J66	SMA connectors for CK differential outputs: J51, J57 for CK0 (populated with a pairs of SMA connectors) J61, J66 for CK1
11	Test Points for CK Outputs	J71, J76, J79, J85, J88, J91, J93, J97, J94, J98	SMA connectors for differential outputs: J71, J76 for CK2 (populated with a pairs of SMA connectors) J79, J85 for CK3 J88, J91 for CK4 J93, J97 for CK5 J94, J98 for CK6
12	Crystal	Y1	25MHz Quartz Crystal

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2. Power and SMBus Connection to a Computer

The evaluation board is connected to a computer via an USB connector. The USB connector is a type-B connector which provides +5V in the USB bus powers the on-board regulators for 3.3V voltage to the entire evaluation board. An on-board USB-to-I2C bridge (FTDI chip) is to handle the data communication between the evaluation board and a computer for a 9SQ440 software (called Timing commander Software). The board can fully function with just the USB cable with a computer.

The evaluation board could also be powered from VDD/GND jacks which is not populated as an option.

Board Power Supply

To power the board, use a USB type-B cable to connect the board with a computer on a USB port.

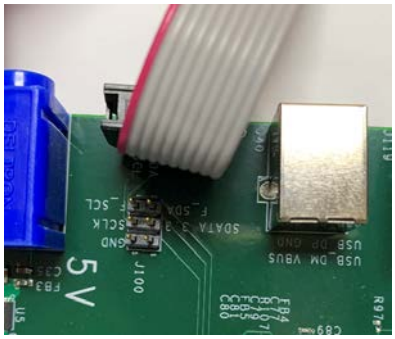
Figure 2. Power Source from USB Connector

Software Connection

Renesas Timing Commander Software can control the 9SQ440 on the board. Timing Commander is compatible using the USB connector or an Aardvark adapter as optional. Timing Commander displays a block diagram for entering the configuration and allows control features into the 9QS440 on the board.

The Bus Source connector J37 can be used to select the source of the communication bus. The bus will be SMBus for most communication. Pins 1 and 2 in J37 are SCL and SDA pins for an Aardvark connector. See Figure 3.

Figure 3. Connect Aardvark Adapter to J37

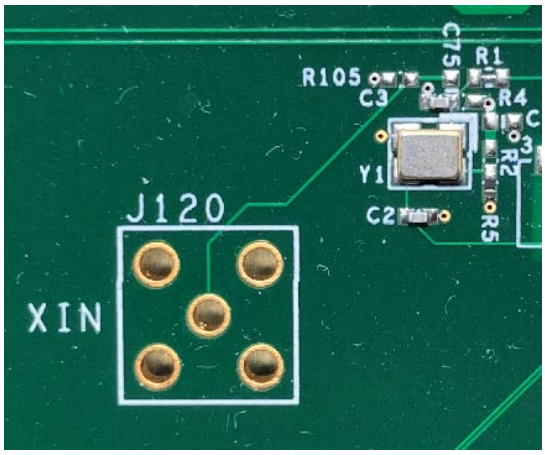


In Figure 3, the Aardvark Adapter communicates with the 9SQ440 part.

3. On-Board Crystal

The evaluation board is assembled with a 25MHz crystal populated on Y1 using 3.2 x 2.5 mm size footprint crystal.

Figure 4. Crystal and XIN Input



The XIN input (J120) can be used to overdrive the XIN pin with an external clock but is not assembled with SMA connector. The board is assembled with a 25MHz crystal as default; coupling capacitor C75 is not assembled.

4. Platform Time Connectors

The 9SQ440 offers 25MHz differential outputs for platform time clock. The 25MHz frequency can be used to communicate to another 9SQ440 device, keeping the 25MHz frequency the same on all devices. This feature ensures the CPU time stamp counter (TSC) is the same on all devices with the frequency lock. The evaluation board has two RJ11 connectors available to evaluate 25MHz for platform time clock. For PFT_IN/PFT_OUT function description, refer to the 9SQ440 datasheet for more information.

Figure 5. RJ11 (J119) Connector for PFT_IN

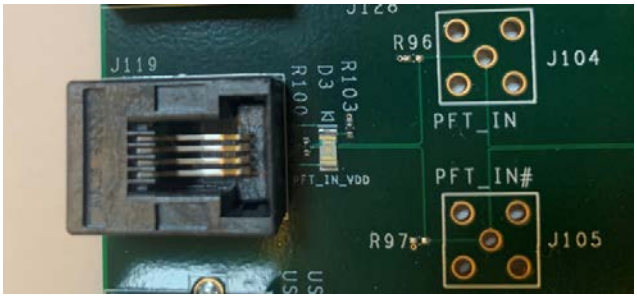
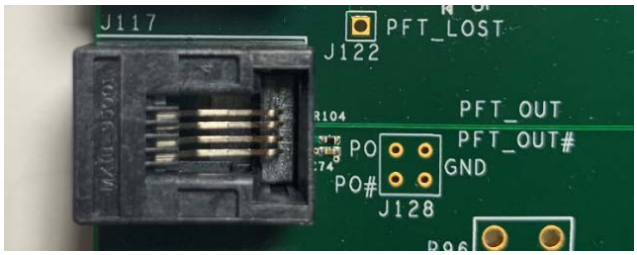
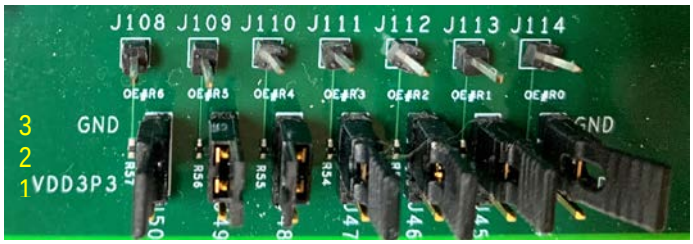


Figure 6. RJ11 (J117) Connector for PFT_OUT



5. Miscellaneous Selectors

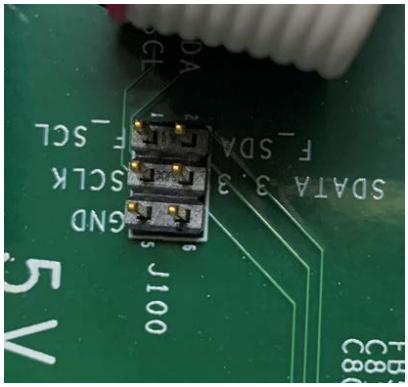
Figure 7. Output OE Pin Control



The 9SQ440 has two methods for enabling and disabling outputs. The evaluation board offers 7 OE# pins for 9SQ440 in hardware control. There are 3 positions using a jumper to apply either 3-2 on OE# pin to pull-low as output enable, or 2-1 on OE# pin to pull-high as output disable. The list in below summarized the outputs can be controlled by those 7 OE# pins.

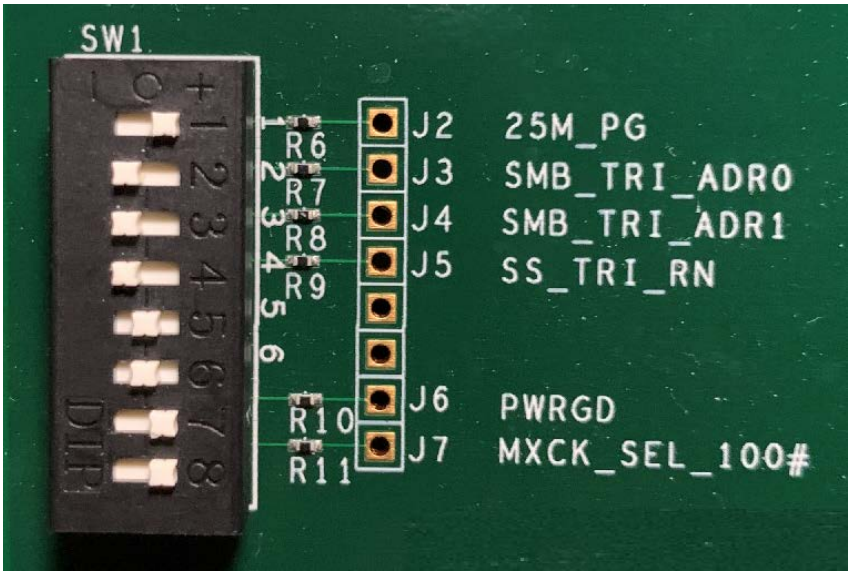
- OE#0 on J44 for 100M0 output
- OE#1 on J45 for 100M1 output
- OE#2 on J46 for 100M2 output
- OE#3 on J47 for 100M3 output
- OE#4 on J48 for 100M4 output
- OE#5 on J49 for 100M5 output
- OE#6 on J50 for 100M6 output

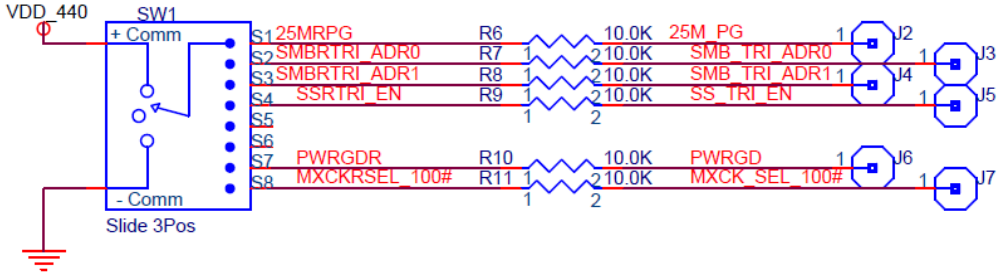
Figure 8. Headers for SCL and SDA Pins



J100 provides headers as another option which can be used to connect with SCL and SDA pins with an Aardvark Adapter.

Figure 9. DIP Switch Control





The DIP switch (SW1) connects to pins on the 9SQ440 devices. The middle position leaves the pin open. This is the default for each switch. Move to the "+" side to pull the pin high and move to the "-" side to pull the pin low.

- Switch 1 = 25M_PG: Connects to the 25MPG pin for 25MHz outputs enable in shut-down operation. Set to High as default on evaluation board
- Switch 2 = SMB_TRI_ADR0: Connects to the SMB_ADR0_tri pin. Set as Low to be default on evaluation board
- Switch 3 = SMB_TRI_ADR1: Connects to the SMB_ADR1_tri pin. Set as Low to be default on evaluation board

The main purpose of Switch 2 and Switch3 is to set SMBus addresses for 9SQ440 based on Table 2 below. The evaluation board has set SMBus address to be D2.

Table 2. SMBus Address Selection

SMB_ADR1_tri	SMB_ADR0_tri	SMBus Address
L	L	D2
L	M	D4
L	H	D6
M	L	B2
M	M	B4
M	H	B6
H	L	BA
H	M	BC
H	H	BE

- Switch 4 = SS_TRI_RN: Connects to the SS_tri_En pin. The main purpose of this switch is to control spread modulation on 100MHz outputs to be enabled as pull-up or disabled as pull-low.
- Switch 5 = No Connect.
- Switch 6 = No Connect.
- Switch 7 = PWRGDR: Connects to the PWRGD pin. The main purpose of this switch is to set 9SQ440 operated in a normal operational mode as this switch to set High or in power-down mode as this switch to set Low. Set as High to be default on evaluation board.
- Switch 8 = MXCK_SEL_100#: Connects to the MXCK_SEL_100# pin. The main purpose of this switch is to control MXCK outputs to run either 100MHz or 25MHz. Pull-low for the outputs to be running at 25MHz. Pull-high for the outputs to be running at 100MHz. The default setting of this switch is to be High for 100MHz on the outputs.

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6. Board Schematics

Figure 10. 9SQ440 Evaluation Board Schematics – Page 1

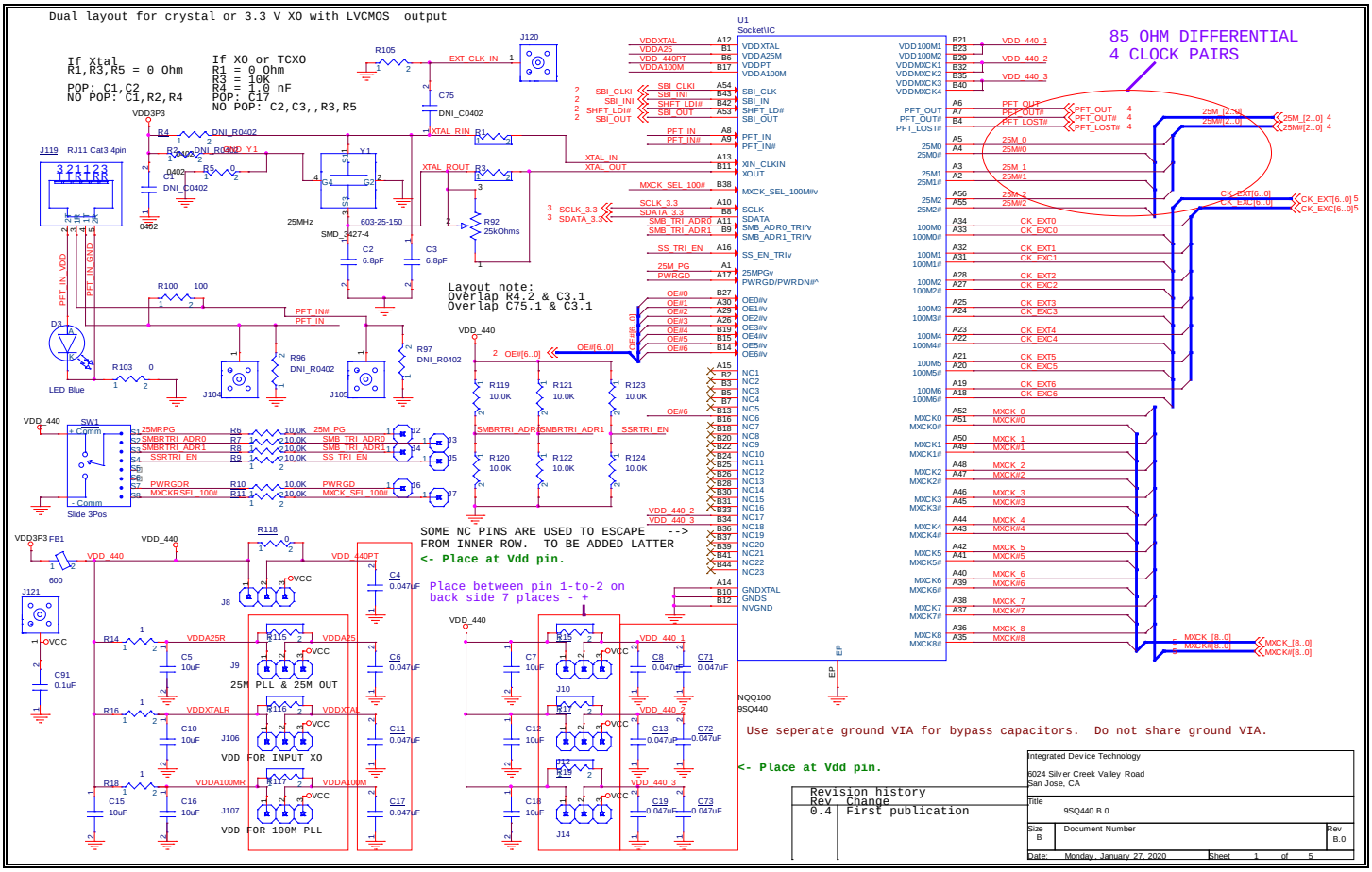


Figure 11. 9SQ440 Evaluation Board Schematics – Page 2

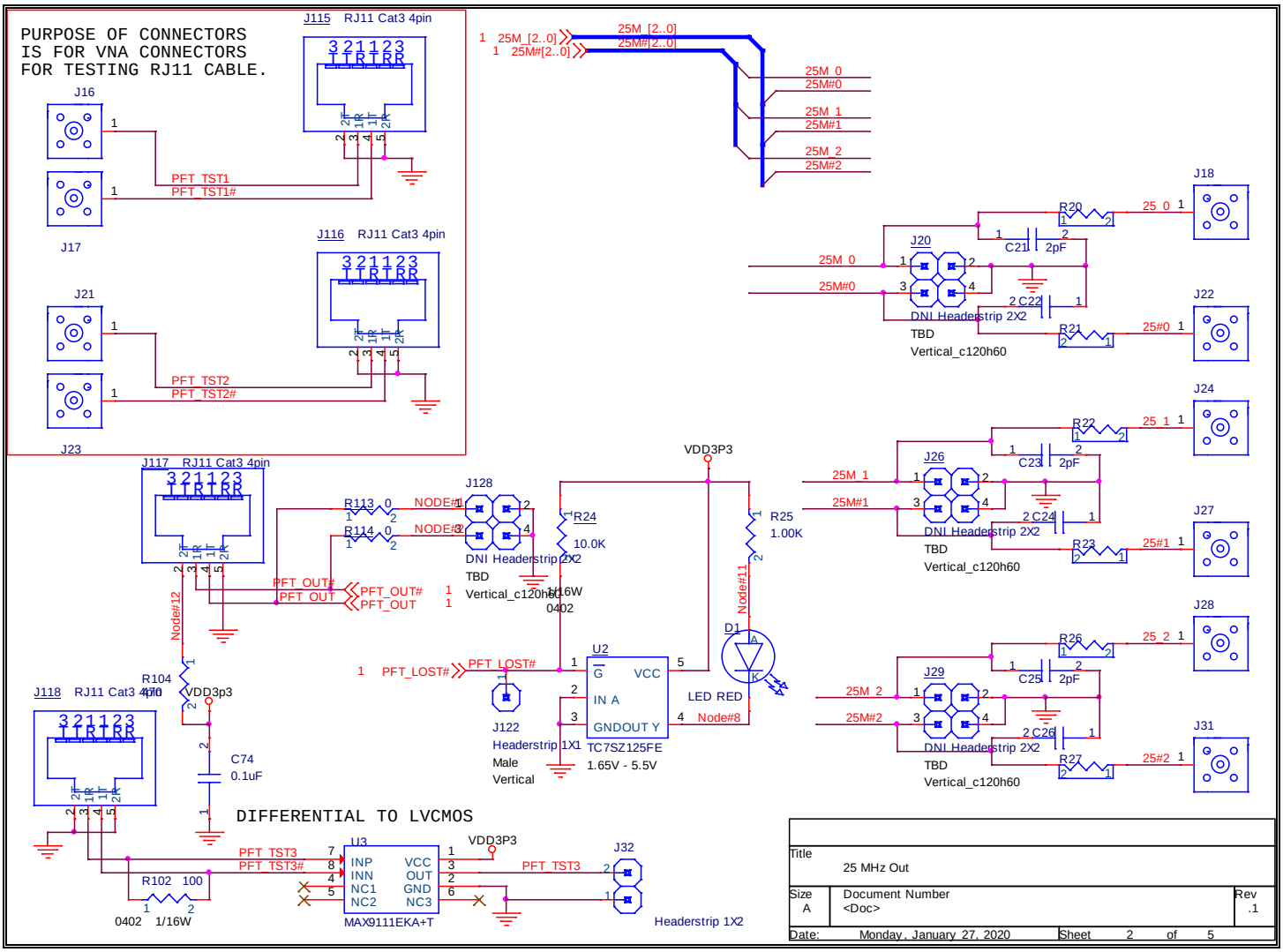


Figure 12. 9SQ440 Evaluation Board Schematics – Page 3

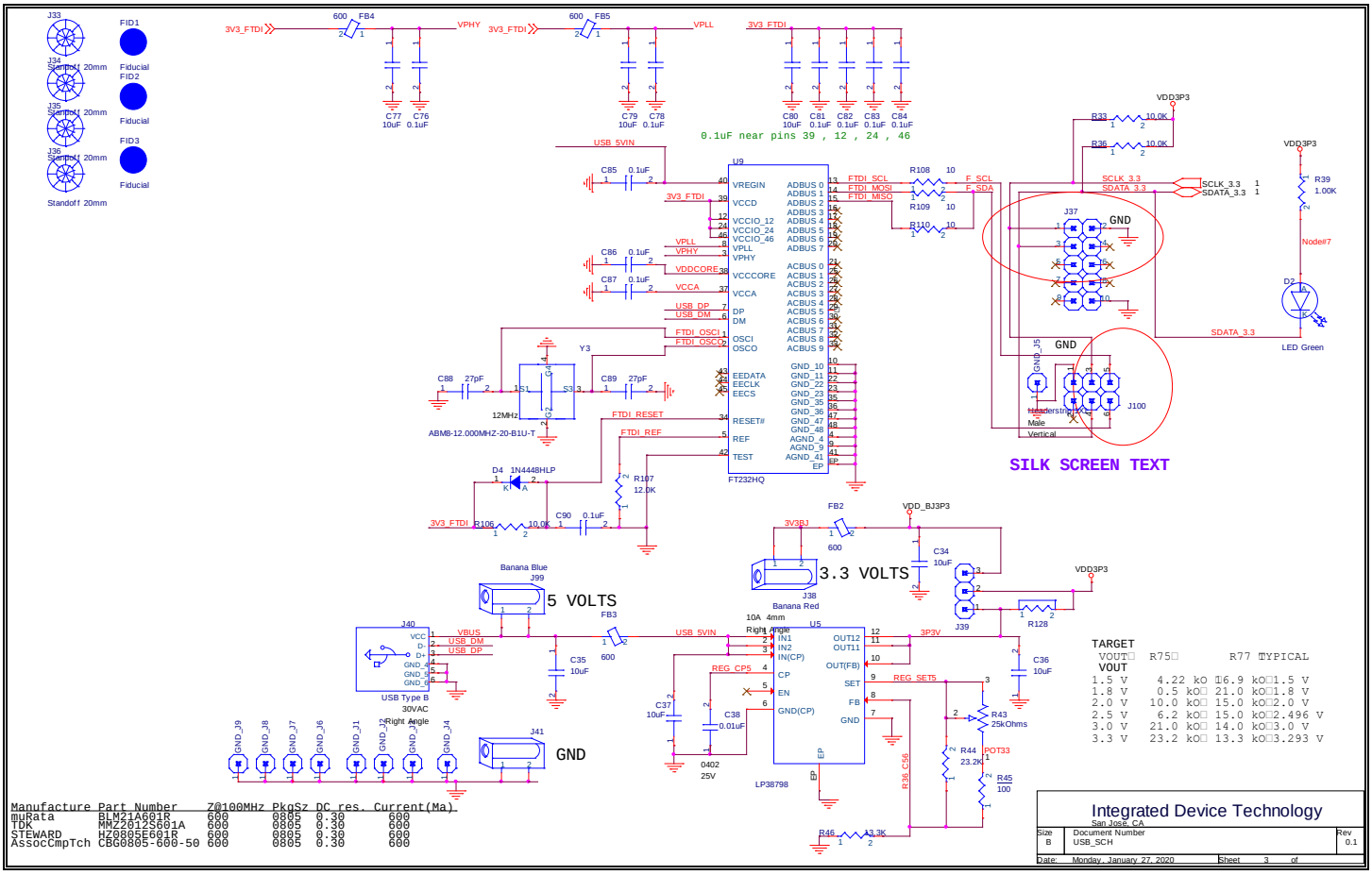


Figure 13. 9SQ440 Evaluation Board Schematics – Page 4

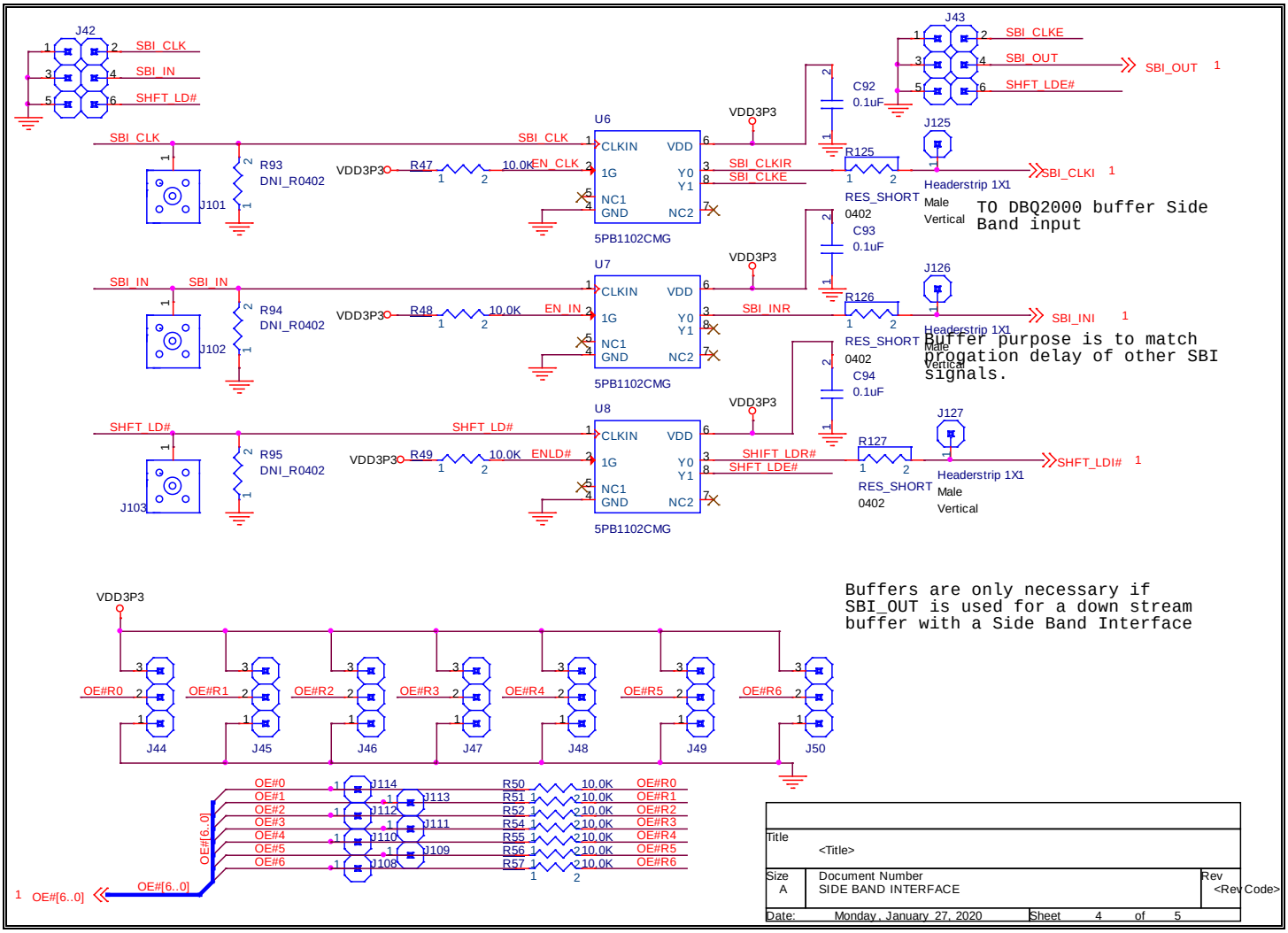
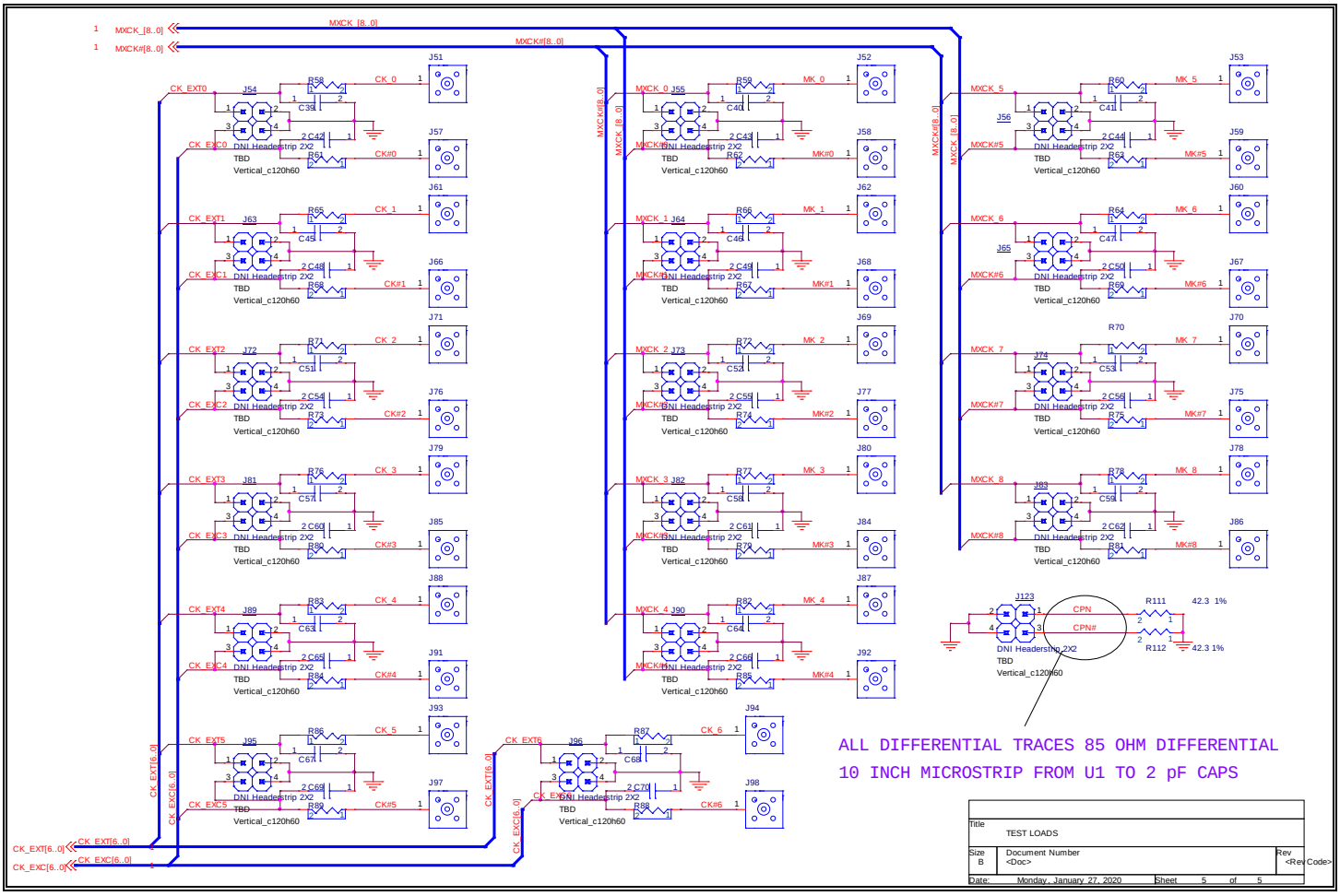


Figure 14. 9SQ440 Evaluation Board Schematics – Page 5



7. Ordering Information

Orderable Part Number	Description
9SQ440-EVB	9SQ440 Evaluation Board.

8. Revision History

Revision Date	Description of Change
May 19, 2020	▪ Rebranded document. ▪ Minor formatting/edits performed.
April 09, 2020	Updated schematic to RevB.
February 09, 2020	Initial release.

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