IDT™ 89EBPES16T4-2 Evaluation Board Manual

(Eval Board: 18-633-000)

May 2007

6024 Silver Creek Valley Road, San Jose, California 95138
Telephone: (800) 345-7015 • (408) 284-8200 • FAX: (408) 284-2775
Printed in U.S.A.

DISCLAIMER

Integrated Device Technology, Inc. reserves the right to make changes to its products or specifications at any time, without notice, in order to improve design or performance and to supply the best possible product. IDT does not assume any responsibility for use of any circuitry described other than the circuitry embodied in an IDT product. The Company makes no representations that circuitry described herein is free from patent infringement or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent, patent rights or other rights, of Integrated Device Technology, Inc.

Boards that fail to function should be returned to IDT for replacement. Credit will not be given for the failed boards nor will a Failure Analysis be performed.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any components of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Table of Contents

Notes

Notes

List of Tables

Notes

Notes

List of Figures

Notes

Notes

Description of the EB16T4-2 Eval Board

Notes

Introduction

The 89HPES16T4 switch (also referred to as PES16T4 in this manual) is a member of the IDT PCI Express® standard (PCIe®) based line of products. It is a 4-port switch, with 4 serial lanes per port. One upstream port is provided for connecting to the root complex (RC), and up to three downstream ports are available for connecting to PCIe endpoints or to another switch. More information on this device can be found in the 89HPES16T4 User Manual.

The 89EBPES16T4-2 Evaluation Board (also referred to as EB16T4-2 in this manual) provides an evaluation platform for the PES16T4 switch. It is also a cost effective way to add a PCIe downstream port (x4) to an existing system with a limited number of PCIe downstream ports. The EB16T4-2 eval board is designed to function as an add-on card to be plugged into a x8 PCIe slot available on a motherboard hosting an appropriate root complex, microprocessor(s), and two downstream ports. The EB16T4-2 is a vehicle to test and evaluate the functionality of the PES16T4 chip. Customers can use this board to get a headstart on software development prior to the arrival of their own hardware. The EB16T4-2 is also used by IDT to reproduce system-level hardware or software issues reported by customers. Figure 1.1 illustrates the functional block diagram representing the main parts of the EB16T4-2 board.

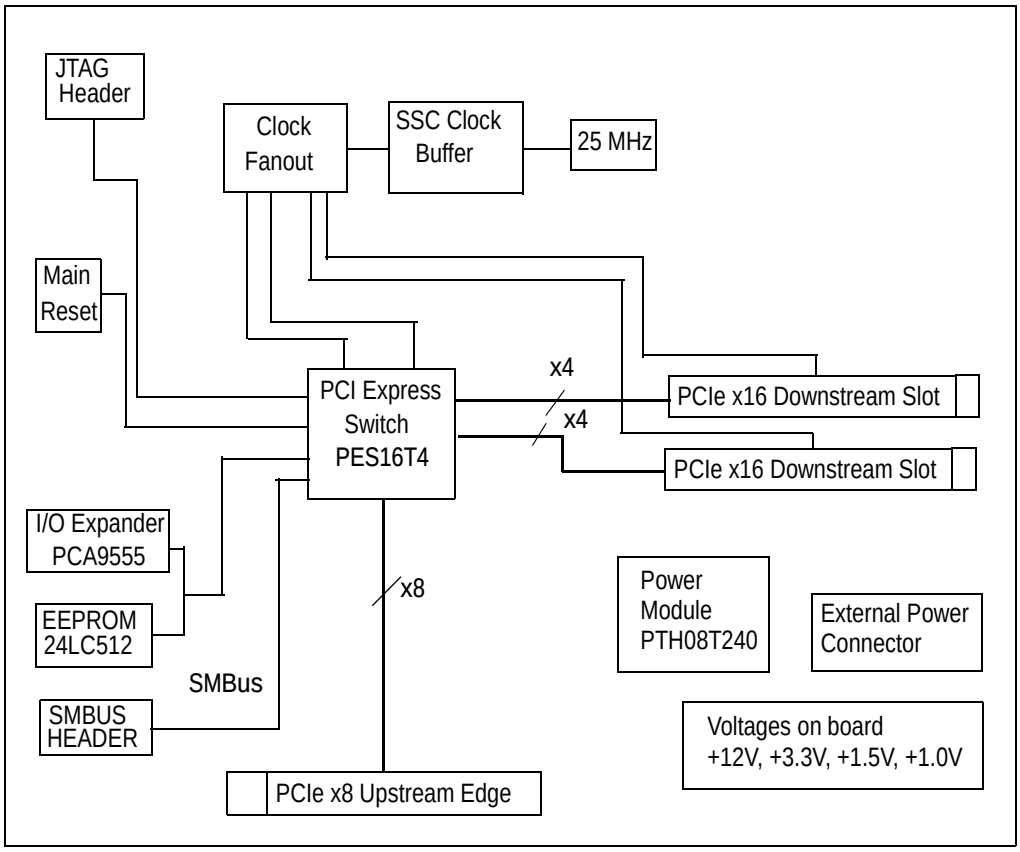


Figure 1.1 Function Block Diagram of the EB16T4-2 Eval Board

Notes

Board Features

Hardware

- PES16T4 PCIe 4 port switch
  - *Two x4 ports and one x8 port, 16 PCIe lanes*
  - *PCIe Base Specification Revision 1.1 compliant*
  - *6 GBps (48Gbps) aggregate switching capacity*
  - *Up to 2048 byte maximum Payload Size*
  - *Automatic lane reversal and polarity inversion supported on all lanes*
  - *Automatic per port link width negotiation to x4, x2, x1*
  - *Load configuration from an optional serial EEPROM via SMBUS*
- Upstream, Downstream Port
  - *One edge connector on the upstream port, to be plugged into a slot with at least x8 capable on a host motherboard*
  - *Two slot connectors on the downstream ports, for PCIe endpoint add-on cards to be plugged in. These slot connectors are x16 mechanically but electronically connected as x4 only.*
- Numerous user selectable configurations set using onboard jumpers and DIP-switches
  - *Source of clock - host clock or onboard clock generator*
  - *Two clock rates and spread spectrum settings*
  - *Boot mode selection*
- SMBUS Slave Interface (4 pin header)
- SMBUS Master Interface connected to the Serial EEPROMs through I/O expander
- “Attention” button for each downstream port to initiate a hot swap event on each port
- Four pin connector for optional external power supply
- Push button for Warm Reset
- Several LEDs to display status, reset, power, “Attention”, etc.
- One 10-pin JTAG connector (pitch 2.54 mm x 2.54 mm)

Software

There is no software or firmware executed on the board. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the PES16T4 within host systems running popular operating systems.

- Installation programs
  - *Operating Systems Supported: Windows2000, WindowsXP, Linux*
- GUI based application for Windows and Linux
  - *Allows users to view and modify registers in the PES16T4*
  - *Binary file generator for programming the serial EEPROMs attached to the SMBUS.*

Other

- A metal bracket is required to firmly hold in place two endpoints plugged into the EB16T4-2 board.
- An external power supply may be required under some conditions.
- SMBUS cable may be required for certain evaluation exercises.
- SMA connectors are provided on the EB16T4-2 board for specific test points.

Revision History

May 9, 2007: Initial publication of board manual.

Installation of the EB16T4-2 Eval Board

Notes

EB16T4-2 Installation

This chapter discusses the steps required to configure and install the EB16T4-2 evaluation board. All available DIP switches and jumper configurations are explained in detail.

The primary installation steps are:

1. Configure jumper/switch options suitable for the evaluation or application requirements.
2. Connect PCI Express endpoint cards to the downstream port PCIe slots on the evaluation board.
3. Insert the evaluation board into the host system (motherboard with root complex chipset).
4. Apply power to the host system.

The EB16T4-2 board is shipped with all jumpers and switches configured to their default settings. In most cases, the board does not require further modification or setup.

Hardware Description

The PES16T4 is a 16-lane, 4-port PCI Express® switch. It is a peripheral chip that performs PCI Express based switching with a feature set optimized for high performance applications such as servers and storage. It provides fan-out and switching functions between a PCI Express upstream port and 2 downstream ports or peer-to-peer switching between downstream ports.

The EB16T4-2 has two PCI Express downstream ports, accessible through four x16 connectors. Both ports are capable of negotiating a x1, x2, or x4 link width. All endpoint cards connected to the PES16T4 must support at least one of these link widths.

Basic requirements for the board to run are:

- Host system with a PCI Express root complex supporting x8 configuration through a PCI Express x8 slot. (If your host system does not offer a x8 slot, please contact ssdhelp@idt.com for alternative solutions.)
- x1, x2, or x4 PCI Express Endpoint Cards.

Host System

The evaluation board cannot be operated as a standalone unit. A host system implementing a PCI Express root complex supporting x8 configuration through a PCI Express x8 slot is required to take full advantage of the PES16T4's capabilities. One such system is the SuperMicro X6DH8-G2 motherboard equipped with an Intel E7520 chipset which was introduced in 2004 to deploy dual-processor server chipset technology. The board has three PCI Express slots. All slots have x8 connectors, but only two are electronically connected for a x8 link width (J15 and J16). The remaining slots are electronically connected for a x4 link width configuration. Figure 2.1 shows the proper connectors.

Notes

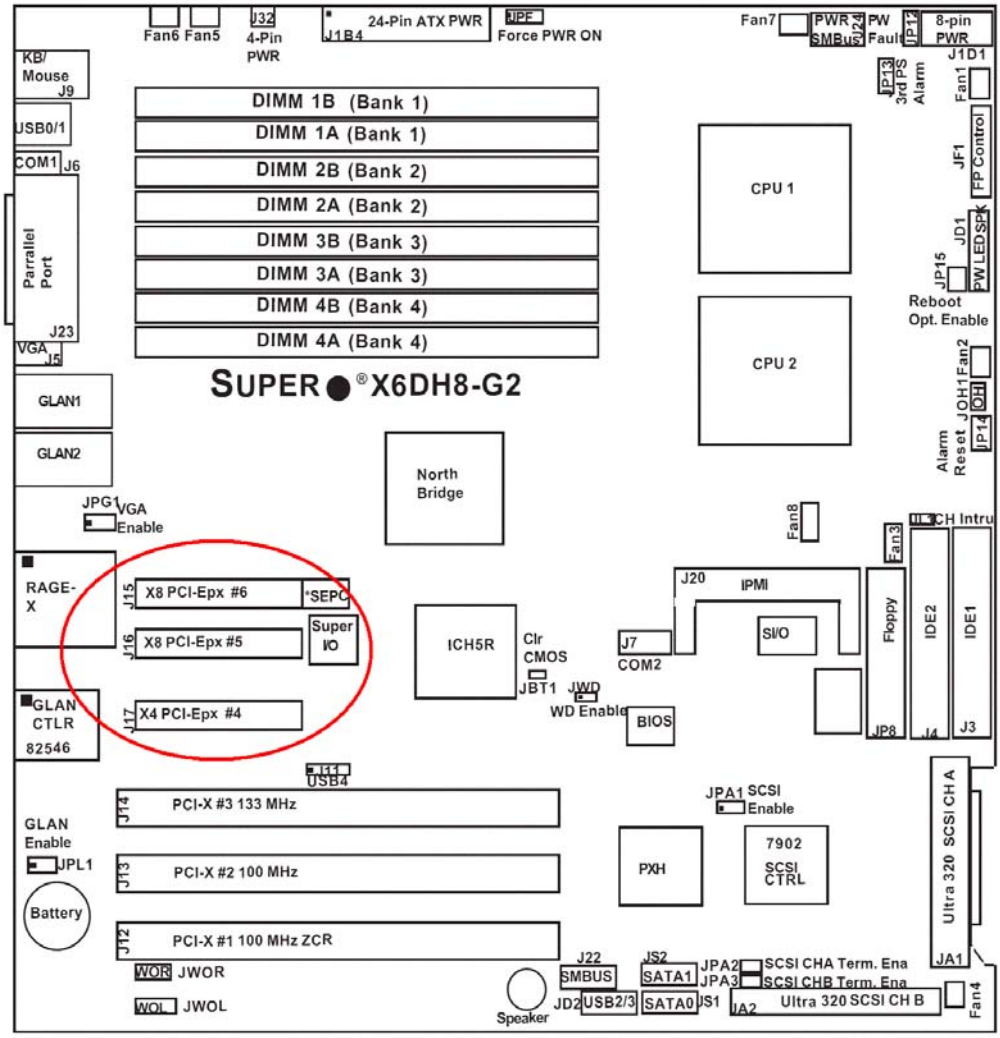


Figure 2.1 SuperMicro X6DH8-G2 Motherboard

Reference Clocks

The PES16T4 requires two differential reference clocks. The EB16T4-2 derives both of these clocks from a common source which is user-selectable. The common source can be either the host system's reference clock or the onboard clock generator. Selection is made by stuffing resistors described in Table 2.1.

Clock Configuration Stuffing Option	
Jumpers W4 and W7	Clock Source
Pins 2 and 3	Onboard Reference Clock – Use onboard clock generator
Pins 1 and 2	Upstream Reference Clock – Host system provides clock (Default)

Table 2.1 Clock Source Selection

Notes

The source for the onboard clock is the ICS557-03 clock generator device (U8) connected to a 25MHz oscillator (Y1). When using the onboard clock generator, the EB16T4-2 allows selection between multiple clock rates and spread spectrum settings via DIP switches as described in Tables 2.2 and 2.3 respectively. Spread Spectrum technology reduces peak EMI emissions by modulating the frequency to spread the peak energy over a wider bandwidth.

Clock Frequency Switch - S2[2:1]		
S2[2]	S2[1]	Clock Frequency
OFF	OFF	Reserved
OFF	ON	125 MHz
ON	OFF	100 MHz (Default)
ON	ON	<Reserved>

Table 2.2 Clock Frequency Selection

Clock Spread Spectrum Switch - S2[4:3]		
S2[4]	S2[3]	Spread%
OFF	OFF	No Spread (Default)
OFF	ON	Down -0.75
ON	OFF	Down -0.50
ON	ON	Center ±0.25

Table 2.3 Clock Spread Spectrum Selection

If the Clock Spread Spectrum is used to modulate data rate, then both ports must use same modulated clock source. Therefore, if your system uses SSC, the on-board clock generator must be disabled and the upstream reference clock should be used instead.

The output of the onboard clock generator is accessible through two SMA connectors located on the Evaluation Board. See Table 2.4. This can be used to connect a scope for probing or capturing purposes and cannot be used to drive the clock from an external source.

Onboard Reference Clock Output (Differential) – J3, J2	
J3	Positive Reference Clock
J2	Negative Reference Clock

Table 2.4 SMA Connectors - Onboard Reference Clock

Power Sources

The EB16T4-2 and all downstream ports are powered from the upstream port slot power. If add-in cards require more power than the upstream slot can support, an external source is required to supply this extra power via an auxiliary 4-pin power connector on the board. Only downstream ports 6 and 7 can be powered by this external power source through jumpers W45, W46, and W47 (see Table 2.18).

External Power Source

If necessary, external power is supplied to the EB16T4-2 board through a 4-pin auxiliary power connector attached to J1. The external power supply provides +12V to the EB16T4-2 as described in Table 2.5. The +5V is unused.

Notes

Pin	Signal
1	+12V
2	GND
3	GND
4	+5V

Table 2.5 External Power Connector - J1

PCI Express Serial Data Transmit Termination Voltage Converter

A DC-DC converter (U6) provides a 1.5V PCI Express serial data transmit termination voltage (shown as VTTPE or VPETVTT) to the PES16T4.

PCI Express Digital Power Voltage Converter

A separate DC-DC converter (U3) provides a 1.0V PCI Express digital power voltage (VDDPE) to the PES16T4.

PCI Express Analog Power Voltage Converter

A separate DC-DC converter (U7) provides a 1.0V PCI Express analog power voltage (shown as VDDAPE or VDDPEA) to the PES16T4.

Core Logic Voltage Converter

A separate DC-DC converter (U1) provides the 1.0V core voltage (VDDCORE) to the PES16T4.

3.3V I/O Power Module

A 12V to 3.3V power module (U5 or U26) provides the 3.3V I/O voltage (VDDIO) to the PES16T4.

Power-up Sequence

The power-up sequence must be as following:

1. VDDIO - 3.3V
2. VDDCORE, VDDAPE, VDDPE - 1.0V
3. VTTPE - 1.5V

When powering up, each voltage level must ramp up and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations between sequential valid power level requirements. To insure that the sequencing requirements are met, a 0.047µF is used at the SOFTSTART cap on the VTTPE's voltage converter (U6 pin 36) in the EB16T4-2.

Required Jumpers

To deliver power to the PES16T4 switch, the following jumpers must be shunted: W10 and W22—W25. These jumpers were implemented so that the power consumption of the PES16T4 can be measured.

Reset

The PES16T4 supports two types of reset mechanisms as described in the PCI Express specification:

- Fundamental Reset: This is a system-generated reset that propagates along the PCI Express tree through a single side-band signal PERST# which is connected to the Root Complex, the PES16T4, and the endpoints.
- Hot Reset: This is an In-band Reset, communicated downstream via a link from one device to another. Hot Reset may be initiated by software. This is further discussed in the 89HPES16T4 User Manual. The EB16T4-2 evaluation board provides seamless support for Hot Reset.

Notes

Fundamental Reset

There are two types of Fundamental Resets which may occur on the EB16T4-2 evaluation board:

- Cold Reset: During initial power-on, the onboard voltage monitor (TLC7733D) will assert the PCI Express Reset (PERSTN) input pin of the PES16T4.
- Warm Reset: This is triggered by hardware while the device is powered on. Warm Reset can be initiated by two methods:
  - Pressing a push-button switch (S1) located on EB16T4-2 board
  - The host system board IO Controller Hub asserting PERST# signal, which propagates through the PCIe upstream edge connector of the EB16T4-2. Note that one can bypass the onboard voltage monitor (TLC7733D) by moving the shunt from pin 1-2 to pin 2-3 (default) on W1.

Both events cause the onboard voltage monitor (TLC7733D) to assert the PCI Express Reset (PERSTN) input of the PES16T4 while power is on.

Downstream Reset

The PES16T4 provides a a choice of either a software-controlled reset for each downstream port through GPIO pins or a fundamental reset through PERST#. Selection is made by jumpers described in Table 2.6.

Port #	Jumper	Selection
6	W30	[1-2] Software controlled reset through GPIO11 [2-3] Fundamental reset PERST# (default)
7	W35	[1-2] Software controlled reset through GPIO12 [2-3] Fundamental reset PERST# (default)

Table 2.6 Downstream Reset Selection

Boot Configuration Vector

A boot configuration vector consisting of the signals listed in Table 2.7 is sampled by the PES16T4 during a fundamental reset (while PERSTN is active). The boot configuration vector defines the essential parameters for switch operation and is set using DIP switches S5 and S6 as defined in Table 2.8.

Signal	Description
CCLKDS	Common Clock Downstream. The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices. This pin is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be overridden by modifying the SCLK bit in the downstream port's PCIELSTS register. Default: 0x1
CCLKUS	Common Clock Upstream. The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This pin is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the P0_PCIELSTS register. Default: 0x1
MSMBSMODE	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 kHz. Default: 0x0
P01MERGEN	Port 0 and 1 Merge: When this pin is asserted (i.e. low), port 1 is merged with port 0 to form a single x8 port. Default: 0x0

Table 2.7 Boot Configuration Vector Signals (Part 1 of 2)

Notes

Signal	Description
P67MERGEN	Port 6 and 7 Merge: When this pin is asserted (i.e. low), port 7 is merged with port 6 to form a single x8 port. Default: 0x1
RSTHALT	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, the PES16T4 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the P0_SWCTL register through the SMBus. The value may be overridden by modifying the RSTHALT bit in the P0_SWCTL register. Default: 0x0
SWMODE[2:0]	Switch Mode. These configuration pins determine the PES16T4 switch operating mode. Default: 0x1 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM-based initialization 0x2 through 0x7 - Reserved
REFCLKM	PCI Express Reference Clock Mode Select. This signal selects the frequency of the reference clock input. Default: 0x0 0x0 - 100 MHz 0x1 - 125 MHz
MSMBADDR[2:0]	Master SMBus Address. These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded. Default: 0x0

Table 2.7 Boot Configuration Vector Signals (Part 2 of 2)

Signal	Description	Default
S6[1]	CCLKDS	OFF
S6[2]	CCLKUS	OFF
S6[3]	MSMBSMODE	ON
S6[4]	P01MERGEN	ON
S6[5]	Not Used	OFF
S6[6]	Not Used	OFF
S6[7]	P67MERGEN	Must be OFF
S6[8]	RSTHALT	OFF
S5[1]	SWMODE[0]	OFF
S5[2]	SWMODE[1]	ON
S5[3]	SWMODE[2]	ON
S5[4]	Not Used	ON
S5[5]	REFCLKM	ON
S5[6]	MSMBADDR[0]	ON
S5[7]	MSMBADDR[1]	ON
S5[8]	MSMBADDR[2]	ON

Table 2.8 Boot Configuration Vector Switches S5 & S6 (ON=0, OFF=1)

Notes

SMBus Interfaces

The System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate. It is based on the principles of operation of I^2C. Implementation of the SMBus signals in the PCI Express connector is optional and may not be present on the host system. The SMBus interface consists of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins.

The PES16T4 contains two SMBus interfaces: a slave SMBus interface and a master SMBus interface. The slave SMBus interface allows a SMBus Master device (such as the Intel E7520) full access to all software-visible registers. The Master SMBus interface provides connection to the external serial EEPROMs used for initialization and the I/O expander used for hot-plug signals.

SMBus Slave Interface

On the EB16T4-2 board, the slave SMBus interface is accessible through the PCI Express edge connector as well as a 4-pin header as described in Table 2.9.

Note: The SMBus signals to the PCI Express edge connector is disabled by default. To enable them, place 0-ohm resistors at locations R202 and R203.

.

Slave SMBus Interface Connector J10	
Pin	Signal
1	N/C
2	SCL
3	GND
4	SDA

Table 2.9 Slave SMBus Interface Connector

A fixed slave SMBus address specified by the SSMBADDR[5,3:1] pins is used.

For a fixed address, the SMBus address of the PES16T4 slave interface is 0b1110111 by default and is configurable using jumpers W40, W41, W42, and W43 as described in Tables 2.10 and 2.11.

Slave Interface Address Configuration	
Address Bit	Signal
1	SSMBUSADDR[1]
2	SSMBUSADDR[2]
3	SSMBUSADDR[3]
4	0
5	SSMBUSADDR[5]
6	1
7	1

Table 2.10 SMBus Slave Interface Address Configuration

Notes

SMBUS Slave Interface Address Setting				
W40 SSMBADDR[1]	W41 SSMBADDR[2]	W42 SSMBADDR[3]	W43 SSMBADDR[5]	Slave Interface Bus Address
OFF	OFF	OFF	OFF	0b1110111 (Default)
ON	OFF	OFF	OFF	0b1110110
OFF	ON	OFF	OFF	0b1110101
ON	ON	OFF	OFF	0b1110100
OFF	OFF	ON	OFF	0b1110011
ON	OFF	ON	OFF	0b1110010
OFF	ON	ON	OFF	0b1110001
ON	ON	ON	OFF	0b1110000
OFF	OFF	OFF	ON	0b1100111
ON	OFF	OFF	ON	0b1100110
OFF	ON	OFF	ON	0b1100101
ON	ON	OFF	ON	0b1100100
OFF	OFF	ON	ON	0b1100011
ON	OFF	ON	ON	0b1100010
OFF	ON	ON	ON	0b1100001
ON	ON	ON	ON	0b1100000

Table 2.11 PES16T4 SMBus Slave Interface Address Setting

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. Initiation of any SMBus transaction other than those listed above produces undefined results. See the SMBus 2.0 specification for a detailed description of the following transactions:

- Byte and Word Write/Read
- Block Write/Read

SMBus Master Interface

Connected to the master SMBus interface are three 16-bit I/O Expanders (PCA9555) and a serial EEPROM (24LC512). Three I/O Expanders are used as the interface for the onboard hot-plug controllers (MIC2591B). The lower three bits of the bus address for the I/O Expander are configurable as described in Tables 2.12 through 2.14

I/O Expander 2			
W3	W6	W9	Bus Address
ON	OFF	ON	0b0100010 (Default)
ON	ON	ON	0b0100000
ON	ON	OFF	0b0100001
ON	OFF	OFF	0b0100011

Table 2.12 I/O Expander 2 Bus Address (Part 1 of 2)

Notes

I/O Expander 2			
W3	W6	W9	Bus Address
OFF	ON	ON	0b0100100
OFF	ON	OFF	0b0100101
OFF	OFF	ON	0b0100110
OFF	OFF	OFF	0b0100111

Table 2.12 I/O Expander 2 Bus Address (Part 2 of 2)

I/O Expander 3			
W2	W5	W8	Bus Address
ON	OFF	OFF	0b0100011 (Default)
ON	ON	ON	0b0100000
ON	ON	OFF	0b0100001
ON	OFF	ON	0b0100010
OFF	ON	ON	0b0100100
OFF	ON	OFF	0b0100101
OFF	OFF	ON	0b0100110
OFF	OFF	OFF	0b0100111

Table 2.13 I/O Expander 3 Bus Address

I/O Expander 4			
W31	W44	W29	Bus Address
OFF	ON	ON	0b0100100 (Default)
ON	ON	ON	0b0100000
ON	ON	OFF	0b0100001
ON	OFF	ON	0b0100010
ON	OFF	OFF	0b0100011
OFF	ON	OFF	0b0100101
OFF	OFF	ON	0b0100110
OFF	OFF	OFF	0b0100111

Table 2.14 I/O Expander 4 Bus Address

The bus address for the selected EEPROM device is **0b1000** by default and is configurable using W39 and the switch S5 as described in Table 2.15.

Notes

W39	S5[8]	S5[7]	S5[6]	Bus Address
OFF	OFF	OFF	OFF	0b0101 1111
OFF	OFF	OFF	ON	0b0101 1110
OFF	OFF	ON	OFF	0b0101 1101
OFF	OFF	ON	ON	0b0101 1100
OFF	ON	OFF	OFF	0b0101 1011
OFF	ON	OFF	ON	0b0101 1010
OFF	ON	ON	OFF	0b0101 1001
OFF	ON	ON	ON	0b0101 1000
ON	ON	ON	ON	0b0101 0000 (Default)

Table 2.15 EEPROM SMBus Address Setting

JTAG Header

The PES16T4 provides a JTAG connector J4 for access to the PES16T4 JTAG interface. The connector is a 2.54 x 2.54 mm pitch male 10-pin connector. Refer to Table 2.16 for the JTAG Connector J4 pin out.

JTAG Connector J4					
Pin	Signal	Direction	Pin	Signal	Direction
1	/TRST - Test reset	Input	2	GND	—
3	TDI - Test data	Input	4	GND	—
5	TDO - Test data	Output	6	GND	—
7	TMS - Test mode select	Input	8	GND	—
9	TCK - Test clock	Input	10	GND	—

Table 2.16 JTAG Connector Pin Out

Attention Buttons

The PES16T4 features four attention buttons, shown in Table 2.17. Each button corresponds to a particular port and is used to initiate hot-swapping events.

Button	Description
S4	Port 6 Attention Button
S7	Port 7 Attention Button

Table 2.17 Attention Buttons

Notes

Miscellaneous Jumpers, Headers

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W45-W47	Header	1-2 Shunted	1-2: 12.0V source from Upstream Port (Default) 2-3: 12.0V source from external power connector
W49-W50	Header	Shunted	Bypass hot-plug controller - Enable REFCLK to downstream ports (Default)
W12	Header	Shunted	Disable EEPROM Write protect feature (Default)
W3, W6, W9 W2, W5, W8 W31, W44, W29	Header	ON, OFF, ON ON, OFF, OFF OFF, ON, ON	I/O Expander 2 Address[2:0]. Default to 0x2 I/O Expander 3 Address[2:0]. Default to 0x3 I/O Expander 4 Address[2:0]. Default to 0x4
W13	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Port 7 (Default)
W17	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 6 (Default)
W16	Header	2-3 Shunted	2-3: Port 7, 3.3Vaux source from Upstream port (Default) 1-2: Port 7, 3.3Vaux source from hot-plug controller
W20	Header	2-3 Shunted	2-3: Port 6, 3.3Vaux source from Upstream port (Default) 1-2: Port 6, 3.3Vaux source from hot-plug controller
W28	Header	2-3 Shunted	2-3: Port 6, +12V source base on W45-W47 (Default) 1-2: Port 6, +12V source from hot-plug controller
W33	Header	2-3 Shunted	2-3: Port 7, +12V source base on W45-W47 (Default) 1-2: Port 7, +12V source from hot-plug controller
W32	Header	2-3 Shunted	2-3: Port 6, +3.3V source base on W45-W47 (Default) 1-2: Port 6, +3.3V source from hot-plug controller
W34	Header	2-3 Shunted	2-3: Port 7, +3.3V source base on W45-W47 (Default) 1-2: Port 7, +3.3V source from hot-plug controller

Table 2.18 Miscellaneous Jumpers, Headers

LEDs

There are several LED indicators on the EB16T4-2 which convey status feedback. A description of each is provided in Table 2.19.

Location	Color	Definition
DS12	Green	Port 6: Power-is-good indicator
DS15	Green	Port 7: Power-is-good indicator
DS8	Green	Port 6: Power Indicator
DS6	Yellow	Port 6: Attention Indicator
DS4	Green	Port 7: Power Indicator
DS3	Yellow	Port 7: Attention Indicator

Table 2.19 LED Indicators (Part 1 of 2)

Notes

Location	Color	Definition
DS13	Red	Hot Plug Controller1: Power Fault Indicator
DS16	Red	Hot Plug Controller2: Power Fault Indicator
DS2	Green	Board Power Indicator (3.3V)
DS1	Red	Board Reset Indicator
DS19	Green	Port 6: link up status output
DS20	Green	Port 6: active status output
DS21	Green	Port 7: link up status output
DS22	Green	Port 7: active status output
DS25	Green	Port 0: link up status output
DS26	Green	Port 0: active status output
DS36	Green	GPIO0
DS32	Green	GPIO1
DS9	Green	GPIO2
DS9	Green	GPIO3
DS9	Green	GPIO6

Table 2.19 LED Indicators (Part 2 of 2)

PCI Express Connectors

Pin	Side A		Side B	
1	+12V	12V power	PRSNT1#	Hot-Plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground

Table 2.20 PCI Express x16 Connector Pinout (Part 1 of 3)

Notes

Pin	Side A		Side B	
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential	RSVD	Reserved
20	PETn1	pair, Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential
22	GND	Ground	PERn1	pair, Lane 1
23	PETp2	Transmitter differential	GND	Ground
24	PETn2	pair, Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential
26	GND	Ground	PERn2	pair, Lane 2
27	PETp3	Transmitter differential	GND	Ground
28	PETn3	pair, Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential
30	RSVD	Reserved	PERn3	pair, Lane 3
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETp4	Transmitter differential	RSVD	Reserved
34	PETn4	pair, Lane 4	GND	Ground
35	GND	Ground	PERp4	Receiver differential
36	GND	Ground	PERn4	pair, Lane 4
37	PETp5	Transmitter differential	GND	Ground
38	PETn5	pair, Lane 5	GND	Ground
39	GND	Ground	PERp5	Receiver differential
40	GND	Ground	PERn5	pair, Lane 5
41	PETp6	Transmitter differential	GND	Ground
42	PETn6	pair, Lane 6	GND	Ground
43	GND	Ground	PERp6	Receiver differential
44	GND	Ground	PERn6	pair, Lane 6
45	PETp7	Transmitter differential	GND	Ground
46	PETn7	pair, Lane 7	GND	Ground
47	GND	Ground	PERp7	Receiver differential
48	PRSNT2#	Hot-Plug presence detect	PERn7	pair, Lane 7
49	GND	Ground	GND	Ground
50	PETp8	Transmitter differential	RSVD	Reserved
51	PETn8	pair, Lane 8	GND	Ground
52	GND	Ground	PERp8	Receiver differential

Table 2.20 PCI Express x16 Connector Pinout (Part 2 of 3)

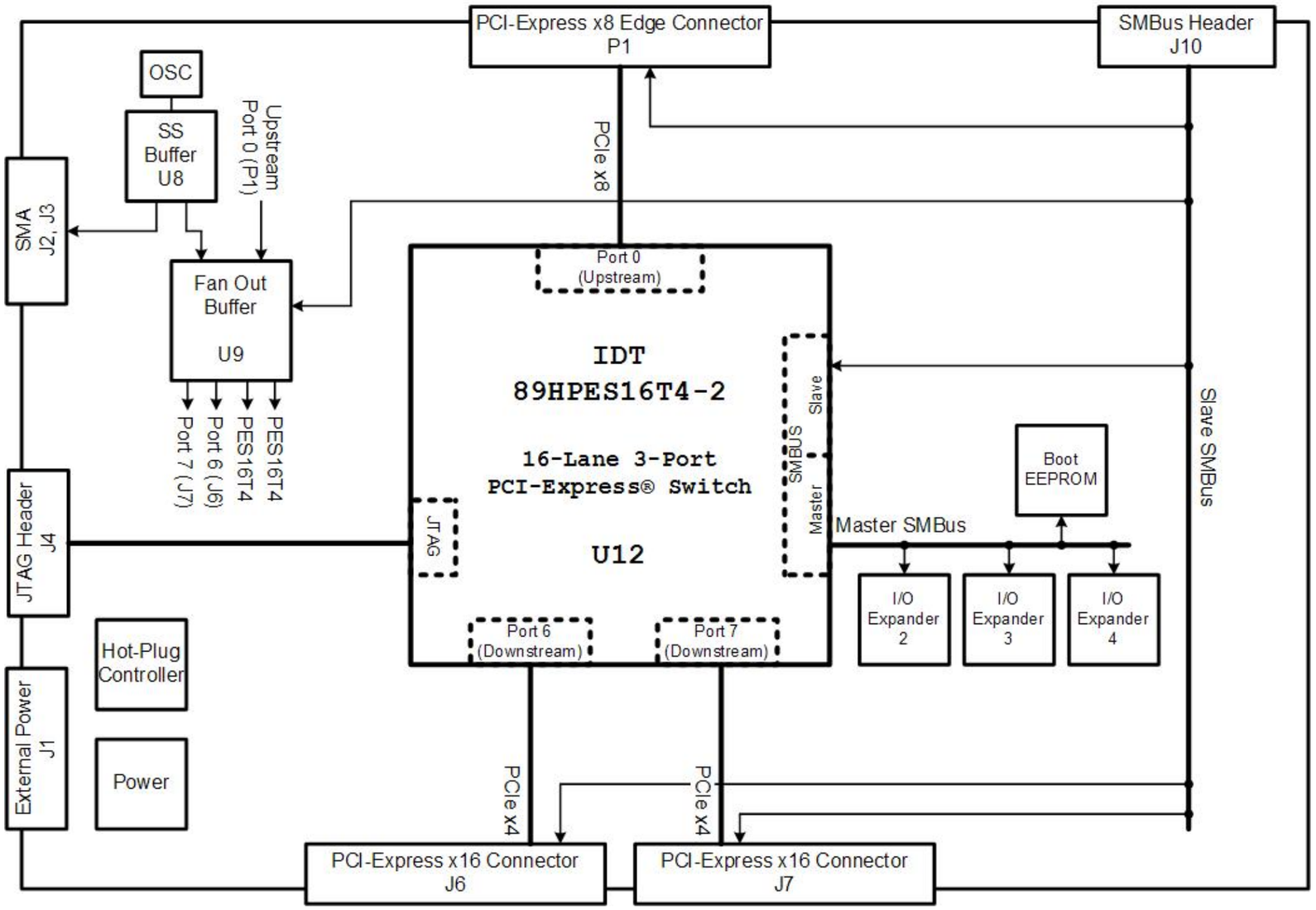
Notes

Pin	Side A		Side B	
53	GND	Ground	PERn8	pair, Lane 8
54	PETp9	Transmitter differential	GND	Ground
55	PETn9	pair, Lane 9	GND	Ground
56	GND	Ground	PERp9	Receiver differential
57	GND	Ground	PERn9	pair, Lane 9
58	PETp10	Transmitter differential	GND	Ground
59	PETn10	pair, Lane 10	GND	Ground
60	GND	Ground	PERp10	Receiver differential
61	GND	Ground	PERn10	pair, Lane 10
62	PETp11	Transmitter differential	GND	Ground
63	PETn11	pair, Lane 11	GND	Ground
64	GND	Ground	PERp11	Receiver differential
65	GND	Ground	PERn11	pair, Lane 11
66	PETp12	Transmitter differential	GND	Ground
67	PETn12	pair, Lane 12	GND	Ground
68	GND	Ground	PERp12	Receiver differential
69	GND	Ground	PERn12	pair, Lane 12
70	PETp13	Transmitter differential	GND	Ground
71	PETn13	pair, Lane 13	GND	Ground
72	GND	Ground	PERp13	Receiver differential
73	GND	Ground	PERn13	pair, Lane 13
74	PETp14	Transmitter differential	GND	Ground
75	PETn14	pair, Lane 14	GND	Ground
76	GND	Ground	PERp14	Receiver differential
77	GND	Ground	PERn14	pair, Lane 14
78	PETp15	Transmitter differential	GND	Ground
79	PETn15	pair, Lane 15	GND	Ground
80	GND	Ground	PERp15	Receiver differential
81	PRSNT2#	Hot-Plug presence detect	PERn15	pair, Lane 15
82	RSVD	Reserved	GND	Ground

Table 2.20 PCI Express x16 Connector Pinout (Part 3 of 3)

Note: These x16 PCI Express connectors comply with the PCIe specification. However, the downstream ports on the EB16T4-2 are electronically connected in a x4 configuration (ports 6 and 7). According to the PCI Express specification, the PRSNT1# pin should be wired to the farthest available PRSNT2# pin on the connector. In the EB16T4-2, all PRSNT2# pins are tied together. This allows the board to be installed in a x1 or a x4 slot via a slot reducer.

89EBPES16T4-2 – 89HPES16T4-2 Evaluation Board



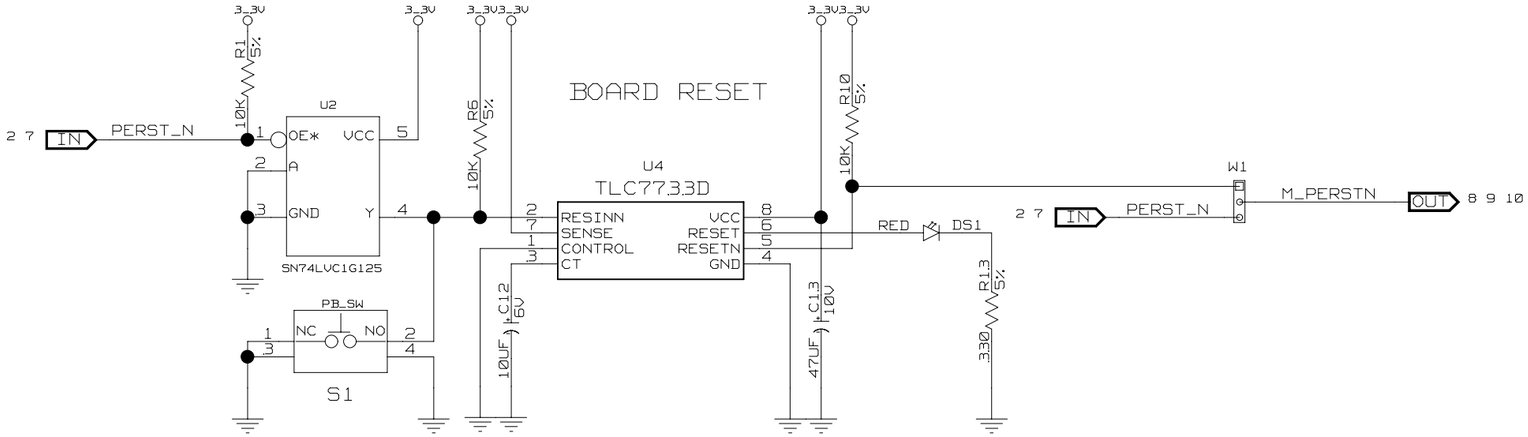
REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
STGC-0113R01	1.0	INITIAL RELEASE	2007-05-08	J. CARRILLO/K. LEUNG

SHEET DESCRIPTION

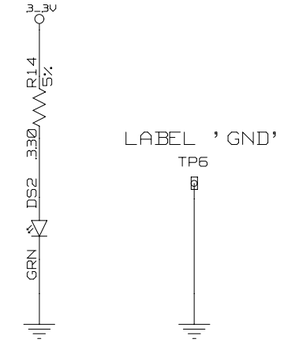
TITLE			
89EBPES16T4-2			
SIZE: B	DRAWING NO.: STGSCH-00113	FAB P/N: 18-633-000	REV.: 1.0
AUTHOR: J. CARRILLO / K. LEUNG		CHECKED BY: J. CARRILLO / K. LEUNG	
Tue May 08 11:34:21 2007		SHEET 1 OF 12	

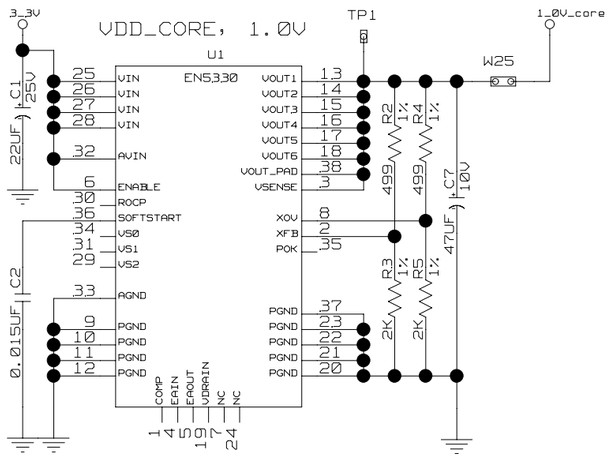
RENESAS

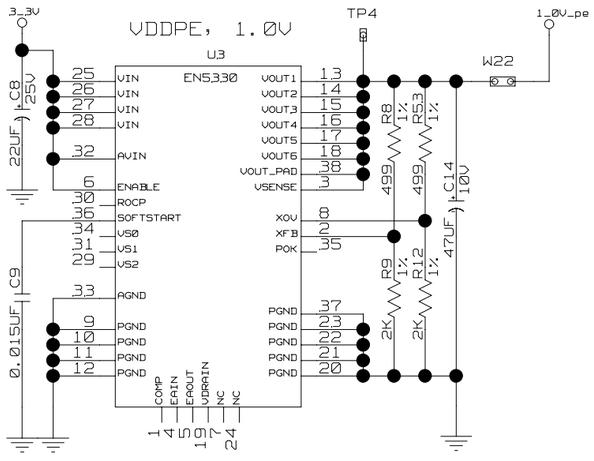
BOARD RESET

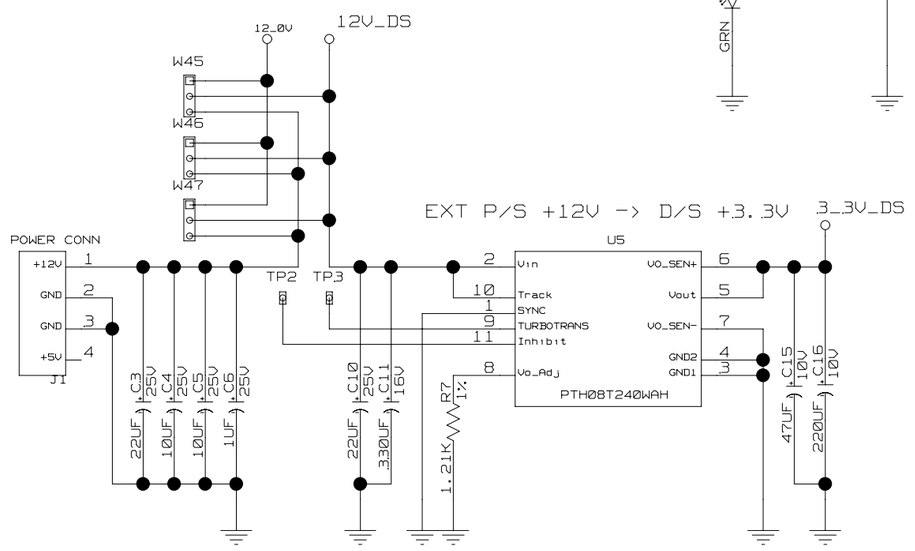


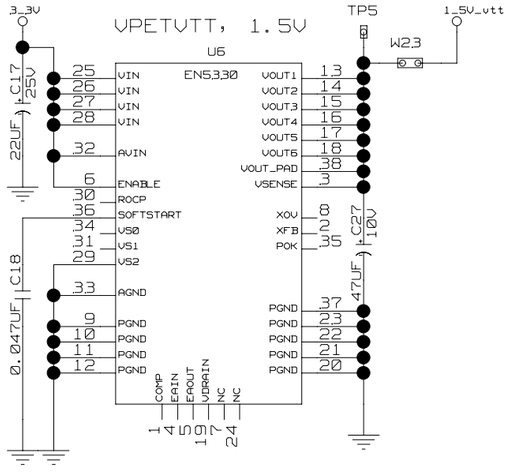
POWER INDICATOR
PLACE NEAR TOP EDGE
LABEL 'POWER'

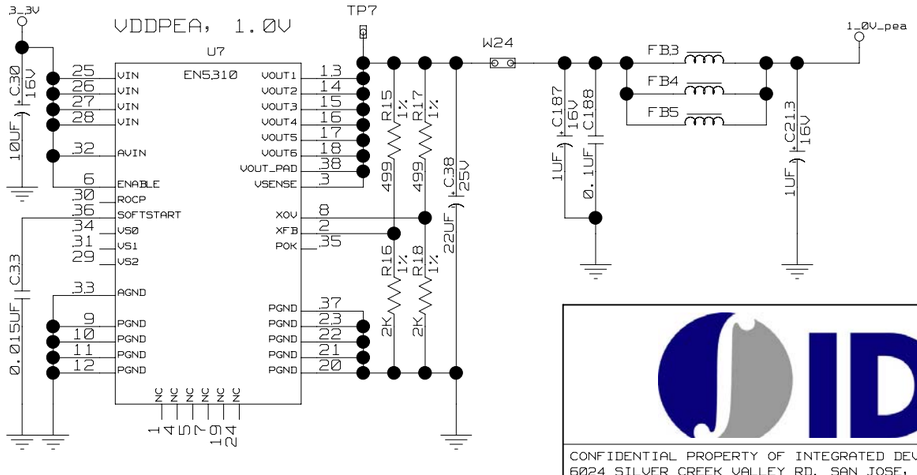


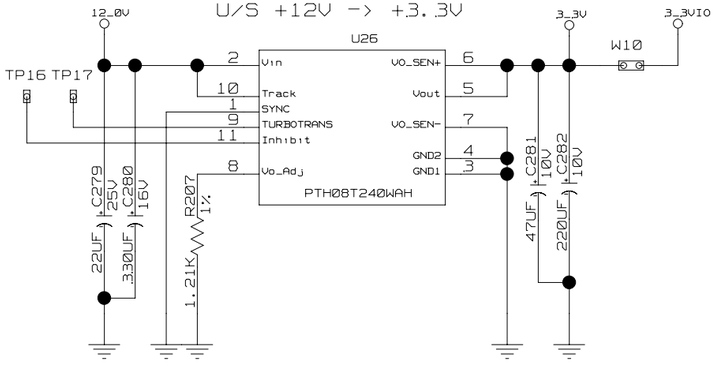






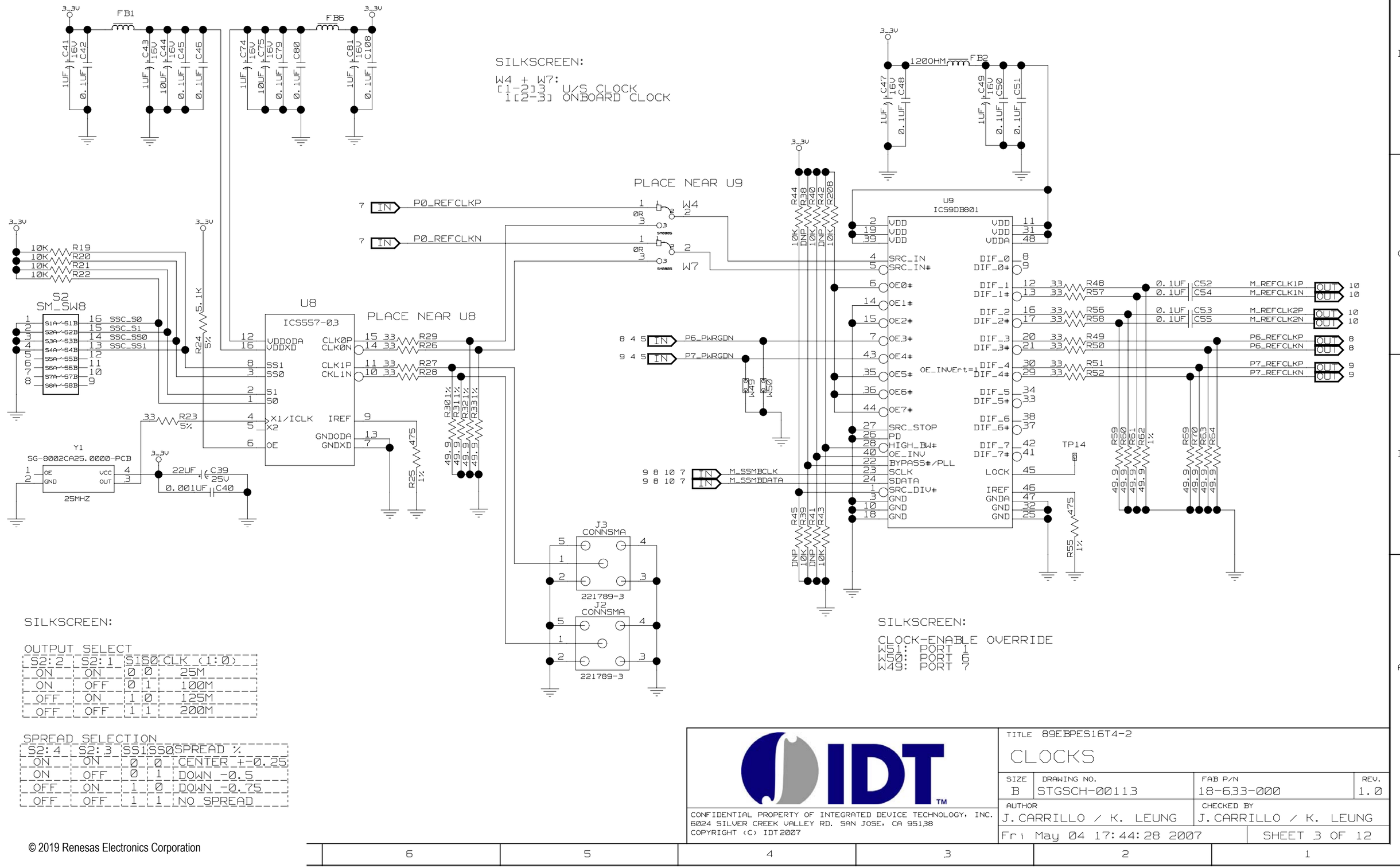






IDT™

TITLE 89EBPES16T4-2			
POWER SUPPLY AND RESET			
SIZE B	DRAWING NO. STGSCH-00113	FAB P/N 18-6333-000	REV. 1.0
AUTHOR J. CARRILLO / K. LEUNG		CHECKED BY J. CARRILLO / K. LEUNG	
Fri May 04 17:30:07 2007		SHEET 2 OF 12	



SILKSCREEN:

OUTPUT SELECT

S2:2	S2:1	SS1	SS0	CLK (1:0)
ON	ON	0	0	25M
ON	OFF	0	1	100M
OFF	ON	1	0	125M
OFF	OFF	1	1	200M

SPREAD SELECTION

S2:4	S2:3	SS1	SS0	SPREAD %
ON	ON	0	0	CENTER +-0.25
ON	OFF	0	1	DOWN -0.5
OFF	ON	1	0	DOWN -0.75
OFF	OFF	1	1	NO SPREAD

SILKSCREEN:

CLOCK-ENABLE OVERRIDE
W51: PORT 1
W50: PORT 0
W49: PORT 7

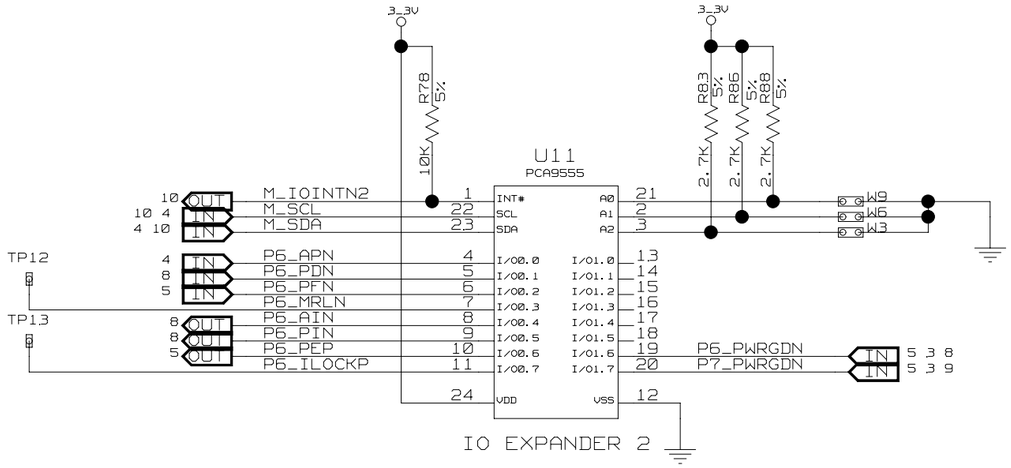
TITLE 89EBPES16T4-2

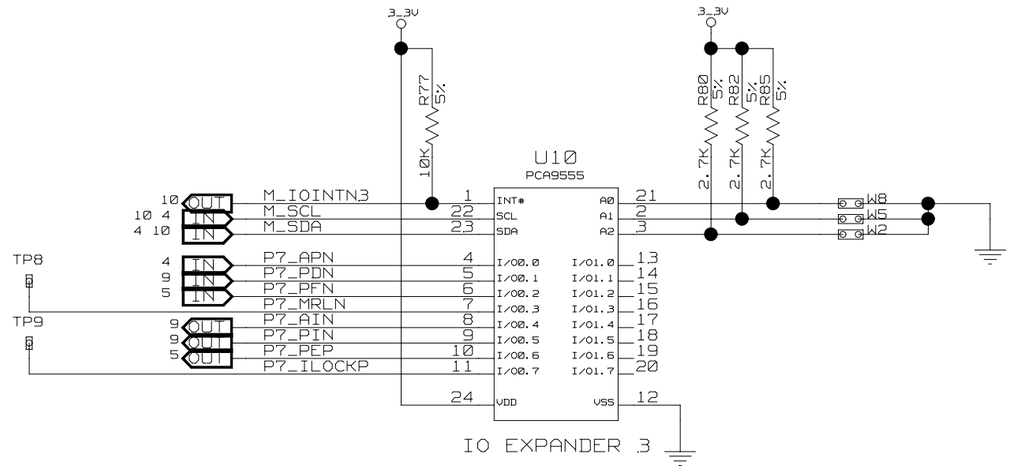
CLOCKS

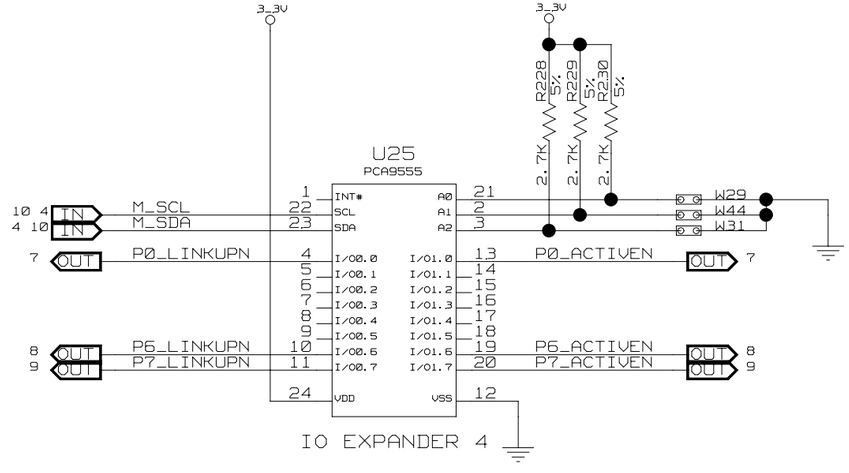
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

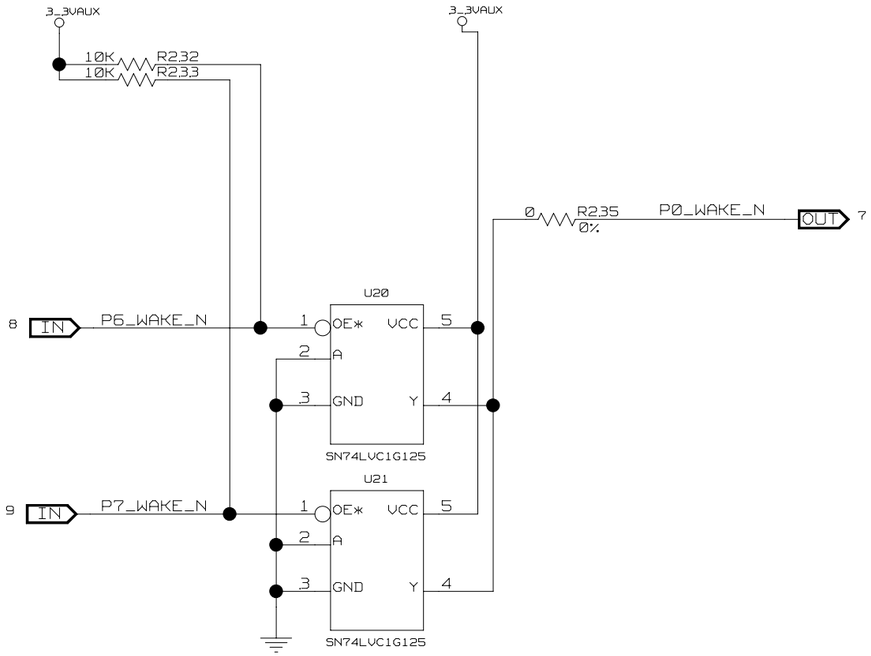
AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

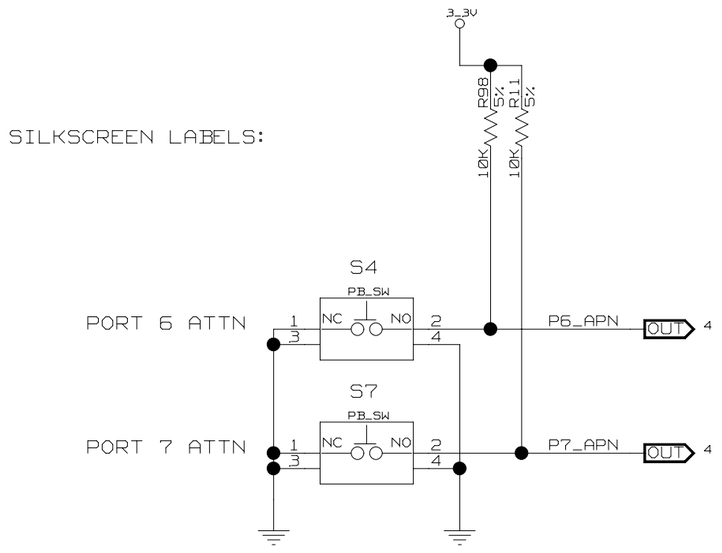
Fri May 04 17:44:28 2007 SHEET 3 OF 12











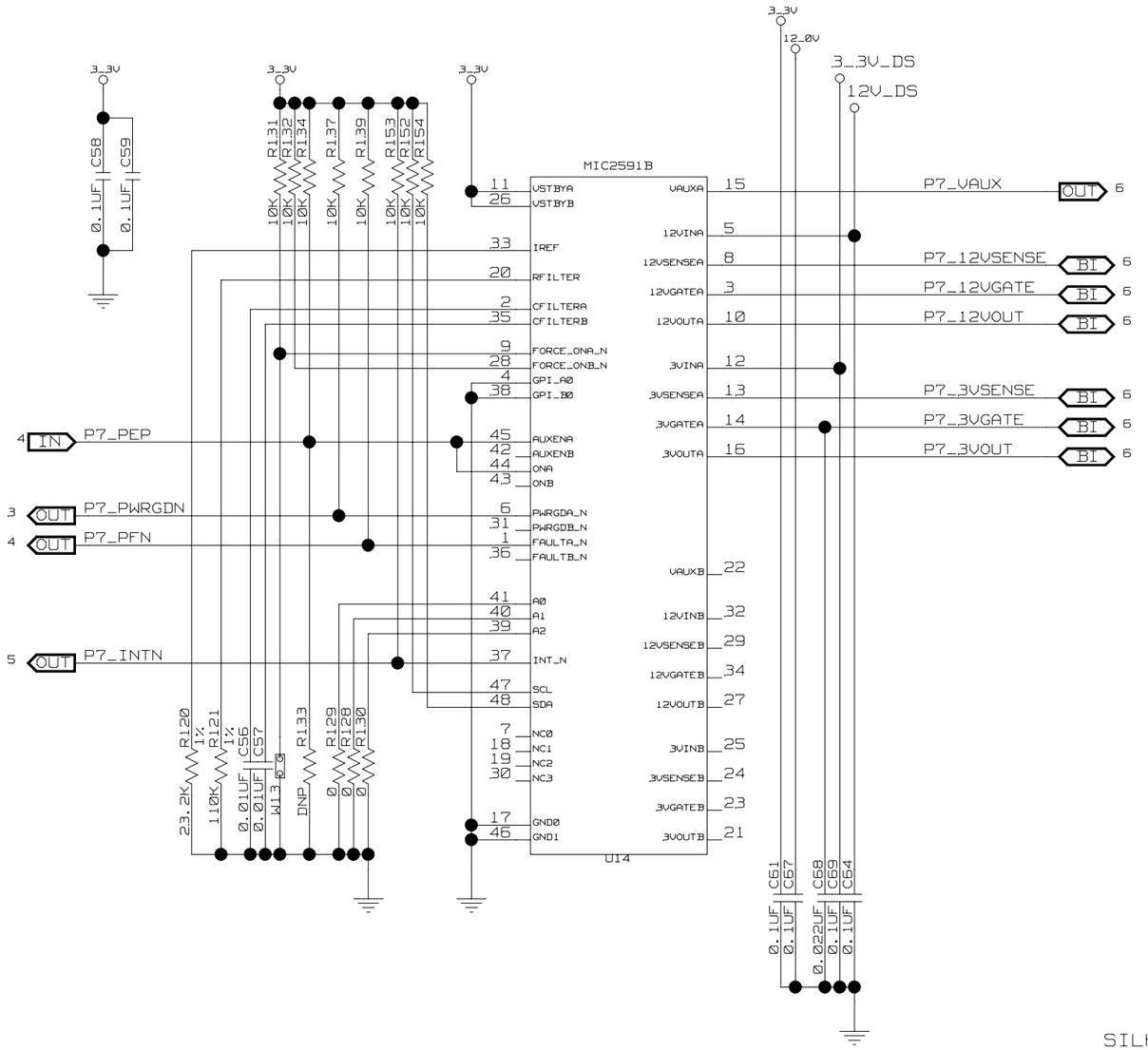
TITLE 89EBPES16T4-2

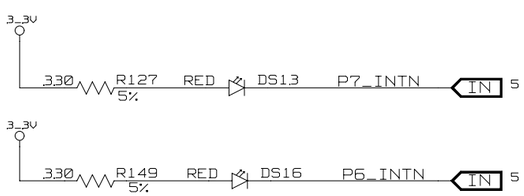
IO EXP, WAKE, ATTN BUTTONS

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

AUTHOR	CHECKED BY
J.CARRILLO / K. LEUNG	J.CARRILLO / K. LEUNG

Fri May 04 17:44:31 2007 — SHEET 4 OF 12





SILKSCREEN LABEL:

W13: P7 FORCE ON

W17: P6 FORCE ON

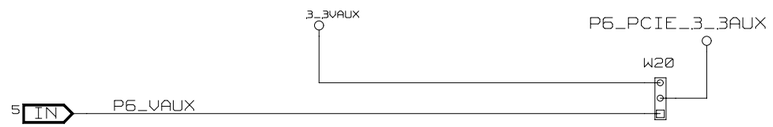
TITLE 89EBPES16T4-2

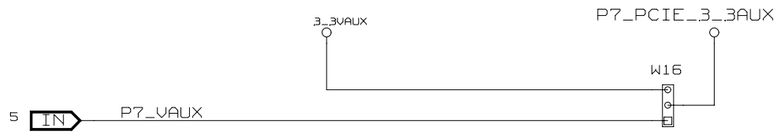
HOT PLUG CONTROLLERS

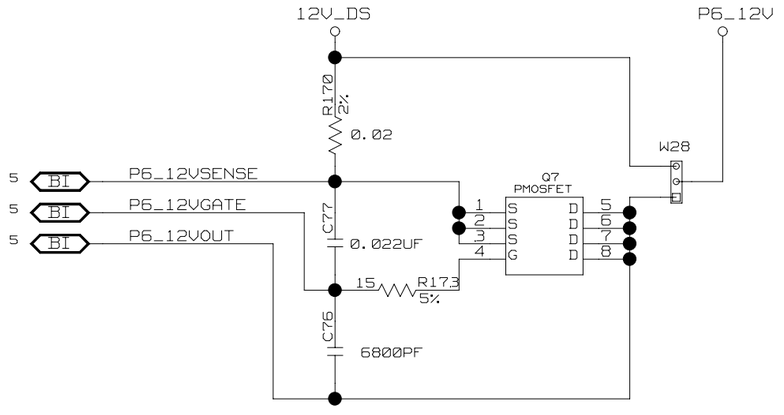
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

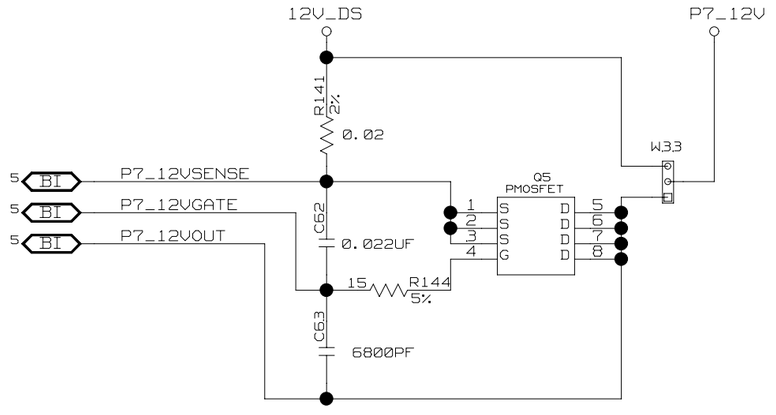
AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

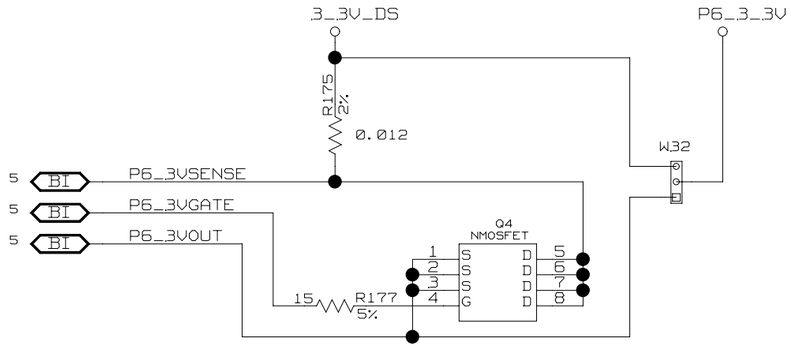
Fri May 04 17:44:37 2007 | SHEET 5 OF 12

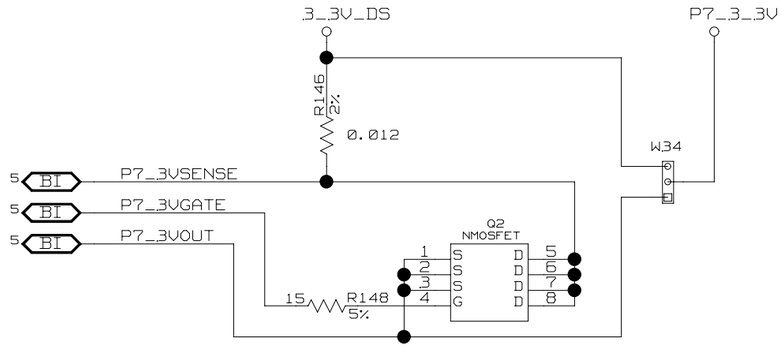












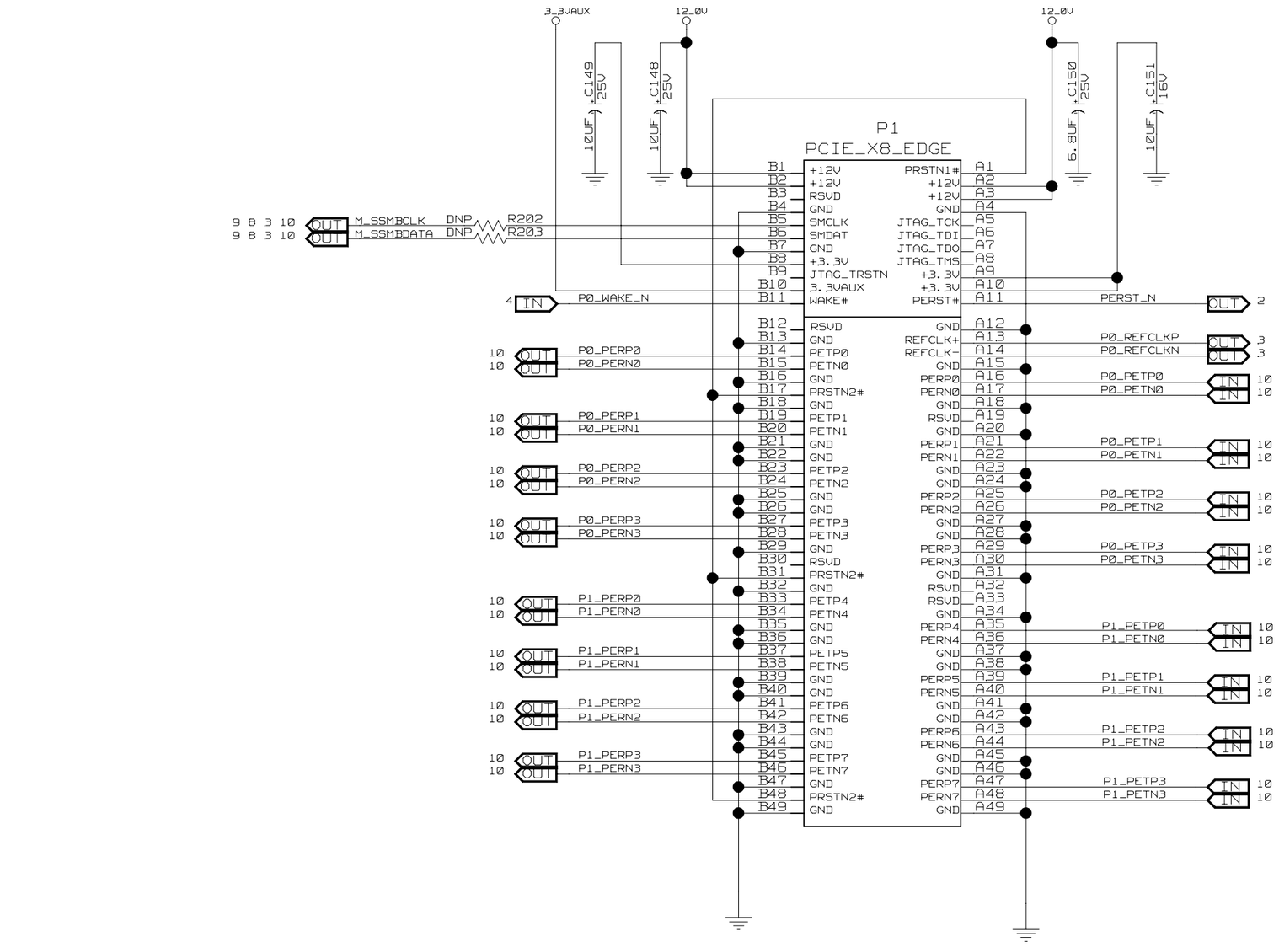
TITLE 89EBPES16T4-2

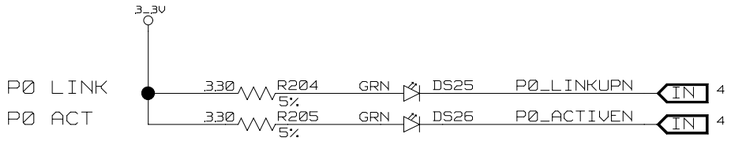
HOT PLUG MOSFETS

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

Fri May 04 17:44:40 2007 — SHEET 6 OF 12





CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
COPYRIGHT (C) IDT 2007

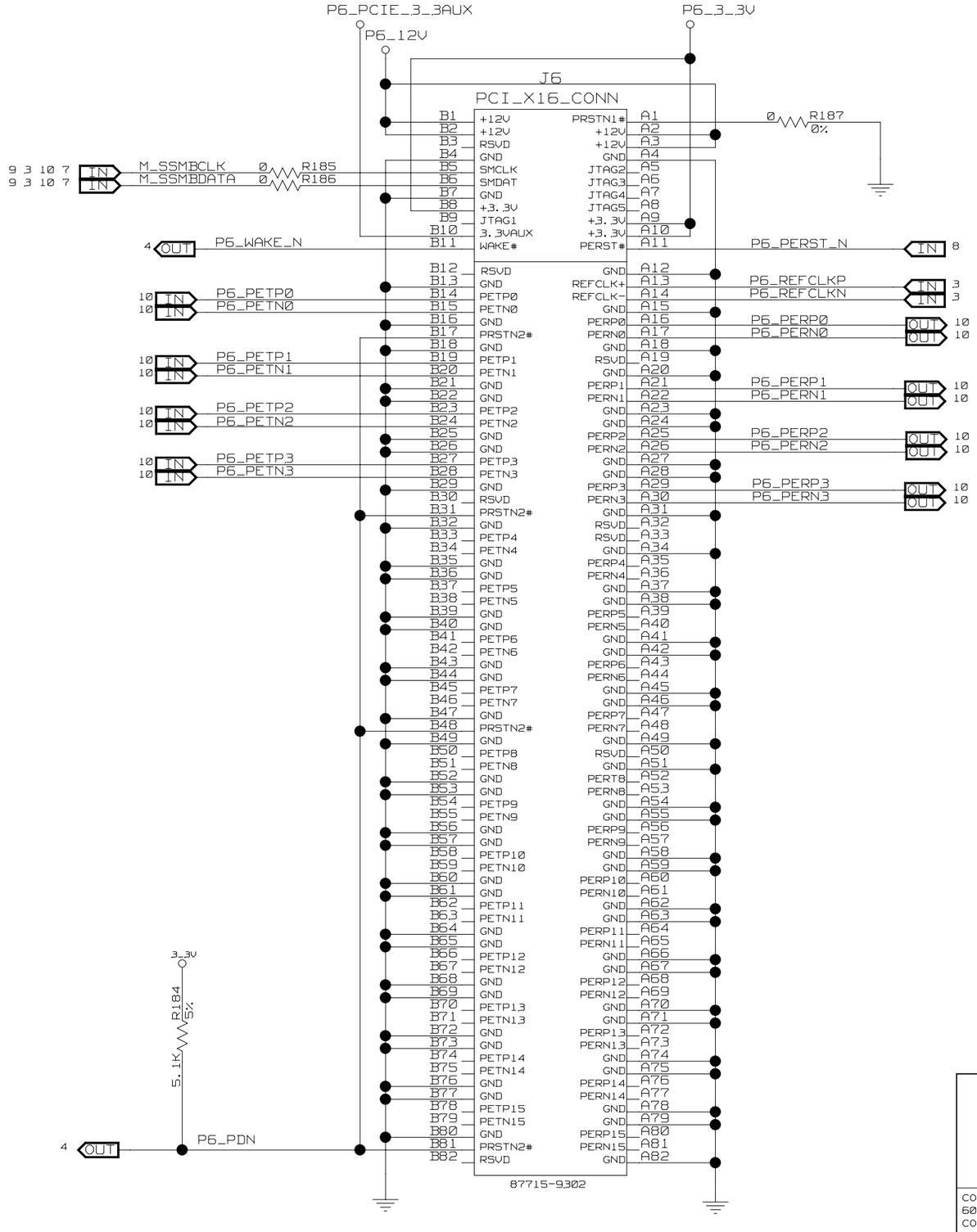
TITLE 89EBPES16T4-2

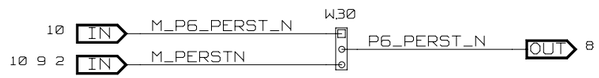
PORT 0 UPSTREAM EDGE CONN.

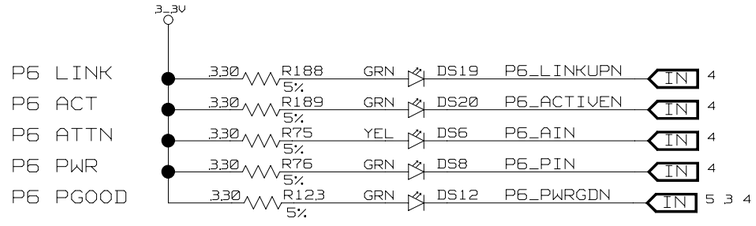
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

Fri May 04 17:44:43 2007 SHEET 7 OF 12







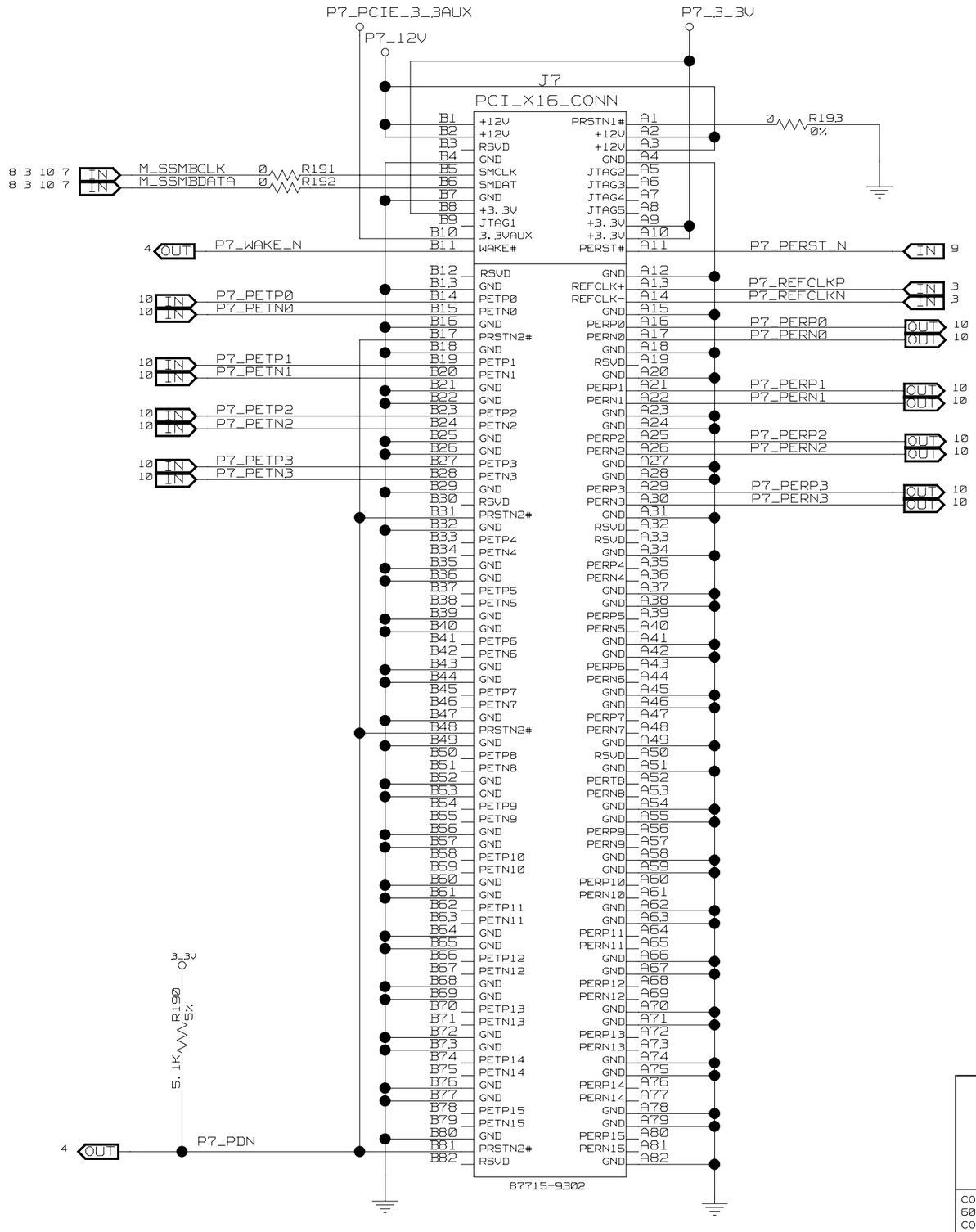
TITLE 89EBPES16T4-2

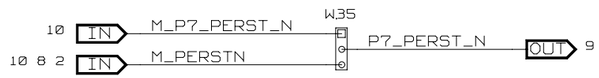
PORT 6 CONNECTOR

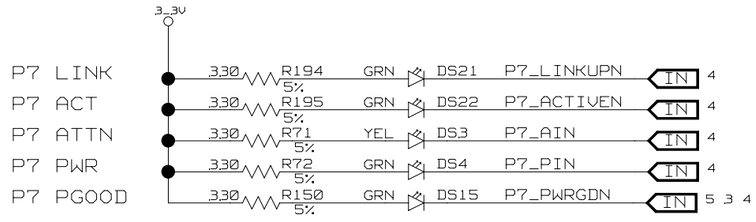
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

Fri May 04 17:44:46 2007 — SHEET 8 OF 12







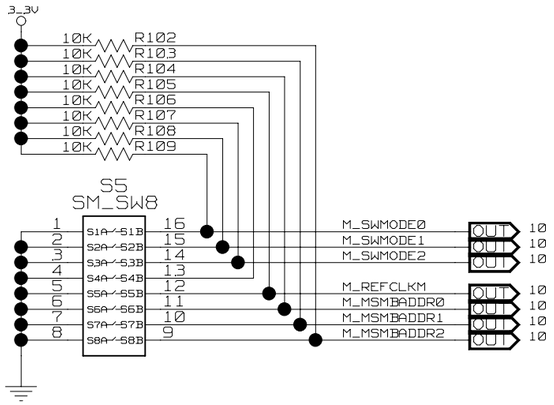
TITLE 89EBPES16T4-2

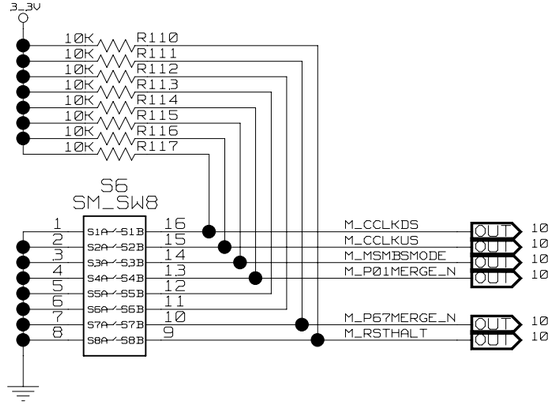
PORT 7 CONNECTOR

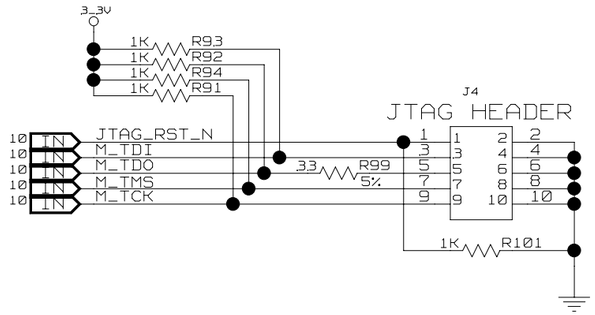
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

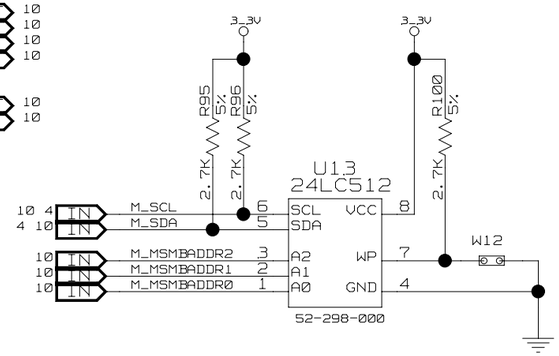
AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

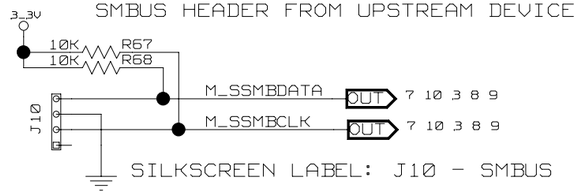
Fri May 04 17:44:49 2007 — SHEET 9 OF 12

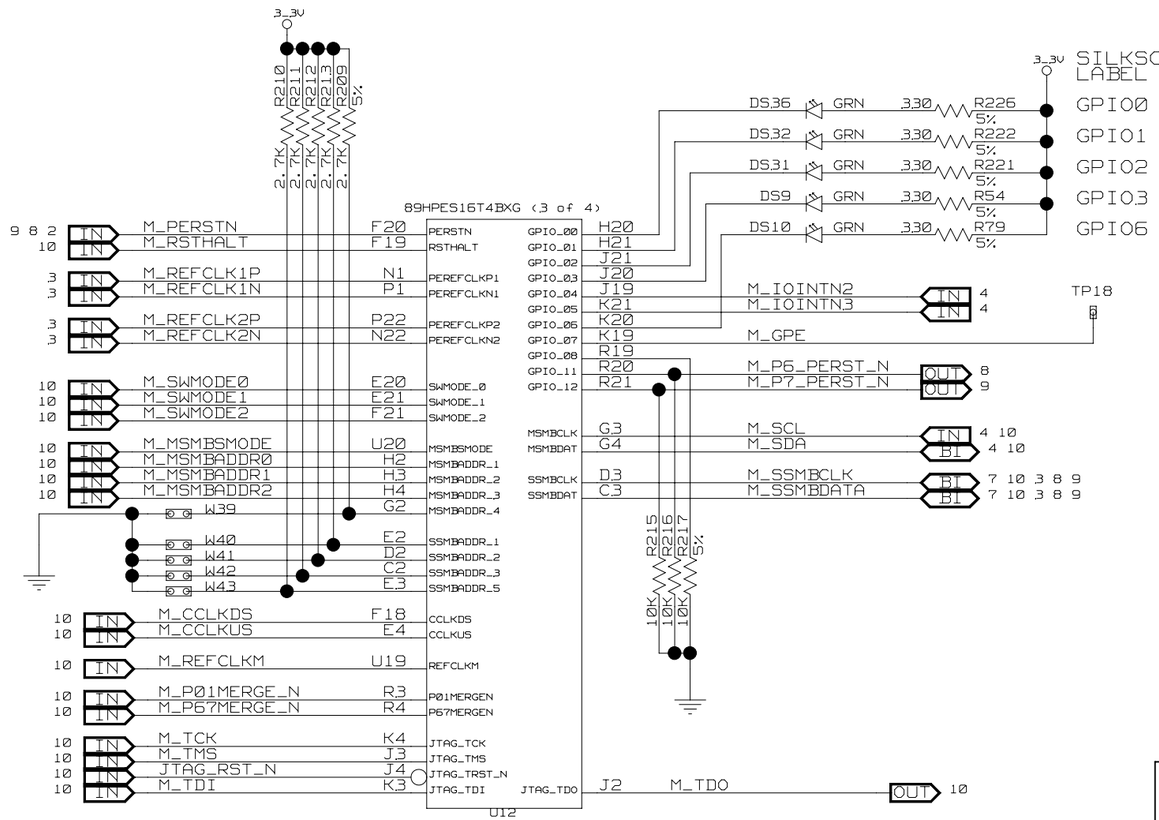


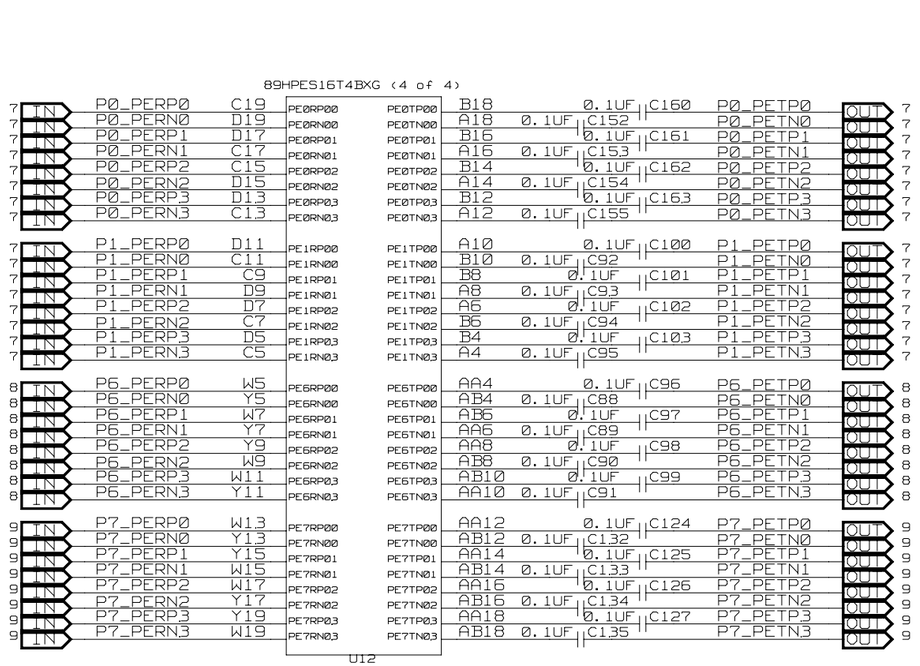












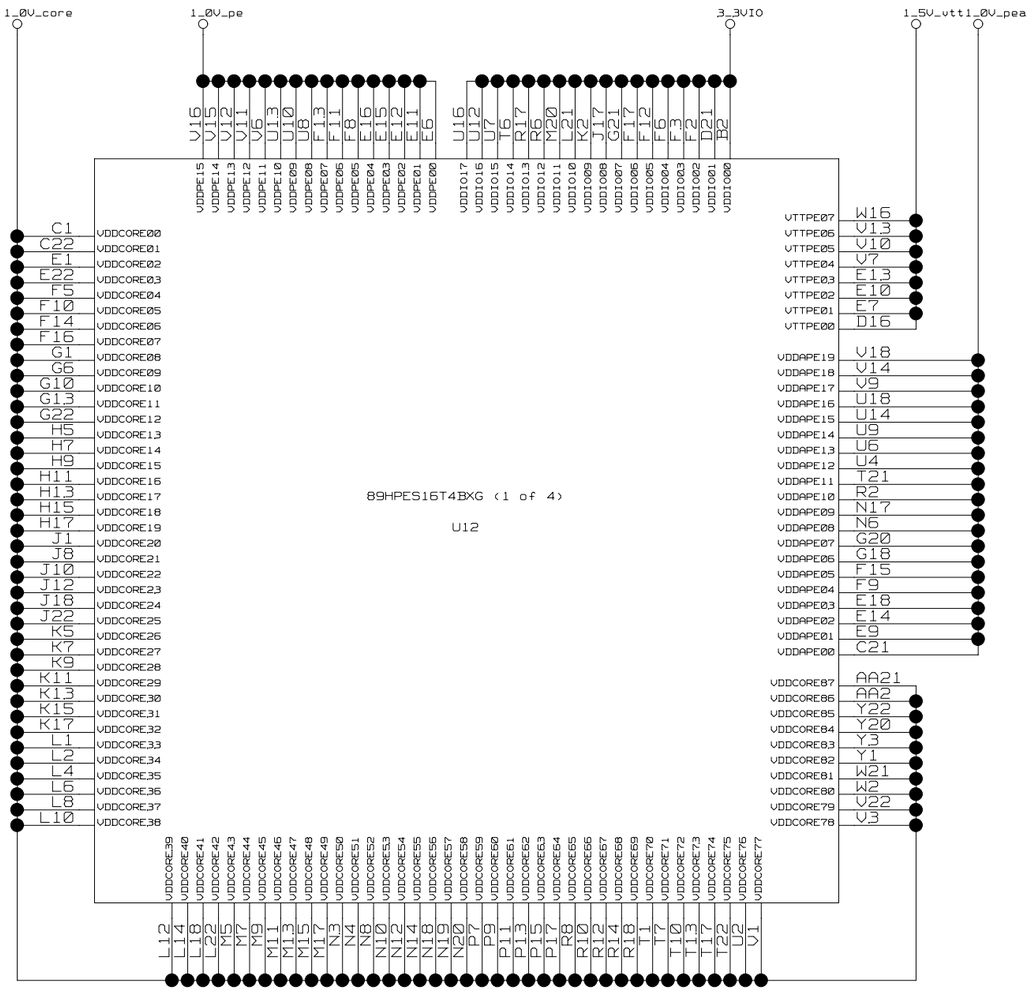
TITLE 89EBPES16T4-2

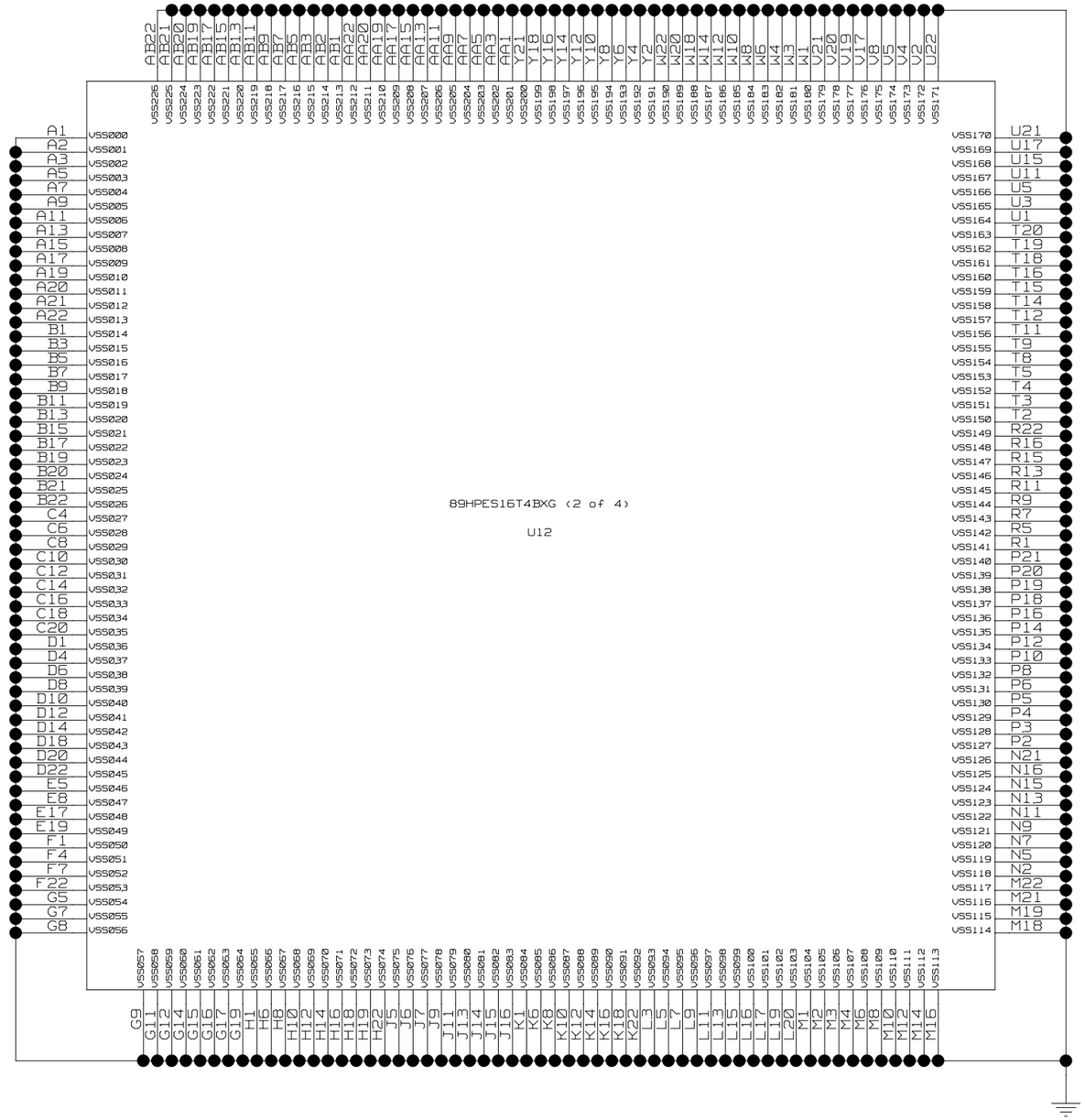
89HPES16T4-2

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

Tue May 08 11:31:37 2007 — SHEET 10 OF 12





TITLE 89EBPES16T4-2

89HPES16T4-2 - POWER

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

Fri May 04 17:44:56 2007 SHEET 11 OF 12

RENESAS

VDDCORE

1_0V_core

C221 0.1UF, C222 0.1UF, C223 0.1UF, C224 0.1UF, C225 0.1UF, C226 0.1UF, C227 0.1UF, C228 0.1UF, C229 0.1UF, C230 0.1UF, C231 0.1UF, C232 0.1UF, C247 0.1UF, C248 0.1UF, C249 0.1UF, C250 0.1UF, C251 0.1UF, C252 0.1UF, C253 0.1UF, C254 0.1UF, C255 0.1UF, C256 0.1UF, C257 0.1UF, C258 0.1UF, C259 0.1UF, C260 0.1UF, C261 0.1UF, C262 0.1UF, C263 0.1UF, C264 0.1UF, C265 0.1UF, C266 0.1UF, C267 0.1UF, C268 0.1UF, C269 0.1UF, C270 0.1UF, C243 47UF 10V, C244 47UF 10V, C246 1UF 16V

VDDPE

1_0V_pe

C191 0.1UF, C192 0.1UF, C193 0.1UF, C194 0.1UF, C195 0.1UF, C196 0.1UF, C197 0.1UF, C198 0.1UF, C199 0.1UF, C200 0.1UF, C201 0.1UF, C202 0.1UF, C203 0.1UF, C204 0.1UF, C205 0.1UF, C206 0.1UF, C207 0.1UF, C208 0.1UF, C209 0.1UF, C210 0.1UF, C211 0.1UF, C189 47UF 10V, C190 47UF 10V, C212 1UF 16V

VDDAPE

1_0V_pea

C233 0.1UF, C234 0.1UF, C235 0.1UF, C236 0.1UF, C237 0.1UF, C238 0.1UF, C239 0.1UF, C240 0.1UF, C241 0.1UF, C242 0.1UF, C245 0.1UF, C271 0.1UF, C272 0.1UF, C273 0.1UF, C274 0.1UF, C275 0.1UF, C276 0.1UF, C277 47UF 10V, C278 47UF 10V

VTT

1_5V_vtt

C171 0.1UF, C172 0.1UF, C173 0.1UF, C174 0.1UF, C175 0.1UF, C176 0.1UF, C177 0.1UF, C178 0.1UF, C179 0.1UF, C180 0.1UF, C181 0.1UF, C182 0.1UF, C184 0.1UF, C183 0.1UF, C186 0.1UF, C185 0.1UF, C168 47UF 10V, C169 47UF 10V, C170 1UF 16V

VDDIO

3_3VIO

C215 0.1UF, C216 0.1UF, C217 0.1UF, C218 0.1UF, C219 0.1UF, C220 0.1UF, C214 1UF 16V

M1

STIFF_7P

1 2 3 4 5 6 7

3_3V_DS

C28 0.1UF, C29 0.1UF, C31 0.1UF, C32 0.1UF, C34 0.1UF, C35 0.1UF, C36 0.1UF, C37 0.1UF

3_3V

C19 0.1UF, C20 0.1UF, C21 0.1UF, C22 0.1UF, C23 0.1UF, C24 0.1UF, C25 0.1UF, C26 0.1UF

TITLE 89EBPES16T4-2

BYPASS/DECOUPLING CAPS

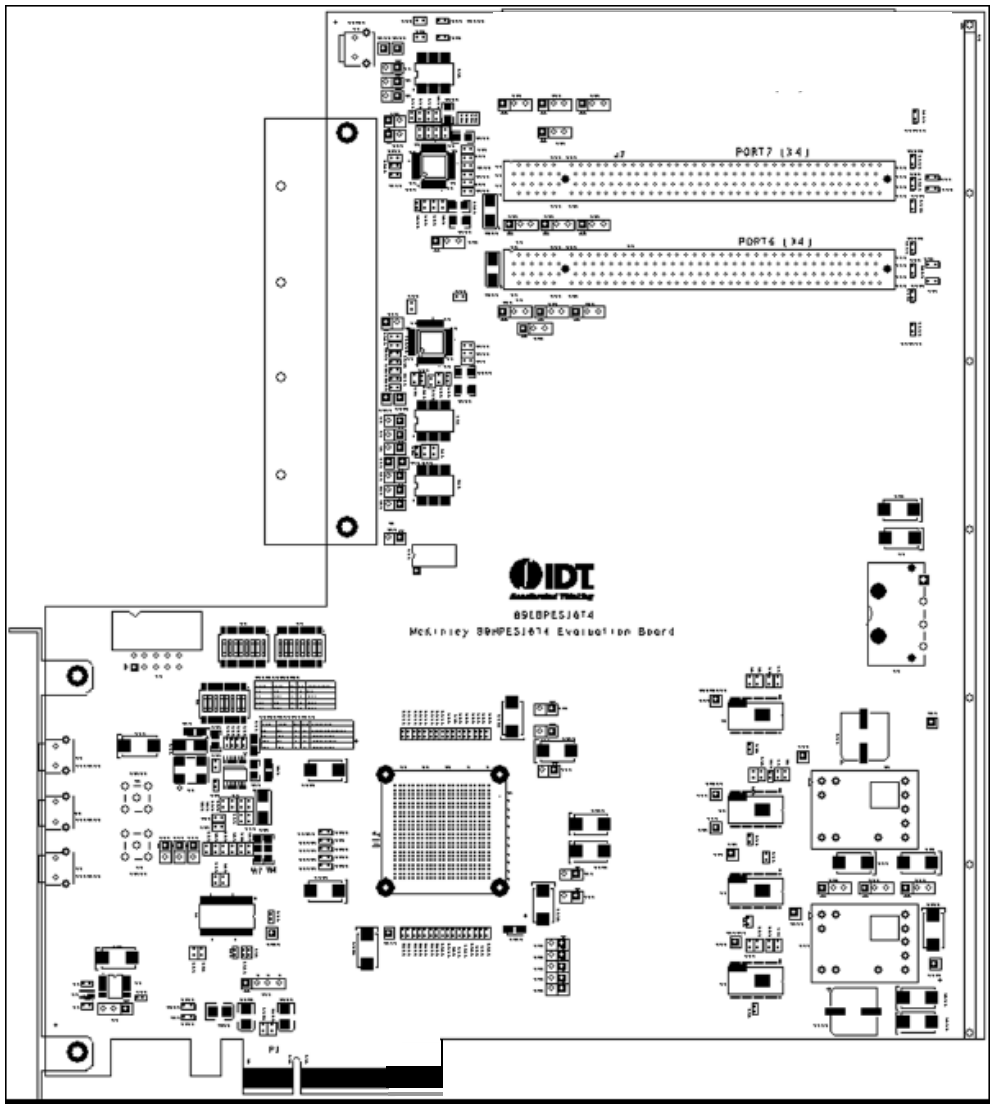
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

Fri May 04 17:44:58 2007 SHEET 12 OF 12

Notes

Locations of Connectors, Jumpers, and Switches



Notes

Software for the EB16T4-2 Eval Board

Notes

Introduction

This chapter discusses some of the main features of the available software to give users a better understanding of what can be achieved with the EB16T4-2 evaluation board using the device management software.

Device management software and related user documentation are available on a CD which is included in the Evaluation Board Kit. This information is also available on IDT's FTP site. For more information, contact IDT at ssdhelp@idt.com.

Device Management Software

The primary use of the Device Management Software package is to enable users of the evaluation board to access all the registers in the PES16T4 device. This access can be achieved using the PCI Express in-band configuration cycles through the upstream port on the PES16T4.

This software also enables users to save a snapshot of the current register set into a dump file which can be used for debugging purposes. An export/import facility is also available to create and use "Configuration" files which can be used to initialize the switch device with specific values in specific registers.

A conversion utility is also provided to translate a configuration file into an EEPROM programmable data structure. This enables the user to program an appropriate serial EEPROM with desirable register settings for the PES16T4, and then to populate that EEPROM onto the Evaluation Board. It is also possible to program the EEPROM directly on the Evaluation Board using a feature provided by the software package.

The front end of the Device Management Software is a user-friendly Graphical User Interface which allows the user to quickly read or write the registers of interest. The GUI also permits the user to run the software in "simulation" mode with no real hardware attached, allowing the creation of configuration files for the PES16T4 in the absence of the actual device.

Much of the Device Management Software is written with device-independent and OS-independent code. The software will be guaranteed to work on Linux (/sys interface) and MS Windows XP. It may function flawlessly on various flavors of MS Windows, but may not be validated on all. The fact that the software is device-independent assures its scalability to future PCIe parts from IDT. Once users are familiar with the GUI, they will be able to use the same GUI on all PCIe parts from IDT. This software is customized for each device through an XML device description file which includes information on the number of ports, registers, types of registers, information on bit-fields within each register, etc.

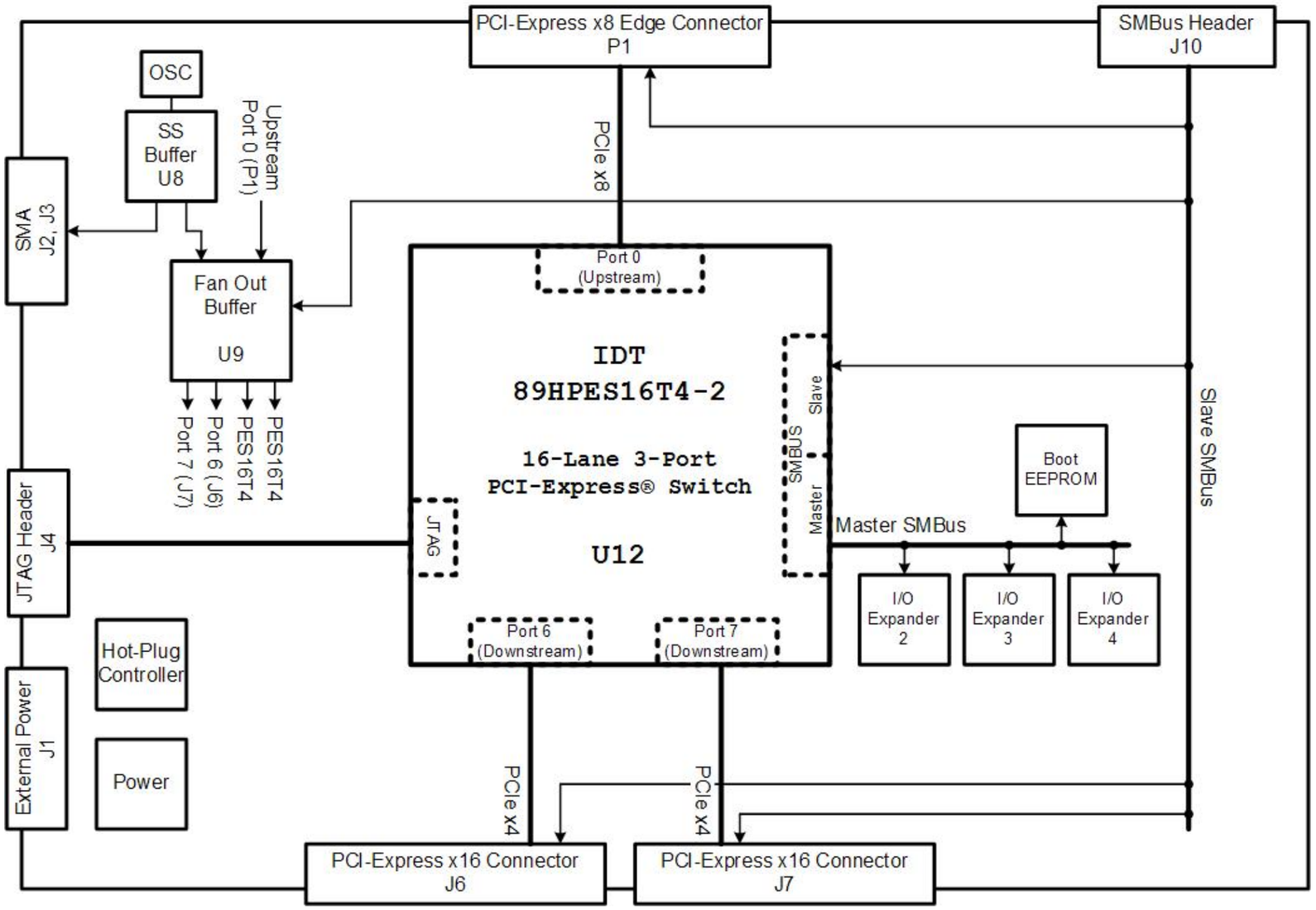
Notes

Schematics

Notes

Schematics

89EBPES16T4-2 – 89HPES16T4-2 Evaluation Board



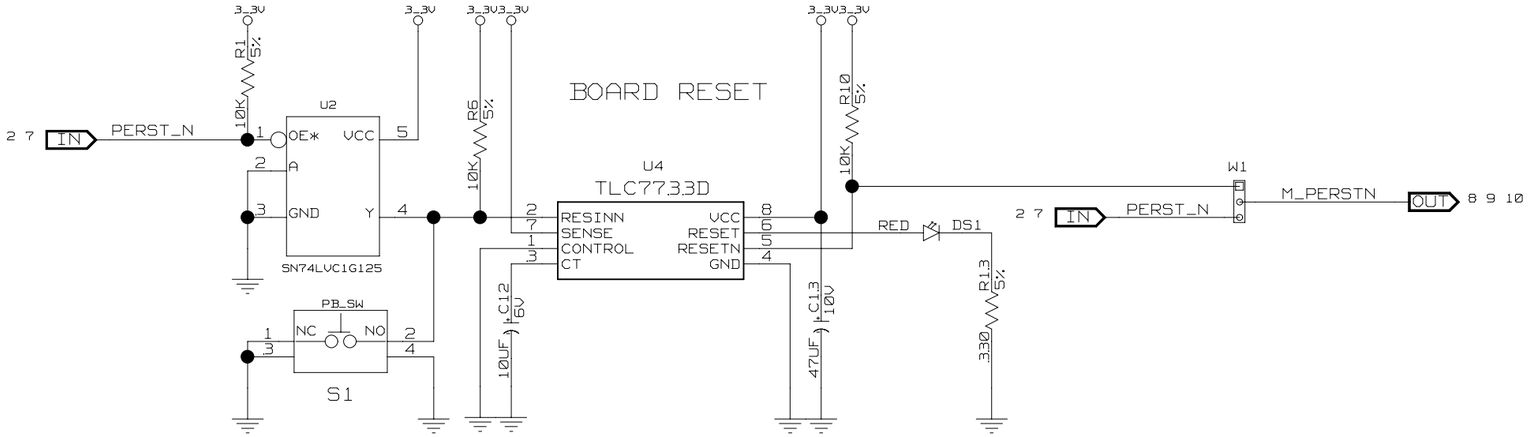
REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
STGC-0113R01	1.0	INITIAL RELEASE	2007-05-08	J. CARRILLO/K. LEUNG

SHEET DESCRIPTION

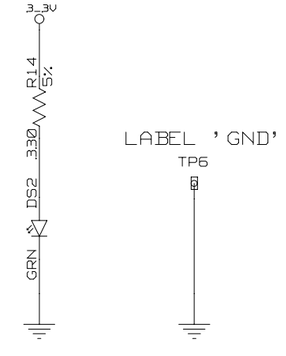
TITLE			
89EBPES16T4-2			
SIZE: B	DRAWING NO.: STGSCH-00113	FAB P/N: 18-633-000	REV.: 1.0
AUTHOR: J. CARRILLO / K. LEUNG		CHECKED BY: J. CARRILLO / K. LEUNG	
Tue May 08 11:34:21 2007		SHEET 1 OF 12	

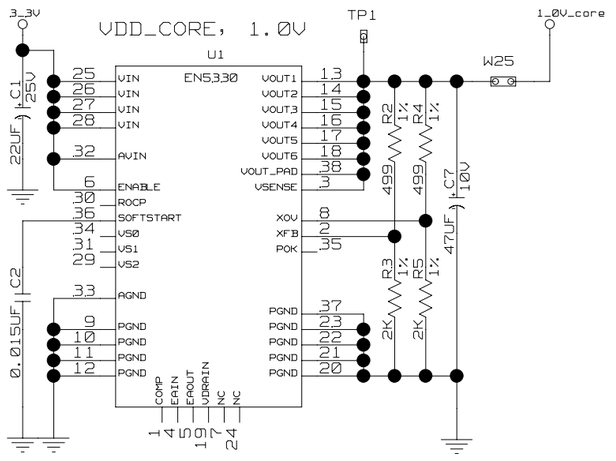
RENESAS

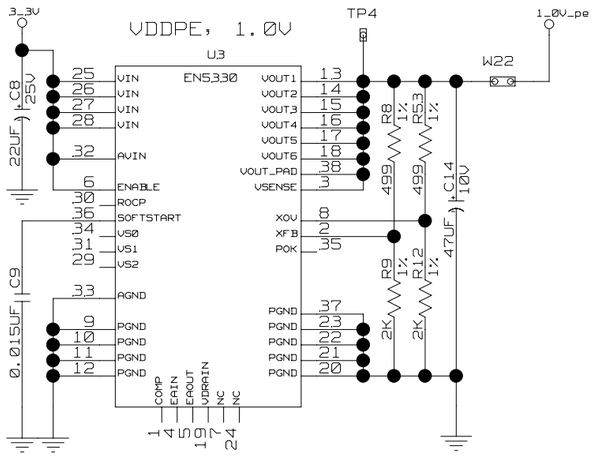
BOARD RESET

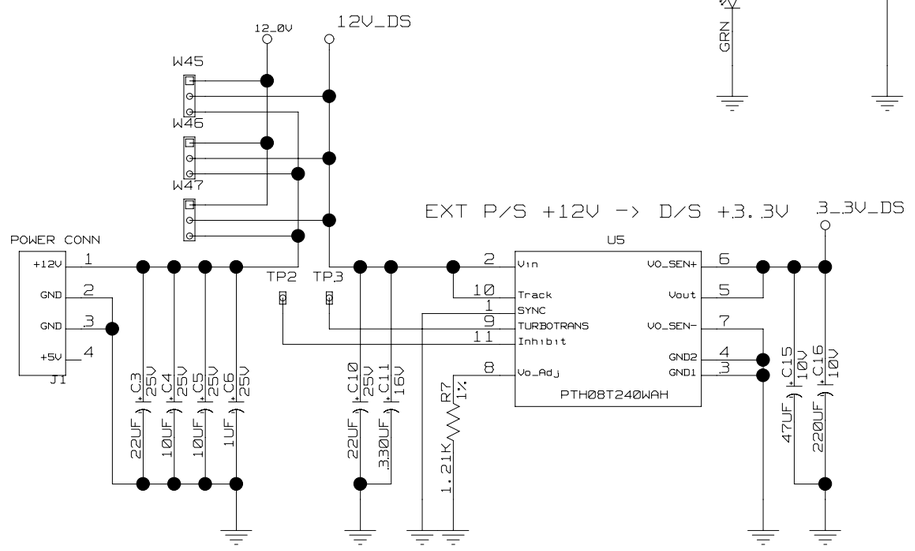


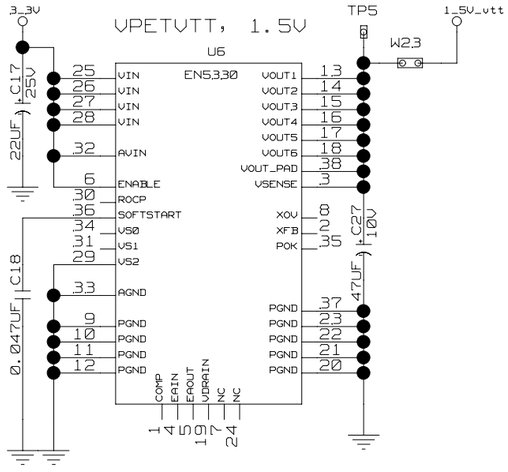
POWER INDICATOR
PLACE NEAR TOP EDGE
LABEL 'POWER'

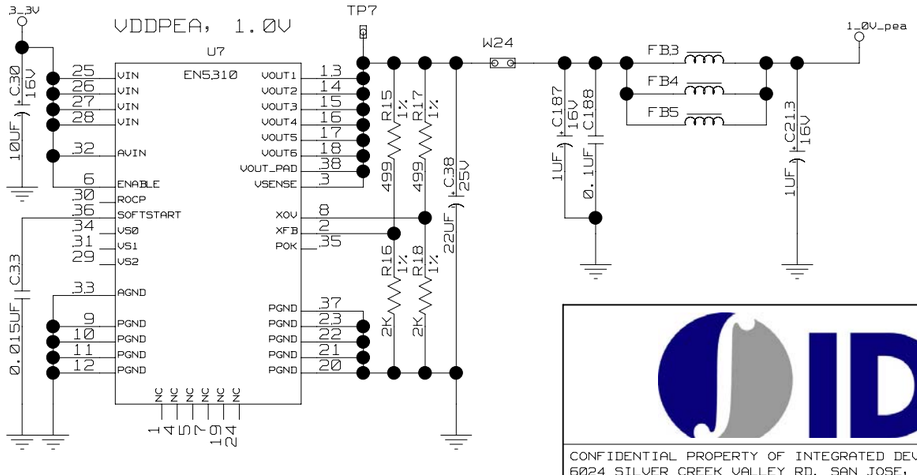


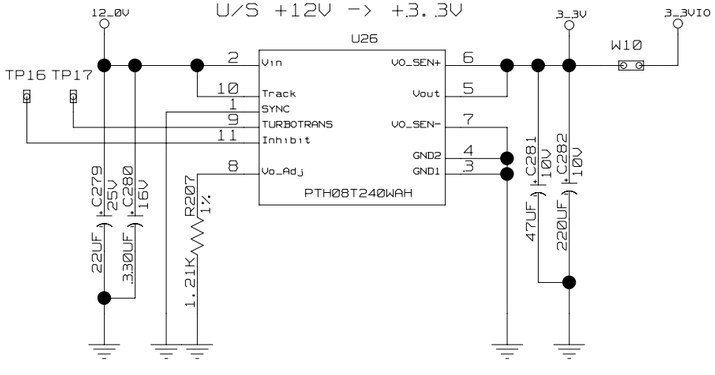






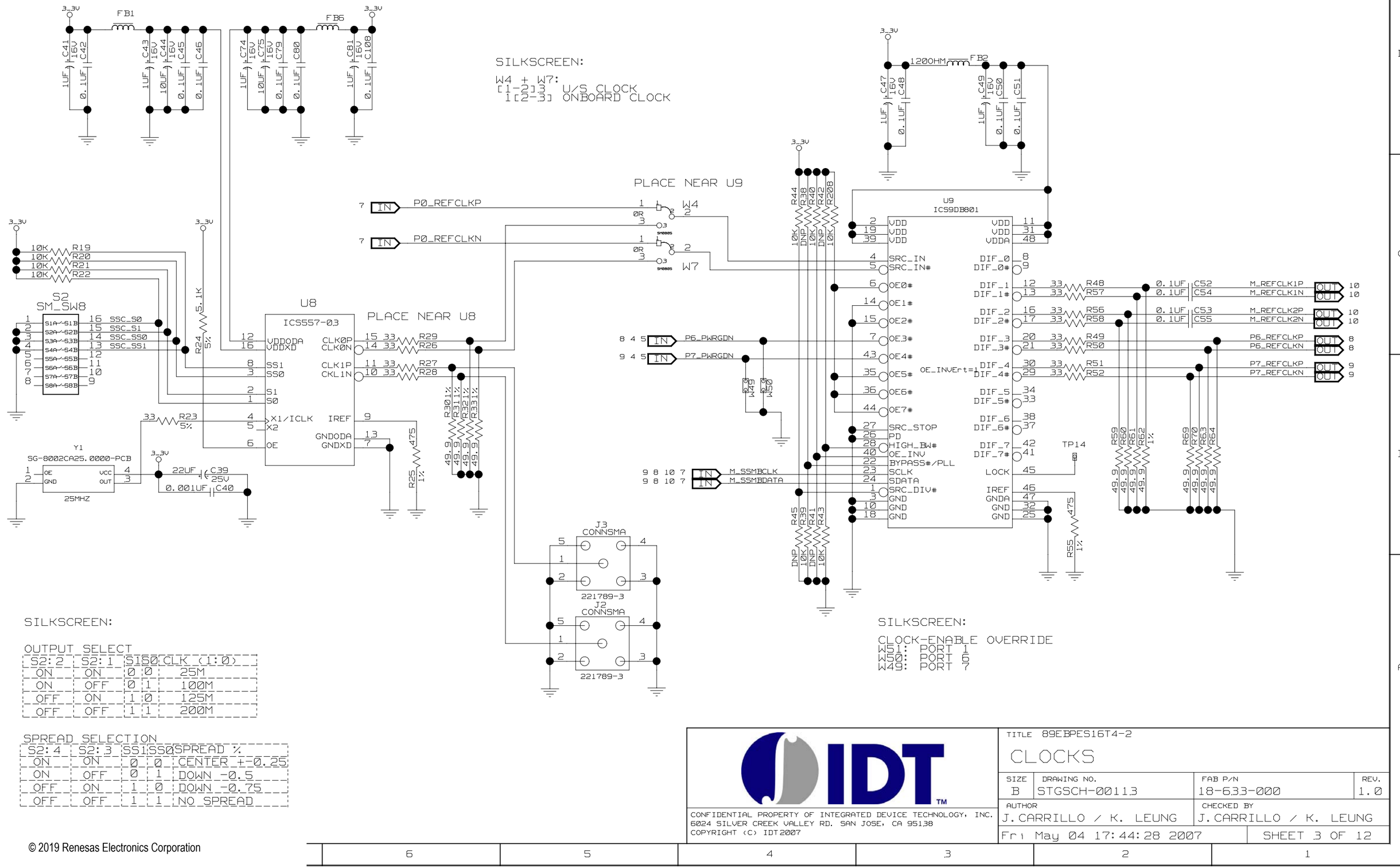






IDT™

TITLE 89EBPES16T4-2			
POWER SUPPLY AND RESET			
SIZE B	DRAWING NO. STGSCH-00113	FAB P/N 18-6333-000	REV. 1.0
AUTHOR J. CARRILLO / K. LEUNG		CHECKED BY J. CARRILLO / K. LEUNG	
Fri May 04 17:30:07 2007		SHEET 2 OF 12	



SILKSCREEN:

OUTPUT SELECT

S2:2	S2:1	SS1	SS0	CLK (1:0)
ON	ON	0	0	25M
ON	OFF	0	1	100M
OFF	ON	1	0	125M
OFF	OFF	1	1	200M

SPREAD SELECTION

S2:4	S2:3	SS1	SS0	SPREAD %
ON	ON	0	0	CENTER +-0.25
ON	OFF	0	1	DOWN -0.5
OFF	ON	1	0	DOWN -0.75
OFF	OFF	1	1	NO SPREAD

SILKSCREEN:

CLOCK-ENABLE OVERRIDE
W51: PORT 1
W50: PORT 0
W49: PORT 7

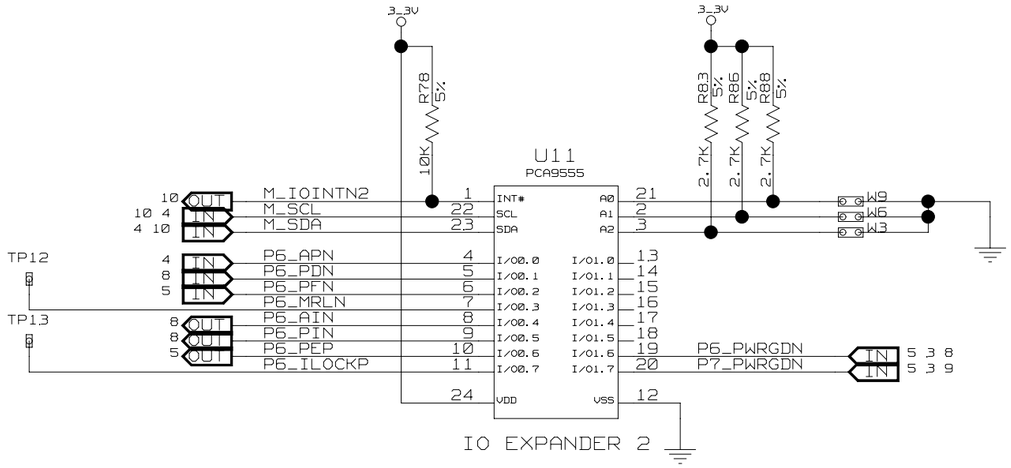
TITLE 89EBPES16T4-2

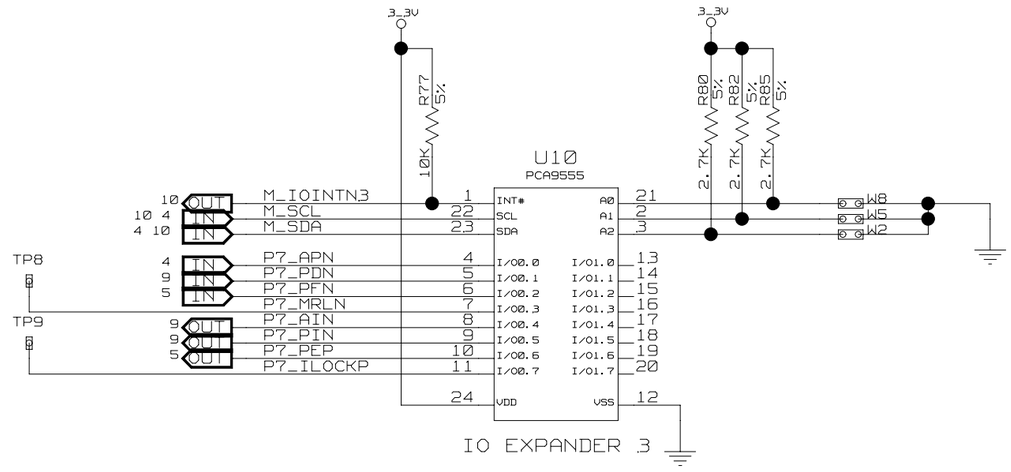
CLOCKS

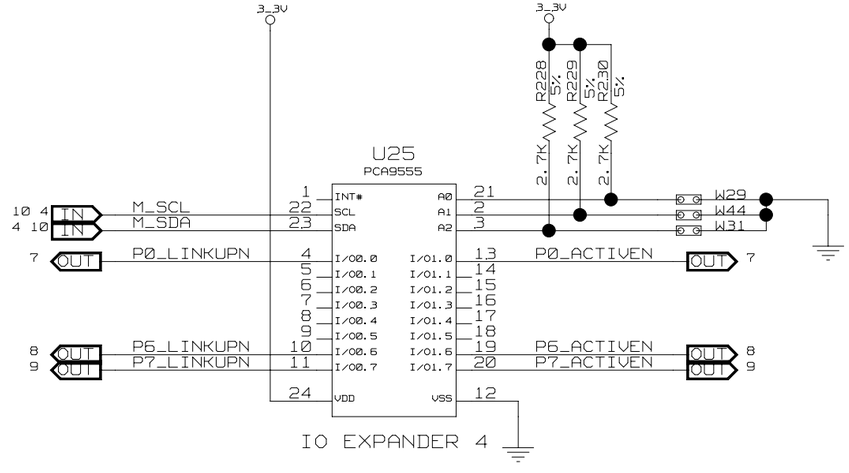
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

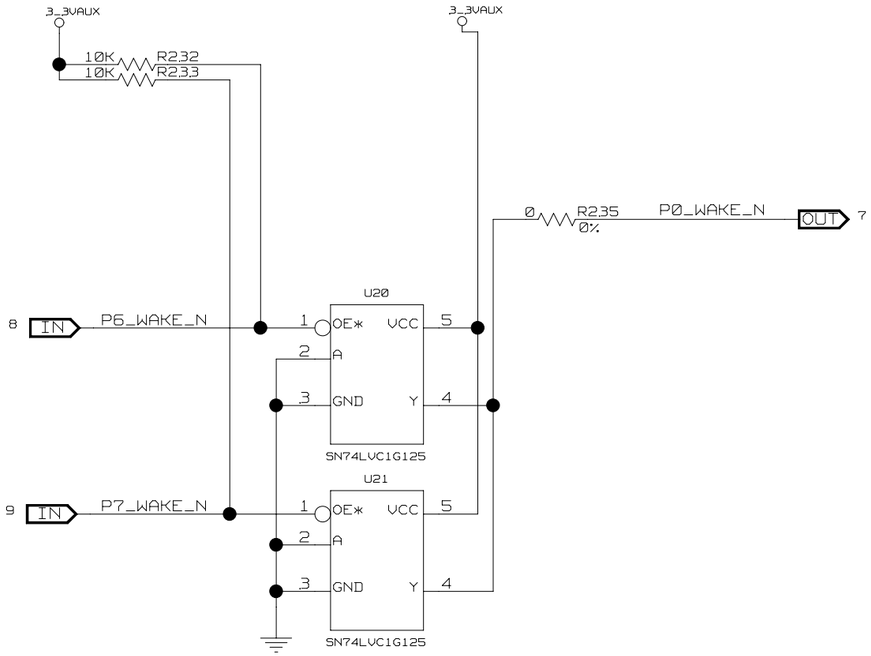
AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

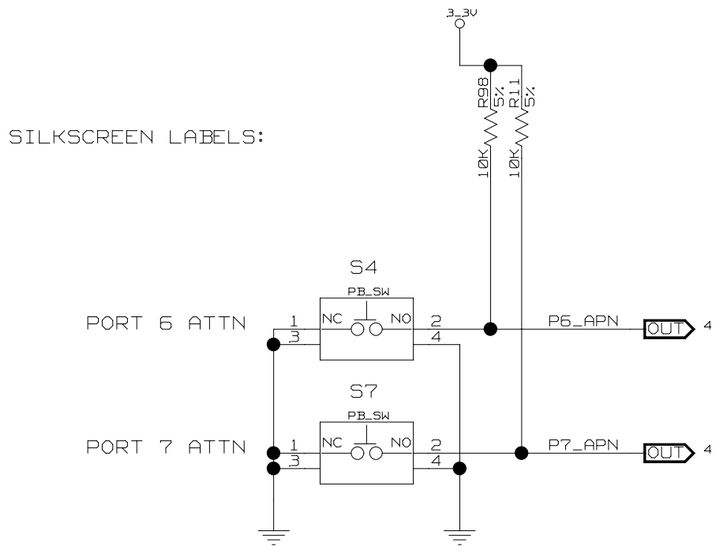
Fri May 04 17:44:28 2007 SHEET 3 OF 12











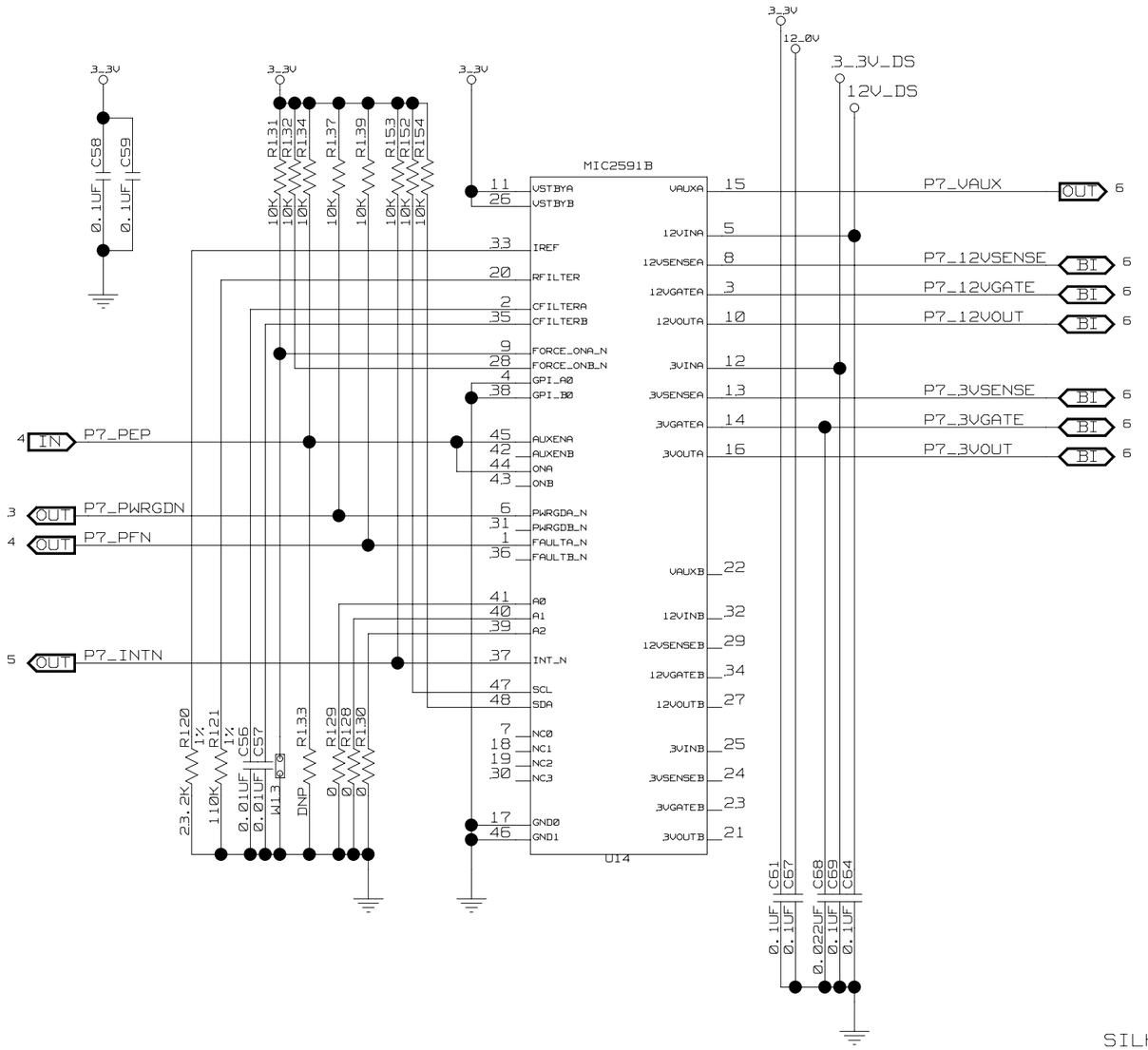
TITLE 89EBPES16T4-2

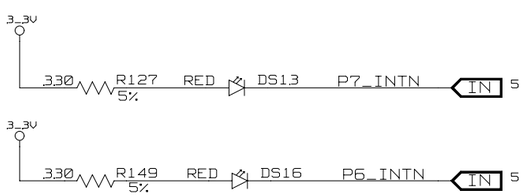
IO EXP, WAKE, ATTN BUTTONS

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

AUTHOR	CHECKED BY
J.CARRILLO / K. LEUNG	J.CARRILLO / K. LEUNG

Fri May 04 17:44:31 2007 — SHEET 4 OF 12





SILKSCREEN LABEL:

W13: P7 FORCE ON

W17: P6 FORCE ON

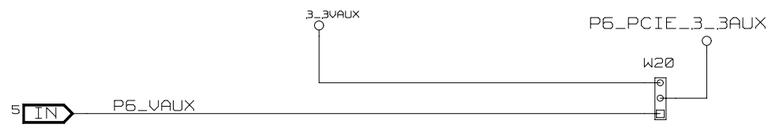
TITLE 89EBPES16T4-2

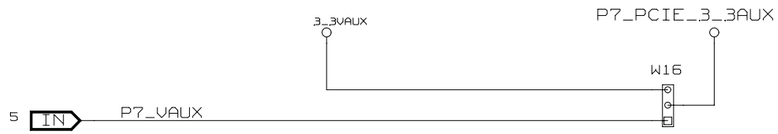
HOT PLUG CONTROLLERS

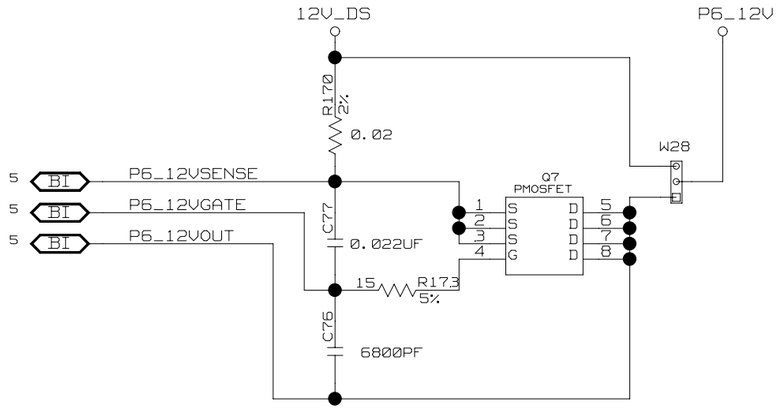
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

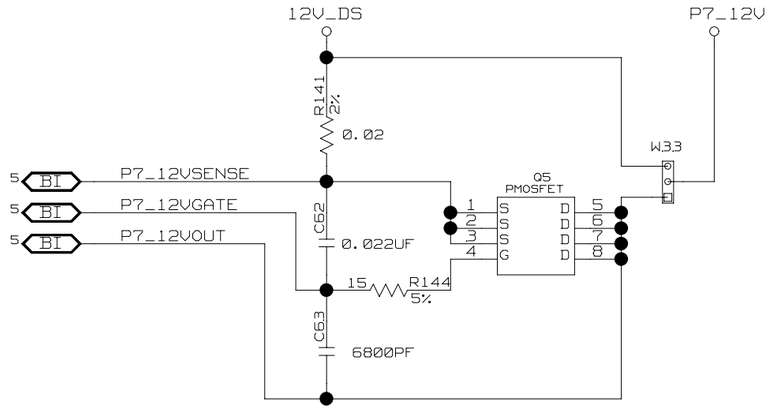
AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

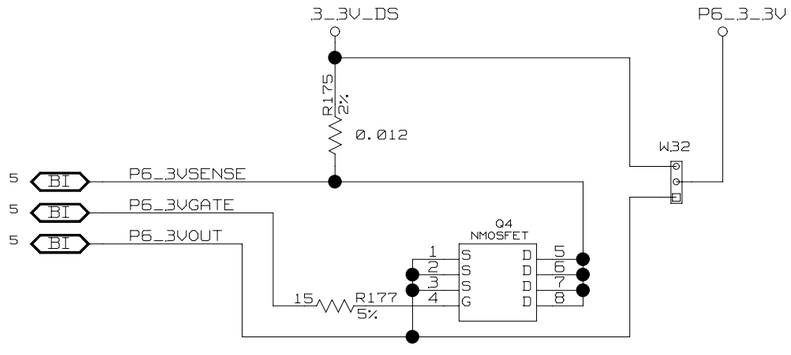
Fri May 04 17:44:37 2007 | SHEET 5 OF 12

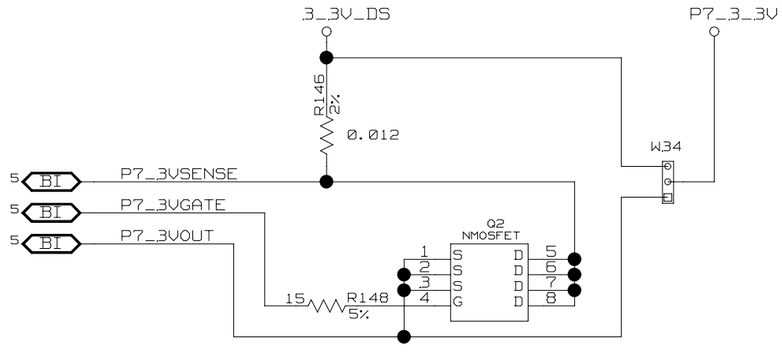












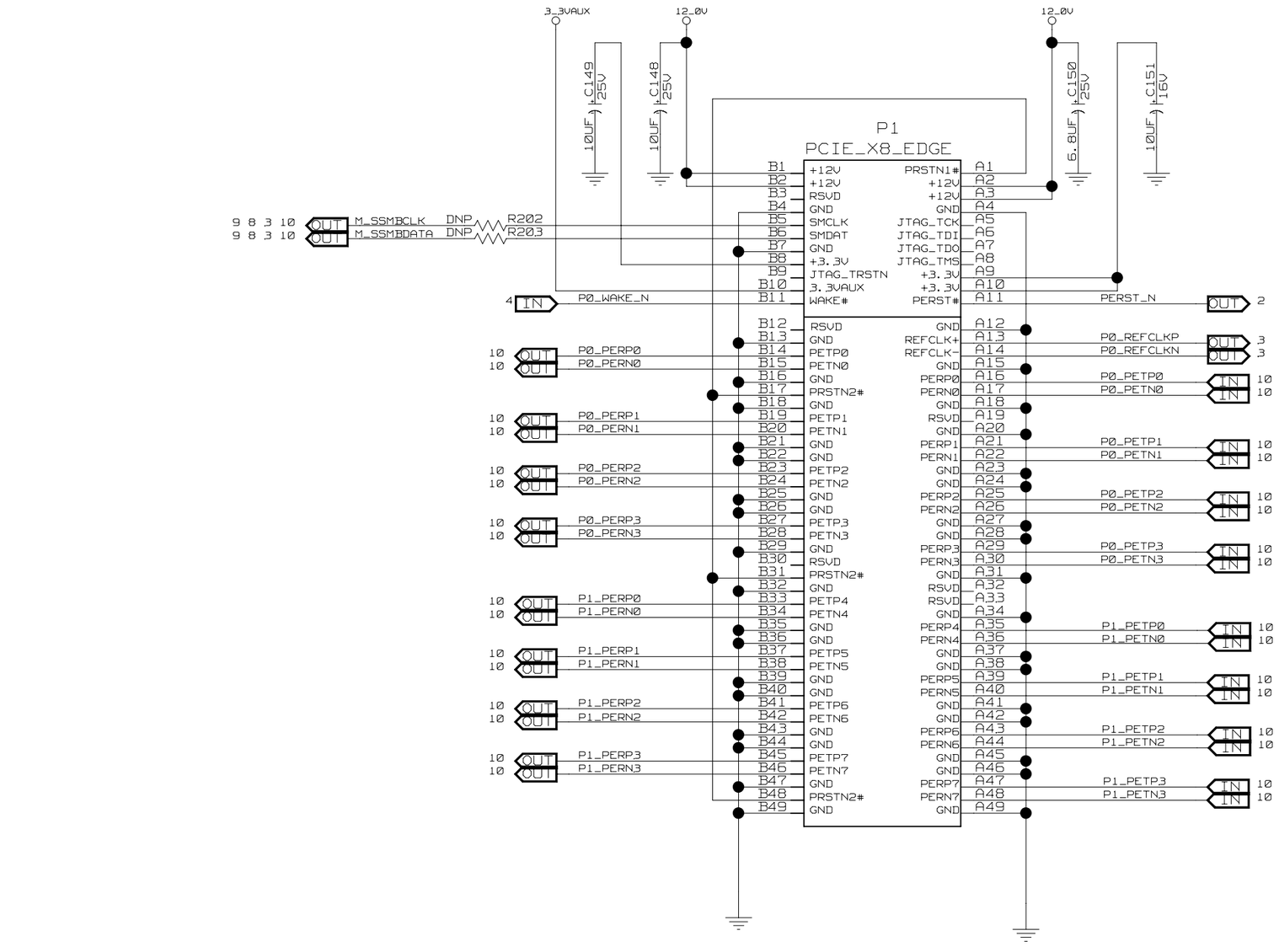
TITLE 89EBPES16T4-2

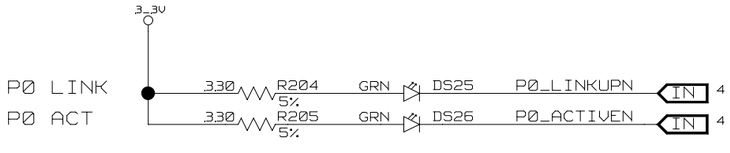
HOT PLUG MOSFETS

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

Fri May 04 17:44:40 2007 — SHEET 6 OF 12





CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
COPYRIGHT (C) IDT 2007

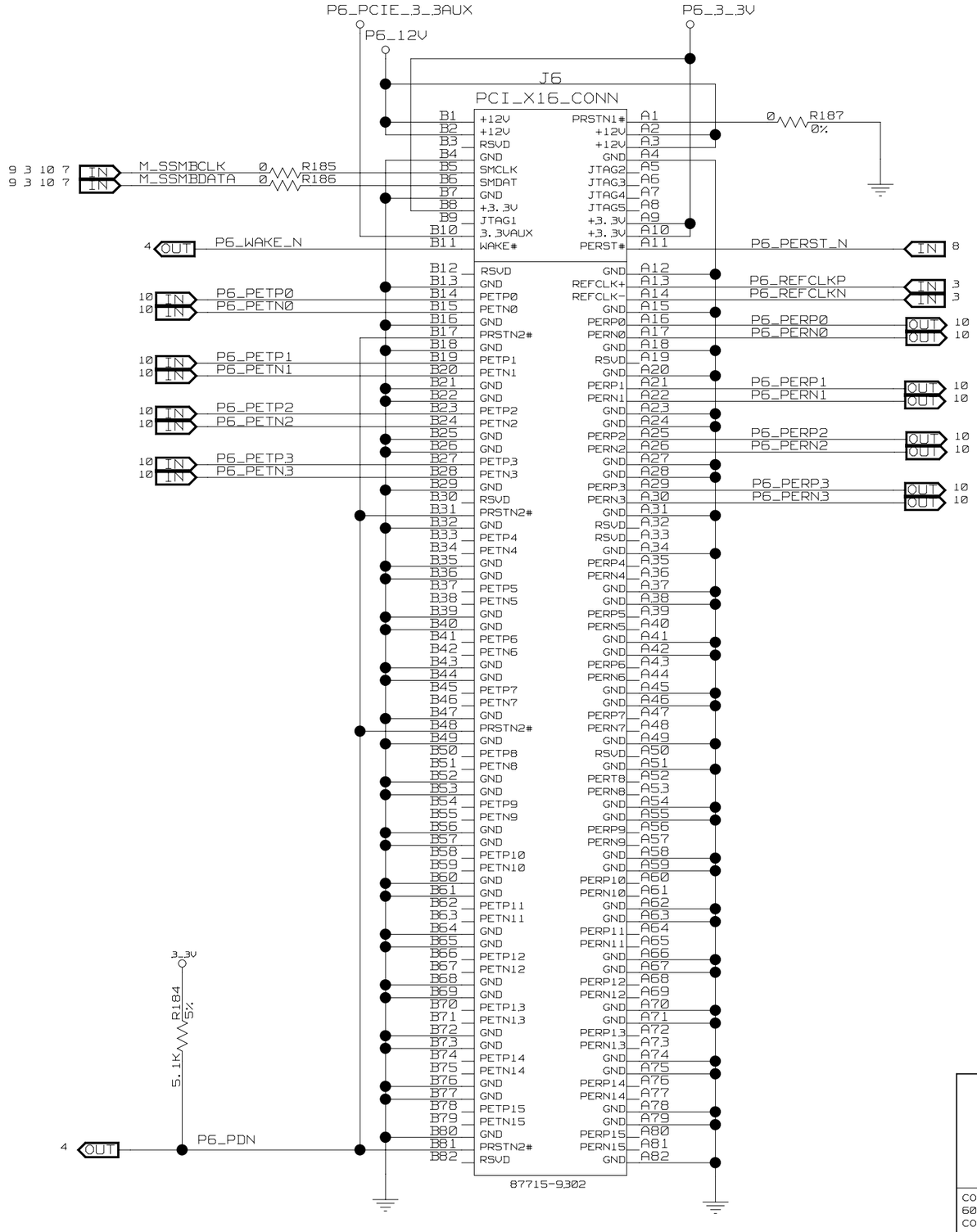
TITLE 89EBPES16T4-2

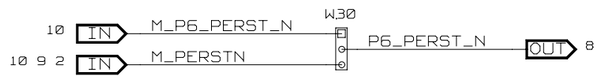
PORT 0 UPSTREAM EDGE CONN.

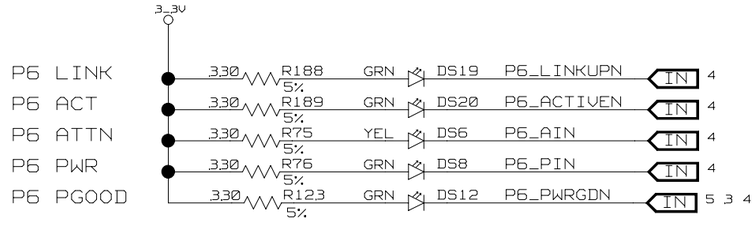
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

Fri May 04 17:44:43 2007 SHEET 7 OF 12







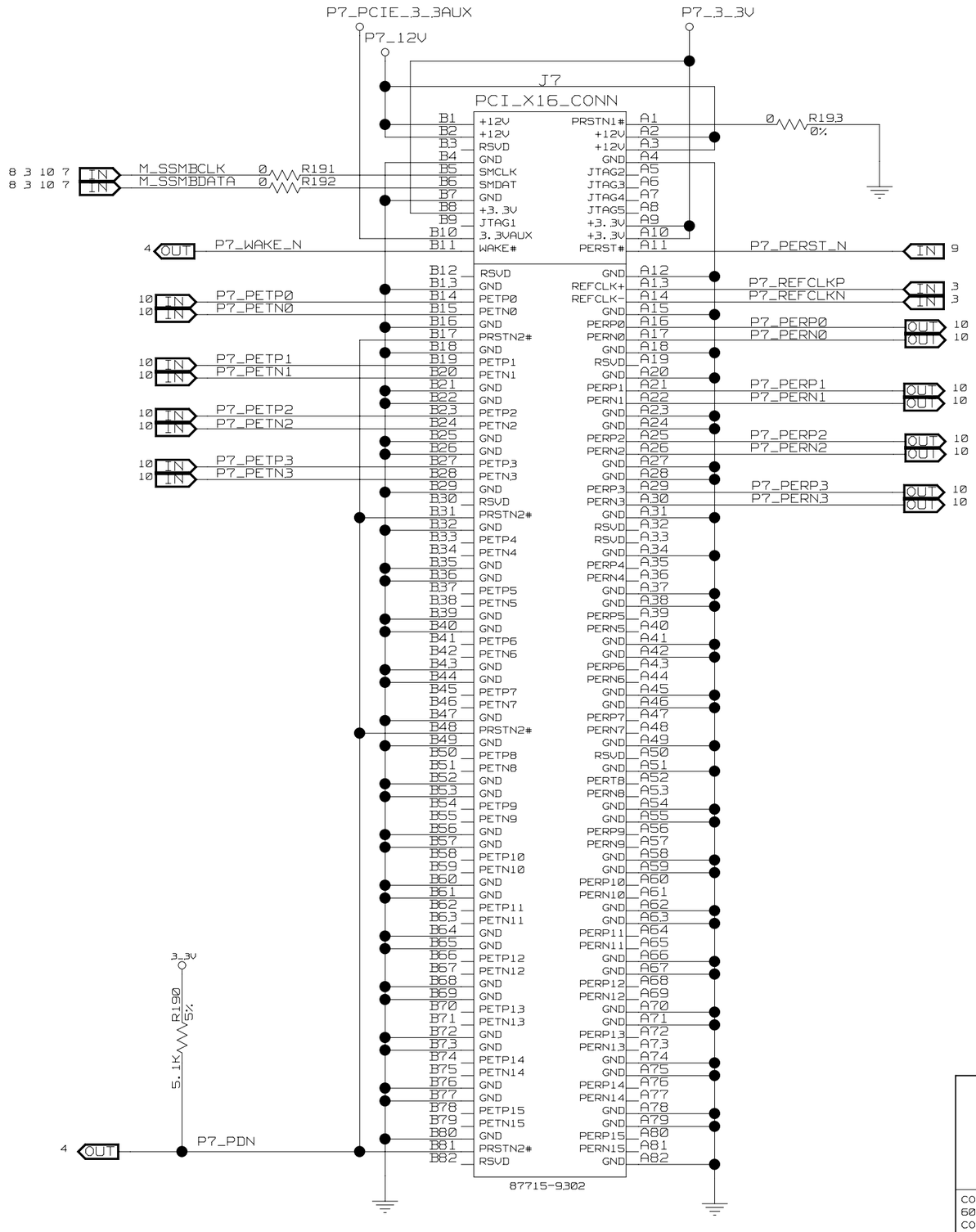
TITLE 89EBPES16T4-2

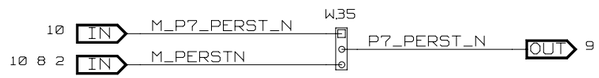
PORT 6 CONNECTOR

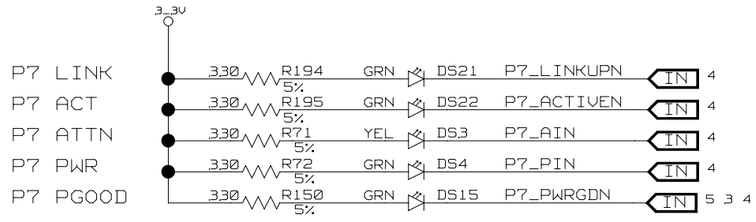
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

Fri May 04 17:44:46 2007 — SHEET 8 OF 12







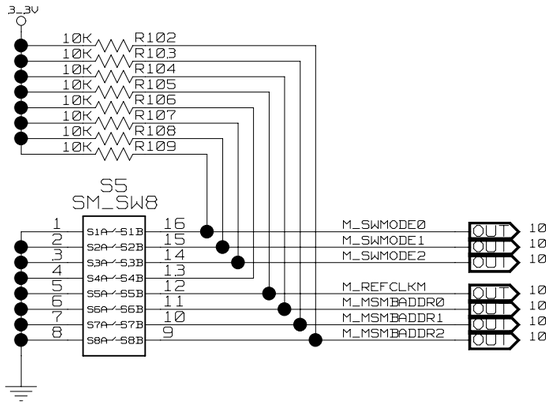
TITLE 89EBPES16T4-2

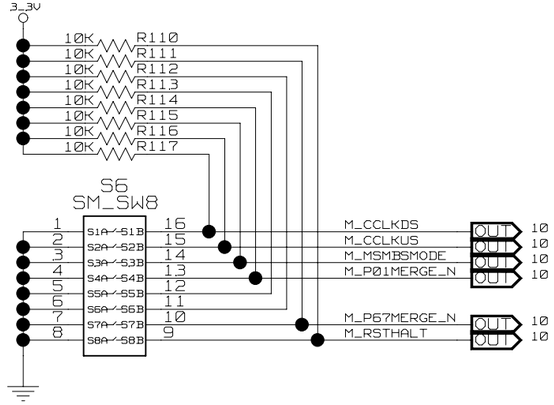
PORT 7 CONNECTOR

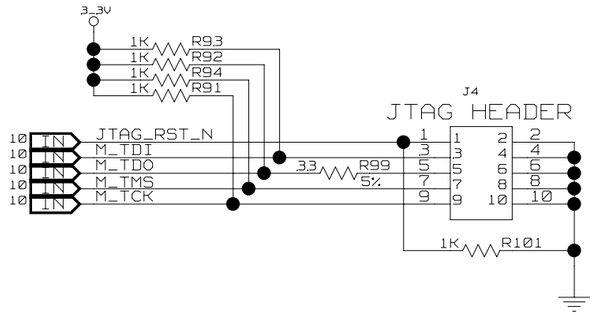
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

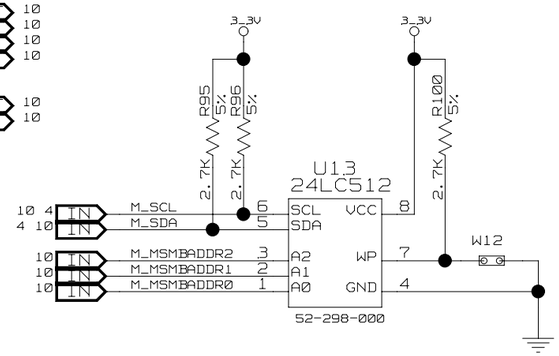
AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

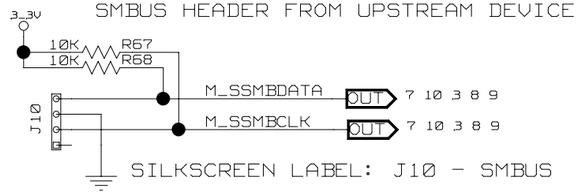
Fri May 04 17:44:49 2007 — SHEET 9 OF 12

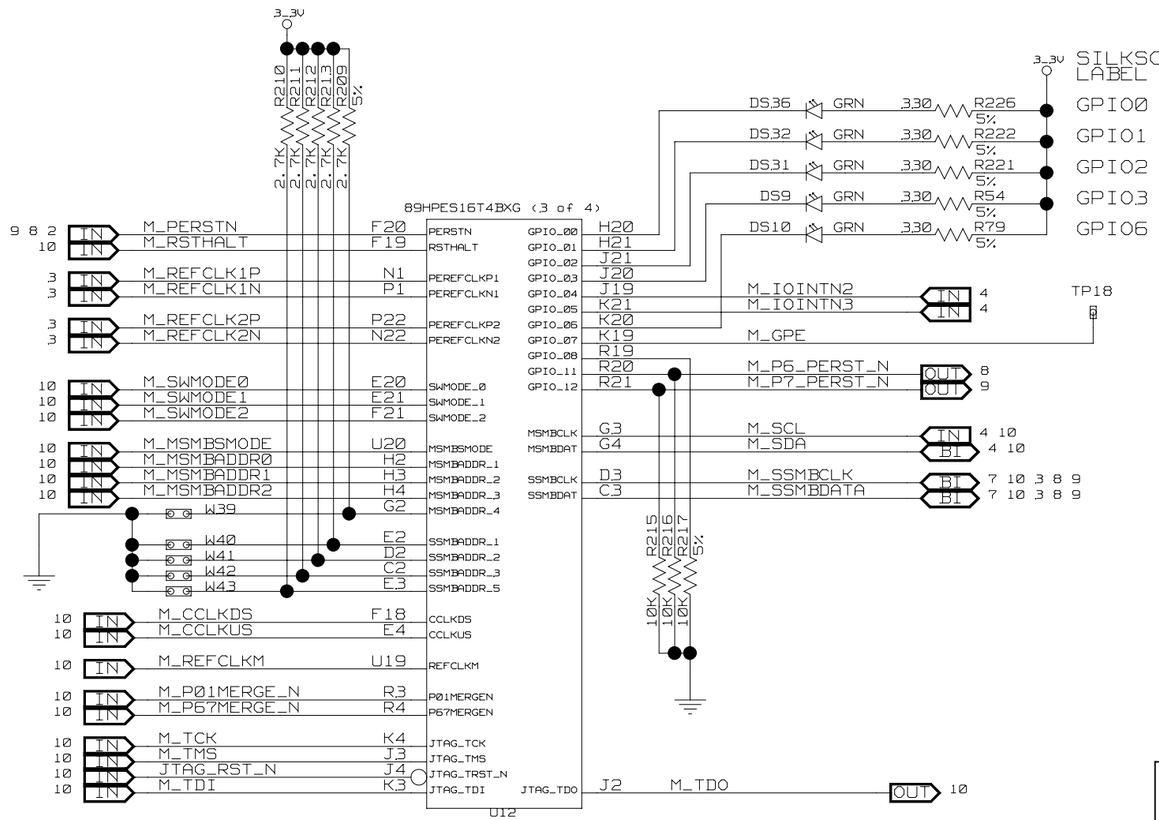


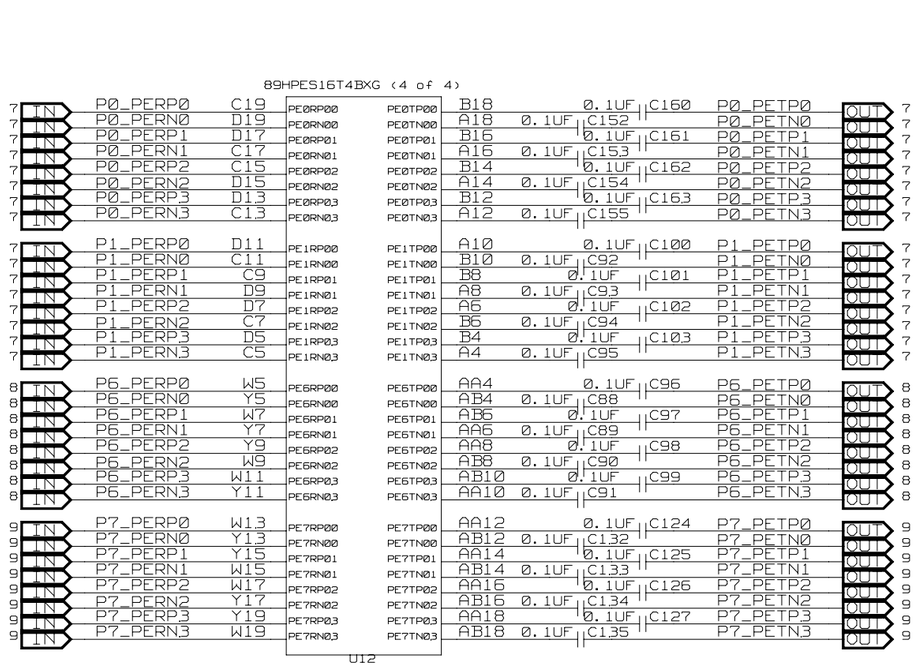












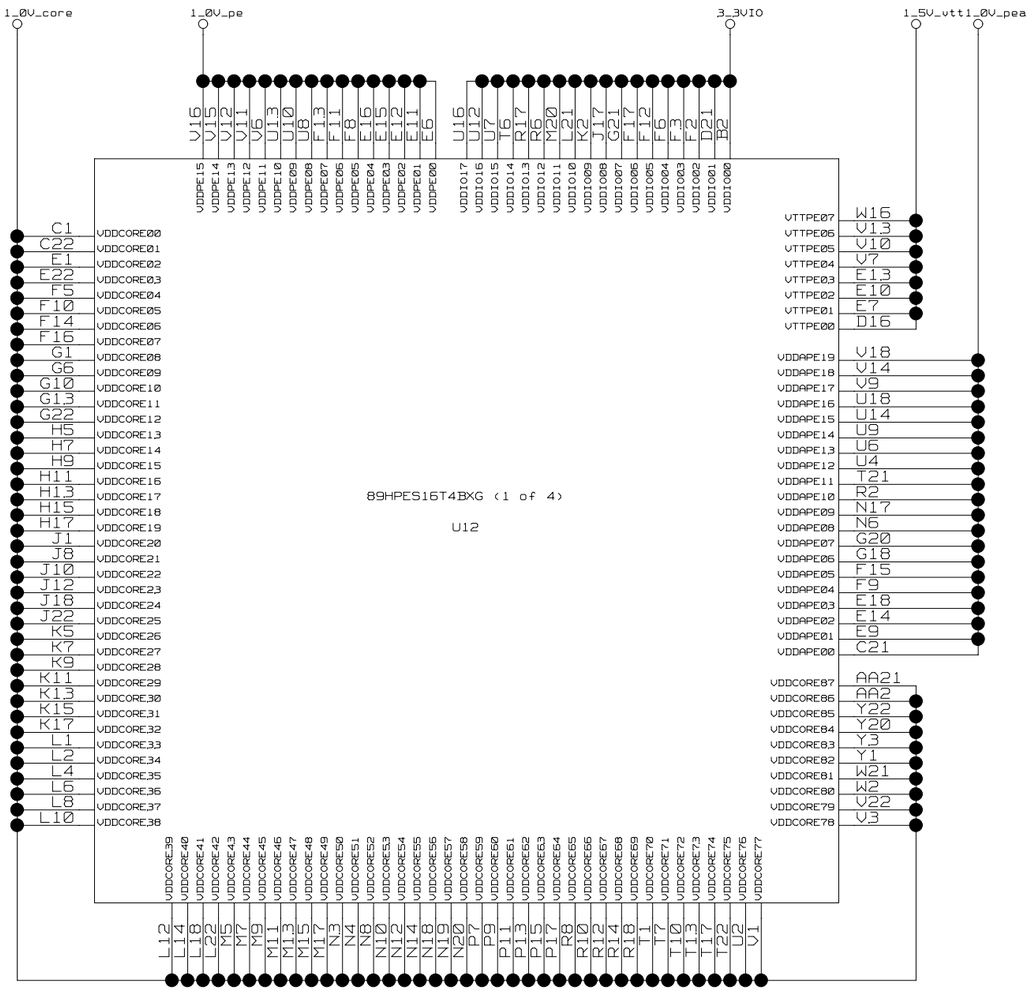
TITLE 89EBPES16T4-2

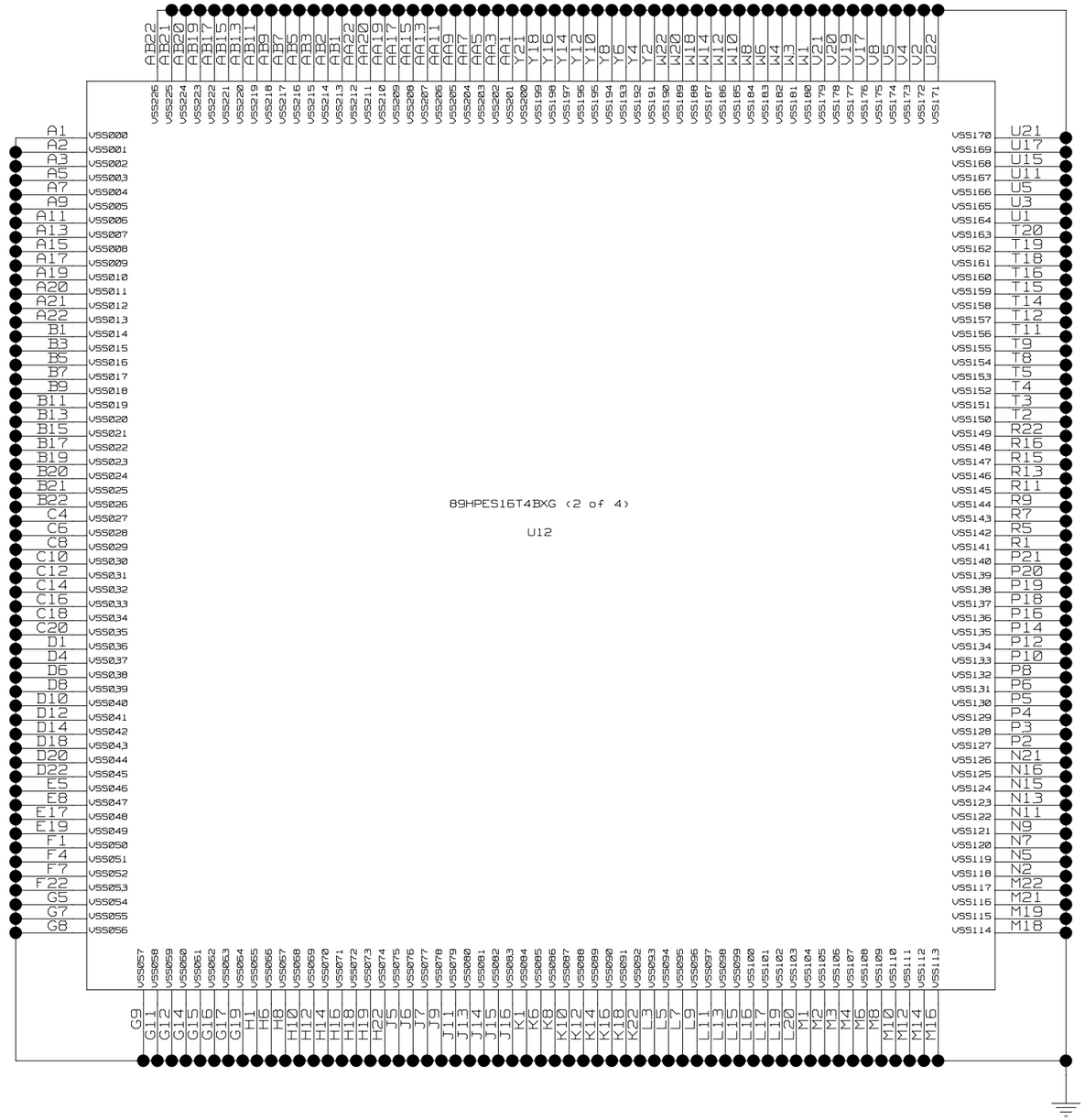
89HPES16T4-2

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

Tue May 08 11:31:37 2007 — SHEET 10 OF 12





TITLE 89EBPES16T4-2

89HPES16T4-2 - POWER

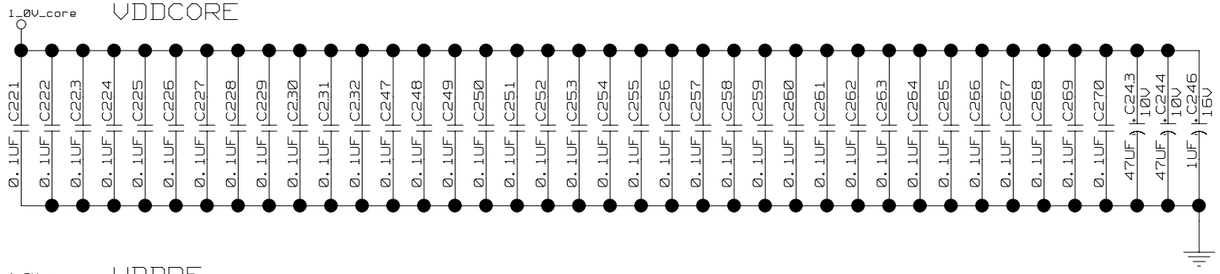
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

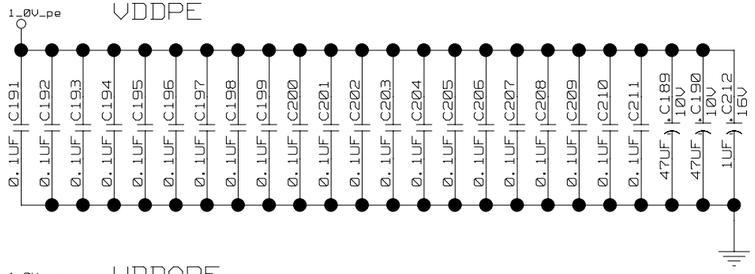
Fri May 04 17:44:56 2007 SHEET 11 OF 12

RENESAS

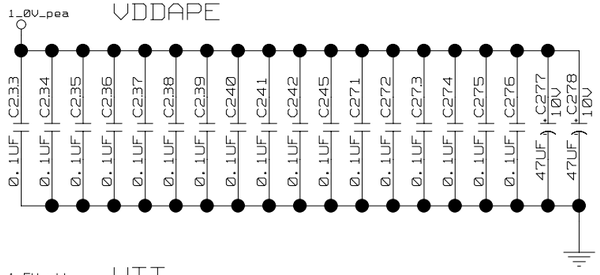
1_0V_core VDDCORE



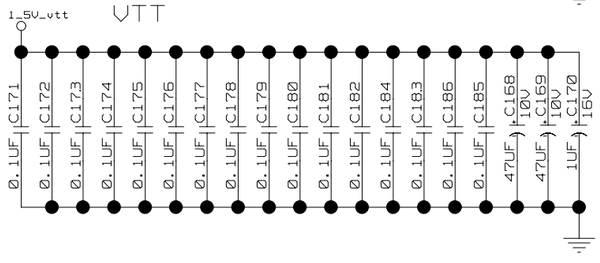
1_0V_pe VDDPE



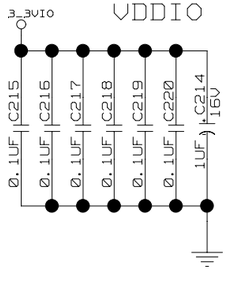
1_0V_pea VDDAPE



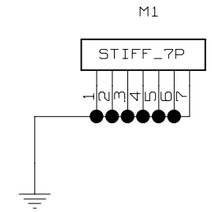
1_5V_vtt VTT



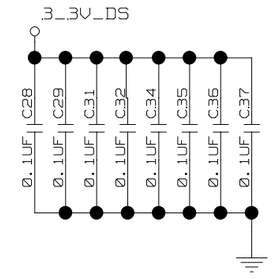
3_3VIO VDDIO



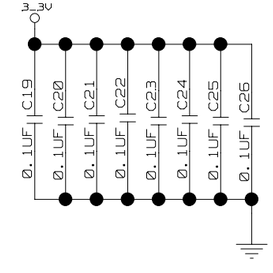
M1



3_3V_DS



3_3V



TITLE 89EBPES16T4-2

BYPASS/DECOUPLING CAPS

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00113	18-633-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO / K. LEUNG	J. CARRILLO / K. LEUNG

Fri May 04 17:44:58 2007 SHEET 12 OF 12

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.