



IDT™ 89EBPES12N3 Evaluation Board Manual

(Eval Board: 18-597-001)

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Description of the EB12N3 Eval Board

Notes

Introduction

The 89HPES12N3 switch (also referred to as PES12N3 in this manual) is a member of IDT's PCI Express standard (PCIe) based line of products. It is a 3 port switch, with 4 serial lanes per port (x4). One upstream port is provided for connecting to the root complex (RC), and two downstream ports are available for connecting to PCIe endpoints or to another switch. More information on this device can be found in the 89HPES12N3 User Manual.

The 89BPES12N3 Evaluation Board (also referred to as EB12N3 in this manual) provides an evaluation platform for the PES12N3 switch. It is also a cost effective way to add a PCIe downstream port (x4) to an existing system with a limited number of PCIe downstream ports. The EB12N3 eval board is designed to function as an add-on card to be plugged into a x4 PCIe slot available on a motherboard hosting an appropriate root complex and microprocessor(s). The EB12N3 is a vehicle to test and evaluate the functionality of the PES12N3 chip, and it can also play an important role for customers to get a headstart on software development while they await the arrival of their own hardware. It is also used inside IDT to reproduce system level hardware or software issues reported by customers. Figure 1.1 illustrates the functional block diagram representing the main parts of the EB12N3 board.

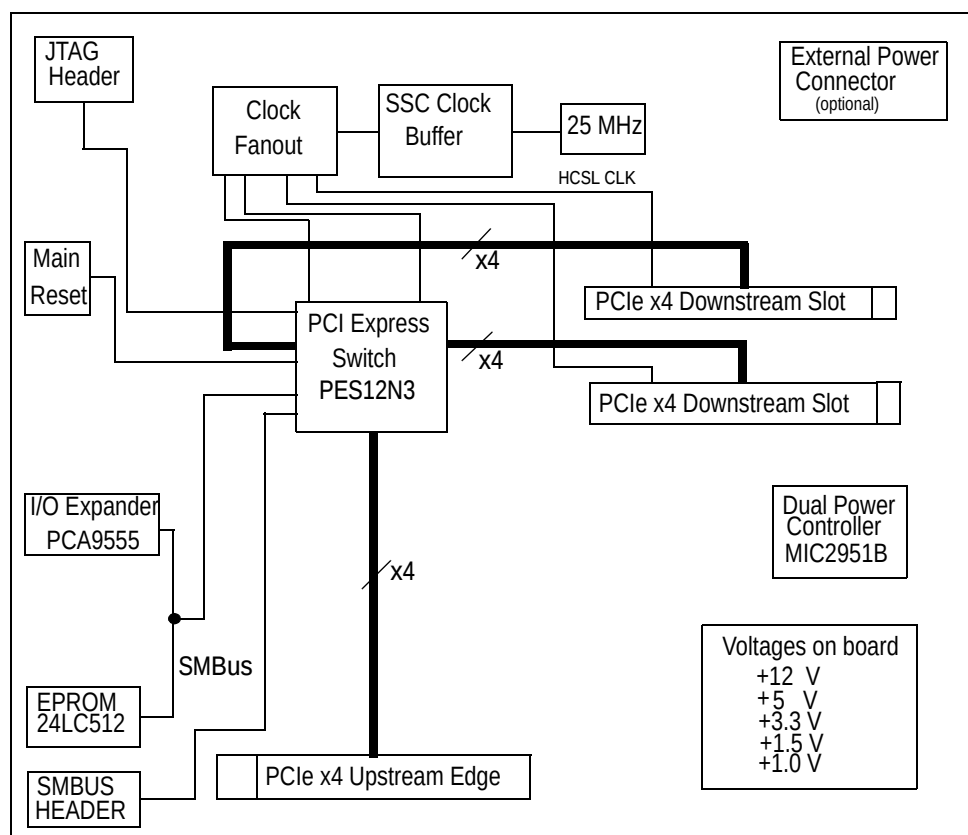


Figure 1.1 Functional Block Diagram of the EB12N3 Eval Board

Notes

Board Features

Hardware

- ◆ *PES12N3 PCIe 3 port switch*
 - Three x4 ports, 12 PCIe lanes
 - PCIe Base Specification Revision 1.0a compliant
 - 48 Gbps aggregate switching capacity
 - 128 to 2048 byte maximum payload size
 - Static lane reversal and polarity inversion supported on all lanes
 - Automatic per port link width negotiation to x4, x2, x1
 - Can load configuration from serial EEPROM via SMBUS
- ◆ *x4 PCIe Connectors*
 - One edge connector on the upstream port, to be plugged into a x4 slot on a host motherboard
 - Two slot connectors on the downstream ports, for PCIe endpoint add-on cards to be plugged in
- ◆ *Numerous user selectable configurations set using onboard jumpers and DIP-switches*
 - Source of clock - host clock or onboard clock generator
 - multiple clock rates and spread spectrum settings
 - Boot mode selection
- ◆ *SMBUS Slave Interface (4 pin header)*
- ◆ *SMBUS Master Interface connected to two optional Serial EEPROMs through I/O expander*
 - Facilitates testing with two different settings of initialization data with a simple change of a jumper
 - Only one EEPROM can be selectively connected to the SMBUS at a time
- ◆ *"Attention" button for each port to initiate a hot swap event on each port*
- ◆ *4 pin connector for optional external power supply Push button for Warm Reset*
- ◆ *Several LEDs to display status, reset, power, "Attention", etc.*
- ◆ *One 10 pin JTAG connector (pitch 2.54 mm x 2.54 mm)*

Software

There is no software or firmware executed on the board. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the PES12N3 within host systems running popular operating systems.

- ◆ *Installation programs*
 - Operating Systems Supported: Windows2000, WindowsXP, Linux
- ◆ *GUI based application for Windows and Linux*
 - Allows users to view and modify registers in the PES12N3
 - Binary file generator for programming the serial EEPROMs attached to the SMBUS

Other

A metal bracket is required to hold firmly in place the two endpoints plugged into the EB12N3 board.

An external power supply may be required under some conditions.

SMBUS cable may be required for certain evaluation exercises.

SMA connectors are provided on the EB12N3 board for specific test points.

Notes

Revision History

September 26, 2006: Initial publication of board manual.

November 2, 2006: Added footnote to Table 2.10 regarding default setting for switch mode pins.

Notes



Installation of the EB12N3 Eval Board

Notes

EB12N3 Installation

This chapter discusses the steps required to configure and install the EB12N3 evaluation board. All available DIP switches and jumper configurations are explained in details.

The primary installation steps are:

1. Configure jumper/switch options suitable to the evaluation or application requirements.
2. Connect PCI Express endpoint cards to the downstream port PCIe slots on evaluation board.
3. Insert Evaluation Board into the host system (motherboard with root complex chipset).
4. Apply power to the host system.

The EB12N3 board is shipped with all jumpers and switches configured to their default settings, and in general, they do not require further modification or setup.

Hardware Description

The PES12N3 is a 12 lane, 3-port PCI Express switch. It is a peripheral chip that performs PCI Express based switching with a feature set optimized for high performance x4 applications such as servers and storage. It provides fan-out and switching functions between a PCI Express upstream port and two downstream ports or peer-to-peer switching between downstream ports.

The PES12N3 has two PCI Express x4 downstream ports accessible through two x4 connectors. Each port is capable of negotiating a x1, x2, or x4 link width. All endpoint cards connected to the 89EBPES12N3 must support at least one of these link widths.

Basic requirements for the board to run are:

- ◆ *Host system with a PCI Express root complex supporting x4 configuration through a PCI Express x4 slot.*
- ◆ *x1, x2, or x4 PCI Express Endpoint Cards.*

Host System

The evaluation board cannot be operated as a standalone unit. A host system implementing a PCI Express root complex supporting x4 configuration through a PCI Express x4 slot is required to take full advantage of the PES12N3's capabilities. One such system is the SuperMicro X6DH8-G2 motherboard equipped with an Intel E7520 chipset which was introduced in 2004 to deploy dual-processor server chipset technology. The board has three PCI Express slots. All slots have x8 connectors. However, only two have a x8 link width (J15 and J16). The remaining slot has a x4 link width. Refer to Figure 2.1 to identify the proper connectors.

Notes

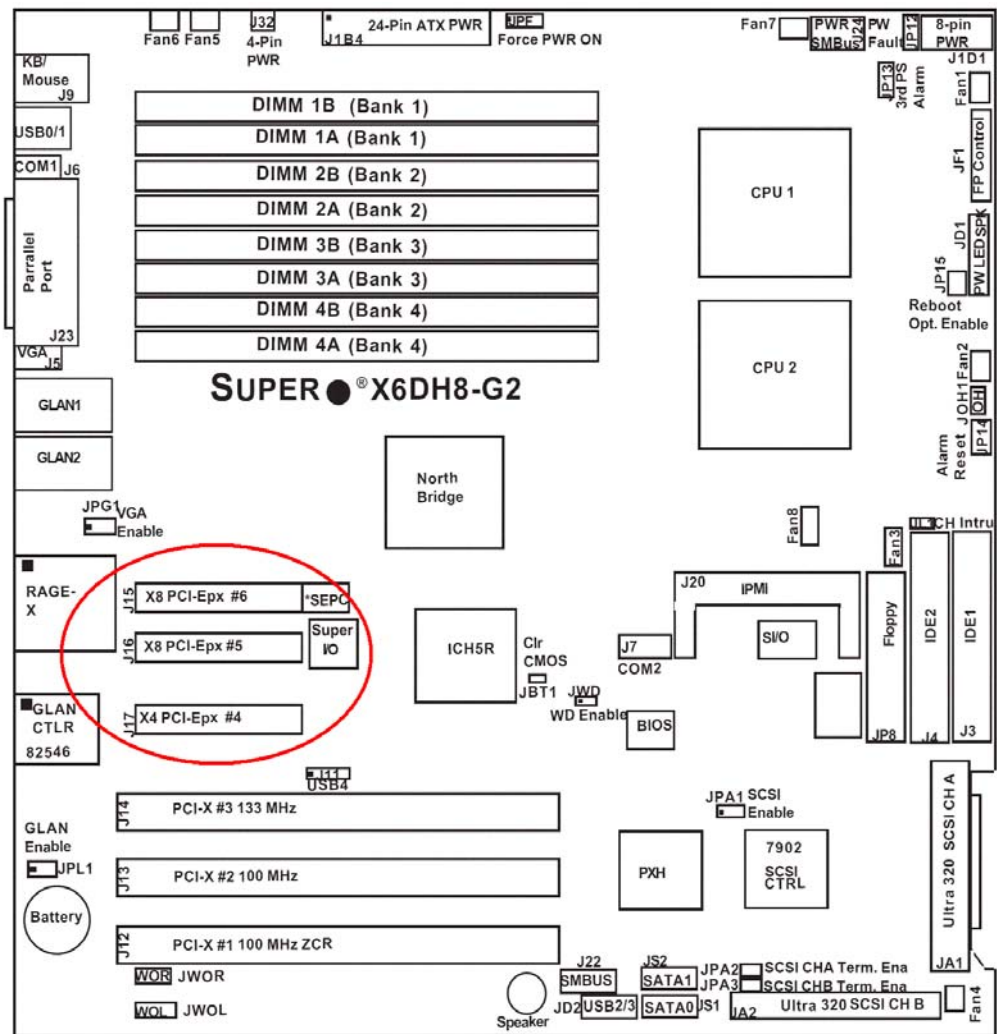


Figure 2.1 SuperMicro X6DH8-G2 Motherboard

Notes

Reference Clocks

The EB12N3 requires two differential reference clocks. The EB12N3 drives both of these clocks from a common source. The source for the reference clock is user-selectable between the host system's reference clock and the onboard clock generator. Selection is made by stuffing resistors described in Table 2.1.

Clock Configuration Stuffing Option	
Install	Clock Source
R79, R81	Onboard Reference Clock – Use onboard clock generator
R75, R78	Upstream Reference Clock – Host system provides clock (Default)

Table 2.1 Clock Source Selection

The source for the onboard clock is the ICS557-03 clock generator device (U9) connected to a 25MHz oscillator (Y1). When using the onboard clock generator, the EB12N3 allows selection between multiple clock rates and spread spectrum settings via DIP switches as described in Tables 2.2 and 2.3 respectively. Spread Spectrum technology reduces peak EMI emissions by modulating the frequency to spread the peak energy over a wider bandwidth.

Clock Frequency Switch - J8[2:1]		
J8[2]	J8[1]	Clock Frequency
OFF	OFF	<Reserved>
OFF	ON	125 MHz
ON	OFF	100 MHz (Default)
ON	ON	<Reserved>

Table 2.2 Clock Frequency Selection

Clock Spread Spectrum Switch - J8[4:3]		
J8[4]	J8[3]	Spread%
OFF	OFF	No Spread (Default)
OFF	ON	Down -0.75
ON	OFF	Down -0.50
ON	ON	Center ± 0.25

Table 2.3 Clock Spread Spectrum Selection

The output of the onboard clock generator is accessible through two SMA connectors located on the Evaluation Board. See Table 2.4. This can be used to connect a scope for probing or capturing purposes and cannot be used to drive the clock from an external source.

Onboard Reference Clock Output (Differential) – J3, J7	
J3	Positive Reference Clock
J7	Negative Reference Clock

Table 2.4 SMA Connectors - Onboard Reference Clock

Notes

Power Sources

The EB12N3 and all attached endpoint cards are powered entirely by the host system through the upstream PCI Express edge connector. In general, this is sufficient and there is no need for an external power-source. If the combined power requirements of the EB12N3 Evaluation Board and the devices attached to the two downstream ports exceed PCI Express specifications, an external source may be required to supply the necessary power.

External Power Source

If necessary, external power is supplied to the EB12N3 board through a 4-pin auxiliary power connector attached to J5. The external power supply provides +12V and +5.0V to the EB12N3 as described in Table 2.5. The +5V is unused.

4-Pin Power Connector – J5	
Pin	Signal
1	+12V
2	GND
3	GND
4	+5V

Table 2.5 Power Connector Pin-Out

PCI Express Serial Data Transmit Termination Voltage Regulator

A low-voltage, low-dropout regulator (Micrel MIC49300BR) provides a 1.5V PCI Express serial data transmit termination voltage to the PES12N3.

PCI Express Digital Power Voltage Regulator

A low-voltage, low-dropout regulator (Micrel MIC49300BR) provides a 1.0V PCI Express digital power voltage to the PES12N3.

PCI Express Analog Power Voltage Regulator

A low-voltage, low-dropout regulator (Micrel MIC49300BR) provides a 1.0V PCI Express analog power voltage to the PES12N3.

Core Logic Voltage Regulator

The EB12N3 employs three low-voltage, low-dropout voltage regulators (Micrel MIC49300BR) to supply the 1.0V core voltage to the PES12N3 switch.

Required Jumpers

To deliver power to the PES12N3 switch, the following jumpers must be shunted: W10, W22-W25.

Notes

Power Selection for Downstream Ports

The following table illustrates the power selection features and hot plug capabilities for downstream ports B and C.

Power Selection for Downstream Ports Jumpers, Headers			
Ref. Designator	Type	Default	Description
J2[6]	Switch	On	On - Downstream clock for port B is always enabled
			Off - Setting for hot plugging - Downstream clock for port B is controlled by MIC2591B, which is controlled by the 12N3
J2[7]	Switch	On	On - Downstream clock for port C is always enabled
			Off - Setting for hot plugging - Downstream clock for port C is controlled by MIC2591B, which is controlled by the 12N3
W6	Header	Shunted	Shunted - Hot Plug disabled, enables direct power to downstream port C
			Open - Downstream port C power will be controlled by power enable signal (Refer to schematic page 5 C7)
W11	Header	Shunted	Shunted - Hot Plug disabled, enables direct power to downstream port B
			Open - Downstream port B power will be controlled by power enable signal (Refer to schematic page 5 C7)
W7	3 pin Header	[1-2] shunted	[1-2]Select onboard (+12V) to Port B
			[2-3]Select external power (+12V) to Port B Note: External Power Connector has to be attached at J5.
W8	3 pin Header	[1-2] shunted	[1-2]Select onboard (+3.3V) to Port B
			[2-3]Select external power (+3.3V) to Port B Note: External Power Connector has to be attached at J5.
W9	3 pin Header	[1-2] shunted	[1-2]Select onboard (+12V) to Port C
			[2-3]Select external power (+12V) to Port C Note: External Power Connector has to be attached at J5.
W12	3 pin Header	[1-2] shunted	[1-2]Select onboard (+3.3V) to Port C
			[2-3]Select external power (+3.3V) to Port C Note: External Power Connector has to be attached at J5.

Table 2.6 Power Selection for Downstream Ports Jumpers, Headers

Notes

Reset

The PES12N3 supports two types of reset mechanisms as described in the PCI Express specifications:

- ◆ Fundamental Reset: This is a system generated reset that propagates along the PCI Express tree through a single side-band signal PERST#, connected to the Root Complex, the PES12N3 and the endpoints.
- ◆ Hot Reset: This is an In-band Reset, communicated downstream via a link from one device to another. Hot Reset may be initiated by software. This is further discussed in the 89HPES12N3 User Manual. The EB12N3 evaluation board does not need to do anything specific to support Hot Reset.

Fundamental Reset

There are two types of Fundamental Resets which may occur on the EB12N3 evaluation board. Both types of resets depend on the location of the shunt on header W13. Refer to the tables below:

- ◆ Cold Reset:

W13 Shunt Selection for Cold Reset	
Shunt	Description
Pins [1-2]	During initial power-on, the onboard voltage monitor (TLC7733D) will assert the PCI Express Reset (PERSTN) input pin of the PES12N3.
Pins [2-3]	During initial power-on, the reset signal (PERSTN) will come from the upstream edge connector.

Table 2.7 W13 Shunt Selection for Cold Reset

- ◆ Warm Reset: This is triggered by hardware while the device is powered on.

W13 Shunt Selection for Warm Reset	
Shunt	Description
Pins [1-2]	A warm reset can be initiated in two ways. Both events cause the onboard voltage monitor (TLC7733D) to assert the PCI Express Reset (PERSTN) input of the PES12N3 while the power is on. The two ways are: – by pressing a push-button switch (X4) located on EB12N3 board – if the system board IO Controller Hub asserts PERST# signal, which propagates through the PCIe upstream edge connector of the EB12N3
Pins [2-3]	This will directly tie the upstream reset to the onboard fundamental reset.

Table 2.8 W13 Shunt Selection for Warm Reset

Downstream Reset

The PES12N3 provides three different downstream reset schemes. By default the reset scheme used is the fundamental reset. There is also a software controlled reset for each downstream port through the GPIO pins. Finally, there is a pgood controlled reset for each downstream port. When hot plugging is enabled, this reset scheme creates a downstream port reset if pgood__N is not asserted. Selection of the downstream reset is made by shunting different header pins as described in Table 2.9.

Notes

Port#	Header	Selection
B	J11	[1-2] PGOOD_B_N controlled reset (used when hot-plugging is enabled) [3-4] Software controlled reset through GPIO0 [5-6] Fundamental reset PERST# (default)
C	J12	[1-2] PGOOD_C_N controlled reset (used when hot-plugging is enabled) [3-4] Software controlled reset through GPIO1 [5-6] Fundamental reset PERST# (default)

Table 2.9 Downstream Reset Selection

Boot Configuration Vector

A Boot Configuration Vector consisting of the signals listed in Table 2.10 is sampled by the PES12N3 during a fundamental reset (while PERSTN is active). The Boot Configuration Vector defines the essential parameters for switch operation and is set using DIP Switches J1 and J2 as defined in Table 2.11

Boot Configuration Vector Signals	
Signal	Description
CCLKDS	Common Clock Downstream. The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices. This pin is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be overridden by modifying the SCLK bit in the PB_PCIEIISTS or PC_PCIEIISTS register. Default: 0x1
CCLKUS	Common Clock Upstream. The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This pin is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the PA_PCIEIISTS register. Default: 0x1
MSMBSMODE	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. Default: 0x0
PEALREV	PCI Express Port A Lane Reverse. When this pin is asserted, the lanes of PCI Express Port A are reversed. This value may be overridden by modifying the value of the PALREV bit in the PA_SWCTL register. Default: 0x0
PEBLREV	PCI Express Port B Lane Reverse. When this pin is asserted, the lanes of PCI Express Port B are reversed. This value may be overridden by modifying the value of the PBLREV bit in the PA_SWCTL register. Default: 0x0
PECLREV	PCI Express Port C Lane Reverse. When this pin is asserted, the lanes of PCI Express Port C are reversed. This value may be overridden by modifying the value of the PCLREV bit in the PA_SWCTL register. Default: 0x0
REFCLKM	PCI Express Reference Clock Mode Select. These signals select the frequency of the reference clock input. Default: 0x0 0x0 - 100 MHz 0x1 - 125 MHz

Table 2.10 Boot Configuration Vector Signals (Part 1 of 2)

Notes

Boot Configuration Vector Signals	
Signal	Description
RSTHALT	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, the PES12N3 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the PA_SWCTL register through the SMBus. The value may be overridden by modifying the RSTHALT bit in the PA_SWCTL register. Default: 0x0
SWMODE[3:0]	Switch Mode. These configuration pins determine the PES12N3 switch operating mode. Default ¹ : 0x0 0x0 - Initialization without serial EEPROM 0x1 - Serial EEPROM-based initialization 0x2 through 0x5 - Reserved 0x6 - Scan test mode (factory use only) 0x7 - PLL Bypass test mode 0x8 - 10-bit loop-back test mode 0x9 - Reserved 0xA - Internal pseudo random bit stream self-test mode 0xB - External pseudo random bit stream self-test mode 0xC - Reserved 0xD - SerDes broadcast test mode 0xE - Reserved 0xF - Reserved

Table 2.10 Boot Configuration Vector Signals (Part 2 of 2)

¹. The default setting is 0x1 if the PES12N3A device is on the board.

Boot Configuration Vector Switches J1 & J2 (ON=0, Off=1)		
Switch	BCV Bit	Default
J1[1]	CCLKDS	OFF
J1[2]	CCLKUS	OFF
J1[3]	MSMBSMODE	ON
J1[4]	PEALREV	ON
J1[5]	PEBLREV	ON
J1[6]	PECLREV	ON
J1[7]	REFCLKM	ON
J1[8]	RSTHALT	ON
J2[1]	<RESERVED>	ON
J2[2]	SWMODE[0]	ON
J2[3]	SWMODE[1]	ON

Table 2.11 Boot Configuration Vector Switches (Part 1 of 2)

Notes

Boot Configuration Vector Switches J1 & J2 (ON=0, Off=1)		
Switch	BCV Bit	Default
J2[4]	SWMODE[2]	ON
J2[5]	SWMODE[3]	ON
J2[8]	<RESERVED>	ON

Table 2.11 Boot Configuration Vector Switches (Part 2 of 2)

SMBus Interfaces

The PES12N3 contains two SMBus interfaces: a slave SMBus interface and a master SMBus interface. The slave SMBus interface allows a SMBus Master device (such as the Intel E7520) full access to all software-visible registers. The Master SMBus interface provides connection to the external serial EEPROMs used for initialization and the I/O expander used for hot-plug signals. Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins.

SMBus Slave Interface

The System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate. See Table 2.12. It is based on the principles of operation of I²C. Implementation of the SMBus signals in the PCI Express connector is optional and may not be present on the host system. On the PES12N3 board, the slave SMBus interface is accessible through the PCI Express edge connector as well as a 4-pin header as described in Table 2.12. *Note: The SMBus signals to the PCI Express edge connector is disabled by default. To enable them, place 0-ohm resistors at locations R34 and R35.*

Slave SMBus Interface Connector W20	
Pin	Signal
1	N/C
2	SCL
3	GND
4	SDA

Table 2.12 Slave SMBus Interface Connector

A fixed slave SMBus address specified by the SSMBADDR[5,3:1] pins is used.

For a fixed address, the SMBus address of the PES12N3 slave interface is 0b1110111 by default and is configurable using the jumpers W1, W5, W2, and W3 as described in Tables 2.13 and 2.14.

Slave Interface Address Configuration	
Address Bit	Signal
1	SSMBUSADDR[1]
2	SSMBUSADDR[2]
3	SSMBUSADDR[3]

Table 2.13 SMBus Slave Interface Address Configuration (Part 1 of 2)

Notes

Slave Interface Address Configuration	
Address Bit	Signal
4	0
5	SSMBUSADDR[5]
6	1
7	1

Table 2.13 SMBus Slave Interface Address Configuration (Part 2 of 2)

SMBUS Slave Interface Address Setting				
W1 SSMBADDR[5]	W5 SSMBADDR[3]	W2 SSMBADDR[2]	W3 SSMBADDR[1]	Slave Interface Bus Address
OFF	OFF	OFF	OFF	0b1110111 (Default)
OFF	OFF	OFF	ON	0b1110110
OFF	OFF	ON	OFF	0b1110101
OFF	OFF	ON	ON	0b1110100
OFF	ON	OFF	OFF	0b1110011
OFF	ON	OFF	ON	0b1110010
OFF	ON	ON	OFF	0b1110001
OFF	ON	ON	ON	0b1110000
ON	OFF	OFF	OFF	0b1100111
ON	OFF	OFF	ON	0b1100110
ON	OFF	ON	OFF	0b1100101
ON	OFF	ON	ON	0b1100100
ON	ON	OFF	OFF	0b1100011
ON	ON	OFF	ON	0b1100010
ON	ON	ON	OFF	0b1100001
ON	ON	ON	ON	0b1100000

Table 2.14 PES12N3 SMBus Slave Interface Address Setting

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. Initiation of any SMBus transaction other than those listed above to the slave SMBus interface produces undefined results. See the SMBus 2.0 specification for a detailed description of these transactions:

- Byte and Word Write/Read
- Block Write/Read

SMBus Master Interface

Connected to the master SMBus interface is a 16-bit I/O Expander (PCA9555) and a serial EEPROM (24LC512). The I/O expander is used as an interface for the onboard dual-slot hot-plug controller (MIC2591B). The lower three bits of the bus address for the I/O expander device is **0b000** by default and is configurable using the jumpers W29, W30, and W31 as described in Table 2.16.

Notes

I/O Expander SMBus Address Setting			
W31	W30	W29	Bus Address
OFF	OFF	OFF	0b0100 111
OFF	OFF	ON	0b0100 110
OFF	ON	OFF	0b0100 101
OFF	ON	ON	0b0100 100
ON	OFF	OFF	0b0100 011
ON	OFF	ON	0b0100 010
ON	ON	OFF	0b0100 001
ON	ON	ON	0b0100 000 (Default)

Table 2.15 I/O Expander Address Setting

The lower three bits of the bus address for the selected EEPROM device is **0b000** by default and is configurable using the jumpers W15, W17, and W21 as described in Table 2.16.

EEPROM SMBus Address Setting			
W21	W17	W15	Bus Address
OFF	OFF	OFF	0b1010 111
OFF	OFF	ON	0b1010 110
OFF	ON	OFF	0b1010 101
OFF	ON	ON	0b1010 100
ON	OFF	OFF	0b1010 011
ON	OFF	ON	0b1010 010
ON	ON	OFF	0b1010 001
ON	ON	ON	0b1010 000 (Default)

Table 2.16 EEPROM SMBus Address Setting

Required EEPROM Headers		
Ref. Design	Default	Description
W4	Shunted	Sets the fourth bit of the Bus address for the EEPROM device
W16	Shunted	Write to onboard EEPROM is enabled

Table 2.17 Required EEPROM Headers

Notes

JTAG Header

The PES12N3 provides a JTAG connector J4 for access to the PES12N3 JTAG interface. The connector is a 2.54 x 2.54 mm pitch male 10-pin connector. Refer to Table 2.18 for the JTAG Connector J4 pin out.

JTAG Connector J4					
Pin	Signal	Direction	Pin	Signal	Direction
1	/TRST - Test reset	Input	2	GND	—
3	TDI - Test data	Input	4	GND	—
5	TDO - Test data	Output	6	GND	—
7	TMS - Test mode select	Input	8	GND	—
9	TCK - Test clock	Input	10	GND	—

Table 2.18 JTAG Connector Pin Out

Attention Buttons

The PES12N3 features three attention buttons. Each button corresponds to a particular port and is used to initiate hot-swapping events.

Attention Buttons	
Button	Description
X2	Port A Attention Button
X3	Port B Attention Button
X1	Port C Attention Button

Table 2.19 Attention Buttons

LEDs

There are several LED indicators on the PES12N3 useful for conveying status feedback to the user. A description of each is provided in Table 2.20

LED Status Indicators		
LED	Color	Description
DS1	Green	Port B: Power-is-good indicator
DS2	Green	Port C: Power-is-good indicator
DS3	Green	Port A: Power Indicator
DS4	Yellow	Port A: Attention Indicator
DS5	Green	Port B: Power Indicator
DS6	Yellow	Port B: Attention Indicator

Table 2.20 LED Status Indicators (Part 1 of 2)

Notes

DS7	Green	Port C: Power Indicator
DS8	Yellow	Port C: Attention Indicator
DS9	Red	Hot Plug Controller: Power Fault Indicator
DS10	Green	Board Power Indicator (3.3V)
DS11	Red	Board Reset Indicator

Table 2.20 LED Status Indicators (Part 2 of 2)

PCI Express Connector

Pin	Side A		Side B	
1	+12V	12V power	PRSNT1#	Hot-Plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential	RSVD	Reserved
20	PETn1	pair, Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential
22	GND	Ground	PERn1	pair, Lane 1
23	PETp2	Transmitter differential	GND	Ground
24	PETn2	pair, Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential
26	GND	Ground	PERn2	pair, Lane 2

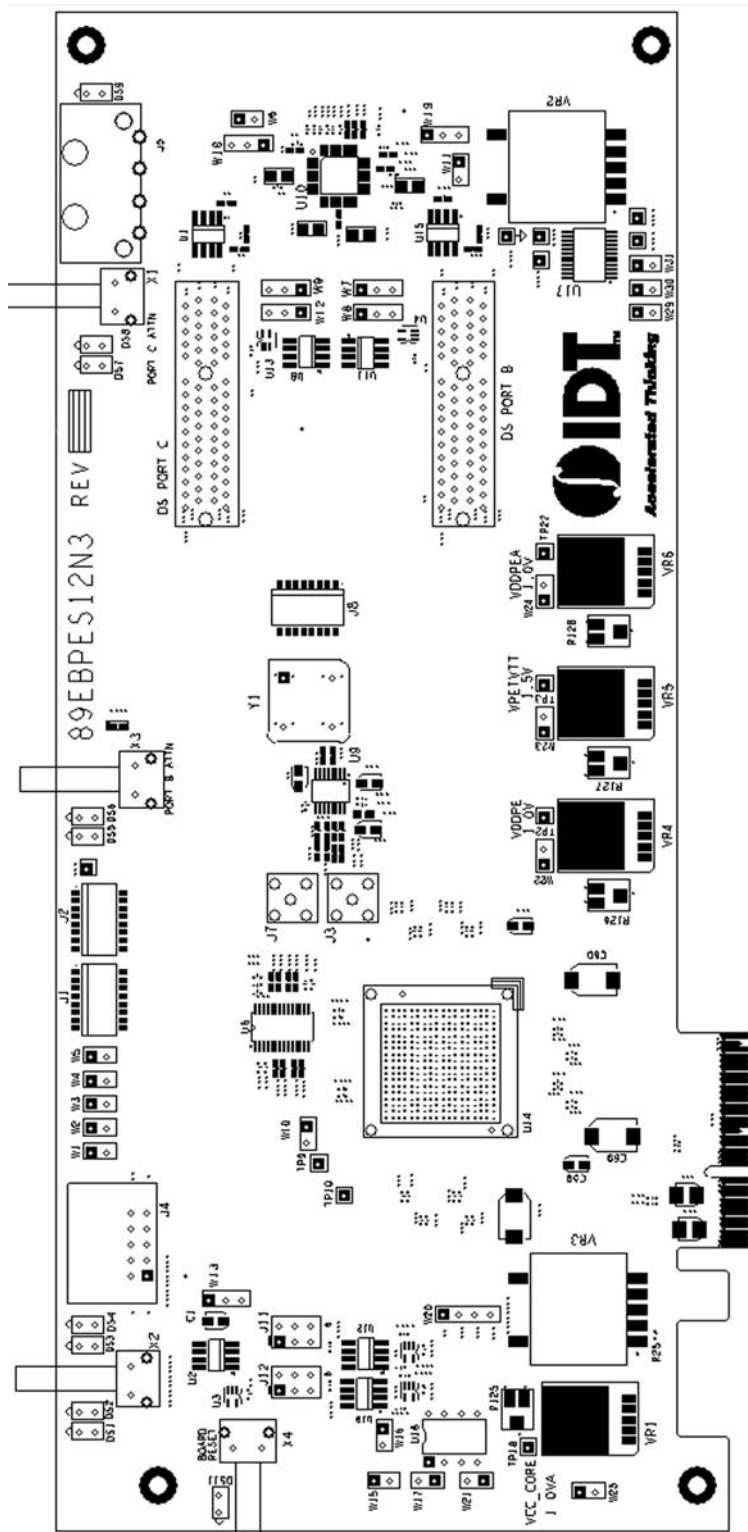
Table 2.21 PCI Express Connector Pin-Out (Part 1 of 2)

Notes

Pin	Side A		Side B	
27	PETp3	Transmitter differential	GND	Ground
28	PETn3	pair, Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential
30	RSVD	Reserved	PERn3	pair, Lane 3
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETp4	Transmitter differential	RSVD	Reserved
34	PETn4	pair, Lane 4	GND	Ground
35	GND	Ground	PERp4	Receiver differential
36	GND	Ground	PERn4	pair, Lane 4
37	PETp5	Transmitter differential	GND	Ground
38	PETn5	pair, Lane 5	GND	Ground
39	GND	Ground	PERp5	Receiver differential
40	GND	Ground	PERn5	pair, Lane 5
41	PETp6	Transmitter differential	GND	Ground
42	PETn6	pair, Lane 6	GND	Ground
43	GND	Ground	PERp6	Receiver differential
44	GND	Ground	PERn6	pair, Lane 6
45	PETp7	Transmitter differential	GND	Ground
46	PETn7	pair, Lane 7	GND	Ground
47	GND	Ground	PERp7	Receiver differential
48	PRSNT2#	Hot-Plug presence detect	PERn7	pair, Lane 7
49	GND	Ground	GND	Ground

Table 2.21 PCI Express Connector Pin-Out (Part 2 of 2)

Locations of Connectors, Jumpers, and Switches



Notes



Software for the EB12N3 Eval Board

Notes

Introduction

Extensive documentation for the software for the EB12N3 evaluation platform and/or the PES12N3 PCIe switch is available separately. This chapter highlights some of the main features of the software offered, so as to enable the board user to get a better understanding of what can be achieved with the EB12N3 evaluation board.

Device management software and related user documentation are available on a CD which is included in the Evaluation Board Kit. This information is also available on IDT's FTP site. For more information, please send an email to ssdhelp@idt.com.

Device Management Software

The primary use of the Device Management Software package is to enable the end user of the evaluation board to access all the registers in the PES12N3 device. This access can be achieved via the PCI express in-band configuration cycles through the device upstream port on the PES12N3.

Additionally, this software also offers the capabilities to save a snapshot of the current register set into a dump file which can be used for debugging purposes. An export/import facility is also available to create and use "Configuration" files which can be used to initialize the switch device with specific values in specific registers.

A conversion utility is provided to translate the configuration file into an EEPROM programmable data structure. This enables the user to program an appropriate serial EEPROM with the desirable register settings for the PES12N3, and then to populate that EEPROM on to the Evaluation Board. It is also possible to program the EEPROM directly on the Evaluation Boards using a feature provided by the software package.

The front end of the Device Management Software is a user friendly Graphical User Interface which allows the user to quickly read or write the registers of interest. The GUI also permits the user to run the software in "simulation" mode with no real hardware attached. This allows the user to create desirable configuration files for the device in the absence of the actual device.

Much of the Device Management Software is written with device independent and OS independent code. The software will be guaranteed to work on Linux (/sys interface) and MS Windows XP. It may function flawlessly on various flavors of MS Windows, but may not be validated on all. The fact that the software is device independent assures its scalability to future PCIe parts from IDT. Users once familiar with the GUI will be able to use the same GUI on all PCIe parts from IDT. Use of the software is customized for each device through a XML device description file which include information on number of ports, registers, types of registers, information on bit-fields within each register, etc.

Notes



Schematics

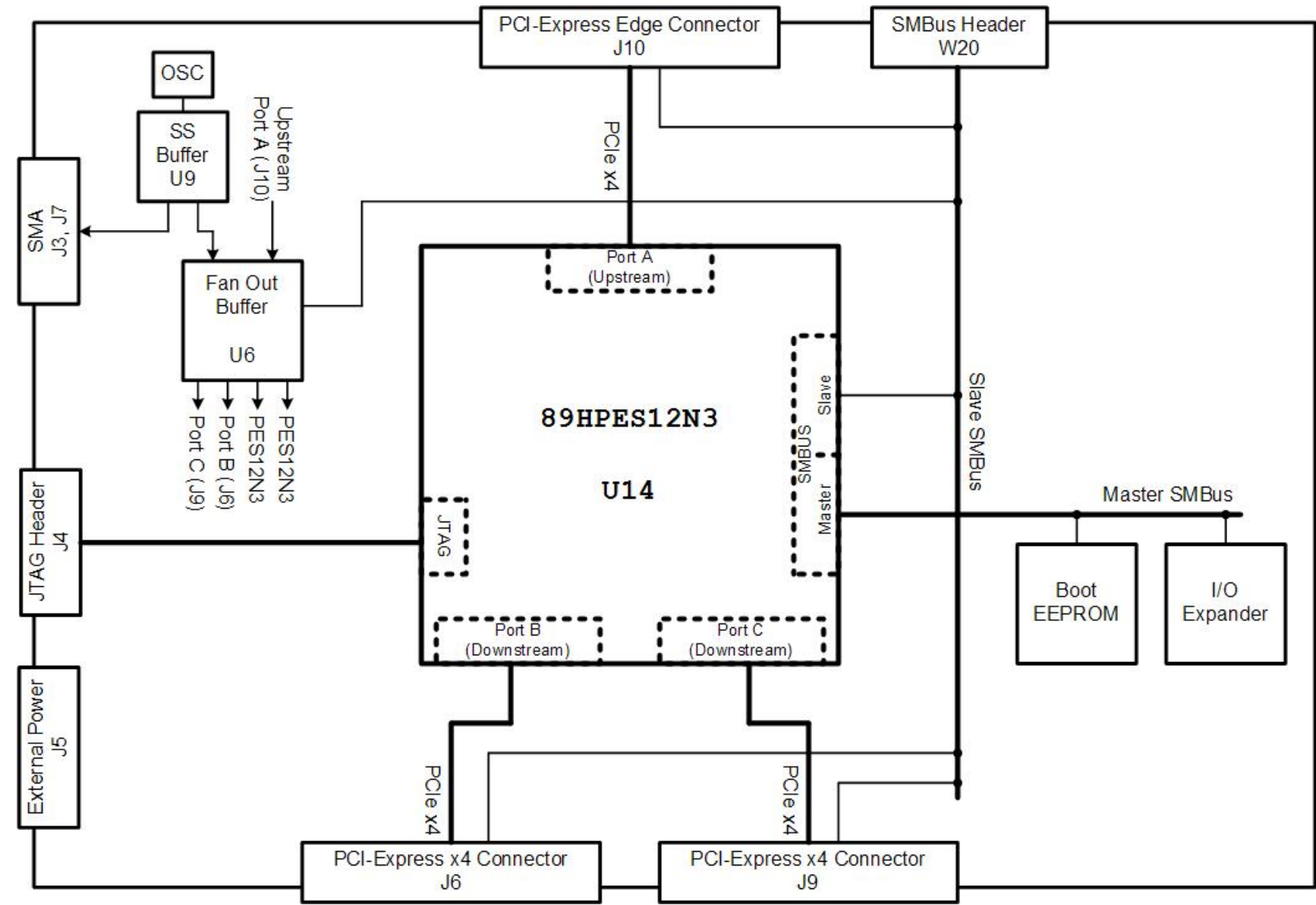
Notes

Schematics



89EBPES12N3 EVALUATION BOARD

REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
STGC-0087R01	1.0	89EBPES12N3 RESPIN (CREATED)	2006-06-15	K. LEUNG
STGC-0087R01	1.0	89EBPES12N3 RESPIN (RELEASED)	2006-09-07	K. LEUNG



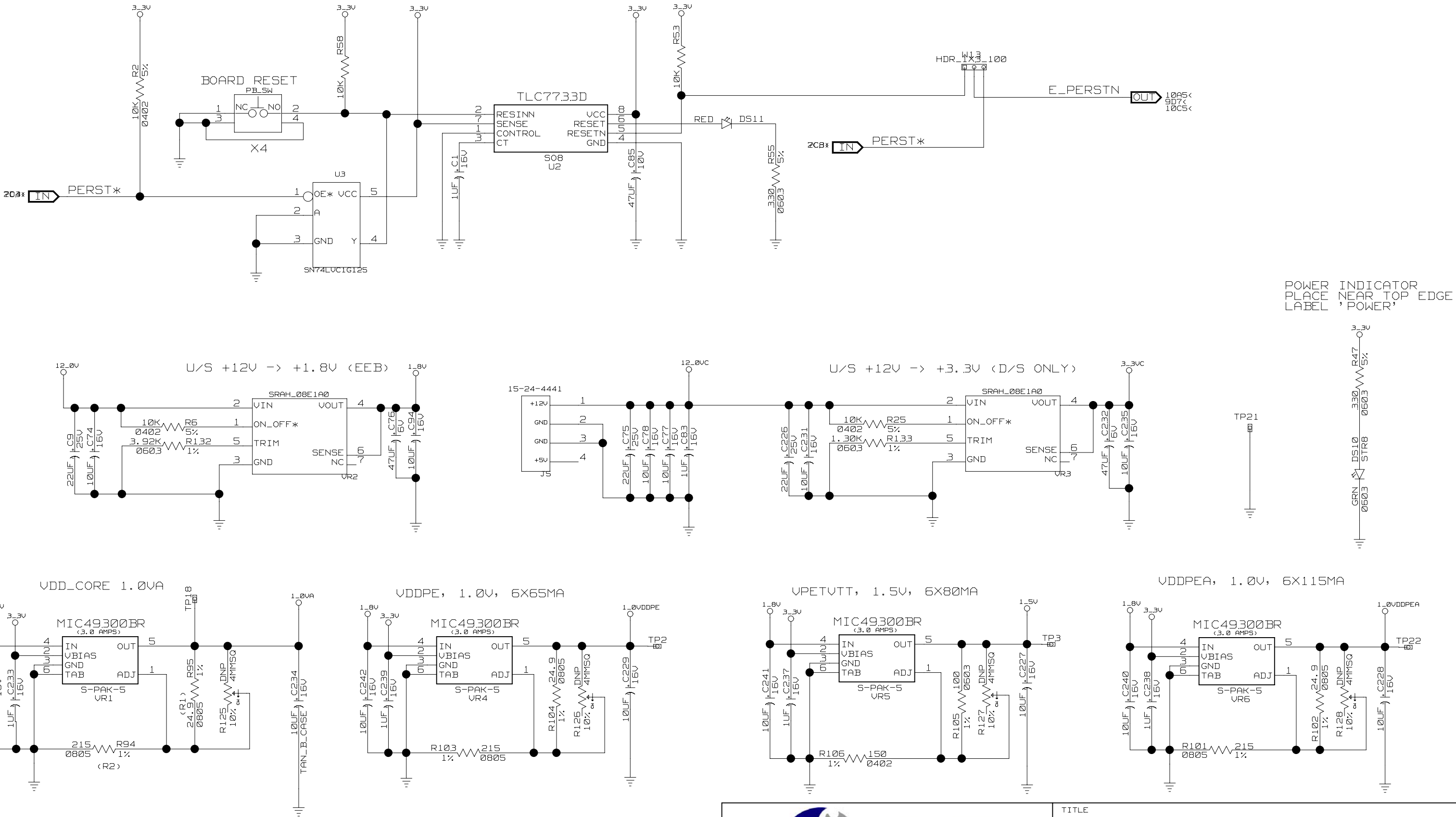
SHEET DESCRIPTION

- 1
- TITLE PAGE, BLOCK DIAGRAM
- 2
- POWER, RESET
- 3
- CLOCK
- 4
- EEPROM, SMBUS, JTAG, I/O EXPANDER
- 5
- HOT PLUG CONTROLLER
- 6
- PCIE CONNECTORS (DOWNSTREAM)
- 7
- PCIE EDGE CONNECTOR (UPSTREAM)
- 8
- PES12N3 - POWER
- 9
- PES12N3 - I/O
- 10
- PCIE WAKE, D/S RESET, DECOUPLING



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TITLE 89EBPES12N3			
SIZE B	DRAWING NO. STGSCH-00088	FAB P/N 18-597-001	REV. 1.0
AUTHOR K. LEUNG		CHECKED BY B. OH	
Thu Sep 07 22:55:09 2006			SHEET 1 OF 10

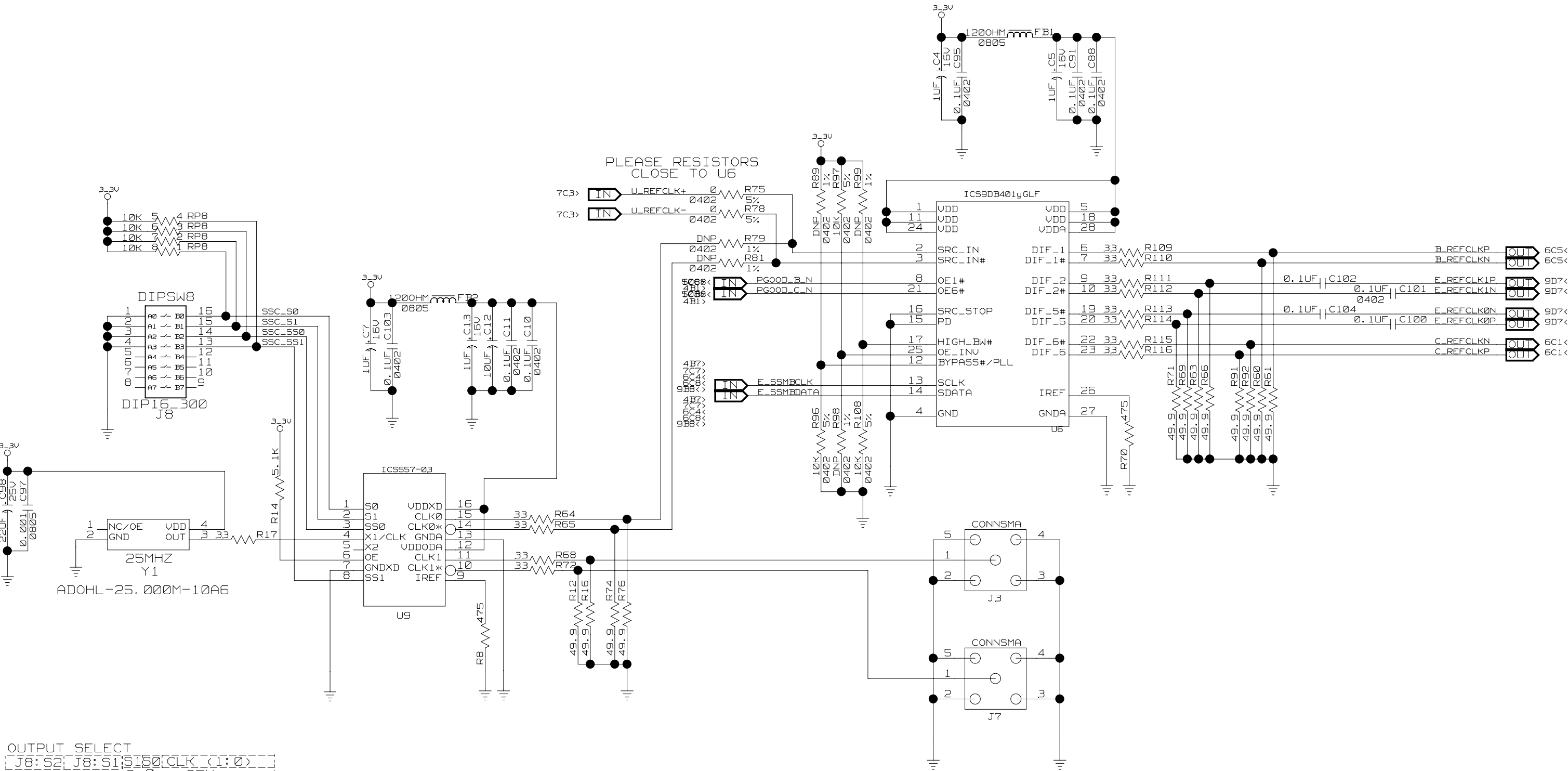


POWER INDICATOR
PLACE NEAR TOP EDGE
'POWER'



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TITLE POWER, RESET			
SIZE B	DRAWING NO. STGSCH-00088	FAB P/N 18-597-001	REV. 1.0
AUTHOR K. LEUNG		CHECKED BY B. OH	
Fri Jul 14 18:25:56 2006			SHEET 2 OF 10



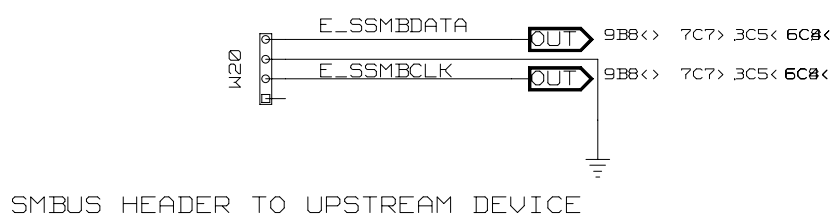
OUTPUT SELECT				
J8: S2	J8: S1	S150	CLK <1:0>	
ON	ON	0 0	25M	
ON	OFF	0 1	100M	
OFF	ON	1 0	125M	
OFF	OFF	1 1	200M	

SPREAD SELECTION				
J8: S4	J8: S3	SS1	SS0	SPREAD %
ON	ON	0 0	CENTER	+/-0.25
ON	OFF	0 1	DOWN	-0.5
OFF	ON	1 0	DOWN	-0.75
OFF	OFF	1 1	NO SPREAD	



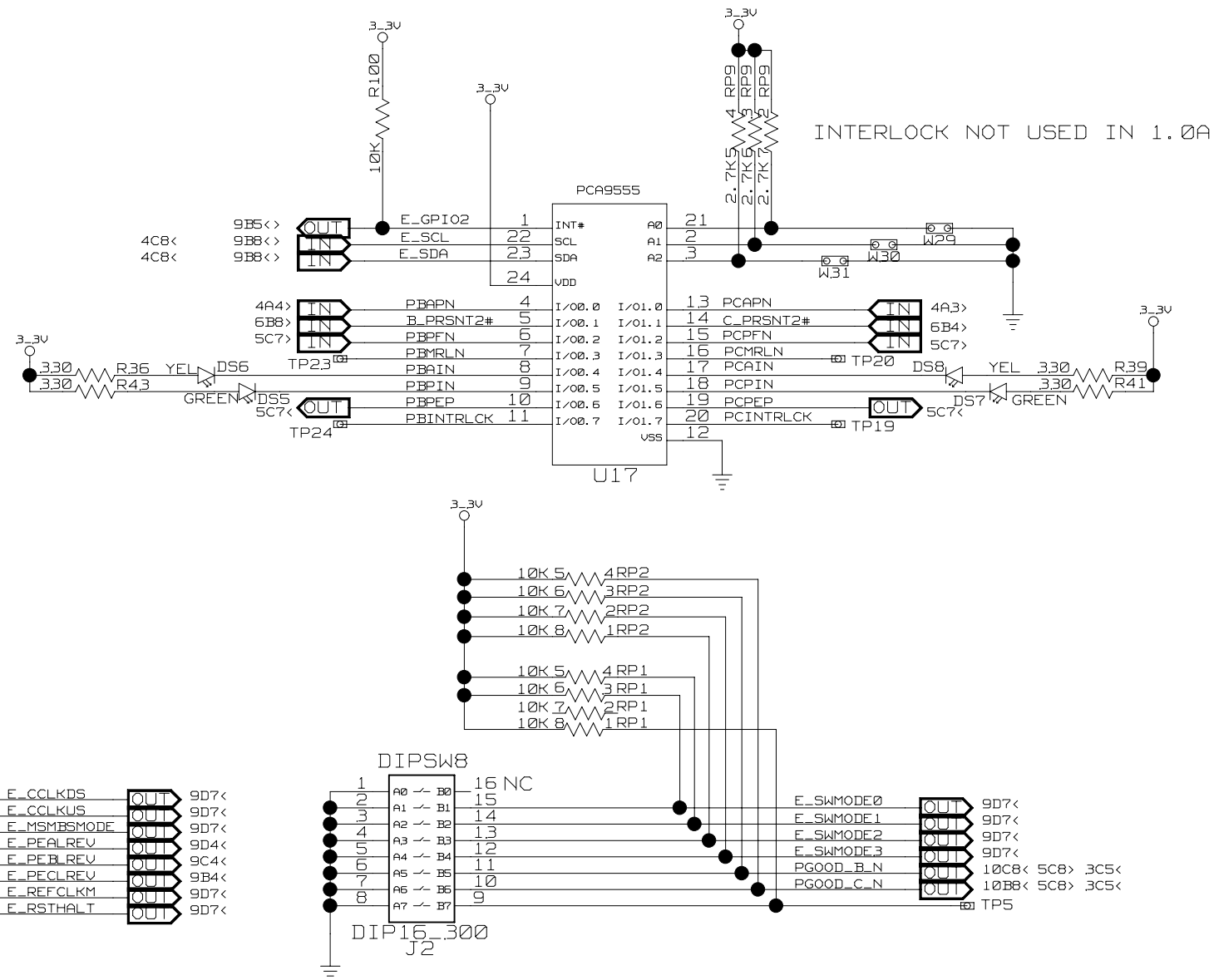
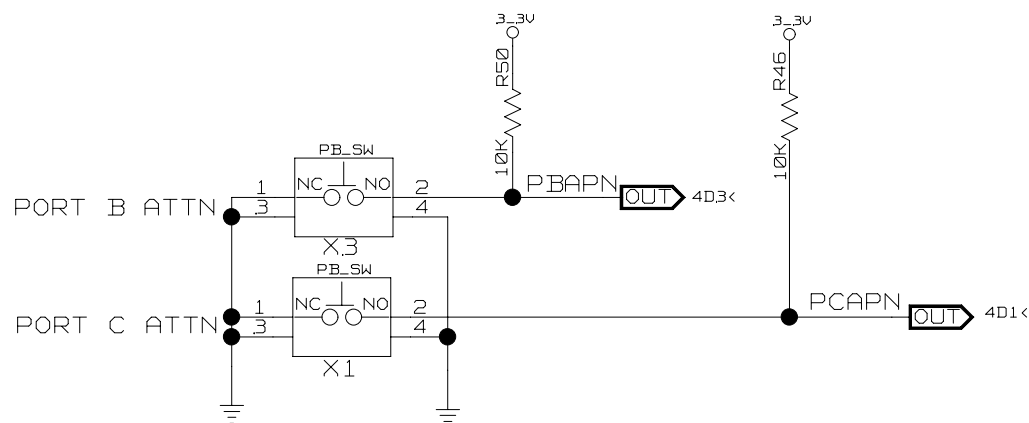
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TITLE			
CLOCK			
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00088	18-597-001	1.0
AUTHOR		CHECKED BY	
K. LEUNG		B. OH	
Fri Jul 14 18:25:56 2006			SHEET 3 OF 10



The schematic diagram illustrates the internal wiring of the DIP16_300 module. It features a 16-pin DIP switch (DIPSW8) and two sets of 4-pin resistors (RP3 and RP4). The connections are as follows:

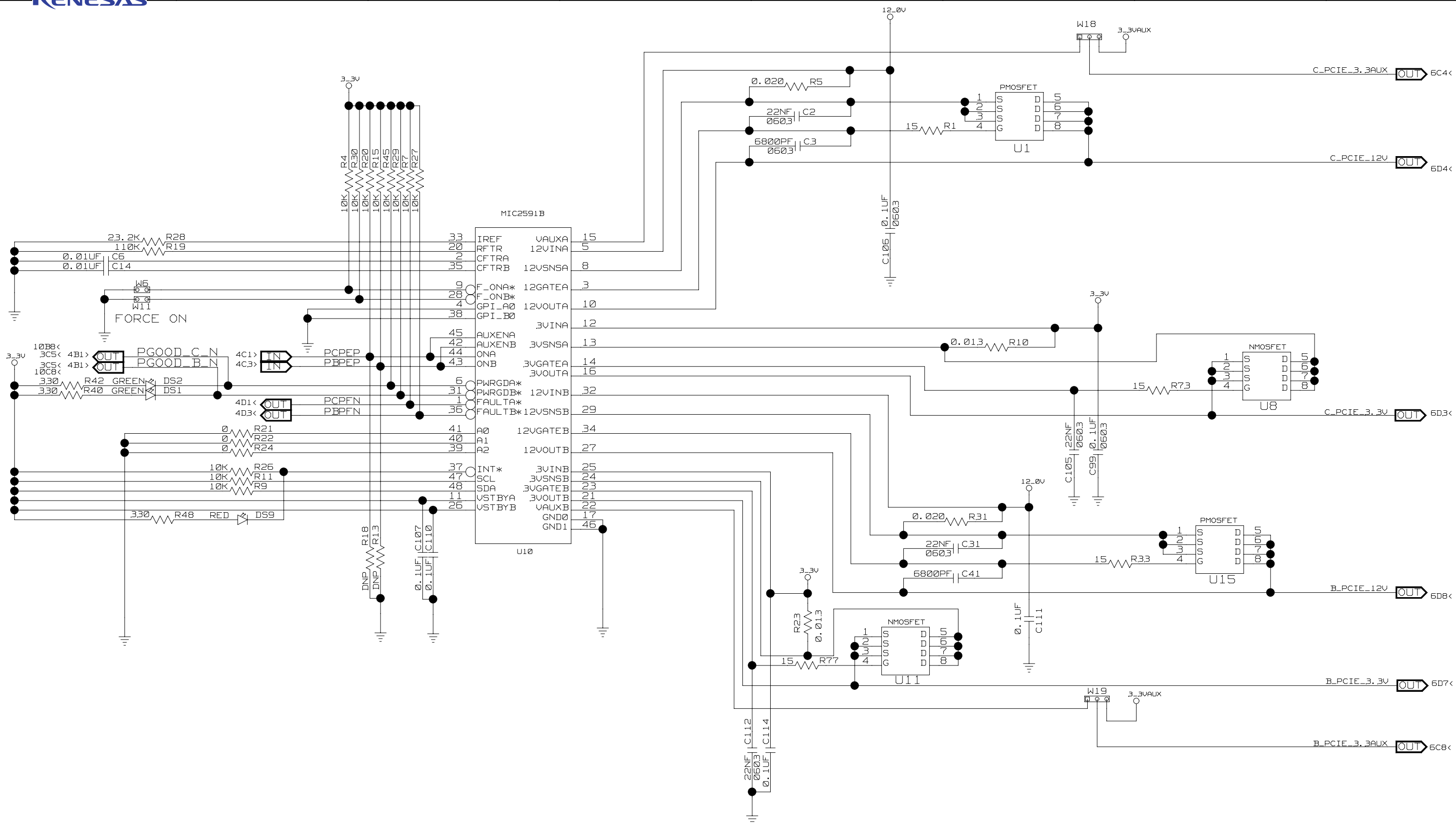
- 3V Supply:** A 3V supply is connected to the top terminal of the resistor network.
- RP4 Resistors:** Four 10K resistors (RP4) are connected in parallel between the 3V supply and the following pins:
 - Pin 15 (A0) to Pin 14 (B0)
 - Pin 15 (A1) to Pin 13 (B1)
 - Pin 15 (A2) to Pin 12 (B2)
 - Pin 15 (A3) to Pin 11 (B3)
- RP3 Resistors:** Four 10K resistors (RP3) are connected in parallel between the 3V supply and the following pins:
 - Pin 15 (A4) to Pin 10 (B4)
 - Pin 15 (A5) to Pin 9 (B5)
 - Pin 15 (A6) to Pin 8 (B6)
 - Pin 15 (A7) to Pin 7 (B7)
- DIPSW8 Connections:** The DIP switch is connected to the 3V supply and ground. The switch pins are labeled 1 through 8, corresponding to pins A0 through A7 on the module.
- Module Pins:** The module has 16 pins labeled A0 through A7 and B0 through B7. The connections for the resistors and switch are shown on the right side of the module.
- Output Signals:** The module outputs several signals, including F_CCLKDS, F_CCLKUS, F_MSMBSMODE, F_PEALREV, F_PECBREV, F_PECLEUV, F_REFCLKM, and F_RSTHALT, which are connected to the 9D7< pins.



INTERLOCK NOT USED IN 1.0A



TITLE			
EEPROM, SMBUS, JTAG, I/O EXP.			
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00088	18-597-001	1.0
AUTHOR		CHECKED BY	
K. LEUNG		B. OH	
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TITLE

HOT PLUG CONTROLLER

SIZE

DRAWING NO.

STGSCH-00088

FAB P/N

18-597-001

REV.

1.0

AUTHOR

K. LEUNG

CHECKED BY

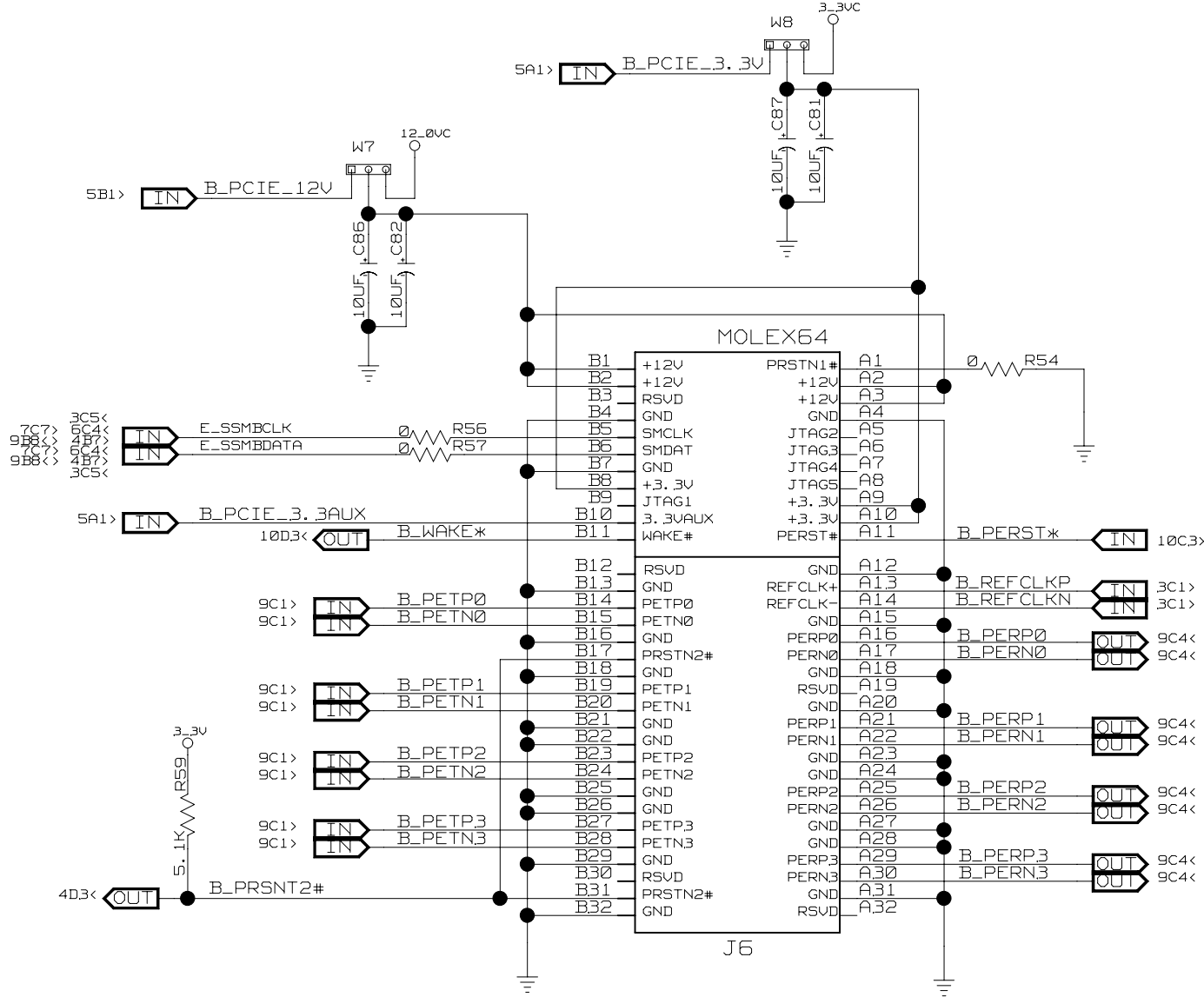
B. OH

Fri Jul 14 18:25:57 2006

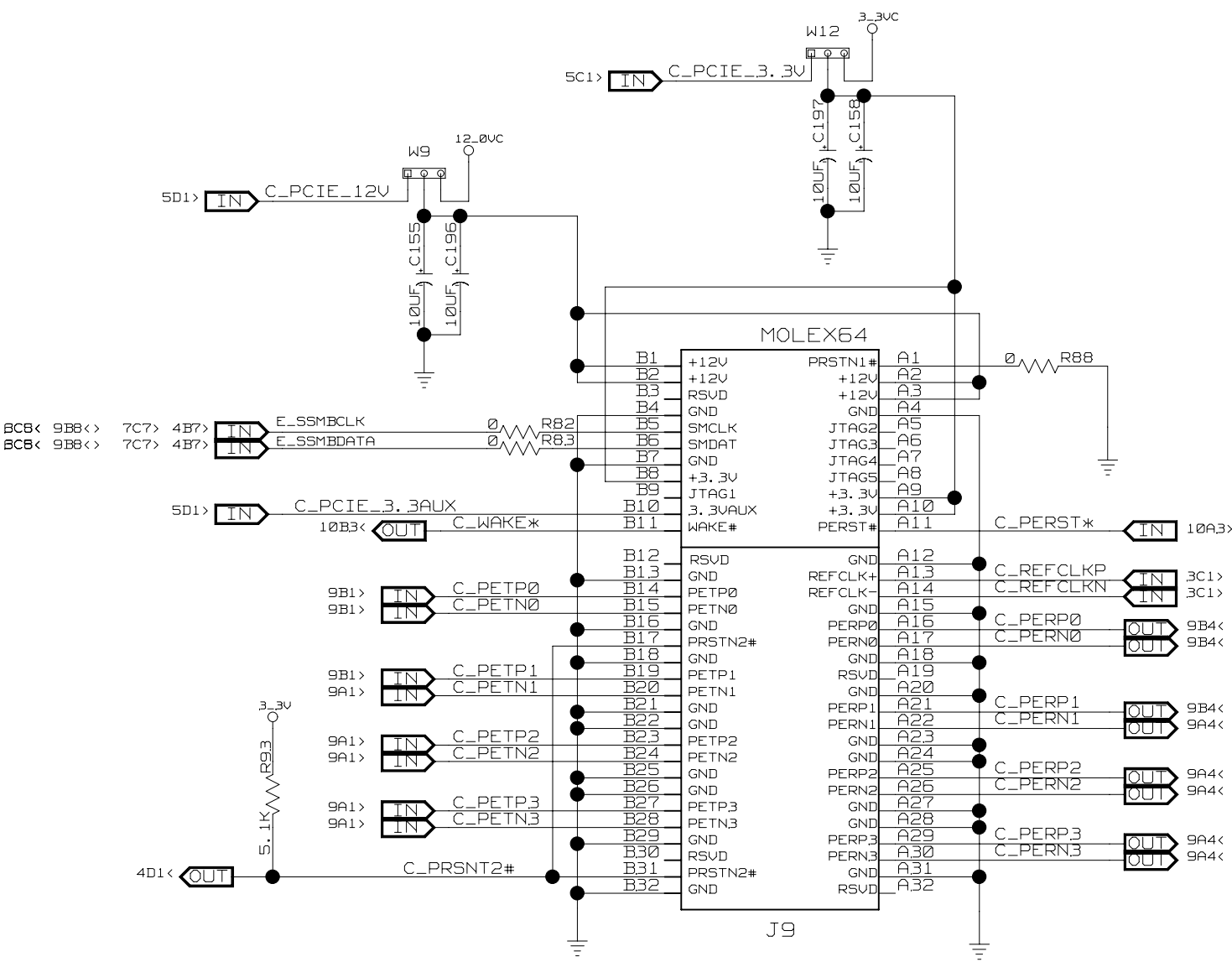
SHEET 5 OF 10



PLACE ALL CAPS NEAR PCIE CONNECTOR



DOWNSTREAM (PORT B) CONNECTOR

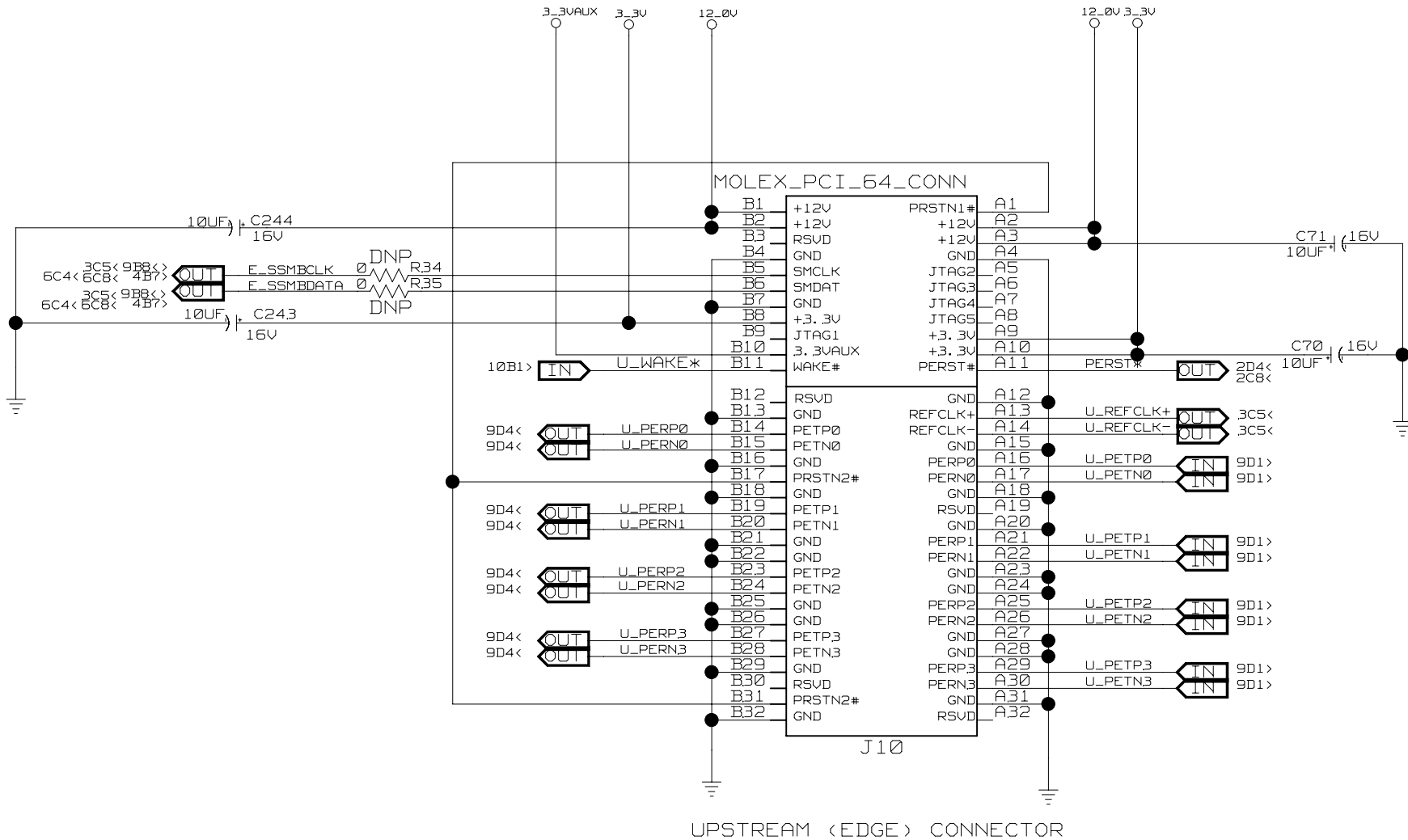


DOWNSTREAM (PORT C) CONNECTOR



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TITLE PCIE CONNECTORS (D/S)			
SIZE B	DRAWING NO. STGSCH-00088	FAB P/N 18-597-001	REV. 1.0
AUTHOR K. LEUNG		CHECKED BY B. OH	
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TITLE PCIE CONNECTOR (U/S)			
SIZE B	DRAWING NO. STGSCH-00088	FAB P/N 18-597-001	REV. 1.0
AUTHOR K. LEUNG		CHECKED BY B. OH	
Thu Sep 07 22:48:32 2006			SHEET 7 OF 10



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TITLE

PES12N3 - POWER

SIZE	
B	

DRAWING NO.
STGSCH-00088

FAB P/N
18-597-001

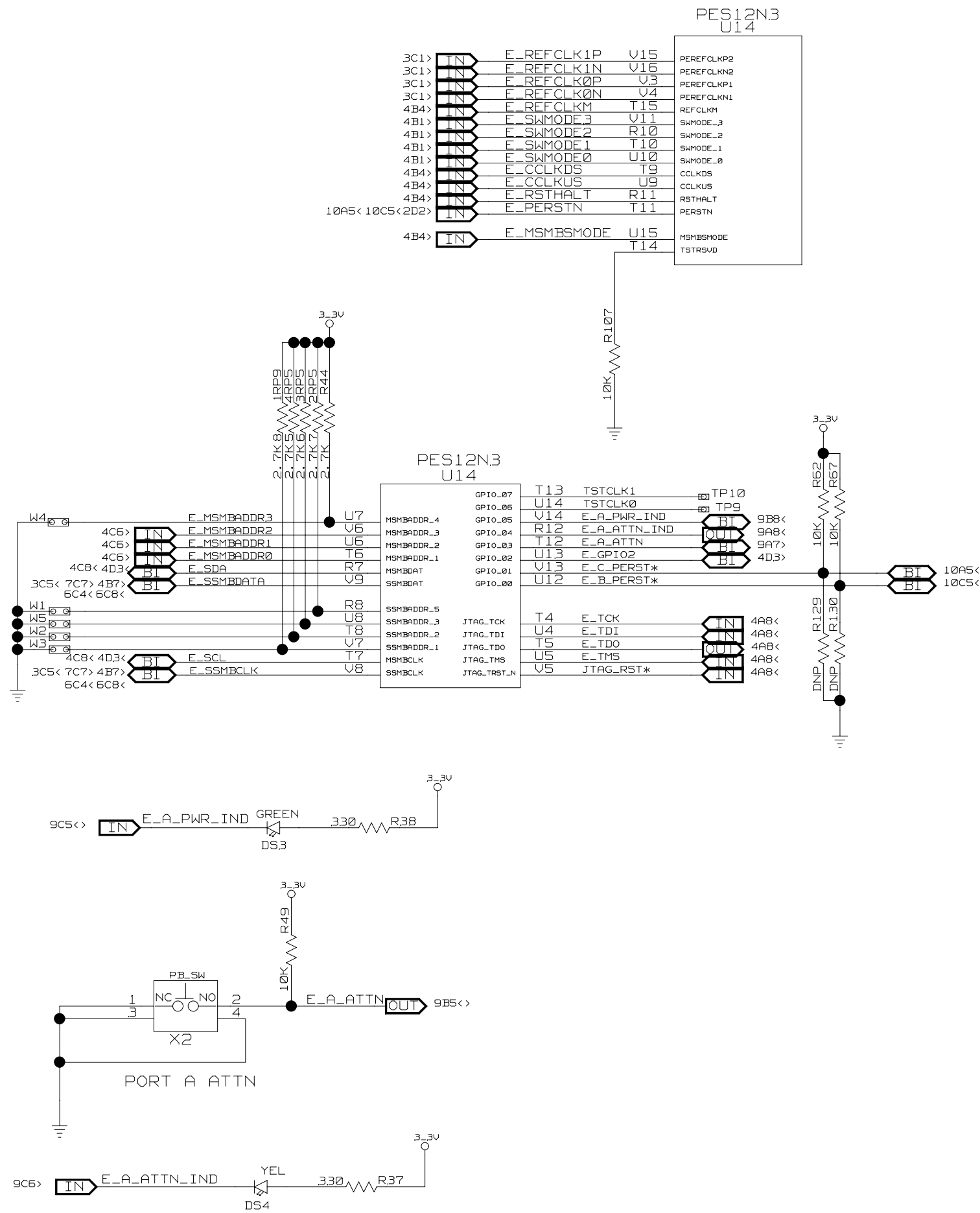
REV.
1. 0

AUTHOR	K. LEUNG
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CHECKED BY	
B. OH	

Fri Jul 14 18:25:54 2006

SHEET 8 OF 10





TITLE			
PCIEWAKE/DECOUPLING/DS RST			
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00088	18-597-001	1.0
AUTHOR		CHECKED BY	
K. LEUNG		B. OH	
Fri Jul 14 18:25:55 2006			SHEET 10 OF 10

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