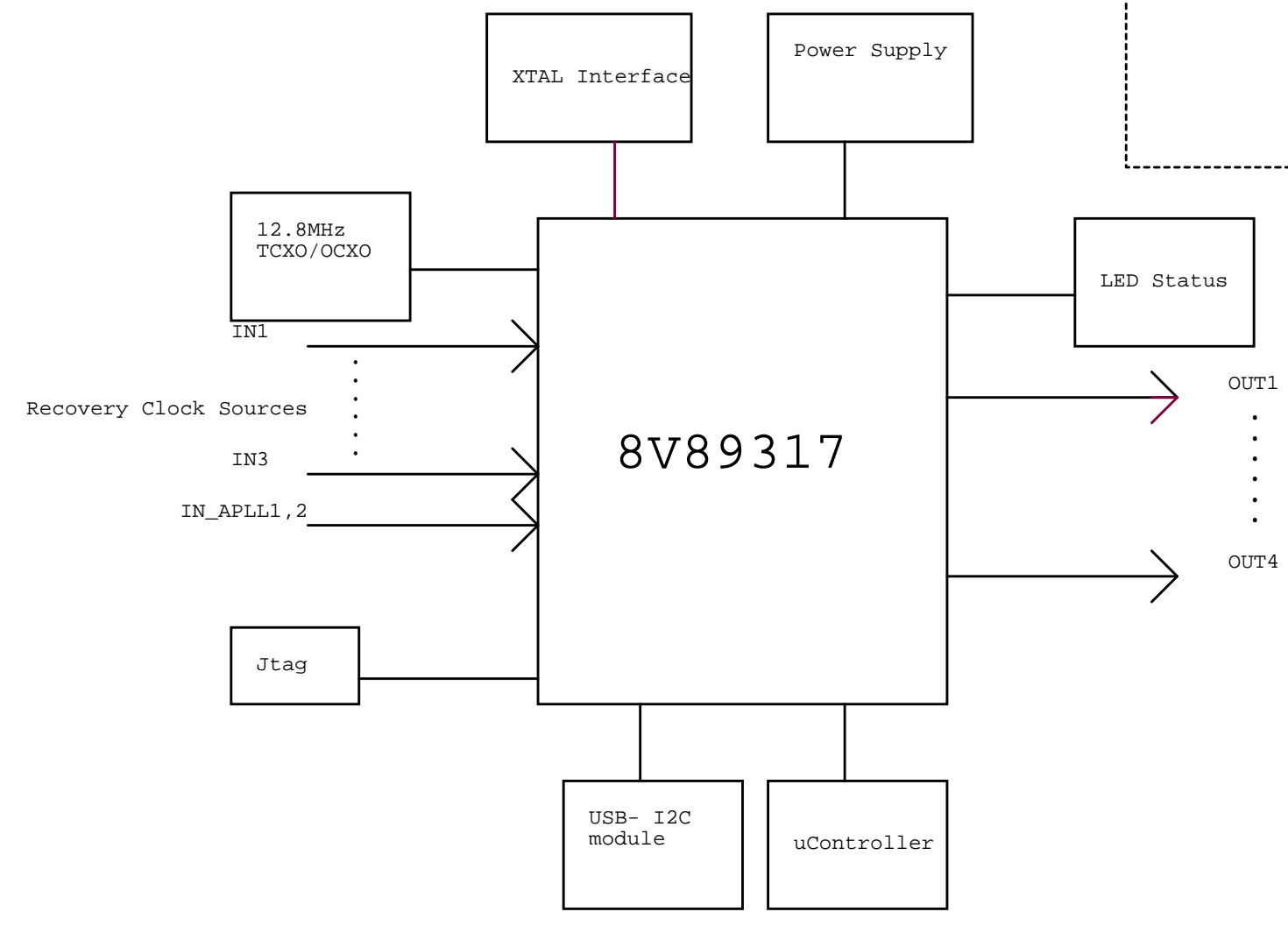
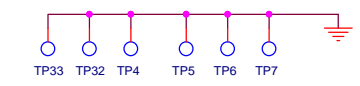
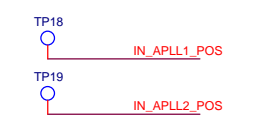
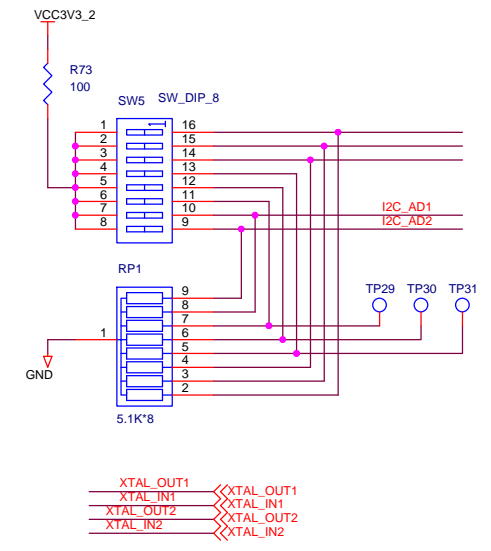
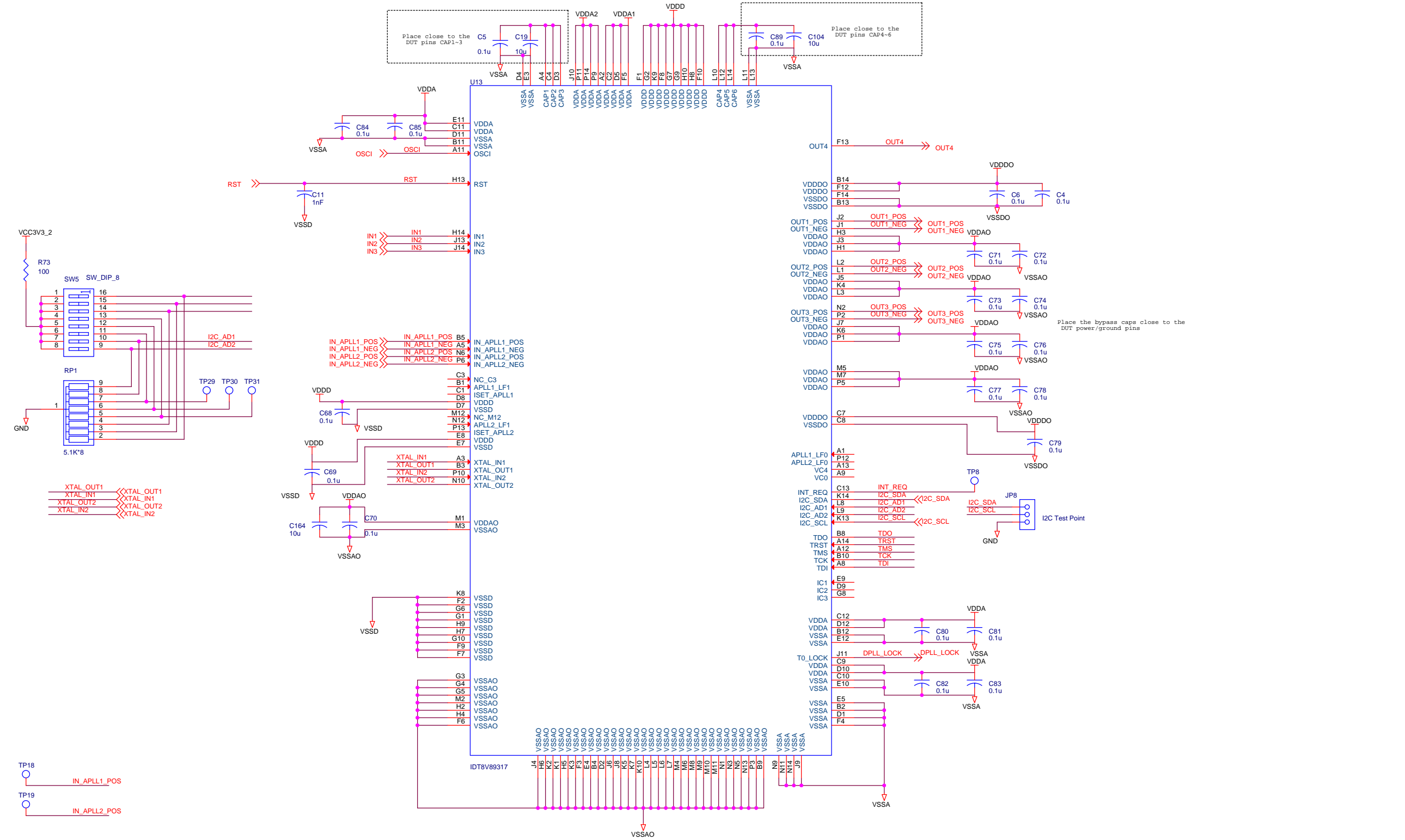
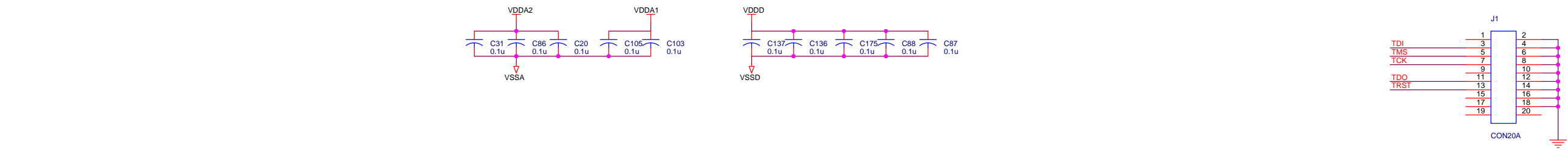


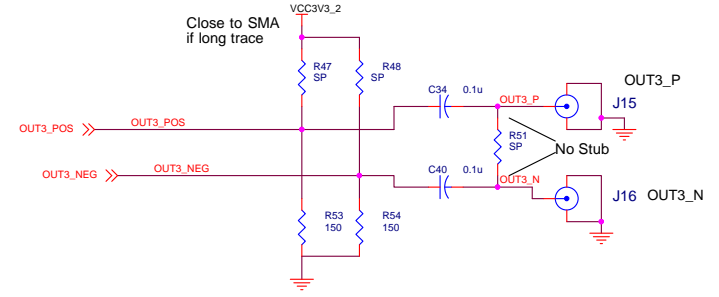
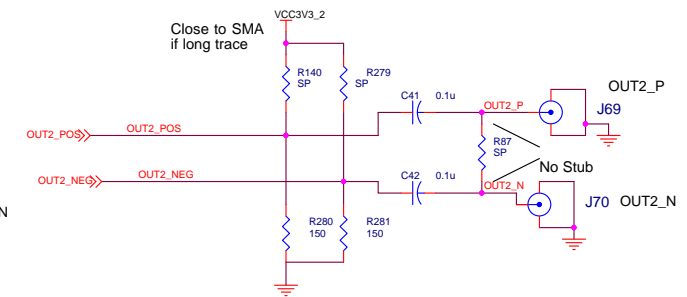
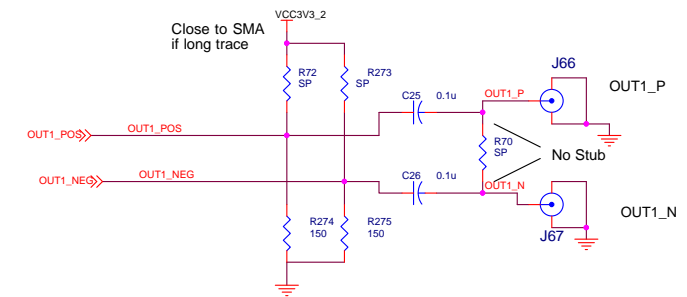
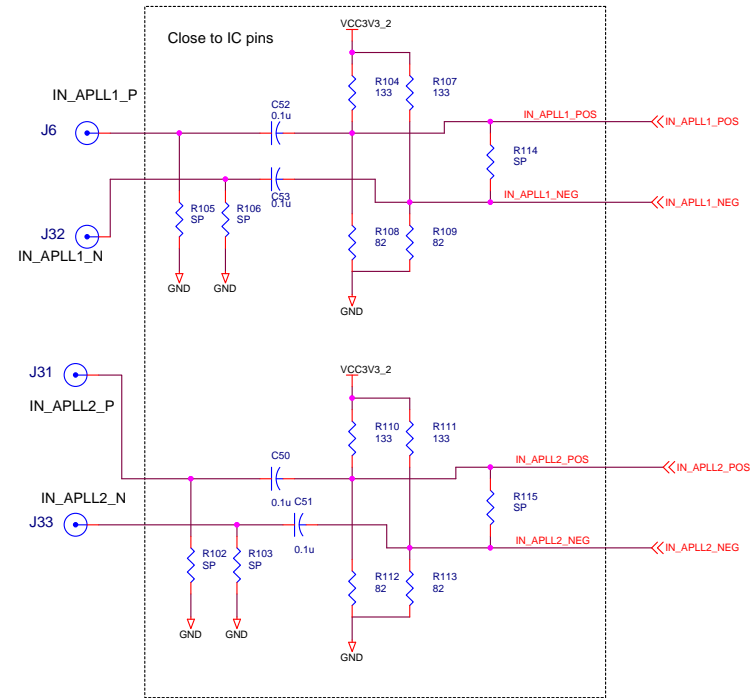
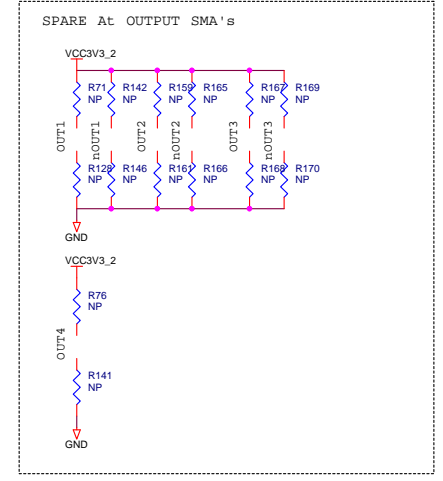
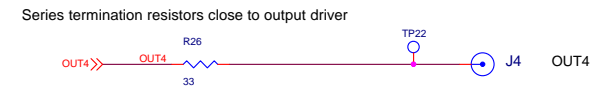
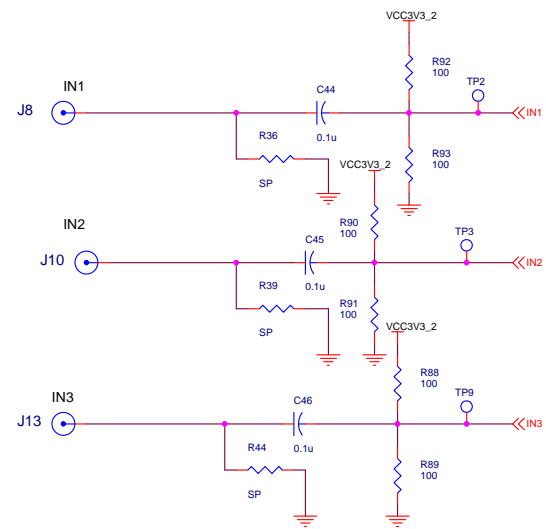
Disclaimer: IDT is providing this schematic for reference purposes only. Although the schematic was taken from a known working design, it is being provided "as is" without any express or implied warranty of any kind.



Title		
SCHEMATIC, 8V89317EVB REV A		
Size	Document Number	Rev
A	Block Diagram	0.0
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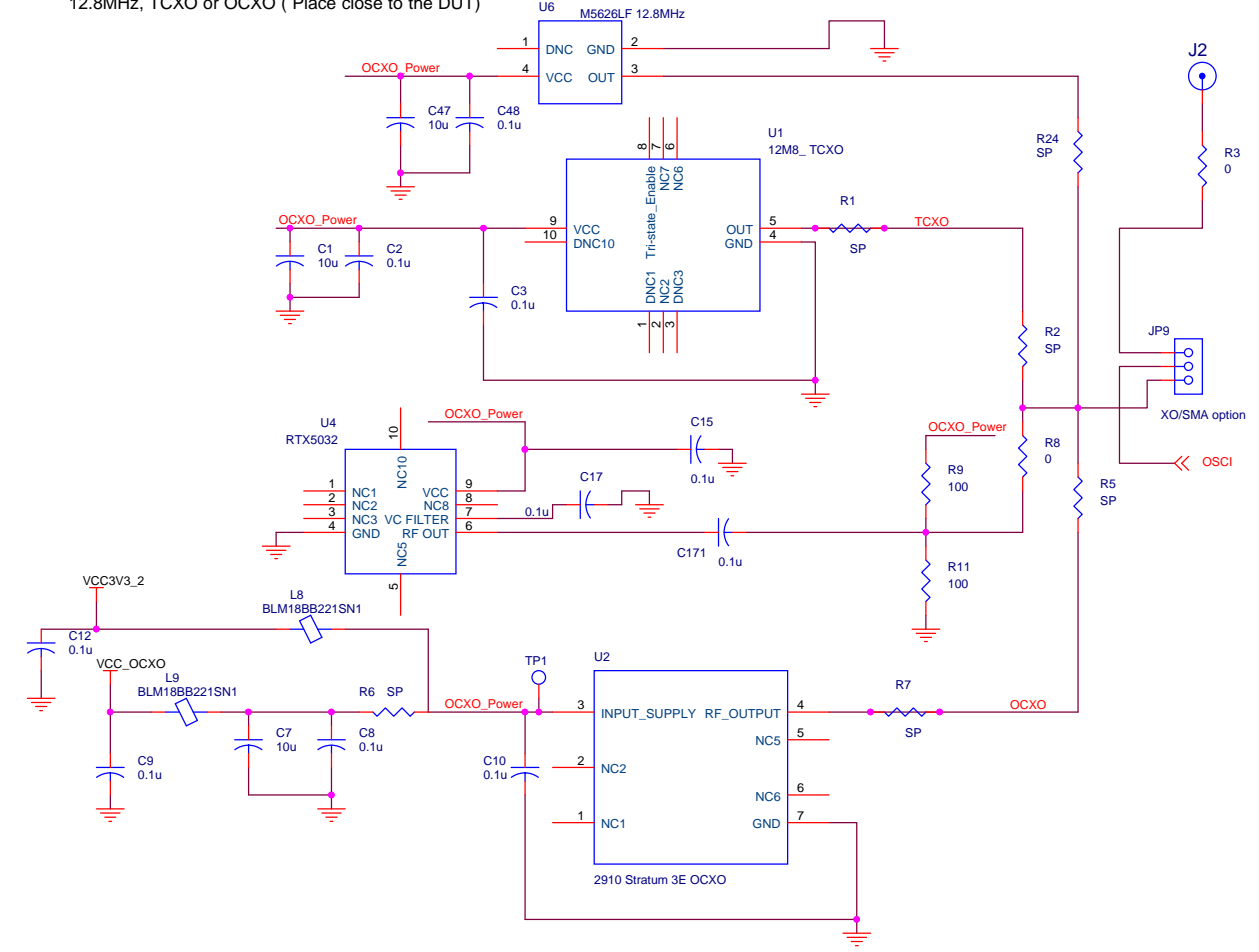
Title			
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SMA's for input can be either END LAUNCH or STRAIGHT depends on which way save space. TBD during layout

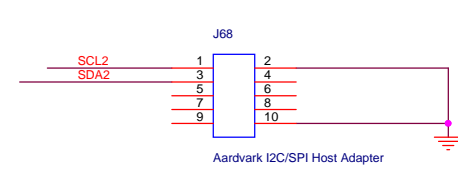
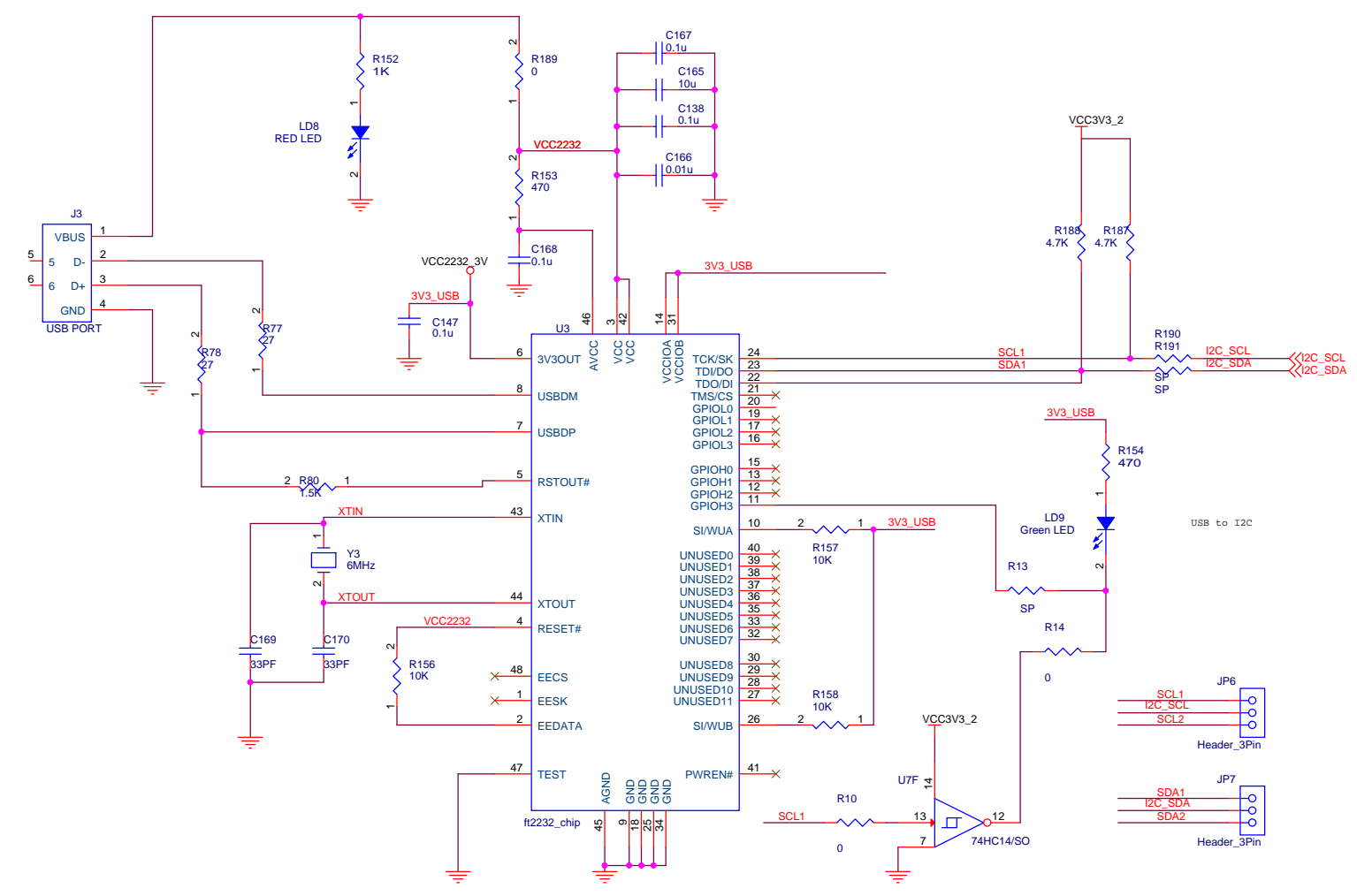
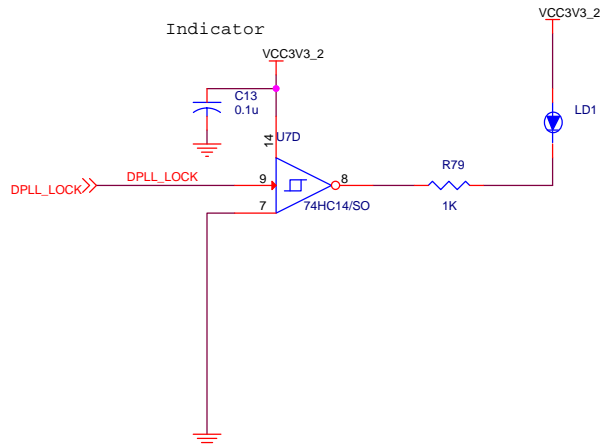
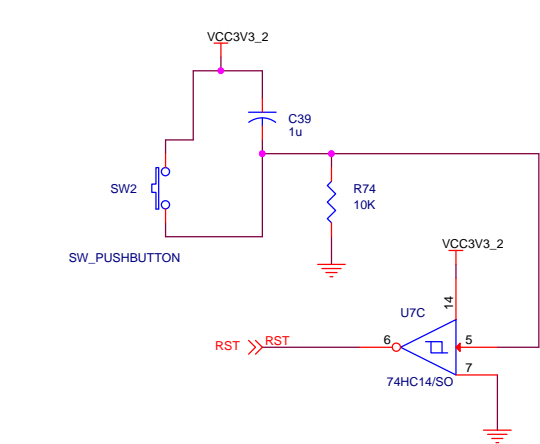
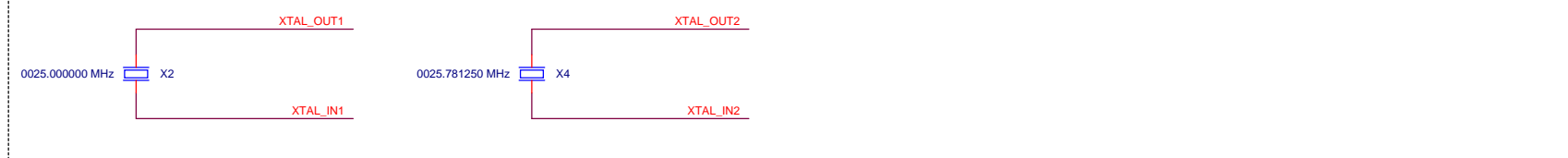
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SCHEMATIC, 8V89317 EVB REV A			
Size	Document Number	Rev	
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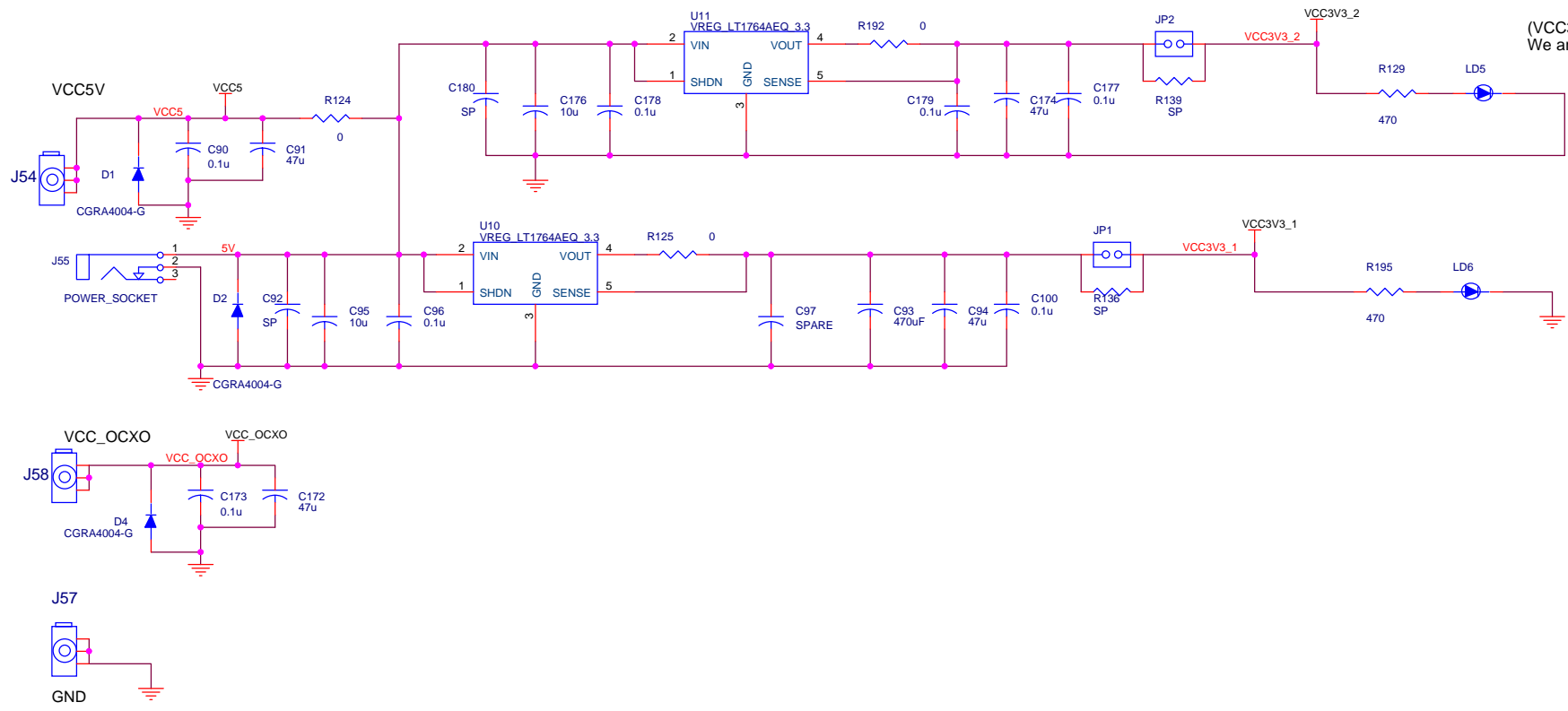
12.8MHz, TCXO or OCXO (Place close to the DUT)



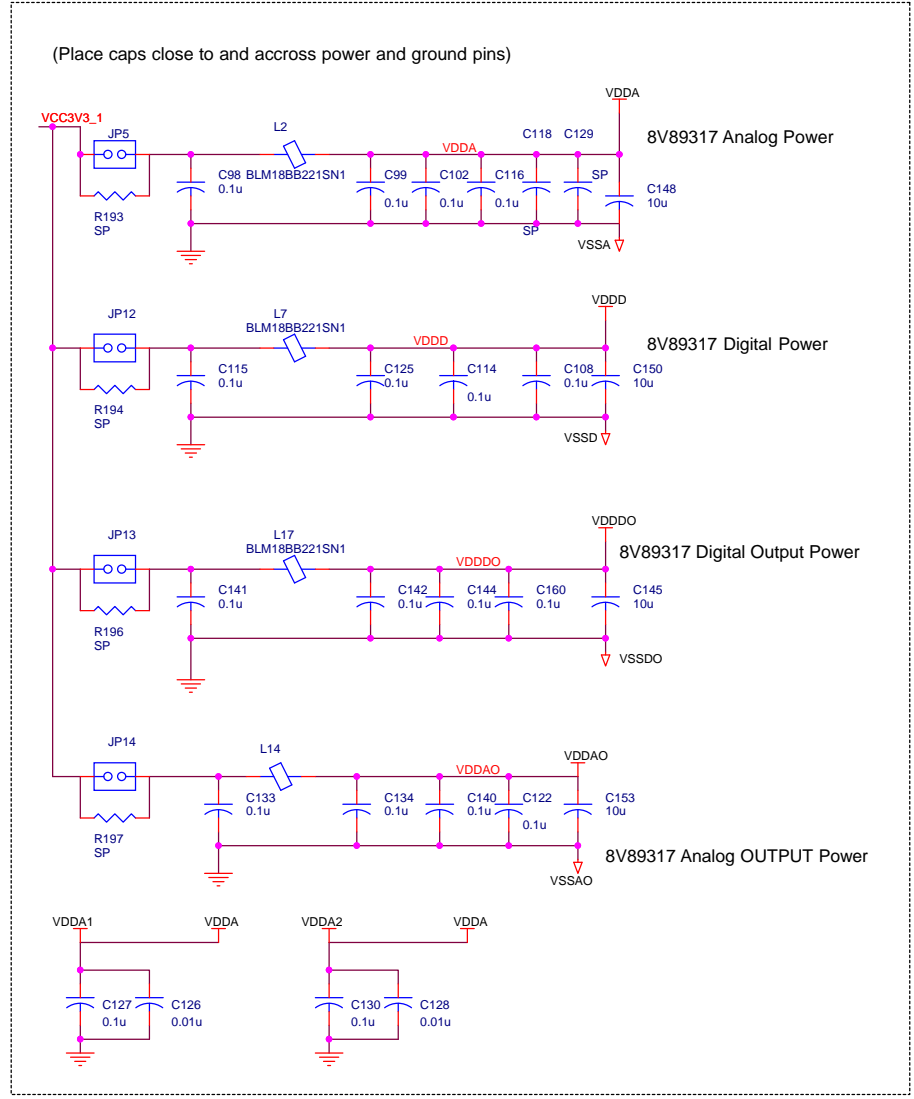
25MHz XTAL Interface (Place close to the DUT and Put xtals on same layer as BGA pads, shorter trace length, no stubs)

- 1) Clocks and frequently switched signals should not be routed close to the crystals.
- 2) Digital signals should not be routed directly under the crystal or XTALn_IN/OUT pins.
- 3) Keep the crystal bond pads and trace width to the XTALn_IN/OUT pins as small as possible.
- 4) All metal layers in the PCB are recommended to be removed under the XTALn_OUT ball, crystal pad and associated trace.
- 5) It is recommended to protect crystal traces with ground traces and guard rings.





(VCC3V3_1 is used for the 8V89317 DUT and VCC3V3_2 is for the rest of the board circuits. We are not suggesting a dedicated LDO for the 8V89317 with this reference design, this is just convenient for the test.)



Title		
SCHEMATIC, 8V89317 EVB REV A		
Size	Document Number	Rev
C	Power/GND	0.0
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