RX FAMILY HARDWARE MANUAL GUIDANCE (ELECTRICAL CHARACTERISTICS 1)

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RENESAS ELECTRONICS

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ABSOLUTE MAXIMUM RATINGS

60.1 Absolute Maximum Ratings

Table 60.1 Absolute Maximum Rating

Conditions: VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, VCC_USB	–0.3 to +4.0	V
V_{BATT} power supply voltage		V_{BATT}	–0.3 to +4.0	V
Input voltage (except for ports for 5 V tolerant*1)		V_{in}	–0.3 to VCC + 0.3 (up to 4.0)	V
Input voltage (ports for 5 V tolerant*1)		V_{in}	–0.3 to VCC + 4.0 (up to 5.8)	V
Reference power supply voltage		VREFH0	–0.3 to AVCC0 + 0.3 (up to 4.0)	V
Analog power supply voltage		AVCC0, AVCC1*2	–0.3 to +4.0	V
Analog input voltage		V_{AN}	–0.3 to AVCC + 0.3 (up to 4.0)	V
Junction temperature	D version	T_j	–40 to +105	°C
	G version	T_j	–40 to +125	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 2. Connect the AVCC0, AVCC1, and VCC_USB pins to VCC, and the AVSS0, AVSS1, and VSS_USB pins to VSS. When the A/D converter unit 0 is not to be used, connect the VREFH0 pin to VCC and the VREFL0 pin to VSS, respectively. Do not leave these pins open. Insert capacitors of high frequency characteristics between the AVCC0 and AVSS0 pins, or AVCC1 and AVSS1 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

The range that does not cause "permanent damage" to the LSI. It doesn't mean the normal operation is guaranteed.

Requirements to guarantee the following electrical characteristics

The voltage ranges of power supply that don't cause permanent damage

The input voltage ranges that don't cause permanent damage to pins.

The value in the bracket is applied when VCC or AVCC is equal or greater than the minimum voltage described in the recommended operating voltage.

Junction temperature range that doesn't cause permanent damage

The storage temperature when the chip doesn't operate

Supplementary information for electrical property items.
Necessary conditions for use.

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RECOMMENDED OPERATING CONDITIONS

The USB power supply's specification differs between when USB is in use (3.3V) and when USB is not in use (5V). If VCC_USB is connected to 5V VCC since USB is not in use initially, the change to use USB later will cause incompliance to USB power supply's specification. Please make sure to comply with USB power supply's specification.

The temperature at which the operation is guaranteed. Equivalent to Ta unless otherwise specified.

This relationship should be maintained during power-up as well

Must follow the recommended value for the smoothing capacitor for internal power supply stabilization. Otherwise, the normal operation couldn't be guaranteed.

Table 45.2 Recommended operating conditions (1)

Item			Symbol	Min.	Typ.	Max.	Unit
Power supply voltage			VCC*1	2.7	—	5.5	V
			VSS	—	0	—	
USB power supply voltage*2		When USB in use	VCC_USB*1	3.0	—	3.6	
			VSS_USB	—	0	—	
		When USB not in use	VCC_USB	—	VCC	—	
			VSS_USB	—	VSS	—	
Analog power supply voltage*3			AVCC0, AVCC1, AVCC2*1	3.0	—	5.5	
			AVSS0, AVSS1, AVSS2	—	0	—	
Input voltage	PB1, PB2, PC0*4, and PD2*4		V_{in}	–0.3	—	5.8	
	P40 to P42, and P44 to P46	With negative input enabled*5		–1.0	—	AVCC1 + 0.3	
		With negative input disabled		–0.3	—		
	PH0, PH4	With negative input enabled*5		–0.5	—	AVCC1 + 0.3	
		With negative input disabled		–0.3	—		
	P43, P47, PH1 to PH3, and PH5 to PH7			–0.3	—	AVCC1 + 0.3	
	P50 to P55, and P60 to P65			–0.3	—	AVCC2 + 0.3	
	USB0_DP, USB0_DM			–0.3	—	VCC_USB + 0.3	
	Other than above			–0.3	—	VCC + 0.3	
Operating temperature	D version		T_{opr}	–40	—	85	°C
	G version			–40	—	105	

Note 1. Comply with the following voltage condition: VCC_USB ≤ VCC ≤ AVCC0 = AVCC1 = AVCC2
Note 2. When the USB interface is not to be used, connect VCC_USB to VCC and VSS_USB to VSS, and set VOLSR.USBVON=0.
Note 3. When not using any of the12-bit A/D converter (unit 0 to 2), 12-bit D/A converter, comparator C, or temperature sensor, connect AVCC0, AVCC1, and AVCC2 to VCC, and AVSS0, AVSS1, and AVSS2 to VSS, respectively. For details, refer to section 38.6.10, Voltage Range of Analog Power Supply Pins.
Note 4. This is only available for products with 128 Kbytes of RAM.
Note 5. When VOLSR.PGAVLS = 0 and ADPGADCR0.PxDEN = 1 (x = 000, 001, 002, 100, 101, 102).

Table 45.3 Recommended operating conditions (2)

Item	Symbol	Value
Decoupling capacitance to stabilize the internal voltage	C_{VCL}	0.47 µF ± 30%*1

Note 1. Use a multilayer ceramic capacitor whose nominal capacitance is 0.47 µF and a capacitance tolerance is ±30% or better.

Conditions to guarantee AC specifications and normal operation

The reference voltage might be different between pins

Refer to the application note for precaution of high-temperature operation.

Notes on High-Temperature Operation

VCL should be connected only to VSS via a capacitor.(Do not connect to VCC)

Only multilayer ceramic capacitors should be used

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Table 45.4 DC Characteristics (1)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	CAN input pin MTU input pin GPTW input pin POE input pin POEG input pin TMR input pin SCI input pin ADTRG# input pin RES#, NMI	V_{IH}	0.8 × VCC	—	—	V	
		V_{IL}	—	—	0.2 × VCC		
		ΔV_T	0.06 × VCC	—	—		
	IRQ input pin (except for P52 to P55, and P60 to P65)	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
		ΔV_T	0.06 × VCC	—	—		
	IRQ input pin (P52 to P55, and P60 to P65)	V_{IH}	0.8 × AVCC2	—	—		
		V_{IL}	—	—	0.2 × AVCC2		
		ΔV_T	0.06 × AVCC2	—	—		
	RIIC input pin (except for SMBus)	V_{IH}	0.7 × VCC	—	—		
		V_{IL}	—	—	0.3 × VCC		
		ΔV_T	0.06 × VCC	—	—		
	Pins for 5 V tolerant (PB1, PB2, PC0*1, and PD2*1)	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
	Analog input pins (P40 to P47, and PH0 to PH7)	V_{IH}	0.8 × AVCC1	—	—		
		V_{IL}	—	—	0.2 × AVCC1		
	Analog input pins (P50 to P55, and P60 to P65)	V_{IH}	0.8 × AVCC2	—	—		
		V_{IL}	—	—	0.2 × AVCC2		
	Other input pins (pins other than those above)	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
High-level input voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	0.9 × VCC	—	—	V	
	EXTAL, WAIT#, RSPI input pin		0.8 × VCC	—	—		
	D0 to D15		0.7 × VCC	—	—		
	RIIC (SMBus)		2.1	—	—		
Low-level input voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	—	—	0.1 × VCC	V	
	EXTAL, WAIT#, RSPI input pin		—	—	0.2 × VCC		
	D0 to D15		—	—	0.3 × VCC		
	RIIC (SMBus)		—	—	0.8		

Note 1. This is only available for products with 128 Kbytes of RAM.

Required conditions to guarantee the following specifications

The reference voltage might be different between pins

Hysteresis width cannot be guaranteed for terminals without ΔV, so only VIH and VIL are guaranteed.

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DC CHARACTERISTICS

Table 45.5 DC Characteristics (2)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V, VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
High-level output voltage	P43, P47, PH1 to PH3, and PH5 to PH7	V_{OH}	AVCC1 – 0.5	—	—	V	I_{OH} = –1.0 mA
	P50 to P55, and P60 to P65		AVCC2 – 0.5	—	—		I_{OH} = –1.0 mA
	P90 to P95, P71 to P76, P81, PB5, and PD3		VCC – 1.0	—	—		I_{OH} = –5.0 mA (when the large current output is set)
	Other than above		VCC – 0.5	—	—		I_{OH} = –1.0 mA
Low-level output voltage	P43, P47, PH1 to PH3, and PH5 to PH7	V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
	P50 to P55, and P60 to P65		—	—	0.5		I_{OL} = 1.0 mA
	P90 to P95, P71 to P76, P81, PB5, and PD3		—	—	1.0		I_{OL} = 15 mA (when the large current output is set)
	RIIC pins		—	—	0.4		I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	Other than above		—	—	0.5		I_{OL} = 1.0 mA
Input leakage current	RES#, MD pin, PE2, and EMLE*1	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = VCC
	P40 to P42, and P44 to P46		—	—	1.0		V_{in} = 0 V V_{in} = AVCC1
	PH0 and PH4		—	—	1.0		V_{in} = 0 V V_{in} = AVCC1 VOLSR.PGAVLS = 1
Three-state leakage current (off state)	RIIC pins	$\lvert I_{TSI} \rvert$	—	—	5.0		V_{in} = 0 V V_{in} = VCC
	Other than above		—	—	1.0		
Input pull-up resistors current	P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65	I_p	–300	—	–10		AVCC1 = AVCC2 = 3.0 to 5.5 V V_{in} = 0 V
	Pins other than those above and PE2		–300	—	–10		VCC = 2.7 to 5.5 V V_{in} = 0 V
Input pull-down resistors current	EMLE		10	—	300		V_{in} = VCC = AVCC
Input capacitance	RIIC pins, PH0, and PH4	C_{in}	—	—	16	pF	V_{bias} = 0 V V_{amp} = 20 mV f = 1 MHz T_a = 25°C
	USB0_DP, and USB0_DM pins		—	—	16		
	Other than above		—	—	8		
Output voltage of the VCL pin		V_{CL}	—	1.25	—	V	

Note 1. The input leakage current value at the EMLE pin is only when V_{in} = 0 V.

Required conditions to guarantee the following specifications

For information under the test conditions which are not listed here, refer to the IBIS model

Leakage current of terminals other than those described in the "Input Leakage Current" item.
The off state refer to the high impedance state

Built-in pull-up resistor value can be calculated by using this value

Pull-up resistor = voltage in use ÷ Ip

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Current consumption when all functions except BGO are in operation.

Current consumption value when BGO is not working and the clock to modules described in Module Stop Control Registers is supplied/stopped

Current consumption value of each low power consumption mode. Refer to Low Power Consumption chapter for the peripheral state of each modes.

(Below is an example of RX66T)

Table 11.2 Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Entering and Exiting Low Power Consumption Modes and Operating States	Sleep Mode	All-Module Clock Stop Mode	Software Standby Mode	Deep Software Standby Mode
Transition condition	Control register + instruction	Control register + instruction	Control register + instruction	Control register + instruction
Method of release other than reset	Interrupt	Interrupt*1	Interrupt*2	Interrupt*3
State after release*4	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Program execution state (reset processing)
Main clock oscillator	Operating possible	Operating possible	Stopped	Stopped
High-speed on-chip oscillator	Operating possible	Operating possible	Stopped	Stopped
Low-speed on-chip oscillator	Operating possible	Operating possible	Stopped	Stopped
IWDT-dedicated on-chip oscillator	Operating possible*5	Operating possible*5	Operating possible*5	Stopped (Undefined)*5
PLL	Operating possible	Operating possible	Stopped	Stopped
CPU	Stopped (Retained)	Stopped (Retained)	Stopped (Retained)	Stopped (Undefined)
RAM and ECCRAM	Operating possible (Retained)	Stopped (Retained)	Stopped (Retained)	Stopped (Undefined)
Flash memory	Operating	Stopped (Retained)	Stopped (Retained)	Stopped (Retained)
USBFS host/function module (USBb)	Operating possible	Stopped*6	Stopped*6	Stopped (Undefined)
Watchdog timer (WDTA)	Stopped (Retained)	Stopped (Retained)	Stopped (Retained)	Stopped (Undefined)
Independent watchdog timer (IWDT)	Operating possible*5	Operating possible*5	Operating possible*5	Stopped (Undefined)*5
Port output enable (POE)	Operating possible	Operating possible*7	Stopped (Retained)	Stopped (Undefined)
8-bit timer (unit 0, unit 1) (TMR)	Operating possible	Operating possible*8	Stopped (Retained)	Stopped (Undefined)
Voltage detection circuit (LVDA)	Operating possible	Operating possible	Operating possible	Operating possible*9
Power-on reset circuit	Operating	Operating	Operating	Operating
Peripheral modules	Operating possible	Stopped (Retained)	Stopped (Retained)	Stopped (Undefined)
I/O ports	Operating	Retained*10	Retained*11	Retained*11

Required conditions to guarantee the following specifications

Table 45.6 DC Characteristics (3) (Products with 64 Kbytes of RAM, D version)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item			Symbol	D version Min.	D version Typ.	D version Max.	Unit	Test Conditions
Supply current*1	Normal operating mode	Full operation*2	I_{CC}*3	—	—	75	mA	ICLK = 160 MHz PCLKA = 80 MHz PCLKB = 40 MHz PCLKC = 160 MHz PCLKD = 40 MHz FCLK = 40 MHz BCLK = 40 MHz BCLK pin = 40 MHz
		Normal operation: Peripheral module clocks are supplied*4		—	21	—		
		Normal operation: Peripheral module clocks are stopped *4, *5		—	12	—		
		CoreMark: Peripheral module clocks are stopped *4, *5		—	21	—		
		Sleep mode: Peripheral module clocks are supplied*4		—	18	37		
		All module clock stop mode (reference value)		—	9.4	23		
		Increase current by BGO operation*6		—	13	—		
		Increase current by operating Trusted Secure IP		—	3.9	5.0		
	Software standby mode			—	0.9	7.0		VOLSR.PGAVLS = 1
	Deep software standby mode			—	14	20	µA	VOLSR.PGAVLS = 1

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.
Note 2. Peripheral module clocks are supplied. This does not include operations as BGO (background operations).
Note 3. I_{CC} depends on f (ICLK) as follows.
(when ICLK : PCLKA : PCLKB : PCLKC : PCLKD : BCLK : BCLK pin = 4 : 2 : 1 : 4 : 1 : 1 : 1 and EX
• D version product
I_{CC} Max. = 0.375 × f + 15 (full operation in high-speed operating mode)
I_{CC} Typ. = 0.099 × f + 5 (normal operation in high-speed operating mode)
I_{CC} Max. = 0.135 × f + 15 (sleep mode)
Note 4. This does not include operations as BGO (background operations). Whether the peripheral module stopped is controlled only by the bit settings in the module stop control registers A to D.
Note 5. When peripheral module clocks are stopped, each clock frequency is set for division by 64, and the f PCLKA, PCLKB, PCLKC, PCLKD, and the BCLK pin are the same.
Note 6. This is an increase caused by program/erase operation to the code flash memory or data flash memory during executing the user program.

Differences in Typ/max are due to temperature, manufacturing variations, etc. (in particular due to temperature)

How to calculate the actual current consumption is described in “Precautions for high temperature operation of each group”. For details, please refer to the document below.

Useful Information for RX MCUs

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Required conditions to guarantee the following specifications

Table 45.11 DC Characteristics (5)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

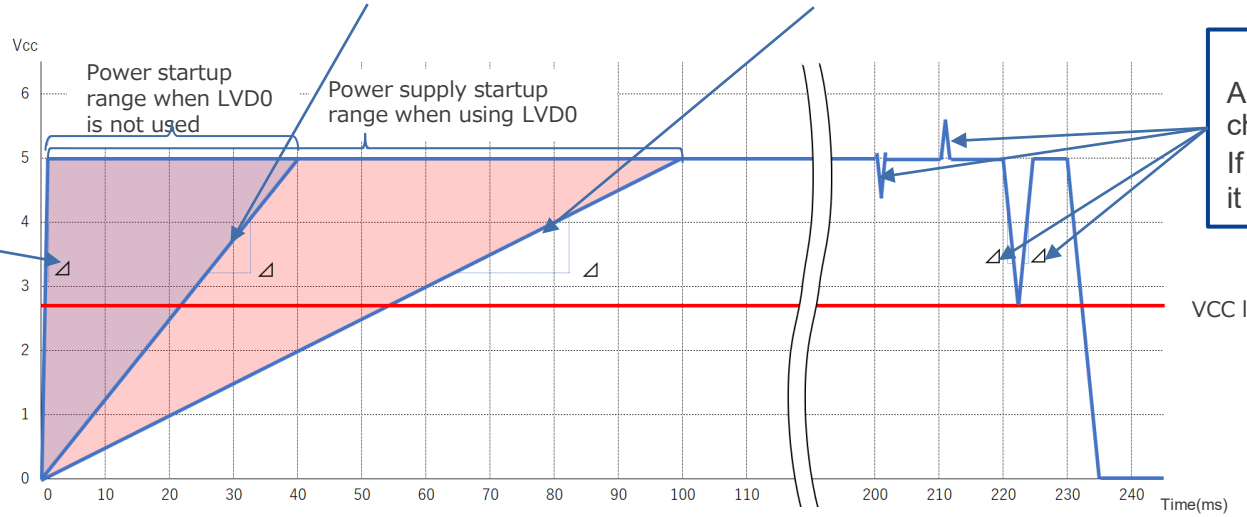
Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VCC ramp rate at power-on	At normal startup	SrVCC	0.02	—	8	ms/V	
	Voltage monitoring 0 reset enabled at startup*1, *2		0.02	—	20		
VCC ramp rate at power fluctuation		dt/dVCC	1.0	—	—		When VCC change exceeds VCC ±10%

Note 1. When OFS1.LVDAS = 0.
Note 2. Settings of the OFS1 register are not read in boot mode or user boot mode, so turn on the power supply voltage with a ramp rate at normal startup.

Allowable slope of power supply variation when VCC variation exceeds ±10%.

SrVCC(MAX)
VCC ramp rate at power-on when LVD0 is not used. If the VCC ramp rate is slower than this, it is out of the guaranteed range (8ms/V)

SrVCC(MAX)
VCC ramp rate at power-on when LVD0 is used. If the VCC ramp rate is slower than this, it is out of the guaranteed range (20ms/V)



Example when VCC=5V

dt/dVCC
Allowable rising/falling slope of a voltage change (greater than ±10%).
If a voltage change is more rapid than this, it is out of the guaranteed range. (1ms/V)

SrVCC(MIN)
if VCC ramp rate at power-on is more rapidly than this, it is out of the guaranteed range (0.02ms/V)

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Required conditions to guarantee the following specifications

The current value that flows in from external

Average current over MCU driving time.

(Example) If the values of 3 pin are 1mAh, 2mAh and 3mAh, the average value per pin is 6mA/3h = Average 2mA/h

The maximum allowable current value that can flow in per pin. If this value is exceeded, reliability cannot be ensured.

Total current value of all MCU output pins

The current value that flows out from MCU

Port driving ability set by Port Capacity Control register (DSCRx). The output impedance is as follows.

Normal drive > High drive > High speed interface high drive

Table 61.8 Permissible Output Currents

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	2.0	mA
	All output pins*2	High drive		—	—	3.8	
	All output pins*3	High-speed interface high-drive		—	—	7.5	
Permissible output low current (max. value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	4.0	mA
	All output pins*2	High drive		—	—	7.6	
	All output pins*3	High-speed interface high-drive		—	—	15	
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–2.0	mA
	All output pins*2	High drive		—	—	–3.8	
	All output pins*3	High-speed interface high-drive		—	—	–7.5	
Permissible output high current (max. value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–4.0	mA
	All output pins*2	High drive		—	—	–7.6	
	All output pins*3	High-speed interface high-drive		—	—	–15	
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	—	—	–80	mA

Caution: To protect the MCU's reliability, the output current values should not exceed the values in Table 61.8.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

Note 3. This is the value when high-speed interface high-driving ability is set with a pin for which high-speed interface high-driving ability is selectable.

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Table 45.13 Thermal Resistance Value (Reference)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Package	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Thermal resistance	144-pin LFQFP (PLQP0144KA-B)	θ_{ja}	—	—	32.4	°C/W	JESD51-2 and JESD51-7 compliant
	112-pin LQFP (PLQP0112JA-B)		—	—	33.8		
	100-pin LFQFP (PLQP0100KB-B)		—	—	35.0		
	80-pin LFQFP (PLQP0080KB-B)		—	—	36.3		
	80-pin LQFP (PLQP0080JA-A)		—	—	35.7		
	64-pin LFQFP (PLQP0064KB-C)		—	—	37.9		
	144-pin LFQFP (PLQP0144KA-B)	Ψ_{jt}	—	—	0.6		
	112-pin LQFP (PLQP0112JA-B)		—	—	0.6		
	100-pin LFQFP (PLQP0100KB-B)		—	—	0.8		
	80-pin LFQFP (PLQP0080KB-B)		—	—	0.8		
	80-pin LQFP (PLQP0080JA-A)		—	—	0.8		
	64-pin LFQFP (PLQP0064KB-C)		—	—	0.8		

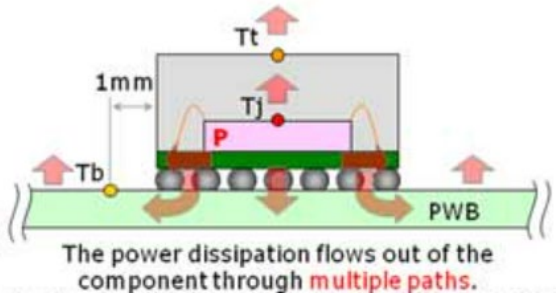
Note: The values are reference values when the 4-layer printed circuit board is used. Thermal resistance depends on the number of layers and size of the board. For details, refer to the JEDEC standards.

Thermal resistance according to JEDEC standard.
Please refer to below for details.

<Heat-dissipation Mechanism | Renesas>

Θja=(Tj-Ta)/P

Ψjt=(Tj-Tt)/P



Ta: Temperature of a place not affected by a heat source

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