

# **RL78 Software Migration Guide**

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CS+ to e<sup>2</sup> studio Migration (CC-RL)

#### Introduction

This application note is a guide that explains how to modify a project created in C compiler CC-RL for the integrated development environment CS+, preparing it for use as a project created in e<sup>2</sup> studio, also a Renesas integrated development environment (IDE).

Supported IDE versions

- CS+ V3.01.00
- $\cdot e^2$  studio V4.0.0.26

#### **Target Device**

RL78 Family

When applying this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.



## Contents

1.	CS+ Project Import	3
2.	Debugger Connection	6
3.	Debug Configuration File Modification	22
4.	Sample Code	23
5.	Reference Documents	23



## 1. CS+ Project Import

(1) After starting up the Renesas Electronics e<sup>2</sup> studio IDE, go to [File] and select [Import...].

File	] Edit Source Refactor Naviga	ate Search Project Rene	sas Views Rui	n Window	Help						
	New Open File	Alt+Shift+N ►	₫ • 🚳 •	<u>c</u> • © •	* • C	• •	• 😕 🔗	•	17   <b>k</b>	- N	
	Close	Ctrl+W									
	Close All	Ctrl+Shift+W									
	Save	Ctrl+S									
	Save As										
B	Save All	Ctrl+Shift+S									
	Revert										
	Move										
	Rename	F2									
Ð	Refresh	F5									
	Convert Line Delimiters To	•									
6	Print	Ctrl+P									
	Switch Workspace	+									
	Restart										
2	Import										
2	Export										
	Properties	Alt+Enter									
	1 rl78_l13_eel_r01an2014_iar.d87 [l	Jse]									
	Exit										

Figure 1.1 File Menu



(2) From [General], select [Renesas Common Project File], then click [Next >].

e² Import	
Select Rename and Import and Existing C/C++ Project into the workspace	Ľ
Select an import source:	
type filter text	
<ul> <li>General</li> <li>Archive File</li> <li>Existing Projects into Workspace</li> <li>File System</li> <li>HEW Project</li> <li>Preferences</li> <li>Renease Common Project File</li> <li>C/C++</li> <li>Code Generator</li> <li>CVS</li> <li>Install</li> <li>Run/Debug</li> <li>Team</li> </ul>	
? < Back Next > Finish	Cancel

Figure 1.1 Project Import Wizard (1/2)



(3) Select the Renesas Common Project File (.rcpe) created in CS+. Change the debug software to [E1/E20 (RL78)], and click [Finish (F)] to import the project. ("Select Target" automatically shows a device setup in CS+.)

Import Import Projects Renesas_CCRL	V1.01.00 version is missing. The project would be upgraded to v1.01.00	
-	e format versions 1.00 or less are supported. ssembler, Linker and Library Generator settings will be imported.	
Select file :	D:\r01an2827_fld\r01an2827_fld.rcpe	Browse
Select Target	R5F100LE	
Debug Hardware	E1/E20 (RL78)	•
?	< Back Next > Finish	Cancel

Figure 1.2 Project Import Wizard (2/2)



### 2. Debugger Connection

(1) Display the menu in Project Explorer by right-clicking on the imported project name. In the menu, select [**Properties (R)**].

		lavigate Search Project Re	
G	0.	• 💀 🔪 💽 💋 🐔	
Project Explorer			
⊿ 🚰 r01an2827_fld [Defa	ultR		
Includes		New	•
incrl78		Go Into	
⊳ 🔁 librl78		Open in New Window	
▷ 2 r01an2827_fld		open in ten thilden	
Src S cstart.asm	Ð	Сору	Ctrl+C
is cstattasti	ß	Paste	Ctrl+V
⊳ lcd.c	×	Delete	Delete
⊳ ln lcd.h		Source	
r_cg_cgc_user.c		Move	
⊳ 💼 r_cg_cgc.c			-
⊳ h r_cg_cgc.h		Rename	F2
r_cg_intc_user.c	R M	Import	
r_cg_intc.c	2	Export	
h r_cg_intc.h		Laportan	
Ic r_cg_it_user.c		Build Project	
⊳ <u>c</u> r_cg_it.c		Clean Project	
⊳ <mark>lh</mark> r_cg_it.h	6	Refresh	F5
h r_cg_macrodriver.		Close Project	
r_cg_port_user.c			
▷ .c r_cg_port.c		Close Unrelated Projects	
▷ In r_cg_port.h ▷ Ic r_cg_timer_user.c		Build Configurations	F.
Image: second		Make Targets	
▷ h r_cg_timer.h		Index	
in r_cg_userdefine.h		INCEX	,
i r_main.c		Exclude from build	
⊳ c r_pfdl.c		Profile As	÷
I r_systeminit.c		Debug As	•
⊳ 🔥 rskrl78g13def.h		Run As	
stkinit.asm			
M hdwinit.asm		Team	•
Main.c		Compare With	+
in r01an2827_fld.mtp		Restore from Local History	
r01an2827_fld.rcp	e <sup>2</sup>	Renesas Quick Settings	Alt+Q
Code Generator	e <sup>2</sup>	Renesas Tool Settings	Alt+T
	*	Run C/C++ Code Analysis	
		Windows Explorer	
	635-	Command Prompt	
		Properties	Alt+Enter

Figure 2.1 Project Menu

(2) From the [C/C++ Build] menu, select [Settings]. From [Tool Settings], select [Converter] → [Output]. In the output settings, delete the output hex file to prevent the file from being output.



Figure 2.2 Project Properties (1/6)

(3) Select [Compiler]  $\rightarrow$  [Source], then modify the include file directory. (Add "../" before the directory name.)

\*Step (3) is only necessary for projects that include a library.



Figure 2.3 Project Properties (2/6)



(4) Select [Assembler]  $\rightarrow$  [Source], then modify the include file directory. (Add "../" before the directory name.)

\*Step (4) is only necessary for projects that include a library.





(5) Select [Linker]  $\rightarrow$  [Input], then input the name of the library to be included. (Select from the library folder.)

\*Step (5) is only necessary for projects that include a library.

-	Settings	
	Configuration: DefaultBuild [ Active ] Tool Settings  Build Steps  Build Artifact  Binary Parsers  Error Parsers C. Click add button.	▼) Manage Configurati

Figure 2.5 Project Properties (4/6)



(6) Select the **[Linker] Device**. Make sure "Set enable/disable on-chip debug by link option" and "Set user option byte" are set in the same manner as CS+. (The import may be disabled even if it is set to enabled in CS+.)



Figure 2.6 Project Properties (5/6)



(7) Select the **[Linker] Section**, and then set the entry point symbol.



Figure 2.7 Project Properties (6/6)

- \* Step (7) can be skipped by pre-setting it as shown in Figure 2.8 on the CS+ side.
  - (1) Select the CC-RL link option tab.
  - (2) Under Output Code, specify YES(-ENTry) in the specify execution start address box.
  - (3) Set execution start address to [\_start].



Figure 2.8 Link Options (CS+)

(8) In the project explorer, right click on the imported project name to display the following menu. Select [Build **Project (B)**].

	New Go Into	÷
	Open in New Window	
D	Сору	Ctrl+C
ß	Paste	Ctrl+V
×	Delete	Delete
	Source	+
	Move	
	Rename	F2
No.	Import	
2	Export	
	Build Project	
	Clean Project	
80	Refresh	F5
	Close Project	
	Close Unrelated Projects	
	Build Configurations	۲
	Make Targets	•
	Index	+
	Exclude from build	
	Profile As	+
	Debug As	+
	Run As	+
	Team	+
	Compare With	+
	Restore from Local History	
e <sup>2</sup>	Renesas Quick Settings	Alt+Q
e <sup>2</sup>	Renesas Tool Settings	Alt+T
梦	Run C/C++ Code Analysis	
	Windows Explorer	
es	Command Prompt	
	Properties	Alt+Enter

Figure 2.9 Build Project

(9) From the **[Run]** menu, select **[Debug Configurations...(B)]**.

Figure 2.10 Run Menu

Select [Renesas GDB Hardware Debugging], click the "New" 📑 icon to create a new configuration. (10)

e <sup>2</sup> Debug Configurations		x
Create, manage, and run configurations		Ť.
Image: Second system         Image: Second system	Configure launch settings from this dialog: <ul> <li>Press the 'New' button to create a configuration of the selected type.</li> <li>Press the 'Duplicate' button to copy the selected configuration.</li> <li>Press the 'Delete' button to remove the selected configuration.</li> <li>Press the 'Filter' button to configure filtering options.</li> <li>Edit or view an existing configuration by selecting it.</li> </ul> <li>Configure launch perspective settings from the 'Perspectives' preference page.</li>	
		Debug Close

Figure 2.11 Debug Configurations (1/5)



(11) Go to the Debug Configurations [Main] tab, click [Search project (H)] in the C/C++ application, and add [Load module file (.x)] located in the project build folder (the file output in step (8)).

e <sup>2</sup> Debug Configurations		<u> </u>
Create, manage, and run configurations Ø Program not specified	1. Go to Main	- <b>A</b>
Image: Second secon	Name: te. tab.	) 🖅 Source
<ul> <li>C GDB Hardware Debugging</li> <li>C GDB Simulator Debugging (SH, RL78, RH850)</li> <li>➢ Renesas GDB Hardware Attach</li> <li>✓ Renesas GDB Hardware Debugging</li> <li>C * New_configuration [local]</li> <li>C * test DefaultBuild [local]</li> <li>C Renesas Simulator Debugging (RX only)</li> </ul>	Project: test C/C++ Application:	2. Click Search Project
E Refession and bebugging (in only)	Build (if required) before launching	Variables Search Project Browse
3. Select load module file.	Build configuration: Select Automatically gram Selection se a program to run: est.abs est.x	© Disable auto build <u>Configure Workspace Settings</u>
Filter matched 7 of 12 items		Apply Revert Debug Close
Quali makeno-print-directory post-bui	fier: r178le - /test/DefaultBuild/test.abs	
15 segments required LMA fixes Converting the DWARF information. Constructing the output ELF image. Saving the ELF output file test.x	OK Cancel	

#### Figure 2.12 Debug Configurations (2/5)

(12) Go to the [Debugger] tab, select E1/E20 (RL78) as the debug hardware, and specify the target device.

Name: test DefaultBuild			
📄 Main 🕸 Debugger 🕟 Startup	🔲 Common 🦫 Source		
Debug hardware: E1/E20 (RL78) 🔻	Target Device: R5F100LE		<u>^</u>
GDB Settings Connection Settings	Debug Tool Settings		
GDB Connection Settings	Host name or IP address: GDB port number: ADM port number:	localhost 61234 61236	E
GDB Command:			
\${eclipse_home}/DebugComp/rl78	-elf-gdb	Browse	Variables
Enable verbose mode			~
		Apply	Revert

Figure 2.13 Debug Configurations (3/5)

Go to the [Connection Settings] tab and set the supply voltage to match that of CS+ setting. (13)

		1
■ × □ ⇒ ▼	Name: test DefaultBuild 1.	Go to Connection
e filter text	📄 Main 🏇 Debugger 🕞 Startup 🙀 S	Settings.
© GDB Hardware Debugging ⓒ GDB Simulator Debugging (SH, RL78, RH850) 診 Renesas GDB Hardware Attach ⓒ Renesas GDB Hardware Debugging	Debug hardware: E1/E20 (RL78)  Tar GDB Settings Connection Settings Debug To	vice: RSF100LE
💽 * New_configuration [local]	GDB Settings Connection Settings Debug To	ooi settings
c× test DefaultBuild	Main Clock Frequency[MHz]	Using Internal Clock
🛯 Renesas Simulator Debugging (RX only)	Sub Clock Frequency[kHz]	Using Internal Concernance 2. Set supply voltage to
	Monitor Clock	Surtan
	Connection with Target Board	match CS+ voltage
	Emulator	(Auto)
	Power Target From The Emulator (MAX	
	Supply Voltage	5.0V -
	▲ Flash	3.3V
	Current Security ID (HEX)	5.0V
	Permit Flash Programming	Yes
	Use Wide Voltage Mode	Yes
	Erase Flash ROM When Starting	Yes 👻
matched 7 of 12 items		Apply Revert

Figure 2.14 Debug Configurations (4/5)

(14) Go to the **[Common]** tab, change the "Save as" radio button to "Shared File." Click **[Browse (B)...]** to select the launch configuration location. This will save the debug configuration in a file (.launch).

ame: test DefaultBuild	1. Go to Common tab.	
🗎 Main ( 🏇 Debugger 🌘 Start	up Common & Source	
Save as © Local file	2. Click Share	ed button.
Shared file: \test		Browse
Display in favorites menu	Folder Selection  Select a location for the launch config  3. Select location for launch configuration.	
Standard Input and Output Allocate console (necessary f	<ul> <li>☆ ↔</li> <li>☆ r01an2827_fld</li> <li>▶ ॐ test [DefaultBuild]</li> </ul>	
Append		/ariables
Append		/ariables Revert

Figure 2.15 Debug Configurations (5/5)

(15) Connection to the debugger can be enabled by clicking **[Debug]**.

Treate, manage, and run configurations		TO T	
📑 🗎 🔚 🚔 🕶	Name: test DefaultBuild	mmon E Source	
<ul> <li>GDB Hardware Debugging</li> <li>GDB Simulator Debugging (SH, RL78, RH850)</li> <li>➢ Renesas GDB Hardware Attach</li> <li>☑ Renesas GDB Hardware Debugging</li> <li>☑ * New_configuration [local]</li> <li>☑ * test DefaultBuild [local]</li> <li>☑ Renesas Simulator Debugging (RX only)</li> </ul>	Save as Cocal file Shared file: \test Browse		
	Display in favorites menu	Encoding	
	☐ 禄 Debug	Other     ISO-8859-1	
	Standard Input and Output          Image: Construction of the standard		
	Append	Workspace File System Variables	
ilter matched 7 of 12 items		Apply Revert	
?	,	Debug	

Figure 2.16 Debug Configurations Main Menu



#### 3. Debug Configuration File Modification

 Local directory files are stored in two places in the debug configuration file (.launch) stored in the project. Modify the locations to "DefaultBuild¥○○.x" and save.



Figure 3.1 Debug Configuration File



## 4. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

#### 5. Reference Documents

RL78 Family User's Manual: Software (R01US0015E) RL78 Compiler CC-RL User's Manual (R20UT3123E) (The latest information can be downloaded from the Renesas Electronics website.)

### Website and Support

Renesas Electronics website <u>http://www.renesas.com/</u>

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1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

— The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
 In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
 In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

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Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access
  these addresses; the correct operation of LSI is not guaranteed if they are accessed.
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After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

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