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April 1st, 2010
Renesas Electronics Corporation

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Customer Notification

IE-703037-MC-EM1

In-circuit Emulator Option
Operating Precautions

Traget Device
V850/SB1

Global Document No. U18077EE6V0IF00 (6th edition)
Document No. IE_703037_TPS-HE-B-2725
Date Published May 2002 N

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(A) Table of Operatiing Precautions

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		A	B	C	D	E
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1	Restrictions related to CLKOUT	💣	💣	💣	💣	💣
2	Restriction when INTWDT interrupt is generated	✋	✋	✓	✓	✓
3	Restriction IIC-bus function	✋	✋	✓	✓	✓
4	When P33 is used as S04, P31 does not operate correctly as an output port.	✋	✋	✓	✓	✓
5	If the compare register is written to at the moment when the compare register matches TM2-7, a matching signal is not generated	✋	✋	✓	✓	✓
6	If the timing of releasing the STOP mode conflicts with the timing of entering the STOP mode, the ICE becomes deadlocked	✋	✋	✓	✓	✓
7	When P113 is set as am output port, interrupt processing is not performed	✋	✋	✓	✓	✓
8	SB2 cannot be emulated	✋	✓	✓	✓	✓
9	INTC (interrupt controller)	✋	✋	✓	✓	✓
10	Restriction on SFR illegal access break.	✓	💣	💣	💣	💣
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15	Baud rate setting for variable-length serial interface CSI4	💣	💣	💣	💣	💣
16	Double interrupt execution	💣	💣	💣	💣	💣

17	16-bit timer (one-shot pulse mode)	💣	💣	💣	💣	💣
18	EI instruction	💣	💣	💣	💣	💣
19	Power save function	💣	💣	💣	💣	💣
20	Products emulation restriction	💣	💣	💣	💣	✓

✓: No problem

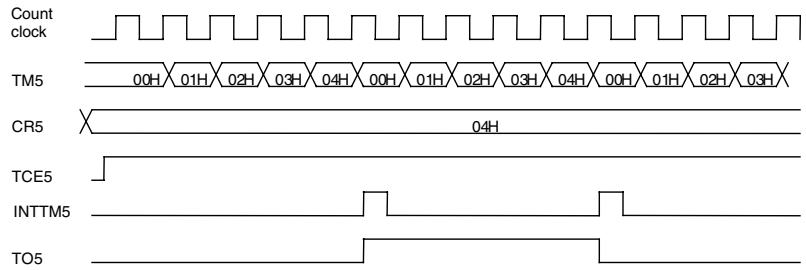
✋: Will be corrected by version upgrade

💣: Restriction, not corrected by version upgrade

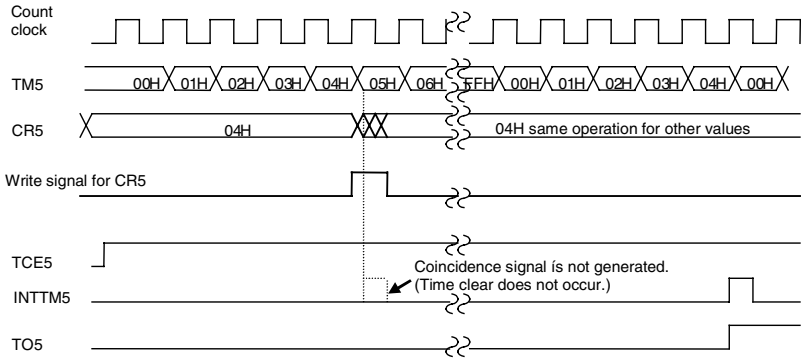
(B) Description of Precautions

No.	Outline	Description
1	Restrictions on CLKOUT	Details In case of reset, the CLOCKOUT is still available Workaround none
2	INTWDT interrupt generation	Details When the interrupt INTWDT (non maskable) has been generated, processing does not branch to the correct handler address (0x20h), but to the address 0x30h (an unused handler address in the device). Workaround Insert the same processing as the program at 0x20h at the address 0x30h.
3	IIC-bus functions	Details The IIC bus is not currently supported. Workaround none
4	Output on port pin P33	Details When P33 is used for SO4, P31 does not work correctly as output port. Workaround Use the port pin P31 only as inport pin, when port pin P33 is used for SO4.
5	TM 2-7 operational defect	Details: When used in interval timer mode If the compare register (CR20-70) is written when the timer register (TM2-7) and compare register (CR20-70) coincide, a coincidence signal is not generated. For this reason, the software must be designed to prevent timer coincidence and writing the compare register occurring at the same time. (Example: use a Vector interrupt) When used in square wave output mode If the compare register (CR20-70) is written when the timer register (TM2-7) and compare register (CR20-70) coincide, a coincidence signal is not generated and the output waveform does not invert. For this reason, the software must be designed to prevent timer coincidence and writing the compare register occurring at the same time. (Example: use a Vector interrupt)

Interval timer and square wave output
(Normal operation)

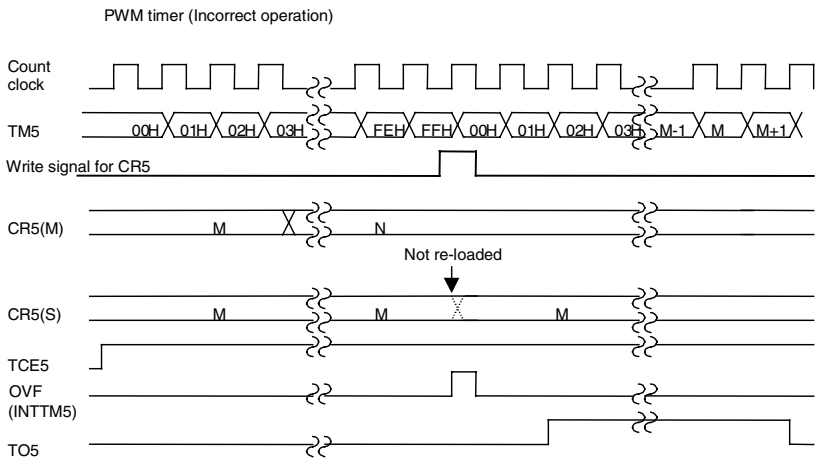


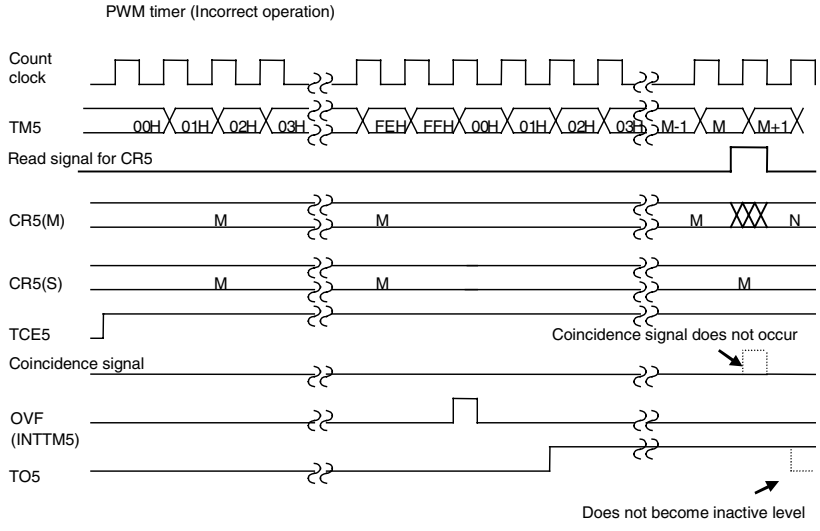
Interval timer and square wave outout
(Incorrect operation)



The timing chart above is intend to show the general operation and does not show precise timing

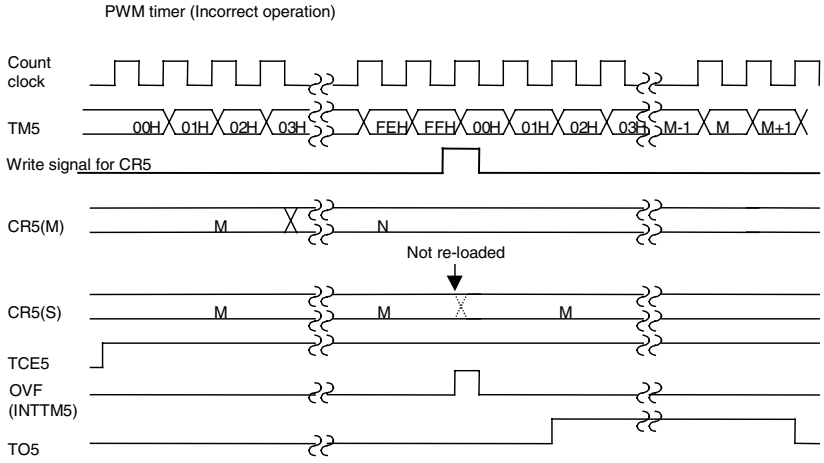
5	TM 2-7 operational defect	When used in PWM output mode - If the CR20-70 (master register) is re-written at the same time as the timer register overflows when the CR20-70 (master register) is written, the expected data sometimes cannot be transferred to the CR20-70 (slave register). (Data value is undefined) The software must be designed to prevent the overflow occurring at the same time as writing in the compare register.





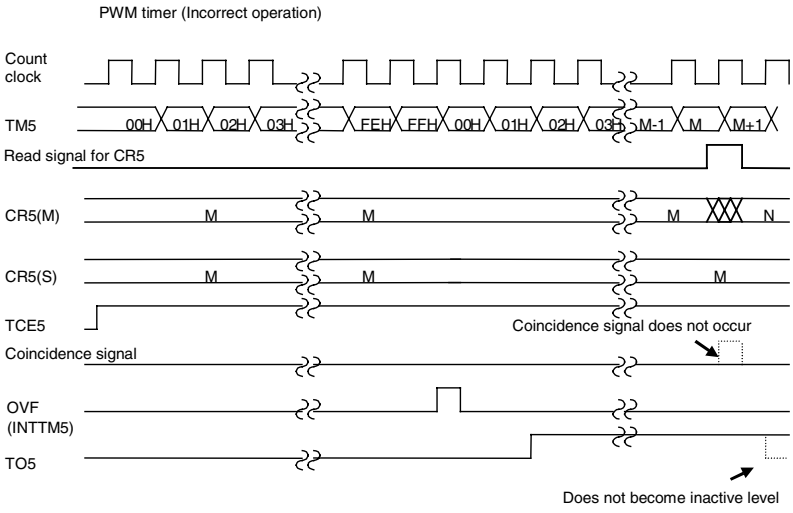
The Timing chart above is intendend to show the general operation, and does not show precise timing.

5	TM 2-7 operational defect	- If the CR20-70 register is read when an overflow occurs, the CR20-70 master register will not transfer data to the CR20-70 slave register. The data is transferred when the next overflow occurs.

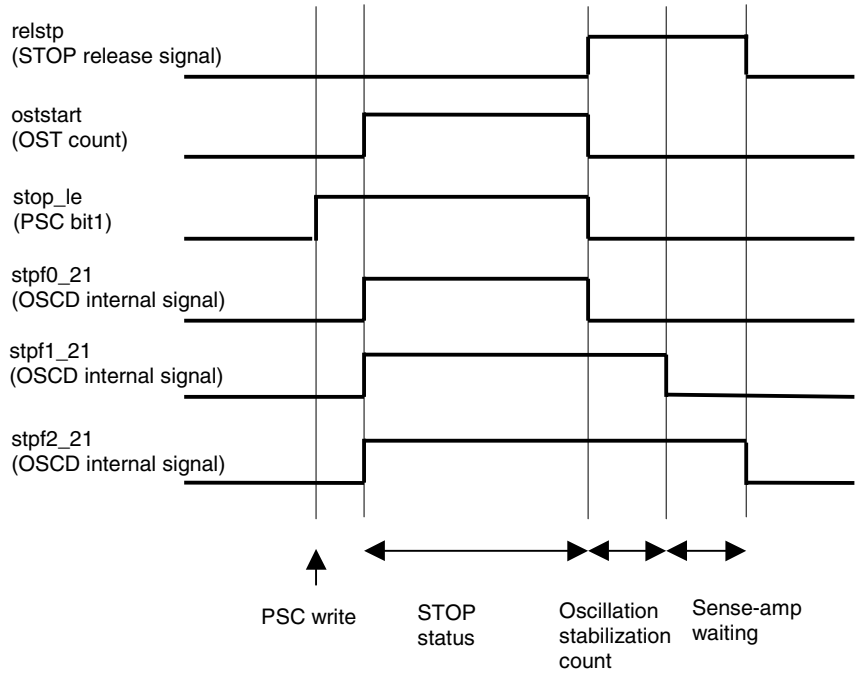


The Timing chart above is intendend to show the general operation, and does not show precise timing.

- If the compare register (CR20-70) is written when the timer register (TM2-7) and compare register (CR20-70 [slave register]) coincide, a coincidence signal is not generated and the inactive level is not attained.



The Timing chart above is intendend to show the general operation, and does not show precise timing.

6	STOP conflict	The CPU becomes deadlocked, if the timing of a STOP mode enable and a Stop mode release are in conflict Details With the V850/SB1, the STOP mode is enable by writing (stop_le:) to the PSC register (Power Save Control register). To release the Stop mode, the count initialization signal (oststart:) is generated to start the WDT (watchdog timer) that counts out the oscillation stabilization time (refer to diagram 1). However, if the stop mode release signal (relstp:) because of an interrupt, etc. conflicts with writing to the PSC register (the timing for this precaution occur within 2 clocks), then the oststart signal is not generated and WDT does not start counting. This means that the microcomputer remains waiting for the oscillation stabilization time to elapse, and even if the stop mode release signal is generated, STOP mode cannot be released (refer to diagram 2). Workaround As a temporary measure it is suggest that you use the IDLE mode or sub-IDLE mode instead of the STOP mode.  Diagramm1: STOP release operation timing (Normal)

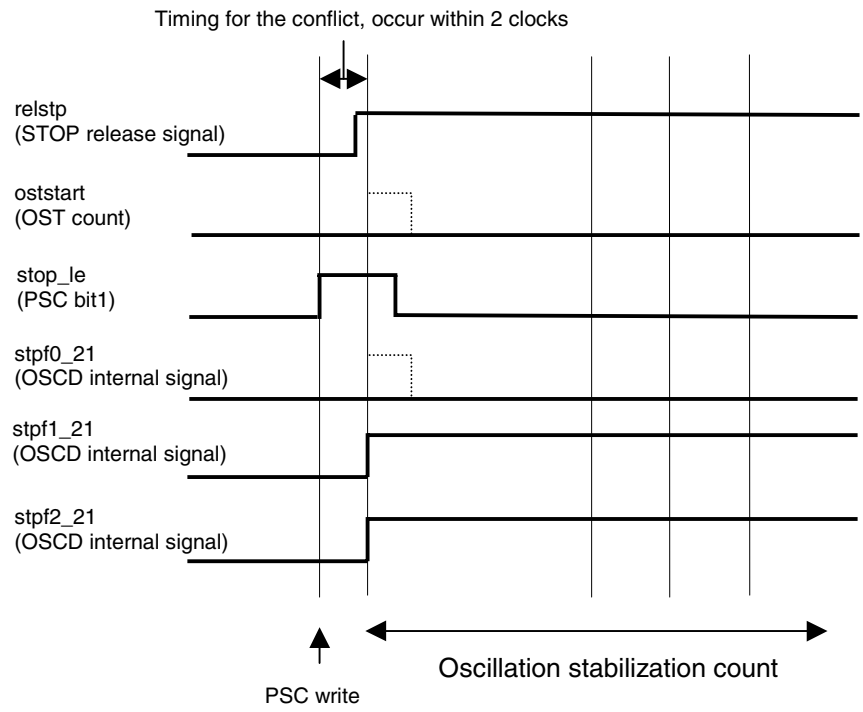
<table>
<tr>
<td>6</td>
<td>STOP conflict</td>
<td>


Diagramm 2: Timing of conflict between
STOP mode enable and release (Error)
</td>
</tr>
<tr>
<td>7</td>
<td>Interrupt of P113</td>
<td>Details
If P113 is specified as an output port, interrupt processing will not work.
Workaround
Use P113 as an input port.</td>
</tr>
<tr>
<td>8</td>
<td>SB2 cannot be emulated</td>
<td>Details
SB2 cannot be emulated
Workaround
none</td>
</tr>
</table>

9	INTC (interrupt controller)	Details This behaviour is the same as that on the original device. Bit operations setl, clrl, notl, tstl are Read-Modify-Write instructions (RMW). This means that this operation reads out the value of a register that is to change to an internal buffer, changes the value, and writes the value to the register. If a cycle in which the hardware of a register on which RMW operation is performed is set/reset [Note] and a DMA cycle conflict, set resetting the hardware of the register is cancled. Example: If the DMA cycle started by a DMA start request (such as INTCSIn) coincides with the DMA transfer count end interrupt (INTDMAn) in a bit manipulation instruction cycle to an interrupt control register (DMAICn) **Note:** Interrupt control register (xxIC), In-service priority register (ISPR) Workaround Registers that are set or reset by hardware are the Interrupt control registers (xxIC) and In-service Priority Register (ISPR). Do not use a bit operation instruction on these registers. Restriction: Do not use xxIC register and ISPR register as the DIOAn register (DMA peripheral address register). (When using DMA, do not access the xxIC and ISPR registers.)

<table>
<tr>
<td>10</td>
<td>Restriction on SFR illegal access break</td>
<td>
Details

Tehre are some addresses that are reserved areas but for wich an SFR illegal access break cannot be detected. The addresses are listed below:

<table>
<tr><th>Access Address</th><th>Emulation of SB1 (Except Y Product)</th><th>Emulation of SB1 (Y Product)</th><th>Emulation of SB2 (Except Y Product)</th><th>Emulation of SB2 (Y Product)</th></tr>
<tr><td>0xFFF138</td><td>x</td><td>o</td><td>x</td><td>o</td></tr>
<tr><td>0xFFF340</td><td>x</td><td>o</td><td>x</td><td>o</td></tr>
<tr><td>0xFFF342</td><td>x</td><td>o</td><td>x</td><td>o</td></tr>
<tr><td>0xFFF344</td><td>x</td><td>o</td><td>x</td><td>o</td></tr>
<tr><td>0xFFF346</td><td>x</td><td>o</td><td>x</td><td>o</td></tr>
<tr><td>0xFFF348</td><td>x</td><td>o</td><td>x</td><td>o</td></tr>
<tr><td>0xFFF34A</td><td>x</td><td>o</td><td>x</td><td>o</td></tr>
<tr><td>0xFFF34C</td><td>x</td><td>o</td><td>x</td><td>o</td></tr>
<tr><td>0xFFF350</td><td>x</td><td>o</td><td>x</td><td>o</td></tr>
<tr><td>0xFFF352</td><td>x</td><td>o</td><td>x</td><td>o</td></tr>
<tr><td>0xFFF354</td><td>x</td><td>o</td><td>x</td><td>o</td></tr>
<tr><td>0xFFF356</td><td>x</td><td>o</td><td>x</td><td>o</td></tr>
<tr><td>0xFFF358</td><td>x</td><td>o</td><td>x</td><td>o</td></tr>
<tr><td>0xFFF35A</td><td>x</td><td>o</td><td>x</td><td>o</td></tr>
<tr><td>0xFFF35C</td><td>x</td><td>o</td><td>x</td><td>o</td></tr>
<tr><td>0xFFF142</td><td>x</td><td>x</td><td>o</td><td>o</td></tr>
<tr><td>0xFFF144</td><td>x</td><td>x</td><td>o</td><td>o</td></tr>
<tr><td>0xFFF3E0</td><td>x</td><td>x</td><td>o</td><td>o</td></tr>
<tr><td>0xFFF3E2</td><td>x</td><td>x</td><td>o</td><td>o</td></tr>
<tr><td>0xFFF3E4</td><td>x</td><td>x</td><td>o</td><td>o</td></tr>
<tr><td>0xFFF3E6</td><td>x</td><td>x</td><td>o</td><td>o</td></tr>
<tr><td>0xFFF3E8</td><td>x</td><td>x</td><td>o</td><td>o</td></tr>
<tr><td>0xFFF3EA</td><td>x</td><td>x</td><td>o</td><td>o</td></tr>
<tr><td>0xFFF3EC</td><td>x</td><td>x</td><td>o</td><td>o</td></tr>
<tr><td>0xFFF3EE</td><td>x</td><td>x</td><td>o</td><td>o</td></tr>
<tr><td>0xFFF3F0</td><td>x</td><td>x</td><td>o</td><td>o</td></tr>
<tr><td>0xFFF3F2</td><td>x</td><td>x</td><td>o</td><td>o</td></tr>
<tr><td>0xFFF3F4</td><td>x</td><td>x</td><td>o</td><td>o</td></tr>
<tr><td>0xFFF3F6</td><td>x</td><td>x</td><td>o</td><td>o</td></tr>
<tr><td>0xFFF3F8</td><td>x</td><td>x</td><td>o</td><td>o</td></tr>
</table>
o: I/O register illegal break is detected
x: I/O register illegal break is not detected

Workaround

Be particularly careful with SFR accesses. This will become a permanent restriction.
</td>
</tr>
<tr>
<td>11</td>
<td>Restriction on initial values of PM6 and PM9</td>
<td>
Details

The read values of PM6 and PM9 at reset are different from the real chip:

<table>
<tr><th>SFR</th><th>Address</th><th>ICE Read Value</th><th>Real Chip Read Valu</th></tr>
<tr><td>PM6</td><td>0xFFF02C</td><td>FF</td><td>3F</td></tr>
<tr><td>PM9</td><td>0xFFF032</td><td>FF</td><td>7F</td></tr>
</table>
Workaround

None. This will become a permanent restriction
</td>
</tr>
</table>

12	Restriction on P11 when set as output port	Description If P11 is read when set as output port, the pin status is read instead of the port register value. Workaround There are no workaround. Please regard this as a permanent restriction.
13	Restriction on interrupts in Stop/Idle mode	Description The emulator is dead-locked under the following conditions. If the device is shifted to the STOP/IDLE mode while the interrupt request flag is set by an interrupt that is not masked. Workaround Be sure to clear the non-masked interrupt request flag before entering the STOP/IDLE mode. If the device is inadvertently shifted before clearing the flag, execute “Go”->”Halt”. The program is forcibly terminated. Then, execute “Go”->”Reset” to restart the emulator
14	Initial value of pull-up resistor option register P10 (PU10)	Description The on-chip pull-up resistors are connected to ports 100 to 107 direct after debugger start up or after a reset (including the time from immediately after emulator power-on to debugger start up). Even though the value of the pull up resistor option register P10 (PU10) is displayed as 00h (on-chip pull-up resistor is not connected) on the debugger at that time. Workaround Write 00h to pull-up resistor option register 10 (PU10) during initialisation immediately after a reset or in the I/O register window. This workaround has been implemented in products with control code D and later.
15	Baud rate setting for variable-length serial interface CSI4	Details On CSI4 data is not transmitted correctly if the baud rate of variable length CSI (CSI4) is set to a transmission speed faster than or equal to the operating clock of the CPU. Example: When operating at $f_{CPU} = f_{XX}/2$, the baud rate $f_{XX}/2$ cannot be selected When operating at fCPU = $f_{XX}/4$, the baud rates $f_{XX}/2$ and $f_{XX}/4$ cannot be selected When operating at $f_{CPU} = f_{XX}/8$, the baud rates $f_{XX}/2$, $f_{XX}/4$ and $f_{XX}/8$ cannot be selected When operating at $f_{CPU} = f_{XX}$ all baud rates can be selected. This restriction does not apply to CSI0 – CS13 or UART0 – UART1. Workaround: Do not use baud rates faster than or equal to the operating clock of the CPU for CSI4.

16	Double interrupt execution	Details An interrupt that should occur only once occurs twice if the following three conditions occur simultaneously while interrupts are enabled: 1) A bit manipulation instruction (set1, clr1, not1 or tst1) is executed on an interrupt request flag (xxIFn) of an interrupt control register (xxICn). 2) Interrupt processing involving the hardware of the same register occurs 3) There is a DMA startup while executing the above bit operation Remark: xx: Identification name of a peripheral unit (WDT, P, WTNI, TM, CSI, SER, ST, AD, DMA, WTN, KR, IIC) n: peripheral unit number If the abovementioned condition appears, the Interrupt Request Flag, which is normally reset to 0 at the acknowledge of interrupt processing, will not be reset. Consequently, after returning from interrupt processing (reti instruction), the interrupt processing is executed again. This does not happen if DMA is not used. Example: During a bit manipulation operation using the clr1 instruction on the interrupt request flag of the CSIC0 register (CSIF0), the non-masked INTCSI0 interrupt occurs at the same time as a DMA startup. As a result the INTCSI0 interrupt processing is executed twice. Workaround: 1) Insert a DI instruction before and an EI instruction after executing a bit manipulation instruction on an interrupt request flag (xxIFn) of an interrupt control register (xxICn) to avoid carrying out interrupt processing immediately after executing the bit manipulation instruction. 2) When interrupt processing begins, the hardware enters a state where interrupts are disabled. Clear the interrupt request flag in all interrupt processing routines before executing the EI instruction.

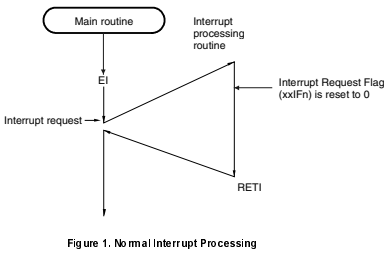


Figure 1. Normal Interrupt Processing

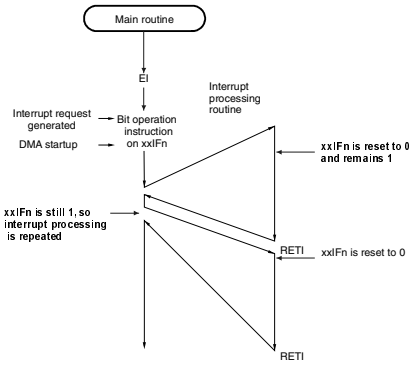


Figure 2. Interrupt Processing Affected by This Phenomen

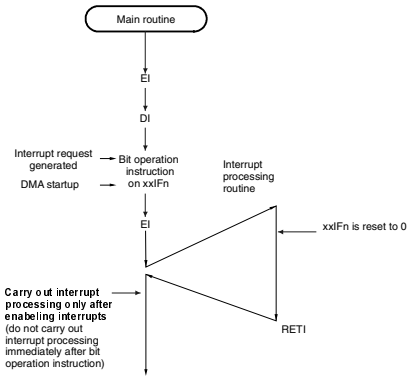


Figure 3. Countermeasure (1)

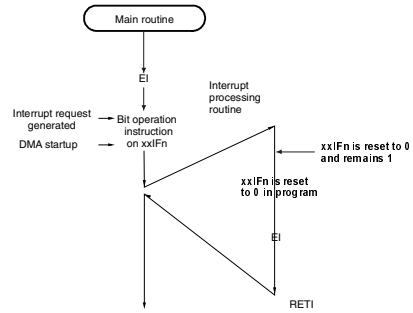


Figure 4. Countermeasure (2)

Remarks xx: Identification name of each peripheral unit (WDT, P, WTNI, TM, CS, SER, ST, AD, DMA, WTM, KR, IIC, IEB)
N: Peripheral unit number (0 to 7)

17	16-bit timer (one-shot pulse mode)	16-bit timer one-shot pulse output function Details When using the one-shot pulse function of timers 0,1 and 7 via a software trigger, the level of the T1pin or its alternate function port cannot be changed. Because the trigger is also enable in this case, the trigger will inadvertently clear & start even if the level of T1 pin or its alternate function port is changed, causing a pulse to be output at an unintended timing.

18	EI instruction	Interrupt servicing acknowledgement after EI instruction Details In this product at least 7 clocks are required as determination time between the generation of an interrupt and its acknowledgement. Because instructions continue to be executed in this period, if the DI instruction(interrupt disable) is executed, interrupts become disabled. This cause all interrupts to be held pending until the re-execution of the EI instruction (interrupt enable). Since this determination time is also when the EI instruction is executed, at least 7 clocks must be allowed before interrupts can be acknowledged after execution of the EI instruction. Consequently, if the DI instruction is executed before these 7 clocks have elapsed, interrupts will be held pending and not acknowledged. To ensure proper acknowledgement of interrupts therefore, insert an instruction (other than those below) of at least 7 execution clocks between the EI and DI instruction. - IDLE/STOP mode setting - EI, DI instruction - RETI instruction - LDSR instruction (for PSW) register - Access to interrupt control register (xxICn) Example: When EI instruction processing is invalid DI : ; MK flag = 0 (interrupt enable) : ; Interrupt request generation (IF flag = 1) EI JR, LP1 : 7 clcoks have not elapsed between EI an DI instructions : (3 clocks) LP1: DI : Workaround example: DI : ; MK flag = 0 (interrupt enable) : ; Interrupt request generation (IF flag = 1) EI NOP ; 1system clock NOP ; 1system clock NOP ; 1system clock NOP ; 1system clock JR, LP1 ; 3 system clocks (branch to LP1 routine) : : LP1: DI ; Interrupt servicing executed on 8th clock : after EI instruction

19	Power save function	Details
		
		If the affected products are used under the following conditions, a discrepancy may occur between the address indicated by the program counter (PC) and the address at which the instruction is actually read following the release of the power save mode.
		
		1. A power save mode (IDLE or STOP) is set while an instruction is being executed on the external ROM.
		
		2. The power save mode is released by an interrupt.
		
		3. The next instruction is executed while interrupts are in a pending state following the release of the power save mode.
		Note that interrupts are held pending under any of the following conditions:
		
		- The NP flag of the PSW register is 1. (NMI servicing in progress/set by software)
		
		- The ID flag of the PSW register is 1. (Interrupt servicing in progress/DI instruction/set by software)
		
		- The EI (interrupt enable) state had been set during interrupt servicing to enable multiple interrupt servicing, but was released by an interrupt with the same priority than the interrupt being serviced.
		
		The operation is shown below, using the power save mode setting example from the user's manual.
		
		(rD: PSC setting value, rX : Value written to PSW, rY: Value written back to PSW, assuming PSW has been set)
		
		ldsr rX, 5 ; Sets PSW to the value of rX
		st.b r0, PRCMD[r0] ; Writes to PRCMD
		st.b rD, PSC[r0] ; Sets the PSC register (PSC setting)
		ldsr rY,5 ; Returns the value of PSW (4 bytes)
		nop ; 2 to 5 NOP instructions (6 bytes) *
		nop ; (8 bytes) *
		nop ; (10 bytes)*
		nop ; (12 bytes)*
		nop ; (14 bytes)*
		(Next instructions) ; (16 bytes)
		
		* the event occurs here:
		<1> Discrepancy with PC
		<2> Instructions ignored
		
		Workaround
		
		1. Do not use a power save mode (IDLE or STOP) while instruction is being executed on the external ROM.
		
		2. If it necessary to use a power save mode (IDLE or STOP) while an instruction is being executed on the external ROM, take the software countermeasures shown below.
		
		- Insert 6 NOP instructions 4 bytes after an instruction that writes to the PSC register.

		Insert the br 2 instruction after the NOP instructions to eleminate the PC discrepancy.
		
		Example
		(rD: PSC setting value, rX: Value written to PSW, rY: Value written back to PSW, assuming PSW has been set)
		
		ldsr rX, 5 ; Sets PSW to the value of rX
		st.b r0, PRCMD[r0] ; Writes to PRCMD
		st.b rD, PSC[r0] ; Sets the PSC register
		ldsr rY, 5 ; Returns the value of value
		
		nop ; <1> 6 or more NOP instructions
		nop
		nop
		nop
		nop
		nop
		
		br 2 ; <2> Eliminates PC discrepancy

20	Products emulation restriction	Details The following product cannot be emulated. V850/SB1: μPD70F3032B(Y), μPD70F3033B(Y), μPD703032B(Y), μPD703030B(Y), μPD703033B(Y), μPD703031B(Y) V850/SB2: μPD70F3035B(Y), μPD703035B(Y), μPD703034B(Y), μPD70F3037H(Y), μPD703037H(Y), μPD703036H(Y)

(C) Revision History

Initial issue:

Date: Feb. 09, 1999

2nd issue:

Date: Jun. 10, 1999

Changes: Update

3rd issue:

Date: Sep. 21, 1999

Changes: Update

4th issue:

Date: May. 08, 2001

Changes:

added new version, control code D

added additional description to restriction no. 12 on P11

added additional description to restriction no. 13 on interrupt in STOP/IDLE mode

added additional description to restriction no. 14 Initial value of pull up register P10

added (C) Revision History

5th issue:

Date: Jan. 28, 2002

Changes:

added disclaimer

added table of contents

added additional description to restriction no. 15, on CSI4

added additional description to restriction no. 16, on double interrupt execution

added additional description to restriction no. 17, 16-bit timer (one–shot pulse mode)

added additional description to restriction no. 18, EI instruction

added additional description to restriction no. 19, power save function

6th issue:

Date: May. 24, 2002

Changes:

added new version, control code E

corrected no. 5

corrected no. 6

corrected no. 8

added no. 20