ISL6559EVAL2: Voltage Regulator Down Solution for AMD Hammer Family Processors

Application Note | August 2004 | AN1137

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Introduction

The AMD Hammer family microprocessors feature higher clock speeds and greater device density than previous product families. The power management solution for this next generation family of microprocessors must contend with lower core voltages, tighter transient specifications, and higher peak current demands. Responding to the changing power management needs of its customers, Intersil introduces the ISL6559 controller to power the AMD Hammer family of microprocessors.

Intersil ISL6559 and HIP6601B

The ISL6559EVAL2 is a versatile voltage regulator-down (VRD) design. The evaluation board comes configured for 3-phase buck operation, designed to meet AMD Hammer Family Desktop Processor specifications. The board layout supports removal of the third phase to support evaluation at lower current specifications. The ISL6559 controller features are specifically designed to compliment and support the Hammer Family processors. Interfaced with HIP6601B drivers, the chipset forms a highly integrated solution for AMD Hammer processor applications.

The ISL6559 regulates output voltage and balances load currents for two to four synchronous buck converter channels. The controller features a 5-bit DAC, which provides a digital interface for accurate step down conversion over the entire Hammer Family range of 1.550V to 0.800V. New multi-phase family features include differential remote output voltage sensing, to improve regulation tolerance; pin-adjustable reference offset, for ease of implementation; VID-on-the-Fly, to respond to DAC changes during operation; and optional load line regulation. For a more detailed description of the ISL6559 functionality, refer to the data sheet [1].

The HIP6601B driver is chosen to drive two N-Channel power MOSFETs in a synchronous-rectified buck converter channel. Each channel has a single logic input that controls the upper and lower MOSFETs. Dead time is optimized on both switching edges to provide shoot-thru protection. Internal bootstrap circuitry only requires an external capacitor and provides better enhancement of the upper MOSFET. For a more detailed description of the HIP6601B, refer to the data sheet [2]. In applications where space is a premium, the HIP6602B driver is recommended. The HIP6602B drives two converter channels and requires less implementation area. For more information refer to the HIP6602B data sheet [3].

The Intersil multi-phase family driver portfolio continues to expand with new selections to better fit our customer's needs. Refer to our website for updated information: **http://www.intersil.com/power/**

ISL6559 VRD Reference Design

The evaluation kit consists of the ISL6559EVAL2 board, associated data sheets on the ISL6559 controller and HIP6601B driver, as well as this application note. The evaluation board provides convenient test points, two types of power supply connectors, and an on-board transient load generator to facilitate the evaluation process. The board is configured for down conversion from 12V to the DAC setting.

TABLE 1. 3-PHASE VRD DESIGN PARAMETERS

PARAMETER	MAX	MIN
Static Regulation	1.350V	1.250V
Transient Regulation	1.350V	1.250V
Continuous Load Current	52A	
Load Current Step	21A	19A
Load Current Transient	30A/μs	

The evaluation board meets the output voltage and current specifications, shown in Table 1, with the VID DIP switch (SW3) set to 01010 (1.300V). Two jumpers near the controller are preset and should be checked before powering up the board. The JP1 jumper should be in the +12V position (center and right leg with the ATX connector to your right), and JP2 should be in the ON position (left and center legs). Additional information on the function of these jumpers is given in the following section.

The printed circuit board is implemented in 4-layer, 2-ounce copper. Layout plots and part lists, for this design, are provided at the end of the application note.

Quick Start Evaluation

Circuit Setup

The ISL6559EVAL2 board will arrive with the VID DIP switch (SW3) set to 01010 (1.300V). If another output voltage level is desired, refer to the ISL6559 data sheet for the complete DAC table and change the VID switches accordingly. Note: changing the SW3 VID states will change the dynamics of the load generator.

JP1 selects the VCC voltage to the ISL6559 controller. This jumper is preset to +12V to create a 12V only converter solution, as presented. Move the JP1 jumper to the right most pins to select operation directly from +5V. JP2 sets the

number of active phases in the converter and is preset for 3-phase operation. JP2 is set with PHASE 3 in the ON position. Before connecting the power supplies to the board, place switches SW1 and SW2 in the OFF position.

Input Power Connections

Two ATX supply connections are provided on the ISL6559EVAL2 board. The main ATX power connector mates with the 20-pin header, J1, labeled ATX. The 12V AUX power connector mates with a 4-pin header, J2, labeled ATX12V. Insure both connections are secure and SW1 and SW2 are in the OFF position before switching on the ATX supply.

Three female-banana jacks are provided for connection of bench-top supplies. Connect the +12V terminal to J3, +5V terminal to J4, and the common ground to terminal J5. Turn on the +5V supply first to energize the ENABLE and power good circuitry, then turn on the +12V supply.

Once power is applied to the board, the PGOOD LED indicator will begin to illuminate red. With SW1 in the OFF position, the ENABLE input of the ISL6559 is held low and the startup sequence is inhibited.

Power Output Connections

The ISL6559EVAL2 output can be exercised using either resistive or electronic loads. Copper alloy terminal lugs provide connection points for loading. Tie the positive load connection to VCORE, terminal J6, and the negative to ground, terminal J7. A shielded scope probe test point, TP8, allows for inspection of the output voltage, VCORE.

Enabling the Controller

The state of VCC, EN, and FS/DIS dictate the beginning of a soft-start interval. The FS/DIS pin is only used to set the per phase switching frequency on the evaluation board. VCC is tied to jumper JP1 which will arrive preset to +12V. Once the input and output terminal connections are made, switch the ENABLE switch (SW1) to the ON position. The EN signal is released to rise above the ENABLE threshold of 1.23V nominal. Once the ENABLE threshold is exceeded, a soft-start interval is initiated. The output voltage will ramp in a controlled manner with PGOOD changing from red to green when the output voltage passes through the under-voltage threshold.

If JP1 is placed in the +5V position, the internal regulator of the controller is disabled. The controller and drivers now are enabled from two different sources. To prevent the controller from enabling before the HIP660X drivers are active, the threshold sensitive EN pin is used for power sequencing between the controller and drivers. A resistor divider from the +12V input is connected to EN. The resistors are selected such that the ISL6559 enable threshold is reached after the VCC rising threshold has been exceeded on all the HIP6601 drivers.

On-Board Load Transient Generator

Most bench-top electronic loads are not capable of producing the current slew rates required to emulate modern microprocessors. For this reason, a discrete transient load generator is provided on the evaluation board, see Figure 1. The generator produces a load pulse of 112μs in duration with a period of 14.5ms. The pulse magnitude is approximately 20A, with rise and fall slew rates of approximately 30A/μs as configured. The short load current pulse and long duty cycle is required to limit the power dissipation in the load resistors (R34-R38) and MOSFETs (Q7, Q8). To engage the load generator, place switch SW2 in the ON position.

If the DAC code is changed from 01010 (1.300V), the transient generator dynamics must be adjusted to the new output voltage level. Place a scope probe in TP9 to measure the voltage across the load resistors and the dv/dt across them as well. Adjust the load resistors, R34-R38, to achieve the correct load current level. Change resistors R30-R33 to increase or decrease the dv/dt, as required, to match the desired di/dt profile.

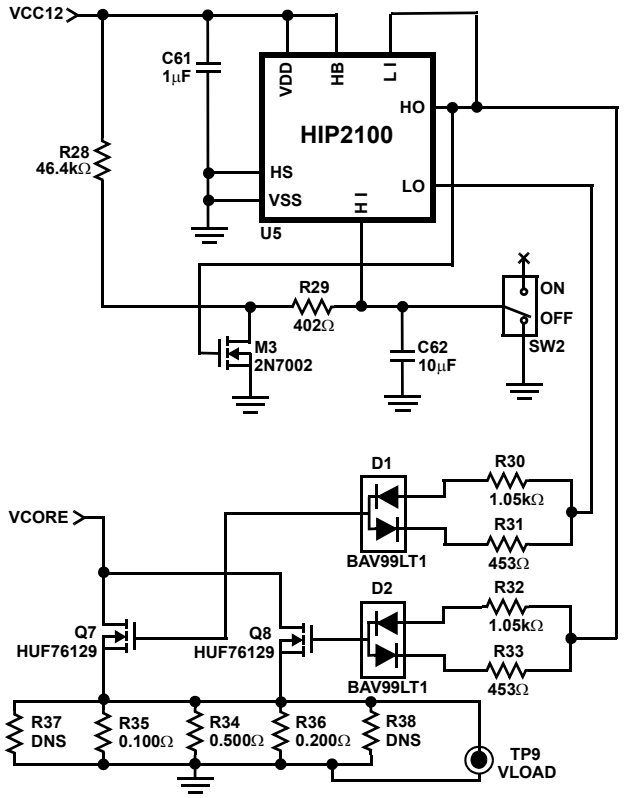


FIGURE 1. LOAD TRANSIENT GENERATOR

ISL6559 VRD Performance

Soft-Start Interval

The typical start-up waveforms for the ISL6559EVAL2 are shown in Figure 2. The DAC is set to 01010 (1.300V) and the converter is started into a 52A load. The ENABLE switch, SW1, is thrown to the ON position and the voltage on EN

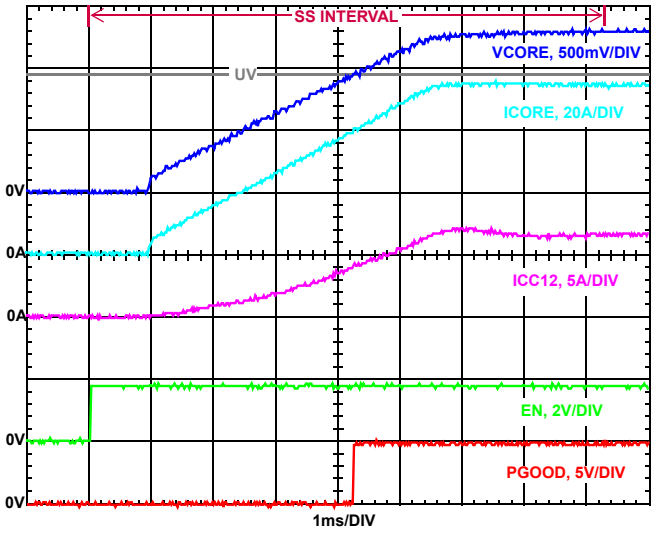


FIGURE 2. SOFT-START INTERVAL WAVEFORMS

quickly rises above the ISL6559 enable threshold, triggering a soft-start interval. The switching frequency of the converter is 250kHz, therefore the soft-start interval (SS Interval) is approximately 8.3ms. VCORE does not move initially due to the manner in which soft-start is implemented within the controller. After a short delay, VCORE begins to ramp linearly towards the DAC set point. Of note, the input current, ICC12, also ramps slowly due to the controlled rise of the output voltage.

About 4.3ms into the soft-start interval, VCORE passes through the under-voltage threshold, UV. The under-voltage threshold is defined as the DAC setting minus 350mV. Once this threshold is surpassed, the internal pull down on the PGOOD pin is released and the PGOOD LED indicator changes to green.

Transient Response

The AMD Hammer desktop specification requires the VRD to support loading at the processor pins from 0 to 52 amps with a maximum load step of 20A. The transient slew rate is defined as 30A/µs for this design. During a transient, the core voltage is required to remain within the static window of ±50mV around the DAC setting. The on-board load generator and a bench-top electronic load simulate these conditions.

The OFS pin allows the user to positively offset the DAC reference voltage by placing a correctly sized resistor, R7, from this pin to ground. For this design, the resistor value is 3.24kΩ, which equates to a positive offset of approximately 20mV at no-load. Load-line regulation is supported by the ISL6559. The average current of the three active channels flows out of pin IDROOP. When this pin is connected to the FB pin, this average current creates a voltage drop across R4 (R_{FB} in the data sheet). This voltage drop is proportional to the output current of the converter, and effectively creates an output voltage droop with a steady-state value of approximately 40mV, for this design.

The leading edge transient response of the ISL6559EVAL2 to the aforementioned maximum load conditions is shown in Figure 3. A bench-top electronic load draws 32A continuously from the converter, while the on-board load generator provides a 20A load step. The core voltage immediately drops to a minimum of 1.265V in response to the 20A step. The effective ESR of the aluminum electrolytic output capacitors contributes to over 80% of the drop as the output capacitors begin to support the core voltage. The controller detects the new load level by the drop in output voltage and responds by pushing the PWM signals wider. Note the difference in pulse widths just before and as the transient slews up to 52A. The inductor currents rapidly increase to meet this new demand, supplying an increasing portion of the load. While the inductor currents are slewing, the bulk output capacitors are supplying the load. The inductors assume a majority of the load current in about 6µs, thereby reducing the bulk capacitance required to support the transient.

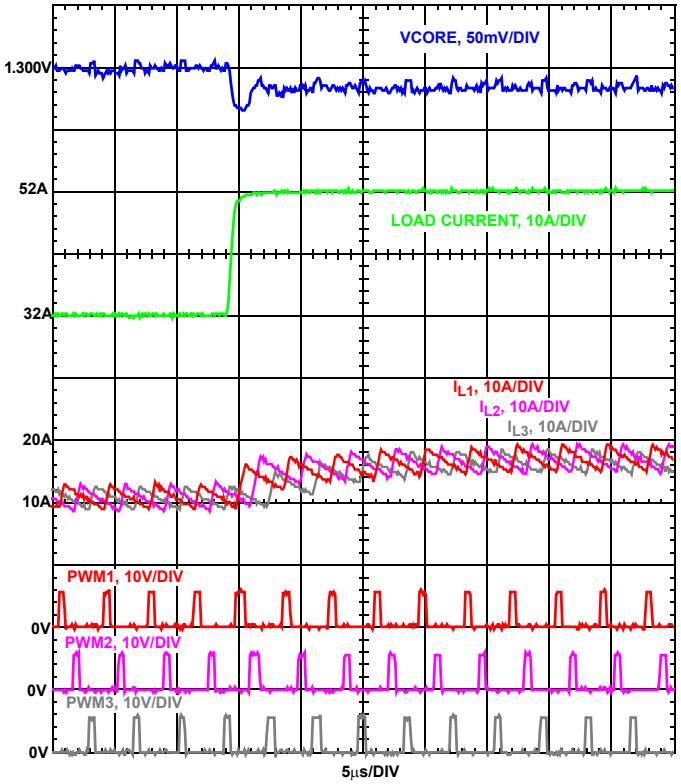


FIGURE 3. RISING EDGE TRANSIENT RESPONSE

The steady-state phase-to-phase current matching is also displayed in Figure 3. A major contributor to good phase-to-phase current matching is layout. Each channel has a nearly identical component layout with tight placement of the critical components.

The electronic load is removed and the on-board load generator alone applies a 20A step. Figure 4 shows the core voltage, load current, channel inductor currents, and PWM signals changing in response to the trailing edge of the

transient load current. As the load is removed, the output voltage rises in response. The controller detects the load change and immediately decreases the channel duty cycles. The duty cycle of PWM1 is reduced to zero for one cycle as those of the other two channels are notably reduced. During this time, the inductors quickly shed load current, and once again reduce the amount of capacitance required to supply the load. The core voltage returns to the no-load offset level of 1.320V.

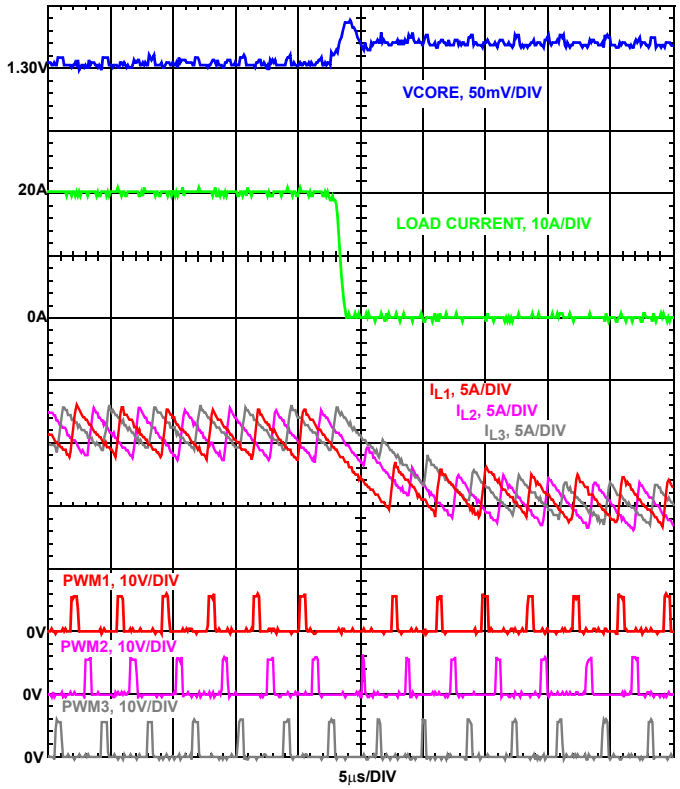


FIGURE 4. FALLING EDGE TRANSIENT RESPONSE

Over-Current Protection

The ISL6559 monitors the output current level by averaging the sampled current from each ISEN pin. The R_{ISEN} resistors (R1, R2, R3) are selected so that the current sourced by the ISEN pins, at maximum load current, is 50µA. The average of the sampled currents is compared with an over-current trip level of 90µA. Once the average current meets or exceeds the OC reference current, the controller immediately places all PWM signals in a high-impedance state, quickly removing gate drive to the HIP6601B drivers, and forcing the core voltage to decay as the output capacitors discharge. The PGOOD signal transitions low when the core voltage drops below the UV threshold.

After the over-current event is detected, the controller waits a short delay time before initiating a soft-start interval to allow the disturbance to clear. The delay time is equivalent to the soft-start interval and is 8.3ms, for this design. If during the soft-start interval another over-current trip is detected, the PWM signals are again placed in a high impedance state and PGOOD remains low. The controller waits another 8.3ms before another soft-start interval is attempted. This hiccup mode of operation repeats up to seven times, with the eighth prompting the converter to latch off.

Figure 5 shows the hiccup mode operation of the converter when a hard short is applied across the output terminals of the evaluation board. The converter quickly places the PWM signals in a high-impedance state and the core voltage decays quickly. The short is not removed, resulting in the controller latching off after the seventh attempt.

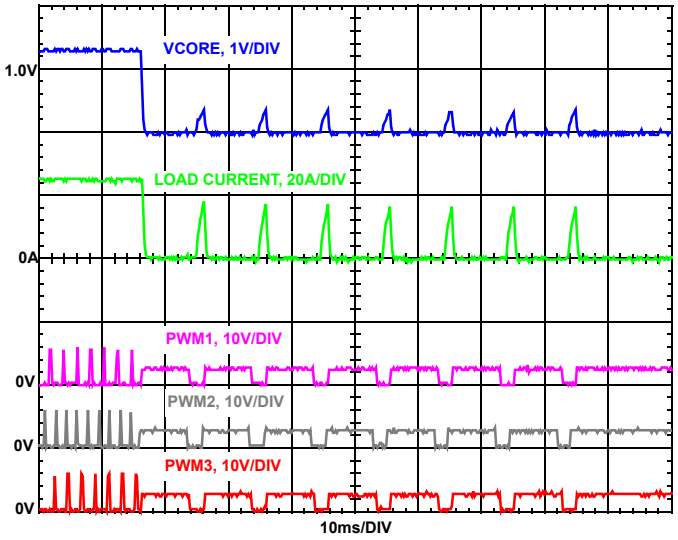


FIGURE 5. OVER-CURRENT PROTECTION

VID on the Fly

The AMD Hammer Family microprocessors can change VID inputs at any time while the regulator is in operation. The power management solution is required to monitor the DAC inputs, and respond to VID voltage transitions in a controlled manner, supervising the safe output voltage transition within the DAC range of the processor without discontinuity or disruption. The ISL6559 checks the five VID inputs at the beginning of each switching cycle. If the VID code has changed, the controller waits one complete switching cycle to validate the new code. If the new code is stable during this one cycle delay, then the controller begins incrementing the reference voltage toward the new DAC code in 25mV steps, every two switching-cycles, until the new DAC code is reached.

Figure 6 shows a 250mV DAC change prompted by changing VID3 and VID1 simultaneously. Originally, at 1.550V (00000), the core voltage ramps down to the new DAC setting of 1.300V (01010). The VID-on-the-Fly transition is completed in 80µs, well within the 100µs maximum window allowed. The converter is supporting a 26A load during the transition. The PGOOD signal is steady throughout the DAC change and indicates no operational problems are encountered.

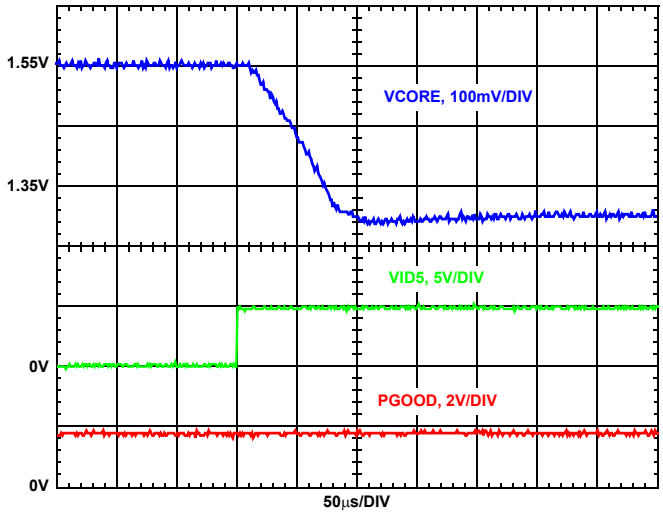


FIGURE 6. VID-ON-THE-FLY TRANSITION FROM 1.55V TO 1.30V

Figure 7 shows the converter returning to a DAC level of 1.550V after the VID3 and VID1 states are returned to ground. Again, the converter is loaded at 26A during the DAC change.

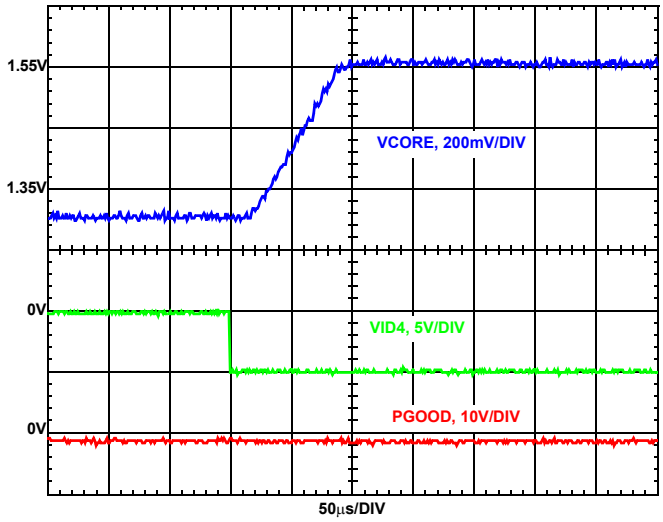


FIGURE 7. VID-ON-THE-FLY TRANSITION FROM 1.30V TO 1.55V

Efficiency

The efficiency of the ISL6559EVAL2 board, loaded from 5 to 55A, is plotted in Figure 8. Measurements were performed at room temperature and taken at thermal equilibrium with **NO AIR FLOW**. The design exceeds the AMD Hammer Desktop minimum requirements of 50% efficiency under minimum loading and 80% efficiency at maximum loading even without forced airflow. The maximum allowed airflow per the desktop specification is 100LFM and will only enhance the converter performance if available.

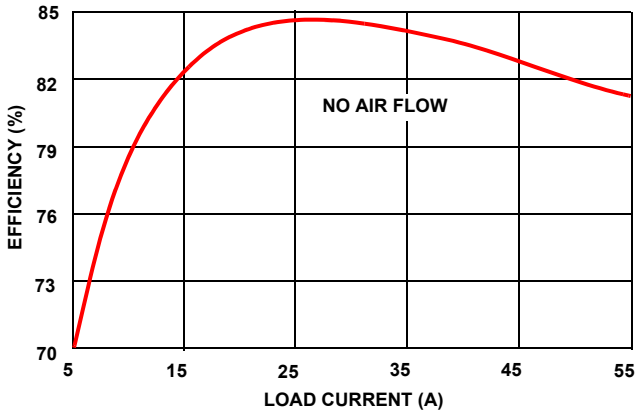


FIGURE 8. EFFICIENCY vs LOAD CURRENT

Thermal Performance

Figure 9 shows the laboratory measured upper and lower MOSFET temperatures versus load current. The measurements were performed at room temperature and taken at thermal equilibrium with **NO AIR FLOW**.

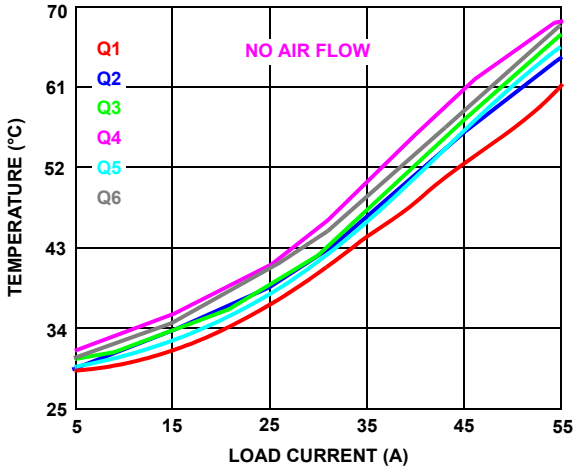


FIGURE 9. MOSFET TEMPERATURE vs LOAD CURRENT

Figure 10 shows the individual channel output inductor and HIP6601B driver temperatures over the same conditions as the MOSFETs.

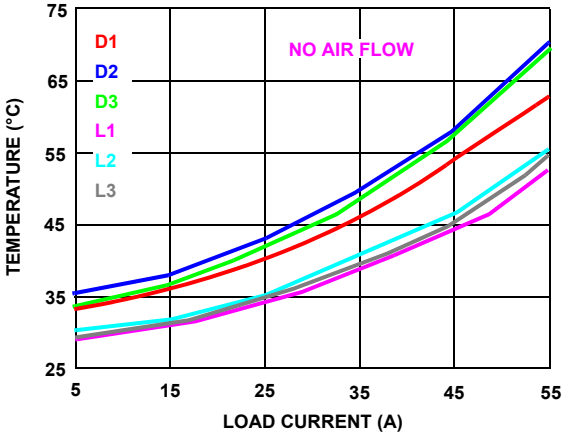


FIGURE 10. INDUCTOR/DRIVER TEMPERATURE vs LOAD CURRENT

Adapting Circuit Performance

This design represents one solution for meeting the present requirements on voltage regulators powering AMD Hammer Family processors. This low cost approach can be augmented to meet changing performance and cost requirements. Over the life of the processor, some features could be enhanced, resulting in higher processor quiescent or transient current specifications. Given suitable motherboard space and component selection, this design can support 20A per phase or more if required. With the flexibility to support 2, 3, or 4 phases, the ISL6559 controller covers an array of future designs.

If the cost curve of a design must be tilted lower, a different combination of upper and lower MOSFETs with higher $r_{DS(ON)}$ can be employed. The trade-off for lowering cost is reduced efficiency and thermal performance.

In cases where efficiency is paramount, a lower $r_{DS(ON)}$ synchronous MOSFET or pair of MOSFETs can achieve efficiencies over 90%.

If board area is a premium, the ISL6559 switching frequency can be raised to reduce solution size. MOSFET technology continues to drive die size down and new packaging options provide improved thermal performance in smaller packages. Implementing designs with 20A per channel or less typically occupy the least amount of board space.

Summary

The ISL6559EVAL2 is an adaptable evaluation tool which showcases the performance of the ISL6559 and HIP6601B chip set. Designed to meet the performance requirements of AMD's Hammer Family Desktop microprocessors, the board allows the user the flexibility to configure the board for contemporary, as well as future, microprocessor offerings. The following pages provide a schematic of the board, bill of materials and layout drawings to support implementation of this solution.

References

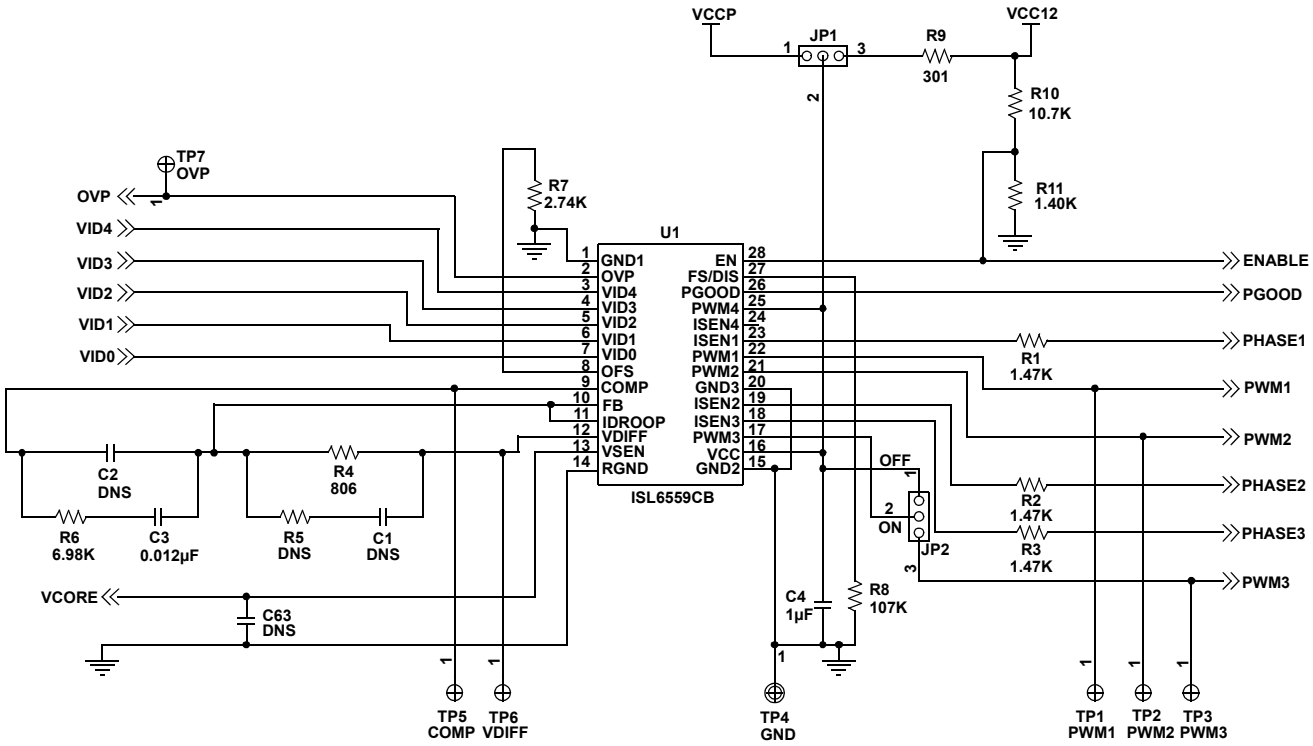
Intersil documents are available on the web at http://www.intersil.com/

[1] ISL6559 Data Sheet, Intersil Corporation, File No. FN9084

[2] ISL6601B Data Sheet, Intersil Corporation, File No. FN9072

[3] ISL6602B Data Sheet, Intersil Corporation, File No. FN9076

Schematic


VCCP
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R9
301
VCC12
R10
10.7K
R11
1.40K
TP7
OVP
OVP
R7
2.74K
VID4
VID3
VID2
VID1
VID0
U1
GND1
OVP
VID4
VID3
VID2
VID1
VID0
OFS
COMP
FB
IDROOP
VDIFF
VSEN
RGND
EN
FS/DIS
PGOOD
PWM4
ISEN4
ISEN1
PWM1
PWM2
GND3
ISEN2
ISEN3
PWM3
VCC
GND2
ISL6559CB
ENABLE
PGOOD
PHASE1
R1
1.47K
PWM1
PWM2
PHASE2
R2
1.47K
PHASE3
R3
1.47K
PWM3
OFF
ON
JP2
C2
DNS
R4
806
R6
6.98K
C3
0.012µF
R5
DNS
C1
DNS
VCORE
C63
DNS
C4
1µF
R8
107K
TP5
COMP
TP6
VDIFF
TP4
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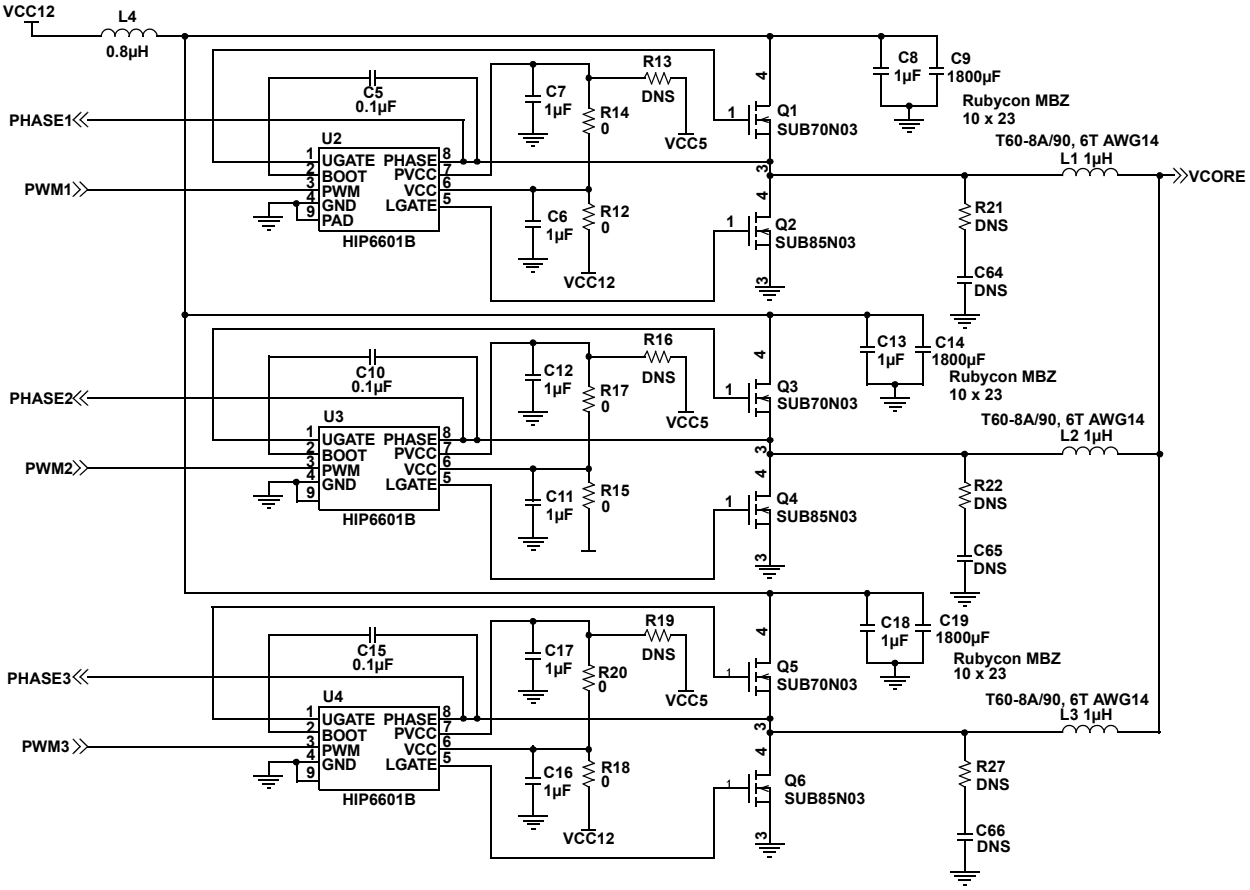
TP1
PWM1
TP2
PWM2
TP3
PWM3


VCC12
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PHASE1
PWM1
U2
UGATE
BOOT
PWM
GND
PAD
PHASE
PVCC
VCC
LGATE
HIP6601B
C5
0.1µF
C7
1µF
R14
0
R13
DNS
VCC5
C6
1µF
R12
0
VCC12
Q1
SUB70N03
Q2
SUB85N03
C8
1µF
C9
1800µF
Rubycon MBZ
10 x 23
T60-8A/90, 6T AWG14
L1 1µH
VCORE
R21
DNS
C64
DNS
PHASE2
PWM2
U3
C10
0.1µF
C12
1µF
R17
0
R16
DNS
VCC5
C11
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R15
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Q3
SUB70N03
Q4
SUB85N03
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1µF
C14
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Rubycon MBZ
10 x 23
T60-8A/90, 6T AWG14
L2 1µH
R22
DNS
C65
DNS
PHASE3
PWM3
U4
C15
0.1µF
C17
1µF
R20
0
R19
DNS
VCC5
C16
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R18
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Q6
SUB85N03
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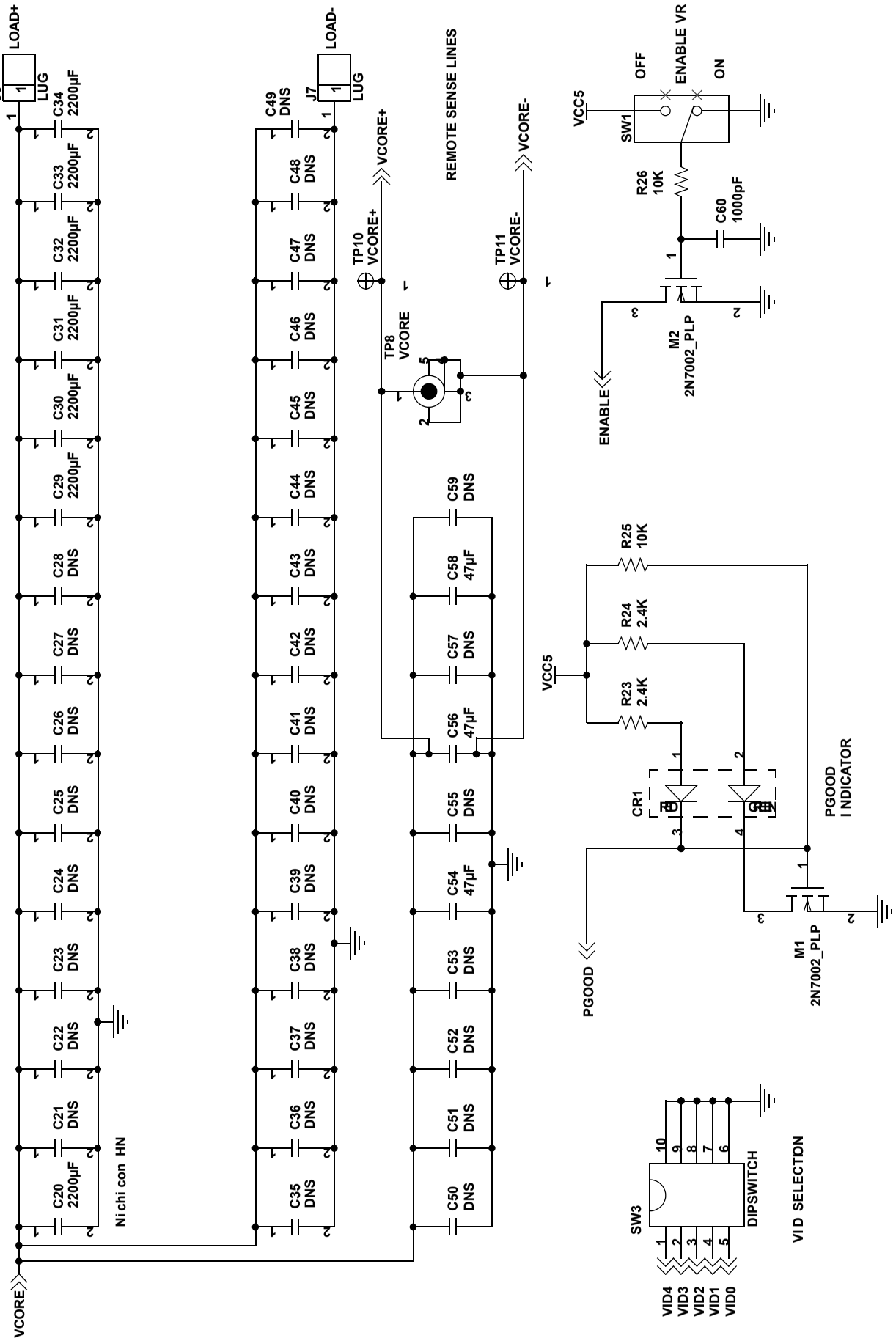
R27
DNS
C66
DNS


J6
LOAD+
LUG
J7
LOAD-
LUG
C20 2200µF
C21 DNS
C22 DNS
C23 DNS
C24 DNS
C25 DNS
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C28 DNS
C29 2200µF
C30 2200µF
C31 2200µF
C32 2200µF
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C41 DNS
C42 DNS
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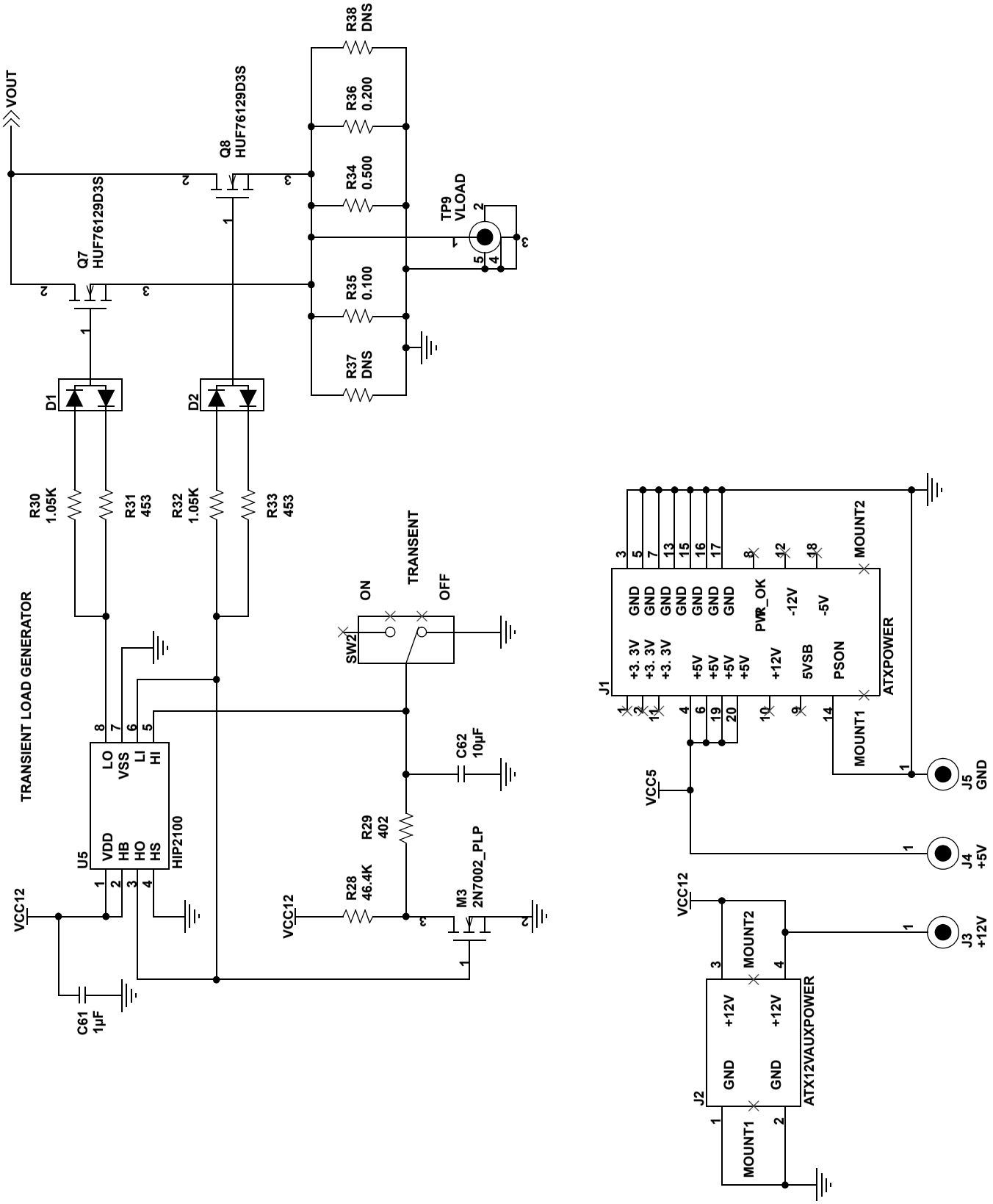
C44 DNS
C45 DNS
C46 DNS
C47 DNS
C48 DNS
C49 DNS
C50 DNS
C51 DNS
C52 DNS
C53 DNS
C54 47µF
C55 DNS
C56 47µF
C57 DNS
C58 47µF
C59 DNS
Nichicon HN
VCORE
VCORE+
VCORE-
REMOTE SENSE LINES
TP10 VCORE+
TP11 VCORE-
TP8 VCORE
VCC5
SW1
OFF
ENABLE VR
ON
R26 10K
C60 1000pF
M2 2N7002_PLP
ENABLE
R25 10K
R24 2.4K
R23 2.4K
CR1
PGOOD
INDICATOR
M1 2N7002_PLP
PGOOD
SW3
DIPSWITCH
VID SELECTION
VID4
VID3
VID2
VID1
VID0


VOUT
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Q7
HUF76129D3S
R38
DNS
R36
0.200
R34
0.500
R35
0.100
R37
DNS
TP9
VLOAD
D1
D2
R30
1.05K
R31
453
R32
1.05K
R33
453
TRANSIENT LOAD GENERATOR
U5
HIP2100
LO
VSS
LI
HI
VDD
HB
HO
HS
VCC12
C61
1µF
C62
10µF
R29
402
R28
46.4K
M3
2N7002_PLP
SW2
ON
OFF
TRANSIENT
J1
ATXPOWER
MOUNT1
MOUNT2
GND
+3. 3V
+5V
+12V
-12V
-5V
5VSB
PSON
PWR_OK
VCC5
J5
GND
J4
+5V
J3
+12V
J2
ATX12VAUXPOWER

Bill of Materials

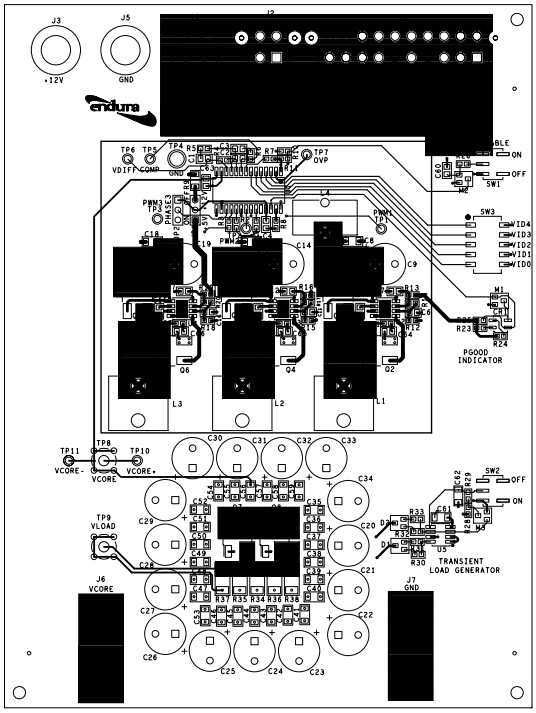
QTY	REFERENCE	VALUE	DESCRIPTION	VENDOR	PART NO.	PACKAGE
0	C1	DNS	Capacitor, Ceramic			0805
0	C2	DNS	Capacitor, Ceramic, 50V, X7R, 10%			0805
1	**C3**	**0.010µF**	**Capacitor, Ceramic, 50V, X7R, 10%**	**Garret**	**MCH215C103KK**	**0805**
7	**C4, C6**, C7, **C11**, C12, **C16**, C17	**1.0µF**	**Capacitor, Ceramic, 16V, X7R, 10%**	**Kemet**	**C0805C105K4RAC**	**0805**
3	**C5, C10, C15**	**0.1µF**	**Capacitor, Ceramic, 25V, X7R, 10%**	**Vishay**	**VJ0805Y104KXX**	**0805**
4	**C8, C13, C18,** C61	**1.0µF**	**Capacitor, Ceramic, 25V, X7R, 10%**	**Panasonic**	**ECJ-3YB1E105K**	**1206**
3	**C9, C14, C19**	**1800µF**	**Capacitor, AL Electrolytic, 16V**	**Rubycon**	**16MBZ1800M**	**Thru Hole**
7	**C20, C29-C34**	**2200µF**	**Capacitor, AL Electrolytic, 6.3V**	**Nichicon**	**UHN0J222MPP**	**Thru Hole**
0	C21-C28	DNS	Capacitor, AL Electrolytic			Thru Hole
3	**C54, C56, C58**	**47µF**	**Capacitor, Ceramic, 6.3V, X5R**	**Panasonic**	**ECJ4YB0J476M**	**1210**
0	C35-C53, C55, C57, C59	DNS	Capacitor, Ceramic, Place Holder			1206
1	C60	1000pF	Capacitor, Ceramic, 50V, NPO	Vishay	VJ0805A102KXA	0805
1	C62	10µF	Capacitor, Ceramic, 16V, Y5V	Various		1206
0	C63, C64, C65, C66	DNS	Capacitor, Ceramic, Place Holder			0805
1	CR1		Red/Green LED	Lumex	SLL-LXA30251GC	SMT
2	D1, D2		Dual Diode	Various	BAV99	SOT-23
1	J1		Mini-Fit, JrTM Header, 20 pin	Molex	39-29-9203	Thru Hole
1	J2		Mini-Fit, JrTM Header, 4 pin	Molex	39-29-9042	Thru Hole
2	J3, J4		Female Banana Connector, Red	Johnson Components	111-0702-001	Screw On
1	J5		Female Banana Connector, Black	Johnson Components	111-0703-001	Screw On
2	J6, J7		Terminal Connector	Burndy	KPA8CTP	Solder Mount
6	JP1, JP2		1X3 Header, PVCC Selection	Berg	68000-236	Thru Hole
3	**L1, L2, L3**	**1.0µH**	**Inductor, T68-8A/90 core, 6T AWG14**	**Vishay - CoEv**	**C9587-02**	**Thru Hole**
1	**L4**	**0.8µH**	**Inductor, T60-26 core, 6T AWG16**	**Vishay - CoEv**	**C9588-01**	**Thru Hole**
3	M1, M2, M3		General Purpose MOSFET	Various	2N7002	SOT23
3	**Q1, Q3, Q5**		**Power MOSFET**	**Vishay**	**SUB70N03-09BP**	**TO-263**
3	**Q2, Q4, Q6**		**Power MOSFET**	**Vishay**	**SUB85N03-04P**	**TO-263**
3	Q7, Q8		Power MOSFET	Fairchild	HUF76129D3S	TO-252AA
3	**R1, R2, R3**	**1.02kΩ**	**Resistor, 1%, 1/16W**	**Vishay-DALE**	**CRCW06031021F**	**0603**
1	**R4**	**806Ω**	**Resistor, 1%, 1/16W**	**Vishay-DALE**	**CRCW06038060F**	**0603**
0	R5	DNS	Resistor, Place Holder			0603
1	**R6**	**6.98kΩ**	**Resistor, 1%, 1/16W**	**Vishay-DALE**	**CRCW0606981F**	**0603**
1	**R7**	**3.24kΩ**	**Resistor, 1%, 1/16W**	**Vishay-DALE**	**CRCW06033241F**	**0603**
1	**R8**	**107kΩ**	**Resistor, 1%, 1/16W**	**Vishay-DALE**	**CRCW06031073F**	**0603**
1	**R9**	**301Ω**	**Resistor, 1%, 1/4W**	**Vishay-DALE**	**CRCW12063010F**	**1206**
1	**R10**	**10.7kΩ**	**Resistor, 1%, 1/16W**	**Vishay-DALE**	**CRCW06031072F**	**0603**
1	**R11**	**1.40kΩ**	**Resistor, 1%, 1/16W**	**Vishay-DALE**	**CRCW06031873F**	**0603**

Bill of Materials (Continued)

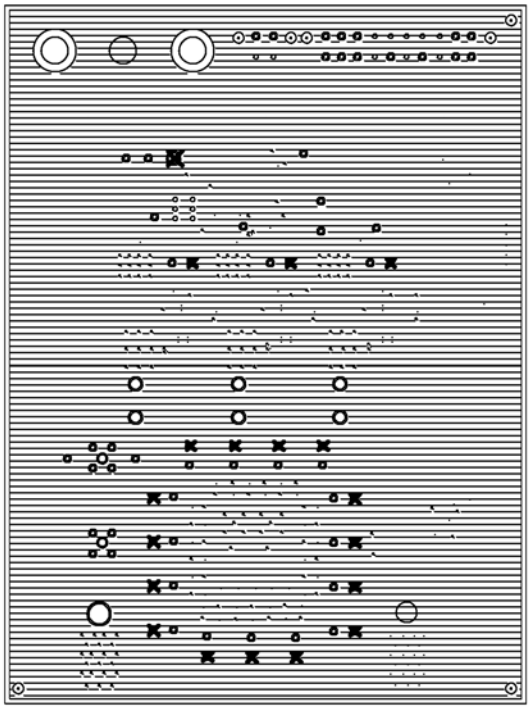
QTY	REFERENCE	VALUE	DESCRIPTION	VENDOR	PART NO.	PACKAGE
4	R12, R14, R15, R17, R18, R20	0Ω	Resistor, 1%, 1/16W	Vishay-DALE	CRCW0603000Z	0603
0	R13, R16, R19, R21, R22, R27	DNS	Resistor, Place Holder			0603
2	R23, R24	2.43kΩ	Resistor, 1%, 1/16W	Vishay-DALE	CRCW06032431F	0603
2	R25, R26	10kΩ	Resistor, 1%, 1/16W	Vishay-DALE	CRCW06031002F	0603
1	R28	46.4kΩ	Resistor, 1%, 1/16W	Vishay-DALE	CRCW06034642F	0603
1	R29	402Ω	Resistor, 1%, 1/16W	Vishay-DALE	CRCW06034020F	0603
2	R30, R32	1.05kΩ	Resistor, 1%, 1/16W	Vishay-DALE	CRCW06035110F	0603
2	R31, R33	453Ω	Resistor, 1%, 1/16W	Vishay-DALE	CRCW06032490F	0603
1	R34	0.1W	Thick Film Chip Resistor, 1W, 1%	Vishay-DALE	WSL2512-0.100-1%	2512
1	R35	0.2W	Thick Film Chip Resistor, 1W, 1%	Vishay-DALE	WSL2512-0.200-1%	2512
1	R36	0.5W	Thick Film Chip Resistor, 1W, 1%	Vishay-DALE	WSL2512-0.500-1%	2512
0	R37, R38	DNS	Thick Film Chip Resistor, Place Holder			2512
2	SW1, SW2		Switch, SPDT, Ultra Mini Toggle	C&K Components	GT11MSCKE	SMD
1	SW3		Low Profile DIP Switch, SPST, 5 position	C&K Components	SD05H0SK	SMT
8	TP1, TP2, TP3, TP5, TP6, TP7, TP10, TP11		Small Test Point	Jolo	SPCJ-123-01	Thru Hole
1	TP4		Turret Test Point	Keystone	1514-2	Thru Hole
2	TP8, TP9		Probe Socket	Tektronics	1314353-00	Thru Hole
1	**U1**		**Endura Multi-phase Controller**	**Intersil**	**ISL6559CB**	**SO-28**
3	**U2, U3, U4**		**Endura Multi-phase Driver**	**Intersil**	**HIP6601BECB**	**EP SO-8**
1	U5		MOSFET Driver IC	Intersil	HIP2100IB	SO-8

NOTE: Application specific components in **bold**.

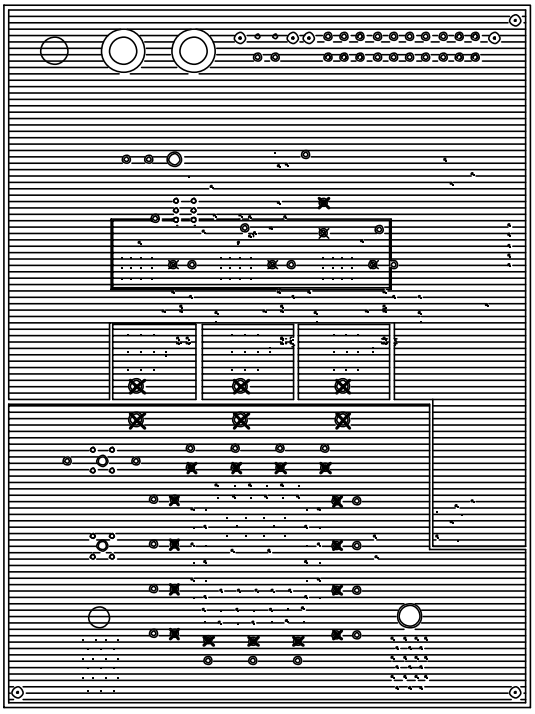
HIP6559EVAL2 Layout



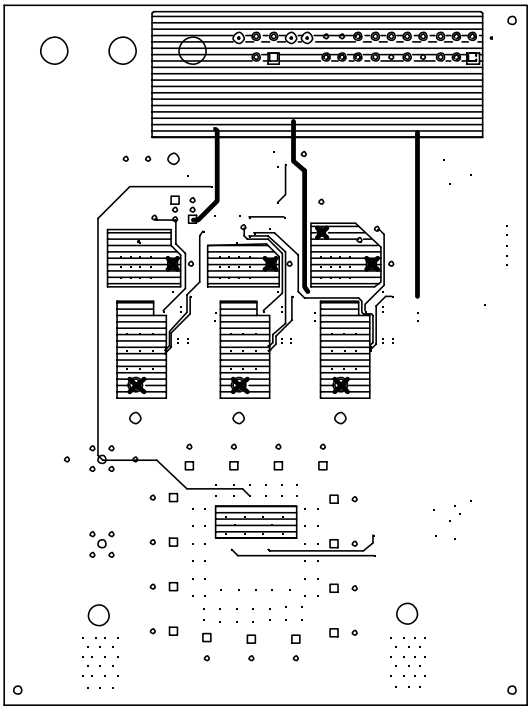
LAYER 1 - ROUTING AND SILK SCREEN



LAYER 2 - GND PLANE



LAYER 3 - POWER PLANE



LAYER 4 - ROUTING