

ISL1904DEMO1Z

Demonstration Board

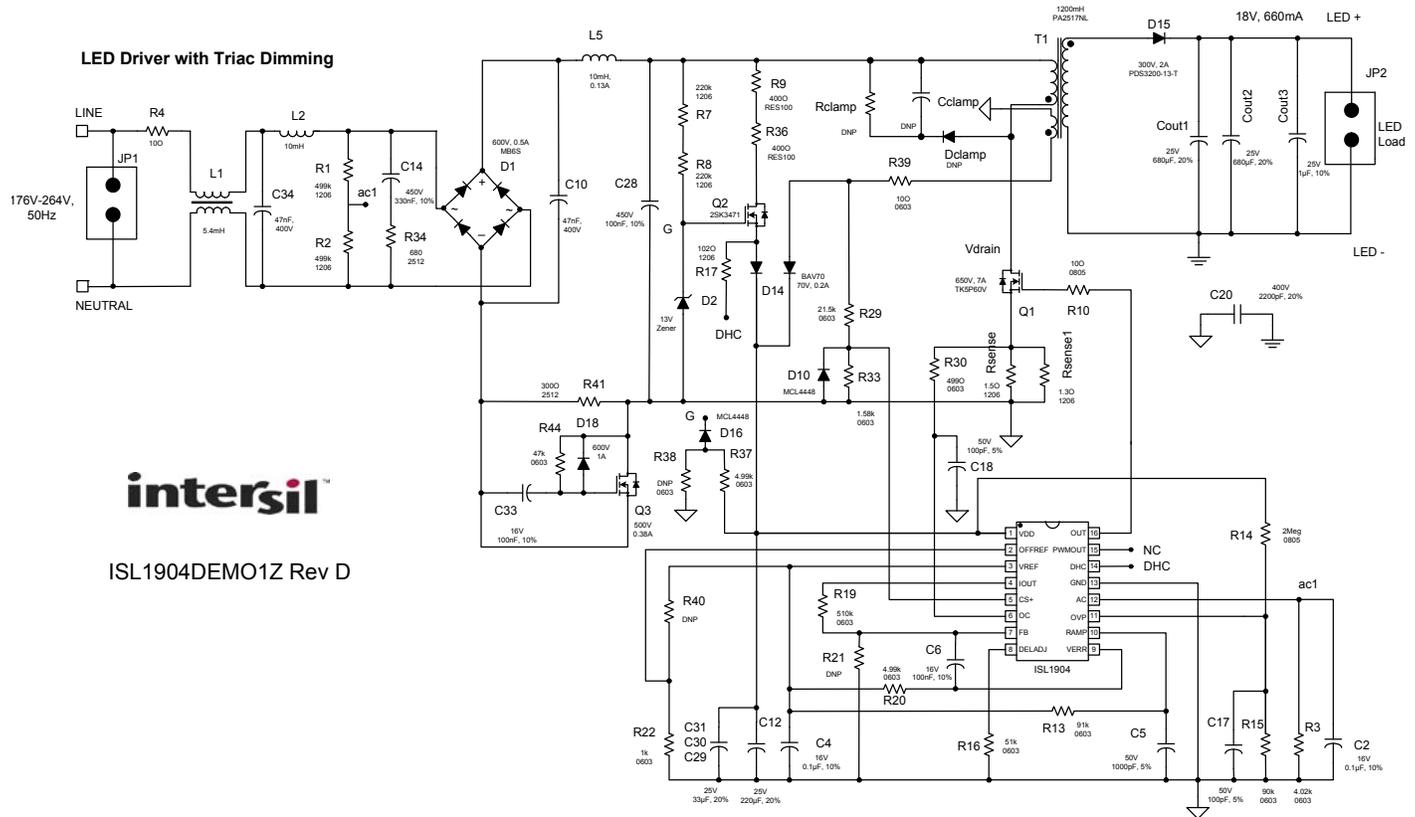
AN1845
Rev 0.00
Aug 28, 2013

Introduction

The ISL1904DEMO1Z demo board converts a high line AC input voltage to a 18V, 700mA DC output. It is implemented with Intersil's critical conduction mode (CrCM) LED driver controller, the ISL1904. It demonstrates the fundamental functions of ISL1904, including soft-start, dimming, over-voltage protection, short circuit protection, etc. The circuit operates in CrCM with variable frequency and allows near zero-voltage switching (ZVS). Typical efficiency is about 81% at full load. The ISL1904DEMO1Z demo board supports phase dimming and is compatible with wide variety of leading and trailing edge dimmers available in the market. This application note covers the performance data, critical waveforms, extensive dimming data, schematics, layout and bill of materials.

Design Specifications

- Input voltage V_{IN} : 176V to 264V
- Output voltage V_O : 12V to 20V
- Output current I_O : 700mA (14W)
- Board dimensions: $68 \times 26 \times 15\text{mm}^3$ (L×W×H)
- Input power factor greater than 0.93 at nominal
- Total harmonic distortion less than 7% at nominal
- Peak efficiency at full load: 81%
- 0-100% flicker free dimming with leading and trailing edge dimmers



ISL1904DEMO1Z Rev D

FIGURE 1. ISOLATED FLYBACK CONVERTER APPLICATION SCHEMATIC

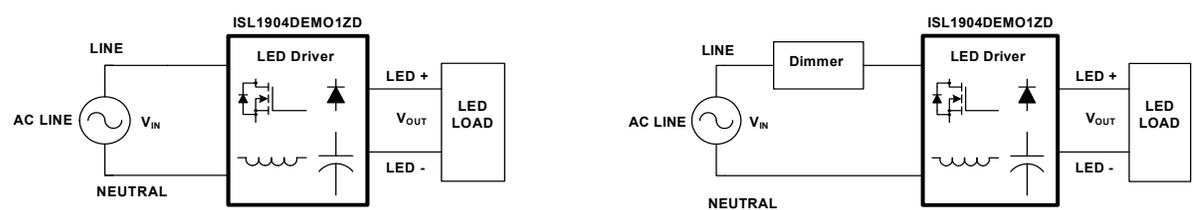


FIGURE 2. TEST SETUP WITH AND WITHOUT DIMMING

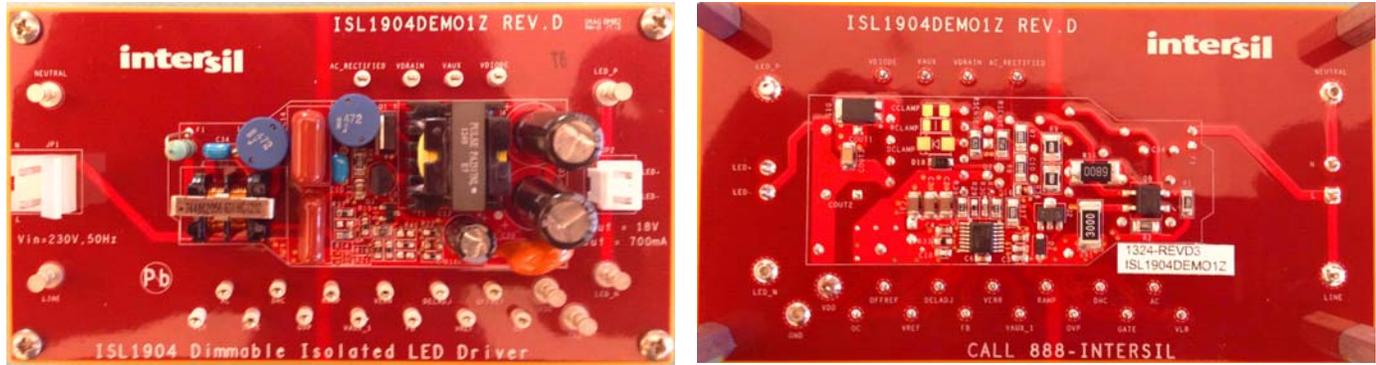


FIGURE 3. TOP/BOTTOM VIEW OF THE EVALUATION BOARD

Schematic Description

General Description of ISL1904

The ISL1904 is a high-performance, critical conduction mode (CrCM), single-ended flyback LED driver controller. It supports single-stage conversion of the AC mains to a constant current source with power factor correction (PFC). It also may be used with DC input converters. The ISL1904 also supports boost, Cuk, sepic and buck-boost converters. Operation in CrCM allows near zero-voltage switching (ZVS) for improved efficiency while maximizing magnetic core utilization. The ISL1904 LED driver provides all of the features required for high-performance dimmable LED driver designs.

Input EMI Filtering

Fusible resistor R4 provides protection from components failure. Input EMI filtering is provided by differential inductors L2, L5 and capacitors C14 and C28. The switching current generated by the power-train to the AC line is filtered by the input filter network.

Start-up Network

A linear regulator startup network is used for initial startup. R7, R8, R9, R36, Q2 and D2 constitute the linear startup circuit. Once the energy is built and voltage is generated on the aux winding, the linear regulator circuit is disabled and the aux winding supplies the voltage and current to the controller IC.

Power Stage

The primary current loop encompasses the transformer primary winding, MOSFET Q1 and the current sense resistors Rsense and Rsense1.

Near zero voltage switching (ZVS) or quasi-resonant switching, as it is sometimes referred to, can be achieved by delaying the next switching cycle after the inductor current decays to zero. The delay allows the inductance and parasitic capacitance to oscillate, causing the switching FET drain-source voltage to ring down to minima. If the FET is turned on at this minima, the capacitive switching losses ($\frac{1}{2}CV^2$) are greatly reduced.

Inductor zero-crossing is detected using the transformer aux winding. R29, R12 scales down the sensed zero crossing voltage and is delivered to the IC. Deladj sets the delay before a new switching cycles starts. This adjustment allows the user to delay the next switching cycle until the switching FET drain-source

voltage reaches a minimum value to allow quasi-ZVS (Zero Voltage Switching) operation. Resistor R16 to ground programs the delay.

DELAY TIME SETTING

In order to reduce electromagnetic interference and switching loss, ISL1904 can insert a delay between the off period and the on period. A resistor connected from deladj pin to ground will program the delay time according to the equation below. The optimal delay time depends on the resonance between the inductance, drain-source capacitance (Coss) and parasitic capacitance on the drain node. Circuit designers should optimize the delay according to the following equation:

$$f_{sw} = \frac{1}{2\pi \sqrt{L_p(C_{oss} + C_{stray})}}$$

After determining the delay time, the resistor can be chosen according to the following equation:

$$R_{del} = \left| \frac{(T_{del} - 73.33)}{10.2} \right| k\Omega$$

Resistor R16 programs this delay in the application schematic.

Feedback

The ISL1904 is designed to regulate the LED current by monitoring the primary switch current at the OC pin through resistors Rsense and Rsense1. The peak primary switch current is captured, processed, and output on I_{OUT} as a PWM voltage signal modulated in proportion to the LED current. The I_{OUT} PWM frequency is the same as the converter switching frequency and its amplitude is equivalent to 4x the peak switch current during the previous ON-time. Resistor R19 scales the signal before being input to the control loop at the FB pin. The OC pin also provides cycle-by-cycle overcurrent protection. The ON-time is terminated if OC exceeds 0.6V nominal. There is ~120ns of leading edge blanking (LEB) on OC to minimize or eliminate external filtering.

Output Rectification

Transformer secondary winding voltage is rectified by diode D15 and filtered by capacitors Cout1, Cout2 and Cout3. The capacitors are connected in parallel as the combination has a lower parasitic inductance and resistance compared to a single capacitor.

Overvoltage Protection

ISL1904 has an independent overvoltage protection accessed through the OVP pin. There is a nominal 20µA switched current source to create hysteresis. The current source is active only during an OV fault; otherwise, it is inactive and does not affect the node voltage.

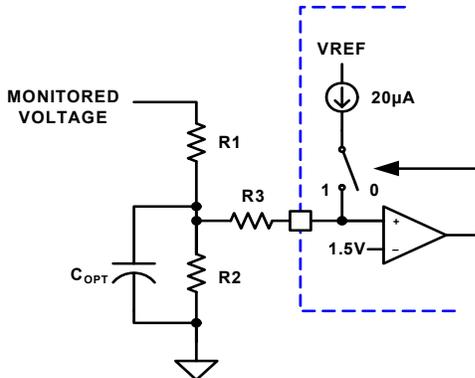


FIGURE 4. OV HYSTERESIS

$$V = 1.5 \frac{(R1 + R2)}{R2} V$$

Hysteresis is given by: $\Delta V = 20 \times 10^{-6} \times R1 V$

DESIGN EXAMPLE

Flyback converter Inductance calculation

TABLE 1.

| PARAMETER | VALUE | DESCRIPTION |
|----------------|--------|--|
| $V_{min(rms)}$ | 176V | Min rms input voltage |
| $V_{max(rms)}$ | 264V | Max rms input voltage |
| η | | Efficiency |
| $f_{min(avg)}$ | 100kHz | Frequency when $V_{IN} = \min V_{IN(rms)}$ |
| D_{max} | 0.4 | Maximum duty cycle |
| V_{OUT} | 18V | Output voltage |
| I_{OUT} | 0.7 | LED current |
| I_{spk} | | Peak secondary current - avg |
| I_{ppk} | | Peak primary current - avg |
| I_{spkmax} | | Peak secondary current - max |
| I_{ppkmax} | | Peak primary current - max |
| C_{OSS} | | MOSFET drain-source capacitance |
| C_{other} | | Parasitic capacitance on drain node |

Secondary inductance is calculated as:

$$L_s = \frac{V_o(1 - D_{max})^2}{2 \times f \times I_{out}} = \frac{18(1 - 0.4)^2}{2 \times 100 \times 10^3 \times 0.7} = 46.3 \mu H$$

Primary to sec turns ratio:

$$N_{sp} = \frac{V_o(1 - D_{max})}{V_{minpk} \times D_{max}} = \frac{18(1 - 0.4)}{176 \times \sqrt{2} \times 0.4} = 0.11$$

Primary Inductance:

$$L_p = \frac{L_s}{N_{sp}^2} = \frac{46.3 \mu H}{0.11^2} = 2.89 mH$$

Bias voltage: $V_{bias} = 12V$

Aux voltage is: $V_{aux} = V_{bias} + 0.7 = 12.7V$

Aux winding inductance is:

$$L_{aux} = L_s \frac{V_{aux}^2}{(N_{sp} \times V_f + V_d)^2} = 16.9 \mu H$$

Peak secondary current (avg) is:

$$I_{spk} = \frac{V_{out}(1 - D_{max})}{f \times L_s} = \frac{18(1 - 0.4)}{100 \times 10^3 \times 46.3 \times 10^{-6}} = 2.75 A$$

Peak primary current (avg) is:

$$I_{ppk} = I_{spk} \times N_{sp} = 2.75 \times 0.11 = 0.344 A$$

Maximum peak primary current is:

$$I_{ppkmax} = \frac{V_{minpk} \times T_{on} \times \sqrt{2}}{L_p} = 0.49 A$$

Maximum peak secondary current is

$$I_{spkmax} = \frac{I_{ppkmax}}{N_{sp}} = 3.88 A$$

Time period is: $T_s = \frac{1}{f_s} = 10 \mu s$

Maximum ON time is $T_{onmax} = D_{max} \times T_s = 4 \mu s$

Delay time to program partial zero voltage switching:

$$T_{delay} = \frac{\pi \sqrt{L_p(C_{oss} + C_{other})}}{2} = 1005 ns$$

Worst case minimum frequency is

$$f_{min} = \frac{1}{T_{on} + T_{offmax} + T_{delay}} = 80.09 kHz$$

OFFREF control:

$$REFIN(off) = OFFREF - 0.1$$

$$REFIN(on) = OFFREF - 0.05$$

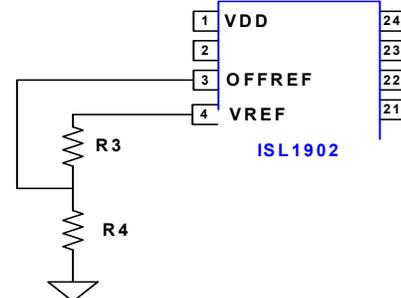


FIGURE 5.

$$OFFREF = \frac{R4}{R3 + R4} V_{ref}$$

Performance Data

TABLE 2. PERFORMANCE DATA WITH VARIATION IN TEMPERATURE

| TEMP (°C) | V _{IN} (V) | V _{OUT} (V) | I _{OUT} (mA) | P _{OUT} (W) | P _{IN} (W) | EFF (%) | PF (%) | THD (%) |
|-----------|---------------------|----------------------|-----------------------|----------------------|---------------------|---------|--------|---------|
| -35 | 220 | 18.57 | 709.21 | 16.86 | 13.17 | 78.13 | 90.97 | 7.704 |
| -20 | 220 | 18.57 | 703.74 | 16.71 | 13.07 | 78.24 | 90.88 | 7.69 |
| 5 | 220 | 18.42 | 714.72 | 16.40 | 13.16 | 80.25 | 90.68 | 8.22 |
| 25 | 220 | 18.47 | 704.50 | 16.31 | 13.01 | 79.80 | 90.68 | 8.19 |
| 50 | 220 | 18.61 | 705.02 | 16.27 | 13.12 | 80.66 | 90.89 | 7.87 |
| 75 | 220 | 18.51 | 709.35 | 16.07 | 13.13 | 81.72 | 90.89 | 7.86 |
| 105 | 220 | 18.46 | 692.26 | 15.81 | 12.78 | 80.82 | 90.75 | 7.56 |
| 125 | 220 | 18.40 | 664.58 | 15.46 | 12.23 | 79.09 | 90.22 | 7.61 |

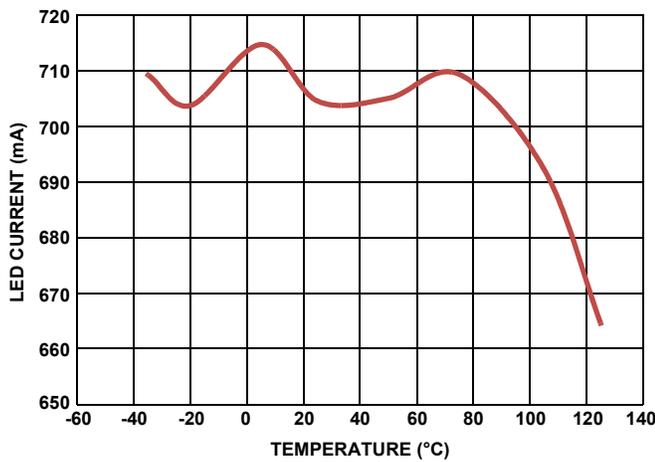


FIGURE 6. VARIATION OF LED CURRENT WITH AMBIENT TEMPERATURE

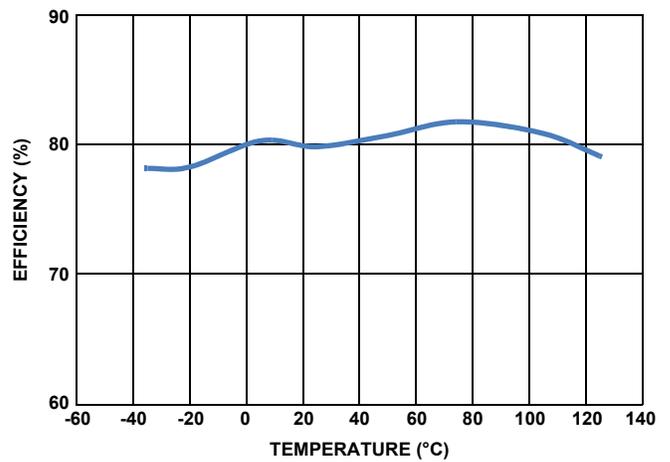


FIGURE 7. VARIATION OF EFFICIENCY WITH AMBIENT TEMPERATURE

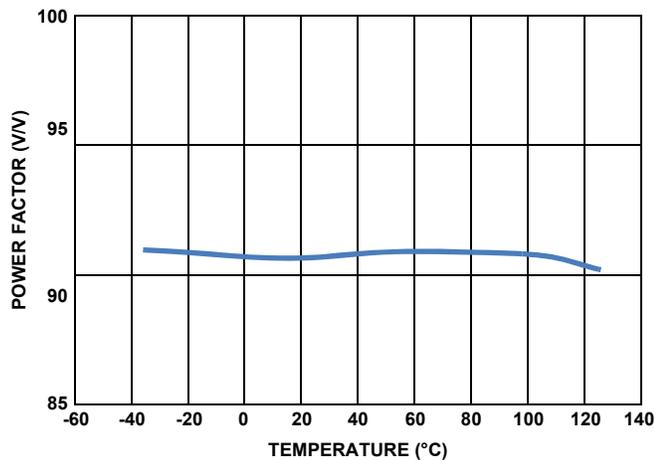


FIGURE 8. VARIATION OF POWER FACTOR WITH AMBIENT TEMPERATURE

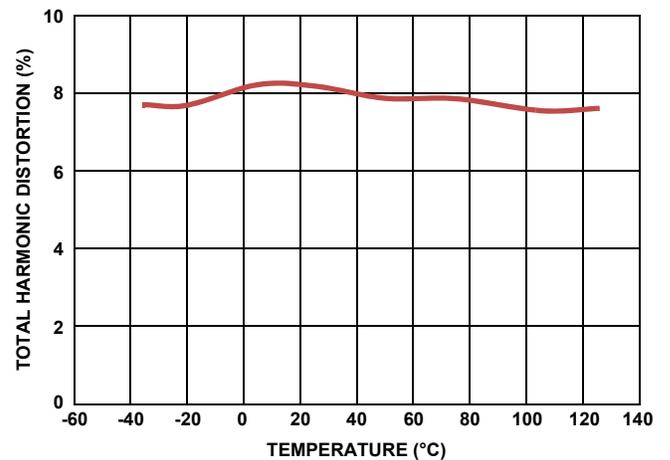


FIGURE 9. VARIATION OF THD WITH AMBIENT TEMPERATURE

TABLE 3. PERFORMANCE DATA WITH 5 LED LOAD

| V _{RMS} (V) | V _{PK} (V) | I _{IN} (mA) | V _{OUT} (V) | I _{OUT} (mA) | P _{IN} (W) | P _{OUT} (W) | P _{LOSS} (W) | EFFI (%) | PF (%) | ATHD (%) |
|----------------------|---------------------|----------------------|----------------------|-----------------------|---------------------|----------------------|-----------------------|--------------|--------------|-------------|
| AVERAGE | | 69.10 | 15.37 | 683.93 | 13.43 | 10.52 | 2.92 | 78.27 | 89.94 | 9.70 |
| 170.10 | 240.60 | 81.25 | 15.36 | 685.02 | 13.39 | 10.52 | 2.87 | 78.56 | 96.92 | 8.02 |
| 180.08 | 254.70 | 77.66 | 15.37 | 703.22 | 13.39 | 10.81 | 2.58 | 80.74 | 95.75 | 8.44 |
| 190.10 | 268.80 | 74.69 | 15.39 | 686.58 | 13.41 | 10.57 | 2.84 | 78.80 | 94.45 | 8.90 |
| 200.08 | 283.00 | 72.09 | 15.41 | 687.77 | 13.45 | 10.60 | 2.85 | 78.79 | 93.23 | 9.15 |
| 210.10 | 297.10 | 69.85 | 15.40 | 700.54 | 13.50 | 10.79 | 2.71 | 79.92 | 91.99 | 9.45 |
| 220.11 | 311.30 | 67.86 | 15.40 | 696.67 | 13.52 | 10.73 | 2.79 | 79.35 | 90.52 | 9.76 |
| 230.11 | 325.40 | 66.06 | 15.38 | 695.25 | 13.51 | 10.69 | 2.82 | 79.13 | 88.87 | 10.25 |
| 240.03 | 339.50 | 64.45 | 15.36 | 679.63 | 13.47 | 10.44 | 3.04 | 77.47 | 87.09 | 10.36 |
| 250.10 | 353.70 | 63.05 | 15.37 | 669.18 | 13.44 | 10.28 | 3.16 | 76.52 | 85.22 | 10.62 |
| 260.14 | 367.90 | 61.81 | 15.34 | 658.98 | 13.37 | 10.11 | 3.26 | 75.62 | 83.13 | 10.89 |
| 264.19 | 373.60 | 61.36 | 15.35 | 660.37 | 13.33 | 10.14 | 3.19 | 76.07 | 82.20 | 10.83 |

TABLE 4. PERFORMANCE DATA WITH 6 LED LOAD

| V _{RMS} (V) | V _{PK} (V) | I _{IN} (mA) | V _{OUT} (V) | I _{OUT} (mA) | P _{IN} (W) | P _{OUT} (W) | P _{LOSS} (W) | EFFI (%) | PF (%) | ATHD (%) |
|----------------------|---------------------|----------------------|----------------------|-----------------------|---------------------|----------------------|-----------------------|--------------|--------------|-------------|
| AVERAGE | | 78.391 | 18.35 | 684.48 | 15.70 | 12.56 | 3.14 | 80.01 | 92.52 | 8.37 |
| 170.12 | 240.60 | 92.10 | 18.32 | 669.43 | 15.32 | 12.27 | 3.05 | 80.08 | 97.77 | 7.04 |
| 180.08 | 254.70 | 87.81 | 18.35 | 673.88 | 15.30 | 12.36 | 2.94 | 80.80 | 96.77 | 7.39 |
| 190.11 | 268.90 | 84.24 | 18.32 | 679.84 | 15.32 | 12.46 | 2.87 | 81.30 | 95.68 | 7.75 |
| 200.09 | 283.00 | 81.25 | 18.36 | 679.71 | 15.40 | 12.48 | 2.92 | 81.02 | 94.72 | 8.12 |
| 210.10 | 297.10 | 78.75 | 18.33 | 676.66 | 15.52 | 12.40 | 3.12 | 79.91 | 93.81 | 8.34 |
| 220.12 | 311.30 | 76.66 | 18.36 | 683.45 | 15.65 | 12.55 | 3.11 | 80.16 | 92.76 | 8.67 |
| 230.11 | 325.40 | 74.91 | 18.35 | 693.90 | 15.79 | 12.73 | 3.06 | 80.63 | 91.61 | 8.82 |
| 240.04 | 339.50 | 73.40 | 18.36 | 698.04 | 15.93 | 12.82 | 3.11 | 80.46 | 90.42 | 8.94 |
| 250.11 | 353.70 | 72.05 | 18.34 | 690.84 | 16.07 | 12.67 | 3.40 | 78.83 | 89.19 | 8.98 |
| 260.15 | 367.90 | 70.80 | 18.37 | 694.93 | 16.17 | 12.76 | 3.41 | 78.93 | 87.80 | 8.99 |
| 264.20 | 373.60 | 70.33 | 18.35 | 688.61 | 16.19 | 12.63 | 3.56 | 78.01 | 87.15 | 9.05 |

TABLE 5. PERFORMANCE DATA WITH 7 LED LOAD

| V _{RMS} (V) | V _{PK} (V) | I _{IN} (mA) | V _{OUT} (V) | I _{OUT} (mA) | P _{IN} (W) | P _{OUT} (W) | P _{LOSS} (W) | EFFI (%) | PF (%) | ATHD (%) |
|----------------------|---------------------|----------------------|----------------------|-----------------------|---------------------|----------------------|-----------------------|--------------|--------------|-------------|
| AVERAGE | | 86.76 | 21.36 | 662.70 | 17.64 | 14.16 | 3.48 | 80.28 | 93.98 | 7.35 |
| 170.11 | 240.60 | 103.45 | 21.38 | 652.23 | 17.32 | 13.95 | 3.37 | 80.549 | 98.39 | 6.35 |
| 180.08 | 254.70 | 98.39 | 21.38 | 649.51 | 17.28 | 13.89 | 3.39 | 80.37 | 97.53 | 6.69 |
| 190.10 | 268.80 | 93.96 | 21.37 | 650.78 | 17.24 | 13.91 | 3.34 | 80.66 | 96.57 | 7.00 |
| 200.07 | 282.90 | 90.17 | 21.39 | 651.76 | 17.27 | 13.94 | 3.33 | 80.70 | 95.76 | 7.23 |
| 210.11 | 297.10 | 87.05 | 21.38 | 659.59 | 17.38 | 14.10 | 3.27 | 81.16 | 95.02 | 7.50 |
| 220.14 | 311.30 | 84.45 | 21.36 | 665.39 | 17.50 | 14.21 | 3.29 | 81.20 | 94.13 | 7.74 |
| 230.11 | 325.40 | 82.28 | 21.39 | 671.36 | 17.64 | 14.35 | 3.29 | 81.37 | 93.16 | 7.63 |
| 240.03 | 339.50 | 80.49 | 21.34 | 671.95 | 17.81 | 14.34 | 3.47 | 80.52 | 92.17 | 7.71 |
| 250.11 | 353.70 | 79.03 | 21.34 | 667.17 | 18.03 | 14.24 | 3.79 | 78.98 | 91.21 | 7.68 |
| 260.14 | 367.90 | 77.81 | 21.33 | 673.70 | 18.25 | 14.37 | 3.88 | 78.76 | 90.15 | 7.67 |
| 264.19 | 373.60 | 77.37 | 21.35 | 676.25 | 18.33 | 14.44 | 3.89 | 78.78 | 89.66 | 7.67 |

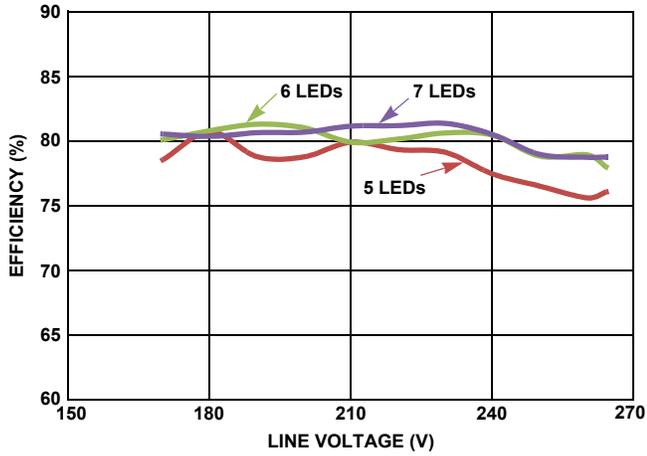


FIGURE 10. EFFICIENCY WITH LINE VOLTAGE AT DIFFERENT LOADS

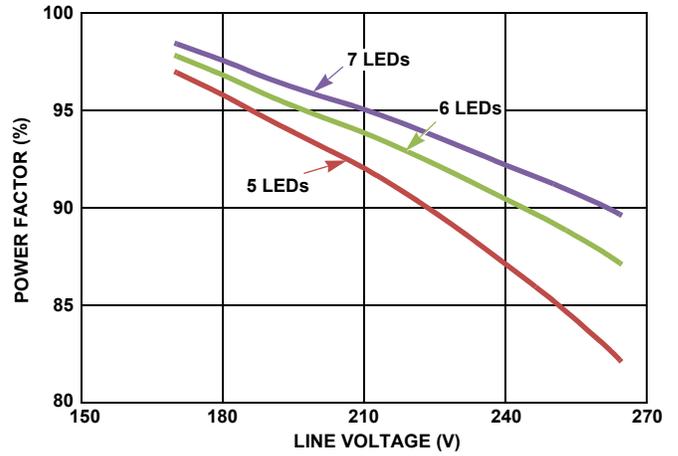


FIGURE 11. POWER FACTOR WITH LINE VOLTAGE AT DIFFERENT LOADS

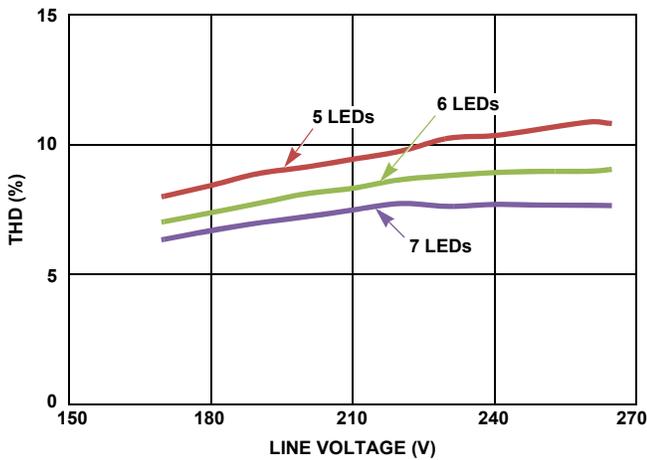


FIGURE 12. THD WITH LINE VOLTAGE AT DIFFERENT LOADS

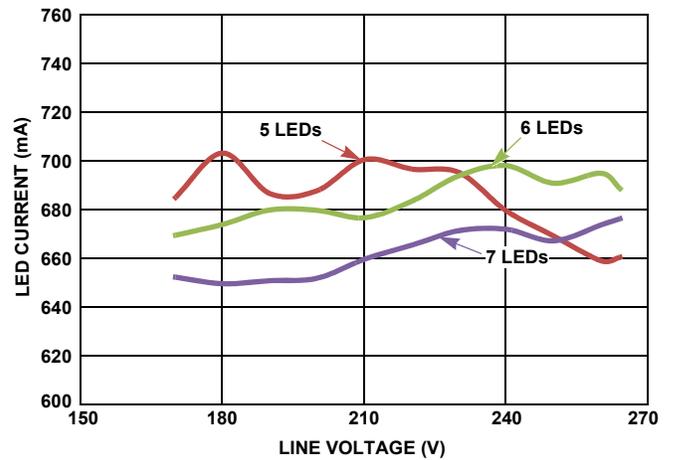


FIGURE 13. LED CURRENT WITH LINE VOLTAGE AT DIFFERENT LOADS

Critical Waveforms

WAVEFORM SHOWING LINE VOLTAGE AND LINE CURRENT: PF = 0.92

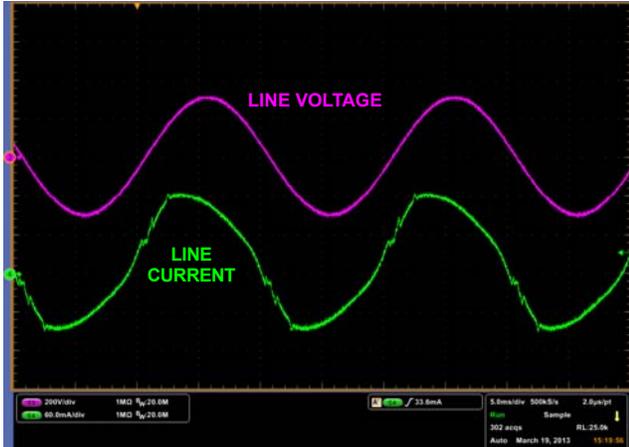


FIGURE 14. TRACE 3 - INPUT VOLTAGE [200V/DIV]; TRACE 4 - INPUT CURRENT [60mA/DIV]

LINE VOLTAGE AND CURRENT DURING STARTUP

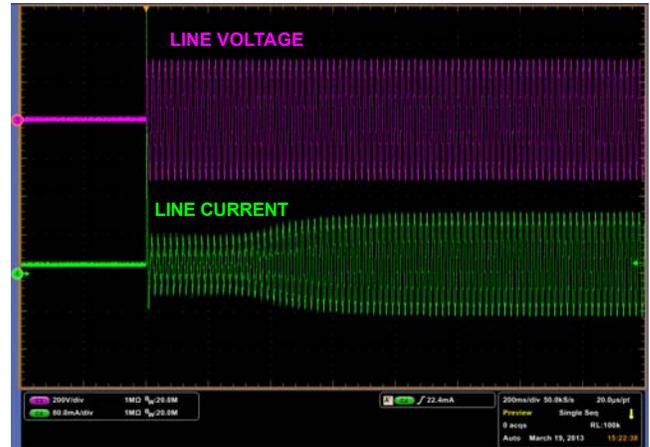


FIGURE 15. INPUTS DURING STARTUP; TRACE 3 - INPUT VOLTAGE [200V/DIV]; TRACE 4 - INPUT CURRENT [60mA/DIV]

Critical Waveforms (Continued)

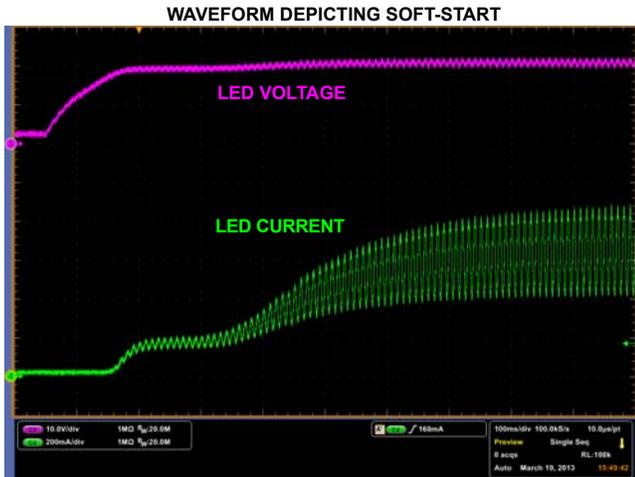


FIGURE 16. TRACE 3 - OUTPUT VOLTAGE [10V/DIV]; TRACE 4 - LED CURRENT [200mA/DIV]

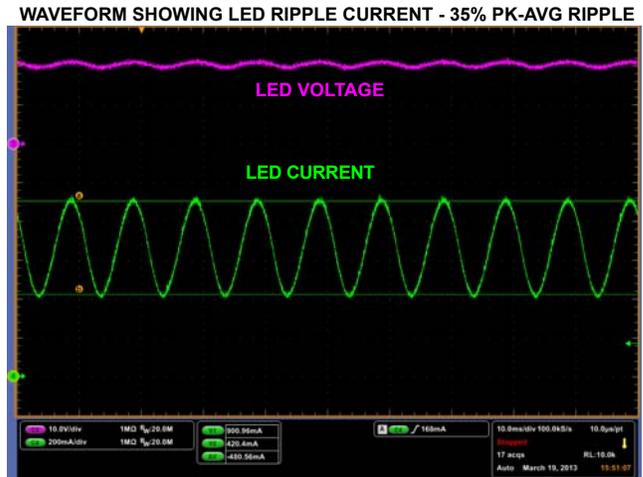


FIGURE 17. TRACE 3 - OUTPUT VOLTAGE [10V/DIV]; TRACE 4 - LED CURRENT [200mA/DIV]; LED CURRENT RIPPLE: 35% PK-AVG OR 1.35 CREST FACTOR

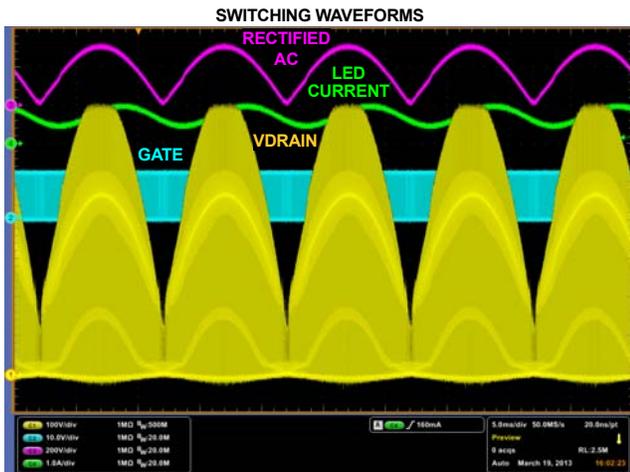


FIGURE 18. TRACE 1 - DRAIN VOLTAGE [100V/DIV]; TRACE 2 - GATE [10V/DIV]; TRACE 3 - RECTIFIED AC [200V/DIV]; TRACE 4 - LED CURRENT [1A/DIV]

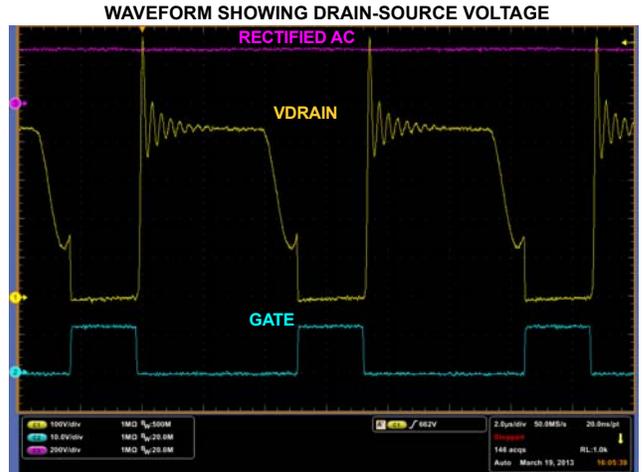


FIGURE 19. TRACE 1 - DRAIN VOLTAGE [100V/DIV]; TRACE 2 - GATE [10V/DIV]; SWITCHING WAVEFORMS

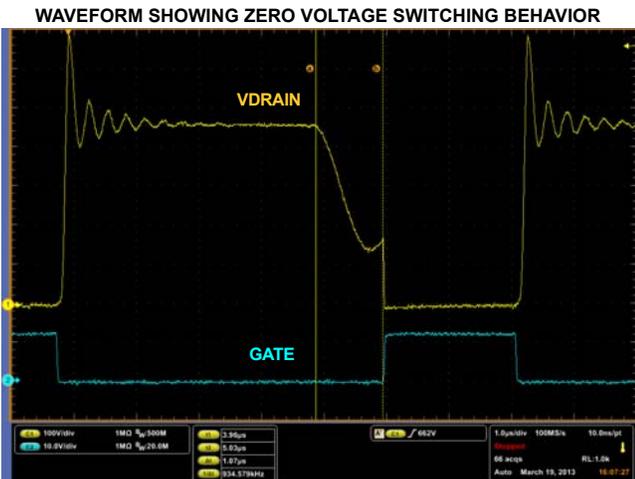


FIGURE 20. TRACE 1 - DRAIN VOLTAGE [100V/DIV]; TRACE 2 - GATE [10V/DIV]; TDELAY = 1.07μs; PARTIAL ZVS

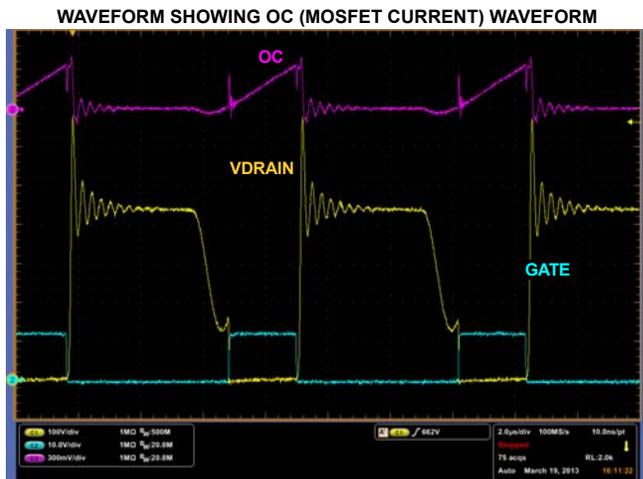


FIGURE 21. TRACE 1 - DRAIN VOLTAGE [100V/DIV]; TRACE 2 - GATE [10V/DIV]; TRACE 3 - DRAIN CURRENT OR OC [300mA/DIV]

Dimming Compatibility

The requirement to provide output dimming with low cost, TRIAC based, leading-edge phase dimmers introduced a number of trade-offs in the design.

Due to the much lower power consumed by LED based lighting, the current drawn by the lamp during dimming is below the holding current of the TRIAC within many dimmers. This causes undesirable behavior - limited dimming range and/or flickering when the TRIAC fires inconsistently. The relatively large impedance presented to the line by the LED driver allows significant ringing to occur due to the inrush current charging the input capacitance when the TRIAC turns on. This effect can cause similar undesirable behavior, as the ringing may cause the TRIAC current to fall to zero and turn off prematurely.

To overcome these issues, an active dimmer current holding circuit (DHC pin, R17), passive bleeder circuit (C14, R34) and an active damping circuit (Q3, D18, R44, C33 and R41) are incorporated into the design. These circuits result in increased power dissipation and hence reduce electrical efficiency and overall lamp efficacy. For non-dimming applications, these circuits can be omitted.

Dimming Curve

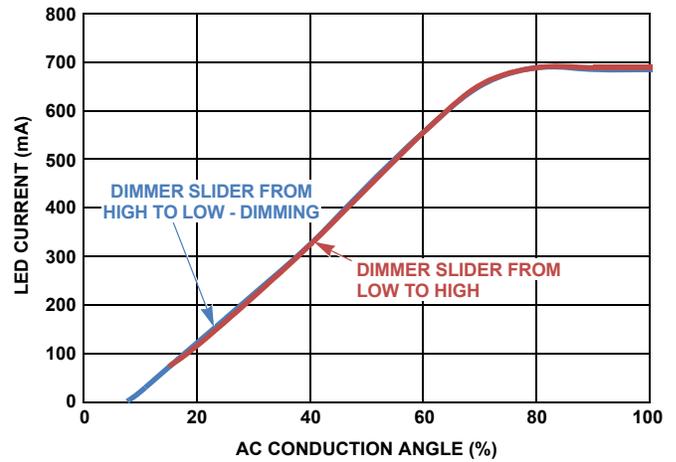


FIGURE 22. DIMMING CURVE - RAMPING DOWN AND RAMPING UP THE DIMMER; DIMMER USED: LEADING EDGE 600VA CHINESE DIMMER

TABLE 6. DIMMING DATA

| CONDUCTION ANGLE (%) | LED CURRENT (mA) | % OF LED CURRENT MEASURED (%) | % OF LIGHT PERCEIVED BY HUMAN EYE |
|----------------------|------------------|-------------------------------|-----------------------------------|
| 100 | 685 | 100 | 100 |
| 91 | 685 | 100 | 100 |
| 80 | 685 | 100 | 100 |
| 70 | 651 | 95.04 | 97.49 |
| 60 | 556 | 81.17 | 90.09 |
| 50 | 444 | 64.82 | 80.51 |
| 40 | 325 | 47.45 | 68.88 |
| 30 | 222 | 32.41 | 56.93 |
| 20 | 122 | 17.81 | 42.2 |
| 10 | 21 | 3.07 | 17.51 |
| 8 | 4 | 0.58 | 7.64 |

Dimming Waveforms

WAVEFORM SHOWING LINE VOLTAGE AND CURRENT;
CONDUCTION ANGLE: 90.6%

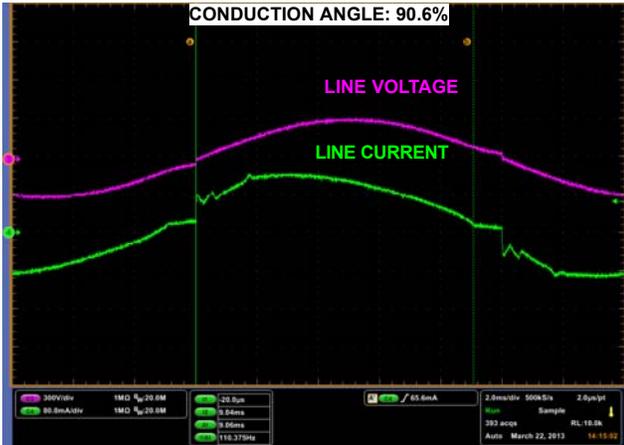


FIGURE 23. TRACE 3 - LINE VOLTAGE [300V/DIV]; TRACE 4 - LINE CURRENT [80mA/DIV]; 90.6% CONDUCTION ANGLE

WAVEFORM SHOWING LINE VOLTAGE AND CURRENT;
CONDUCTION ANGLE: 80%

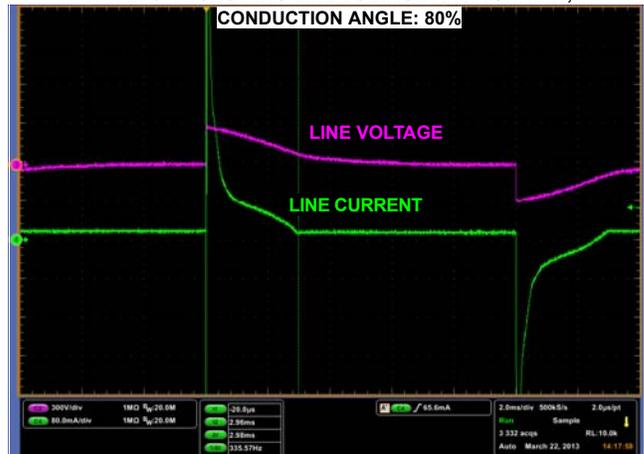


FIGURE 24. TRACE 3 - LINE VOLTAGE [300V/DIV]; TRACE 4 - LINE CURRENT [80mA/DIV]; 80% CONDUCTION ANGLE

WAVEFORM SHOWING LINE VOLTAGE AND CURRENT;
CONDUCTION ANGLE: 50%

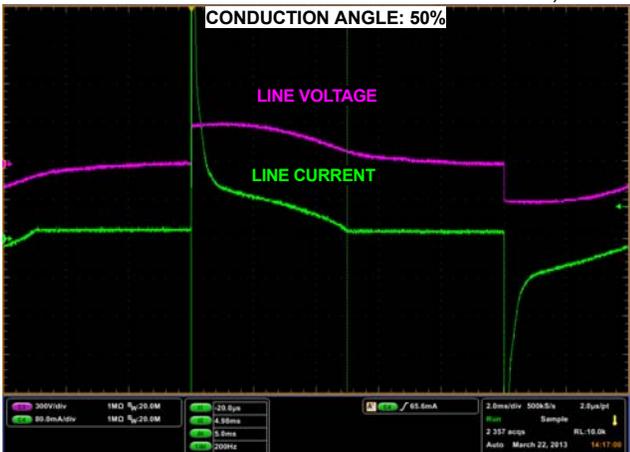


FIGURE 25. TRACE 3 - LINE VOLTAGE [300V/DIV]; TRACE 4 - LINE CURRENT [80mA/DIV]; 50% CONDUCTION ANGLE

WAVEFORM SHOWING LINE VOLTAGE AND CURRENT;
CONDUCTION ANGLE: 30%

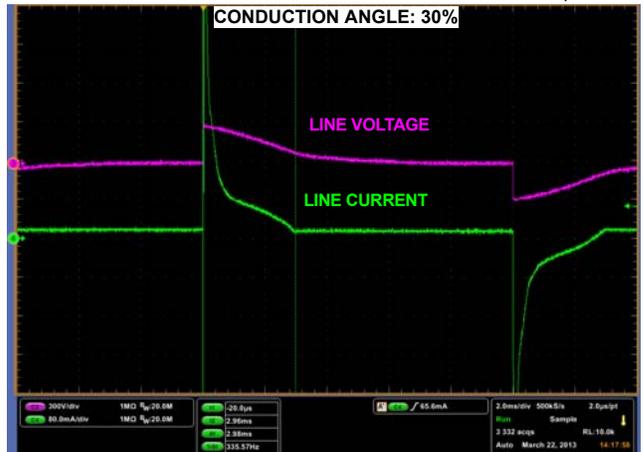


FIGURE 26. TRACE 3 - LINE VOLTAGE [300V/DIV]; TRACE 4 - LINE CURRENT [80mA/DIV]; 30% CONDUCTION ANGLE

WAVEFORM SHOWING LINE VOLTAGE AND CURRENT;
CONDUCTION ANGLE: 10%

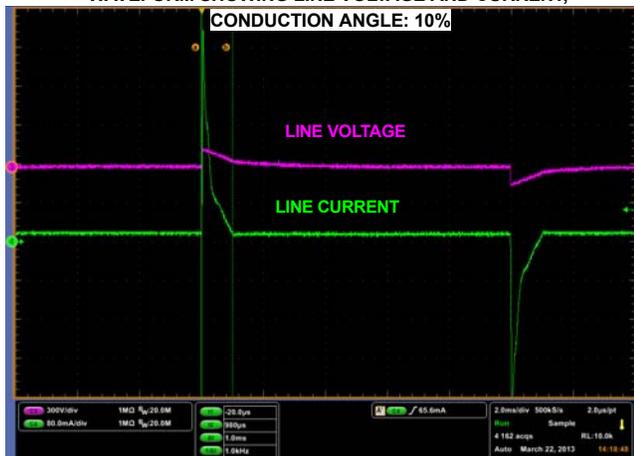


FIGURE 27. TRACE 3 - LINE VOLTAGE [300V/DIV]; TRACE 4 - LINE CURRENT [80mA/DIV]; 10% CONDUCTION ANGLE

WAVEFORM SHOWING LINE VOLTAGE AND CURRENT;
CONDUCTION ANGLE: 6.25%

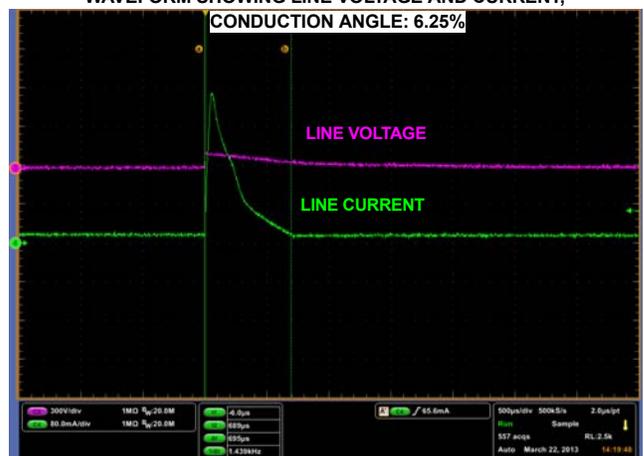


FIGURE 28. TRACE 3 - LINE VOLTAGE [300V/DIV]; TRACE 4 - LINE CURRENT [80mA/DIV]; 6.95% CONDUCTION ANGLE

Overvoltage Protection

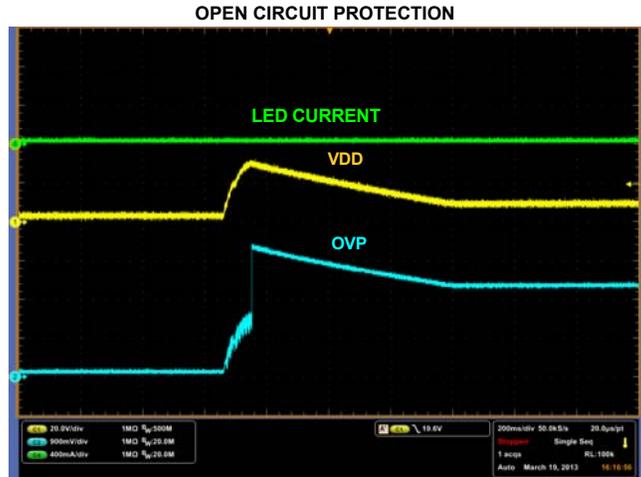


FIGURE 29. TRACE 1 - V_{DD} [20V/DIV]; TRACE 2- OVP [900mV/DIV]; TRACE 4 - LED CURRENT [400mA/DIV]

EMI Results - Cispr 22 Class B

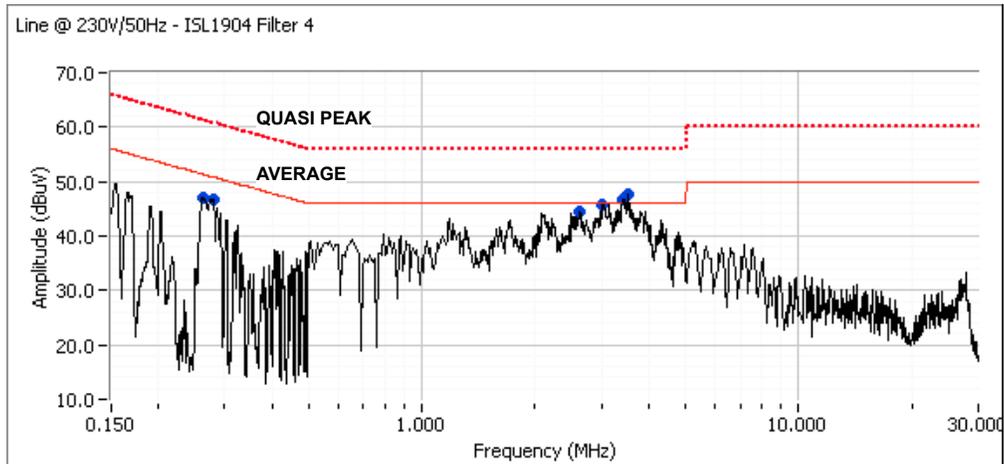


FIGURE 30. LINE AT 230V, 50Hz

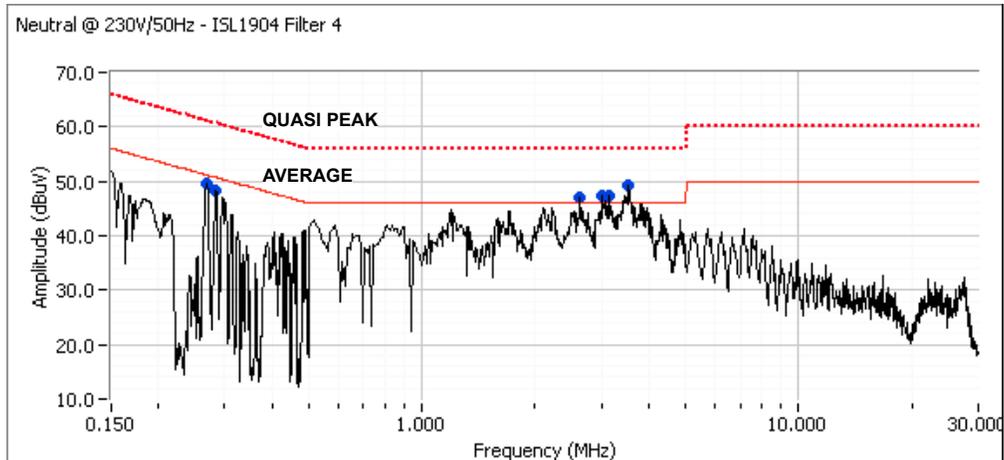


FIGURE 31. NEUTRAL AT 230V, 50Hz

TABLE 7. QUASI PEAK AND AVERAGE READINGS

| FREQUENCY (MHz) | LEVEL (dB μ V) | AC LINE | CLASS B | |
|-----------------|--------------------|---------|---------|--------|
| | | | LIMIT | MARGIN |
| 3.513 | 45.5 | Line 1 | 56 | -10.5 |
| 0.268 | 49.3 | Neutral | 61.2 | -11.9 |
| 2.61 | 44.1 | Neutral | 56 | -11.9 |
| 3.009 | 43.6 | Neutral | 56 | -12.4 |
| 3.535 | 43.6 | Neutral | 56 | -12.4 |
| 3.134 | 43.5 | Neutral | 56 | -12.5 |
| 0.284 | 47.9 | Neutral | 60.7 | -12.8 |
| 3.41 | 43 | Line 1 | 56 | -13 |
| 3.008 | 42.2 | Line 1 | 56 | -13.8 |
| 2.612 | 41.2 | Line 1 | 56 | -14.8 |
| 0.262 | 46.3 | Line 1 | 61.4 | -15.1 |
| 3.513 | 30.8 | Line 1 | 46 | -15.2 |
| 3.535 | 30.7 | Neutral | 46 | -15.3 |
| 0.28 | 44.5 | Line 1 | 60.8 | -16.3 |
| 3.41 | 29.4 | Line 1 | 46 | -16.6 |
| 3.134 | 29.4 | Neutral | 46 | -16.6 |
| 3.009 | 29.2 | Neutral | 46 | -16.8 |
| 2.61 | 28.2 | Neutral | 46 | -17.8 |
| 3.008 | 27.7 | Line 1 | 46 | -18.3 |
| 0.268 | 32.9 | Neutral | 51.2 | -18.3 |
| 2.612 | 25.9 | Line 1 | 46 | -20.1 |
| 0.262 | 30.6 | Line 1 | 51.4 | -20.8 |
| 0.284 | 27.8 | Neutral | 50.7 | -22.9 |
| 0.28 | 25.6 | Line 1 | 50.8 | -25.2 |

Temperature Mapping

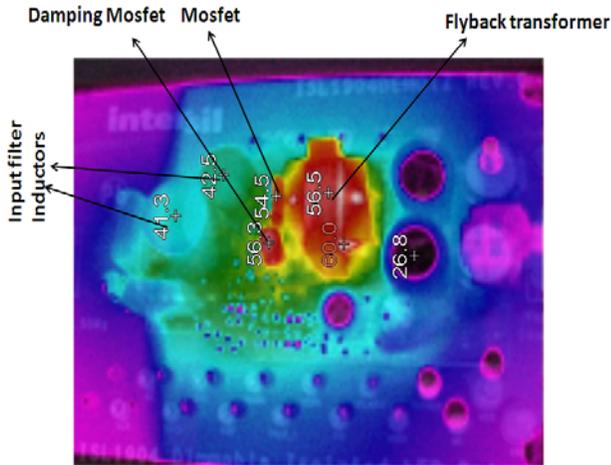


FIGURE 32. TOP SIDE TEMPERATURE SNAPSHOT DURING 100% CONDUCTION AND FULL LOADING

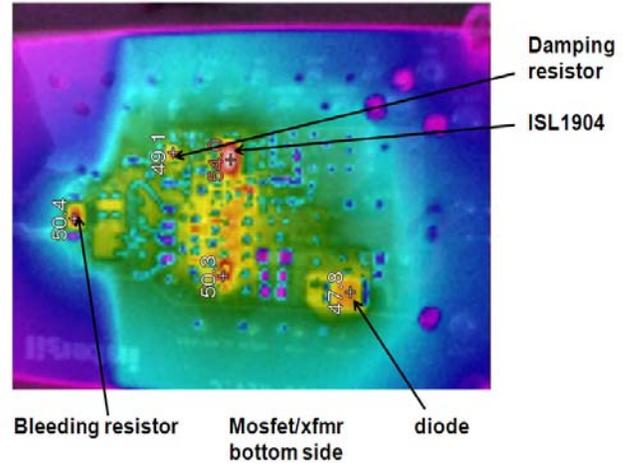


FIGURE 33. BOTTOM SIDE TEMPERATURE SNAPSHOT DURING 100% CONDUCTION AND FULL LOADING

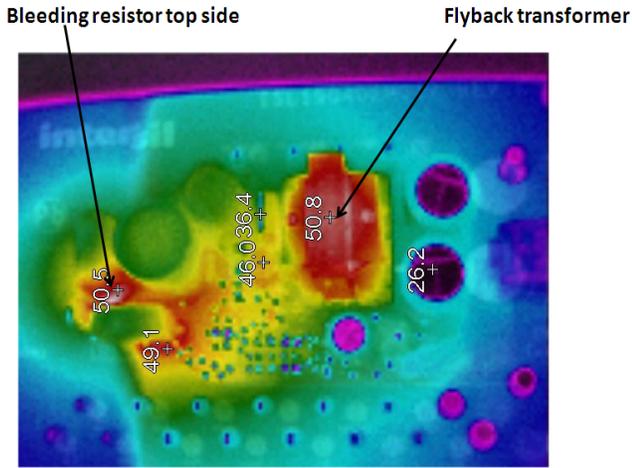


FIGURE 34. TOP SIDE TEMPERATURE SNAPSHOT DURING DEEP DIMMING

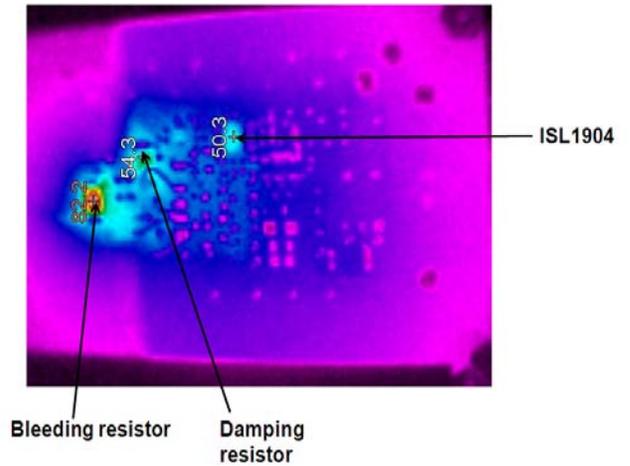
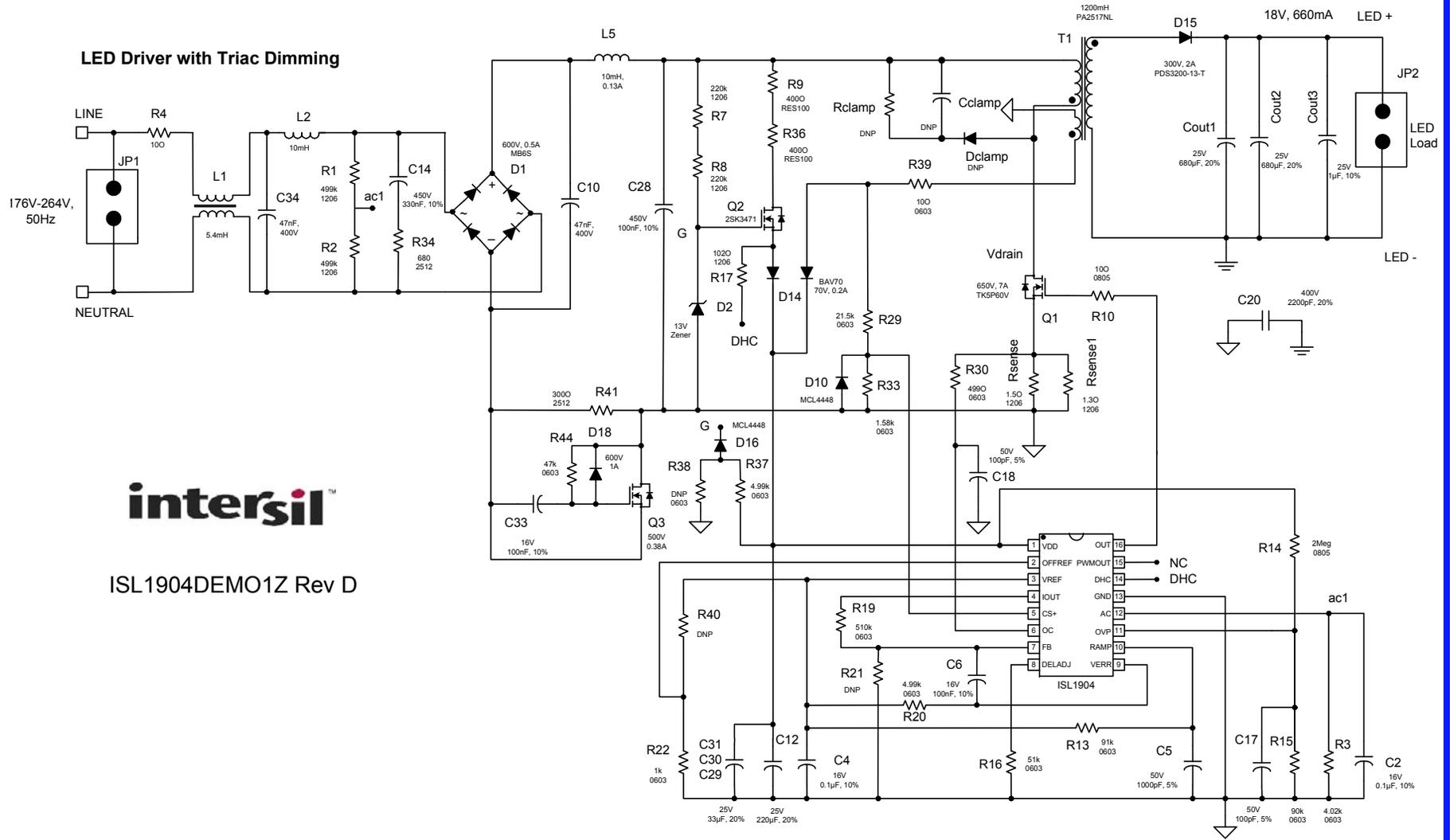


FIGURE 35. BOTTOM SIDE TEMPERATURE SNAPSHOT DURING DEEP DIMMING

Application Schematic



Electrical Bill of Materials

TABLE 8. BOM FOR ISL1904DEMO1Z REV. D

| QTY | REFERENCE DESIGNATOR | TYPE/MOUNT/PACKAGE/VOL/TOL/MAT | MANUFACTURER | MANUFACTURER PART # |
|-----|----------------------|--|--------------|-----------------------|
| 2 | C10, C34 | Cap, TH, CAPR_190x90_200, 47n, 400V, 10%, X7R | PANASONIC | ECQ-E4473KF |
| 3 | C2, C4, C6 | Cap, SM, 0603, 100n, 16V, 10%, MKT | | H1045-00104-16V10 |
| 1 | C5 | Cap, SM, 1000p, 50V, 5%, MKT | | H1045-00102-50V5 |
| 1 | C12 | Cap, TH, CAPR_248x354_100_P, 220 μ , 25V, 20% | RUBYCON | 25PX220MEFC6.3X11 |
| 1 | C14 | Cap, TH, CAPR_472x248_400, 0.33 μ , 450V, 10% | PANASONIC | ECW-F2W334JAQ |
| 1 | C17 | Cap, SM, 0603, 100p, 50V, 10% | | H1045-00101-50V10 |
| 1 | C18 | Cap, SM, 0603, 10p, 50V, 5%, COG | | |
| 1 | C20 | Cap, TH, CAPR_394x500_160, 2200p, 400V | VISHAY | 440LD22-R |
| 1 | C28 | Cap, TH, CAPR_472x248_400, 0.1 μ , 400V, 10% | PANASONIC | ECQ-E4104KF |
| 3 | C29, C30, C31 | Cap, SM, 1206, 33 μ , 25V, 20% | | H1065-00336-25V20-T |
| 1 | C33 | Cap, SM, 0805, 100n, 25V, 10% | | |
| 1 | Cclamp | Cap, SM, 1206, DNP | | |
| 2 | Cout1, Cout2 | Cap, TH, CAPR_393x630_200_P, 680 μ , 25V, ALUM | PANASONIC | EEUFR1E681 |
| 1 | Cout3 | Cap, SM, 1206, 1 μ , 25V, 10% | | |
| 1 | DB | Diode, SMD, DIO_MCC_MBS, 600V, 05A | MICRO COM | MB6D-TP-T |
| 1 | Dclamp | Diode, SMA, DNP | | |
| 1 | D2 | Diode, SM, SOD123FL, 13V, zener | MICRO COM | BZX84C20/MMSZ5243B-TP |
| 2 | D10, D16 | Diode, SM, MCL4448, 75V, 200mA, general purpose | VISHAY | MCL4448 |
| 1 | D14 | Diode, SM, SOT23, 75V, 150mA, switching | NXP | BAV70-TP |
| 1 | D15 | Diode, SM, SOD123FL, 600V, 1A, ultra fast | DIODES INC | PDS3200-13-T |
| 1 | D18 | Diode, SM, DIO_POWERD1-5, 200V, 3A, ultra fast | MICRO COM | SM4005PL-TP |
| 1 | F1 | RES, TH, RES100, 10 Ohms, fusible | YAGEO | FKN1WSJR-52-10R |
| 1 | L1 | IND, TH, 11x17x17mm, 5.4mH, common mode | WURTH | 744862056 |
| 2 | L2, L5a | IND, TH, 10mH, Radial | RENCO | |
| 1 | Q1 | MOSFET, TH, TO251, 600V, 7.5A | TOSHIBA | TK5Q60V |
| 1 | Q2 | MOSFET, SMD, SOT89, 500V, 0.5A | TOSHIBA | 2SK3471 |
| 1 | Q3 | MOSFET, TH, TO92, 500V, 0.38A | FAIRCHILD | FQN1N50CTA |
| 1 | Rclamp | Res, SM, 1206, DNP | | |
| 1 | Rsense | Res, SM, 1206, 1.5, 1%, Thick Film | | |
| 1 | Rsense1 | Res, SM, 1206, 1.2, 1%, Thick Film | | - |
| 2 | R1, R2 | Res, SM, 1206, 499k, 1%, Thick Film | | H2511-04993-1/8W1 |
| 1 | R3 | Res, SM, 0603, 4.02k, 1%, Thick Film | | H2511-04021-1/16W1 |
| 2 | R7, R8 | Res, SM, 1206, 220k, 1%, Thick Film | | H2513-02203-1/8W5 |
| 2 | R9, R36 | Res, SM, 1210, 499, 1%, Thick Film | | |
| 2 | R10, R39 | Res, SM, 0805, 10, 1%, Thick Film | | H2512-00100-1/10W1 |
| 1 | R13 | Res, SM, 0603, 43k, 1%, Thick Film | | H2511-04302-1/16W5 |
| 1 | R14 | Res, SM, 0805, 2Meg, 1%, Thick Film | | |
| 2 | R15, R16 | Res, SM, 0603, 91k, 1%, Thick Film | | H2511-09112-1/16W1 |

TABLE 8. BOM FOR ISL1904DEMO1Z REV. D (Continued)

| QTY | REFERENCE DESIGNATOR | TYPE/MOUNT/PACKAGE/VOL/TOL/MAT | MANUFACTURER | MANUFACTURER PART # |
|-----|----------------------|--------------------------------------|--------------|---------------------|
| 1 | R17 | Res, SM, 1206, 102, 1%, Thick Film | | H2513-01020-1/8W1 |
| 1 | R19 | Res, SM, 0603, 510k, 1%, Thick Film | | H2511-05103-1/16W5 |
| 2 | R20, R37 | Res, SM, 0603, 4.99k, 1%, Thick Film | | H2511-04991-1/16W1 |
| 2 | R21, R40 | Res, SM, 0603, DNP | | |
| 1 | R22 | Res, SM, 0603, 1k, 1%, Thick Film | | |
| 1 | R29 | Res, SM, 0603, 21.5k, 1%, Thick Film | | H2511-02152-1/16W1 |
| 1 | R30 | Res, SM, 0603, 499, 1%, Thick Film | | H2511-04990-1/16W1 |
| 1 | R33 | Res, SM, 0603, 1.58k, 1%, Thick Film | | |
| 1 | R34 | Res, SM, 2512, 680, 1%, Thick Film | | |
| 1 | R38 | Res, SM, 0603, DNP | | |
| 1 | R41 | Res, SM, 2512, 300, 1%, Thick Film | | |
| 1 | R44 | Res, SM, 1206, 47k, 1%, Thick Film | | |
| 1 | T1 | xfmr, TH, 1.2mH, 8:1 turns ratio | PULSE | PA2517NL |
| 1 | U1 | IC, SM, QSSOP, ISL1904FAZ | INTERSIL | ISL1904FAZ |

Assembly Drawing

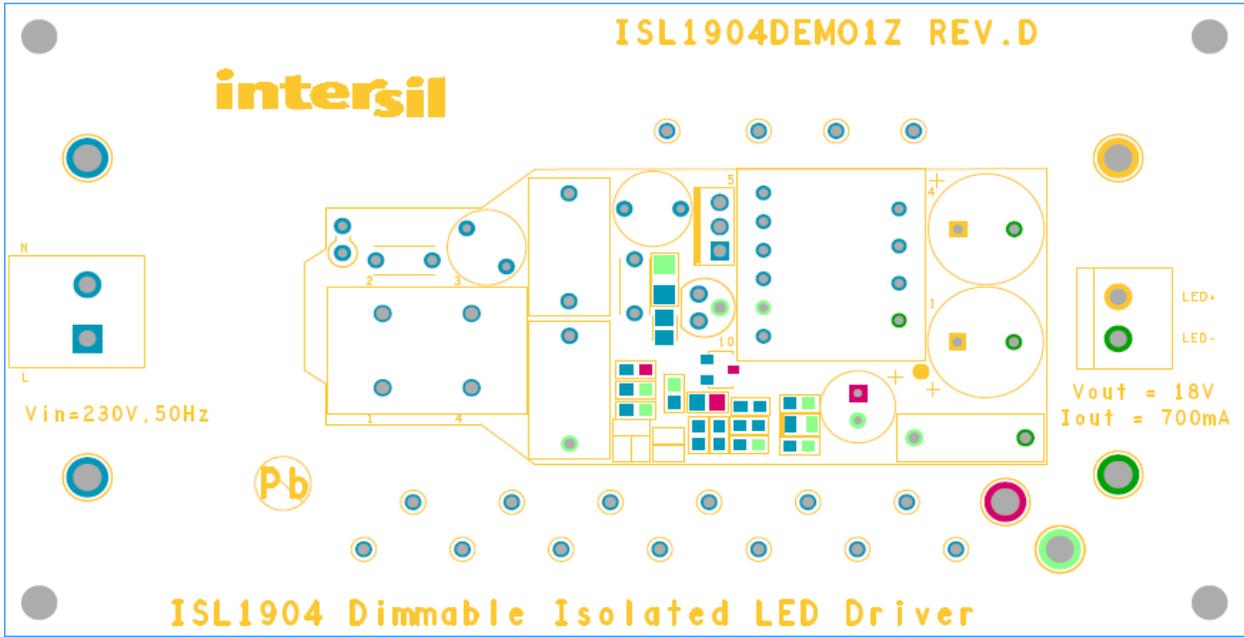


FIGURE 36. SILKSCREEN TOP

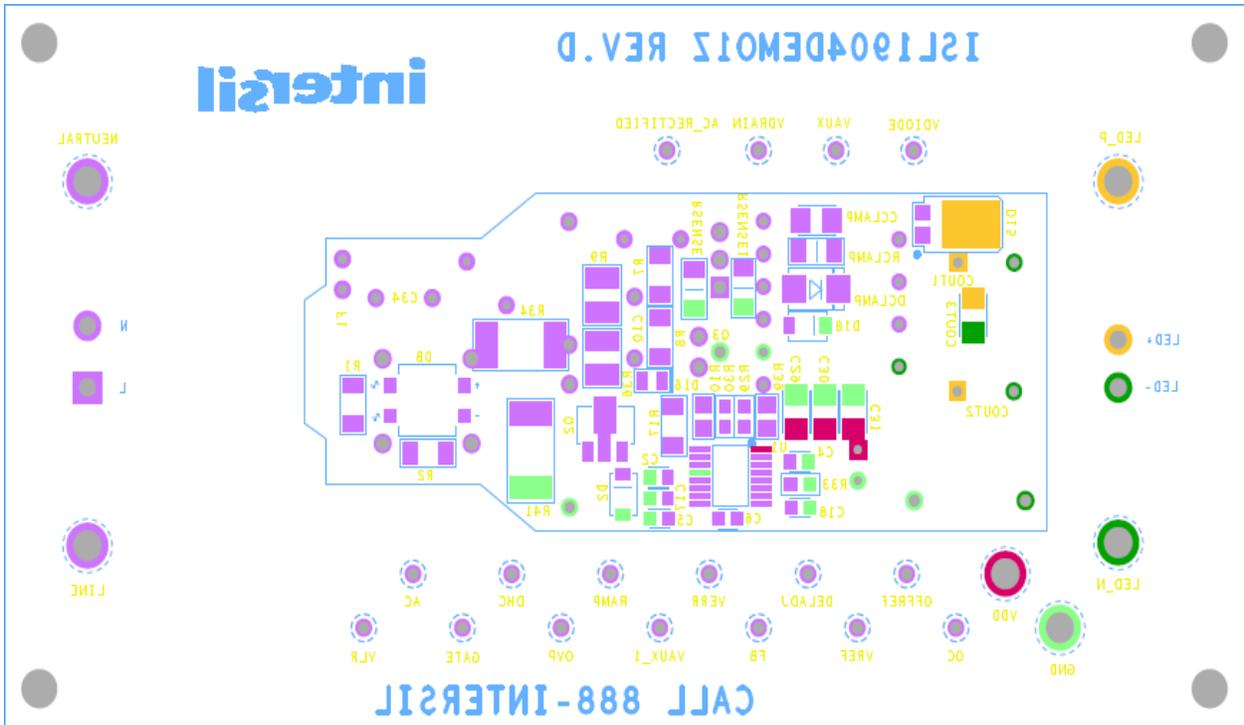


FIGURE 37. SILKSCREEN BOTTOM

PCB Layout

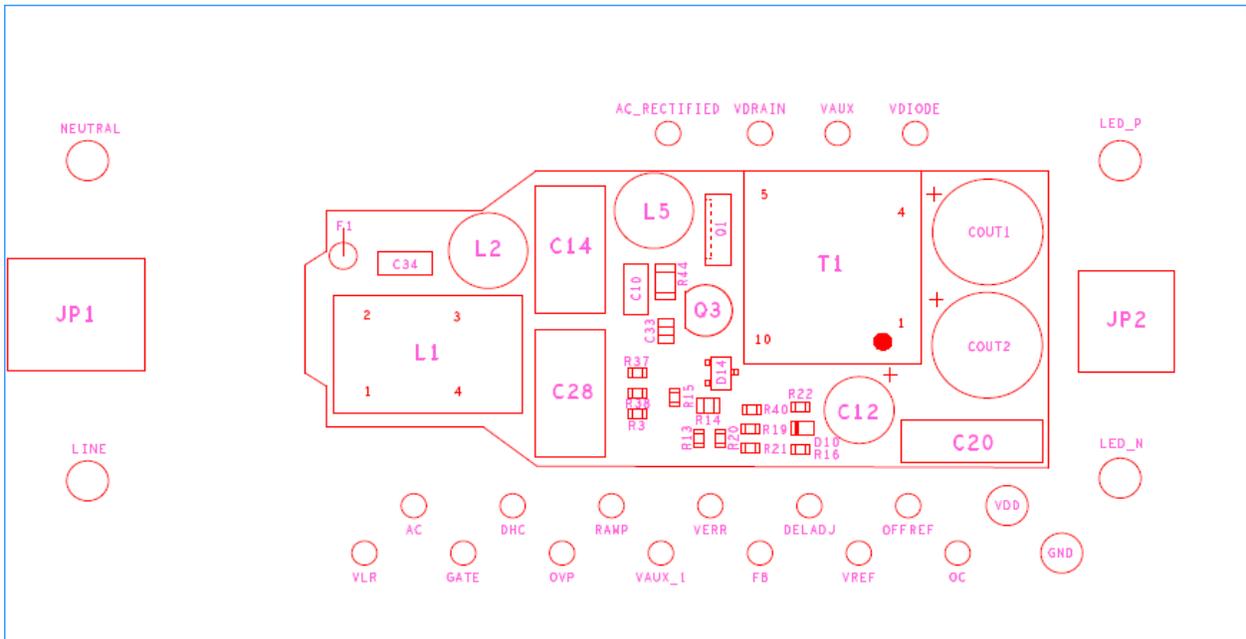


FIGURE 38. ASSEMBLY TOP

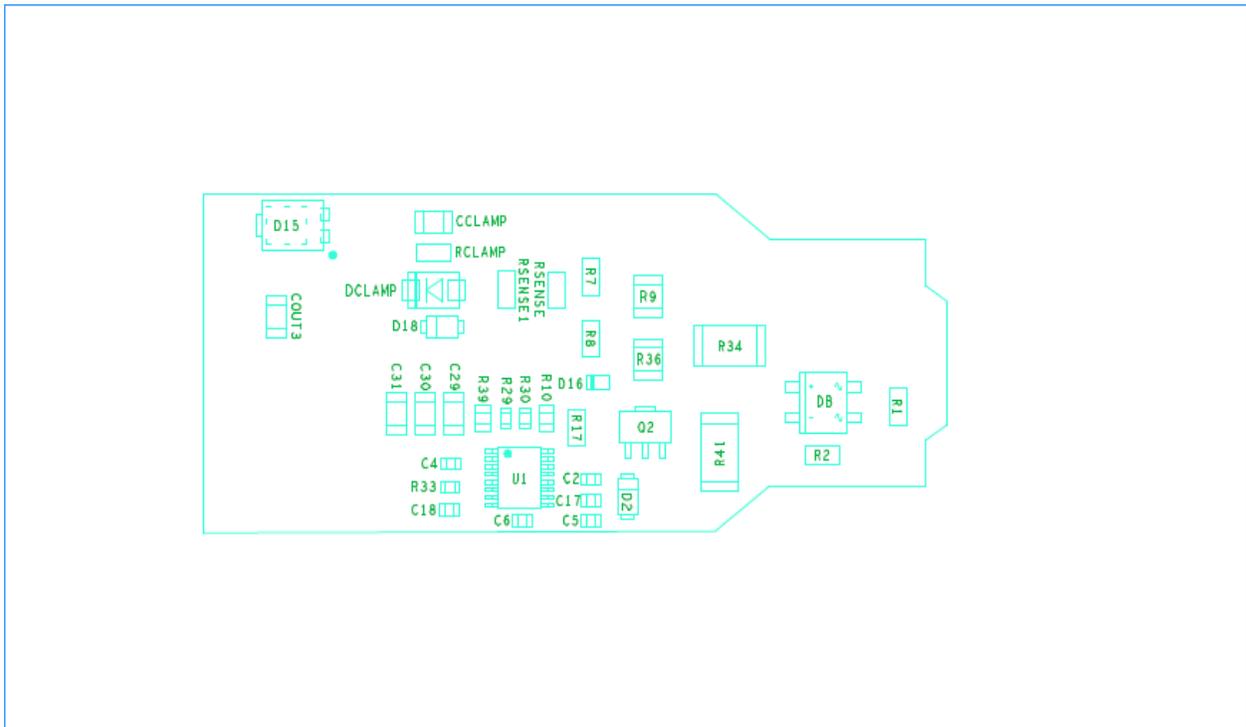


FIGURE 39. ASSEMBLY BOTTOM

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