

## Introduction

The HI5630 evaluation kit can be used to examine the performance of the HI5630 triple 8-bit analog to digital converter (ADC). The evaluation board consists of a triple ADC, latches, Digital to Analog Converter (DAC) and supporting clock circuit. The board is fabricated on a 4 layer PCB containing a top and bottom signal layers, ground and power layers. The ADC will digitize the analog input and the three latches will hold the output data until the three DACs convert the data back to analog. In addition, the digital data can be obtained via the 2x1 jumpers for use with a digital analysis system (DAS). Please refer to the functional block diagram in Figure 1.

## Evaluation Board

The HI5630 evaluation board is a four layer board with a layout optimized for the best performance of the ADC. The optimization includes segmenting the analog and digital signals to prevent digital noise from degrading the analog-to-digital conversion process. The physical board is divided into an analog and digital area with supporting analog and digital ground planes. The power supplies hook-up is detailed in Table 1.

Included in the application note is an electrical schematic of the evaluation board circuitry, a components layout, a components part list and views of the various board layers that make up the printed wiring board. Please refer to the Schematic Diagrams. The user should feel free to copy the layout in their application. Refer to the components layout and the evaluation board electrical schematics for the following discussions.

Table 1 lists the operational supply voltages for the evaluation board. Single supply operation of the converter is possible but the overall performance of the converter may degrade.

TABLE 1. EVALUATION BOARD POWER SUPPLIES

POWER SUPPLY	NOMINAL VALUE	CURRENT (TYP)	FUNCTION(S) SUPPLIED
AVDD	5.0V $\pm$ 5%	240mA	Analog power to ADC, Reference and DAC
AGND	-	-	Analog Ground
DVDD	5.0V $\pm$ 5%	80mA	Digital power to ADC, Clock, Latches and DAC
DGND	-	-	Digital Ground

## Analog Input

The analog inputs to the HI5630 are obtained via SMA connectors defined in Table 2. The inputs are terminated by a 75 $\Omega$  resistor and DC blocking capacitors. To bias the inputs at the desired 1.5 to 2.5V range the user can select via 3 terminal jumpers either the internal VDC bias voltage or an external bias derived from potentiometers. Care should be taken to ensure the inputs do not exceed the absolute maximum ratings of the ADC. For typical applications, the negative inputs are connected to the applicable V<sub>DC</sub> (2.0V)

TABLE 2. INPUT CONNECTIONS AND BIAS SELECTION

ANALOG INPUTS	SMA#	BIAS JUMPER	ADJUST POT#
R <sub>IN</sub> <sup>-</sup>	SMA6	J16	R22
R <sub>IN</sub> <sup>+</sup>	SMA3	J13	R7
G <sub>IN</sub> <sup>-</sup>	SMA7	J17	R23
G <sub>IN</sub> <sup>+</sup>	SMA4	J14	R8
B <sub>IN</sub> <sup>-</sup>	SMA5	J15	R21
B <sub>IN</sub> <sup>+</sup>	SMA2	J12	R6

NOTE: Jumpers in top position selects the external POT.

## Reference Voltage Circuit

The board can be configured to use the internal reference voltage generator or an external source via the 3 terminal J41. When the jumper is inserted in top position of J41 the internal reference is connected. If the user requires an external reference, use the center terminal for V<sub>RIN</sub> and with the bottom terminal analog ground.

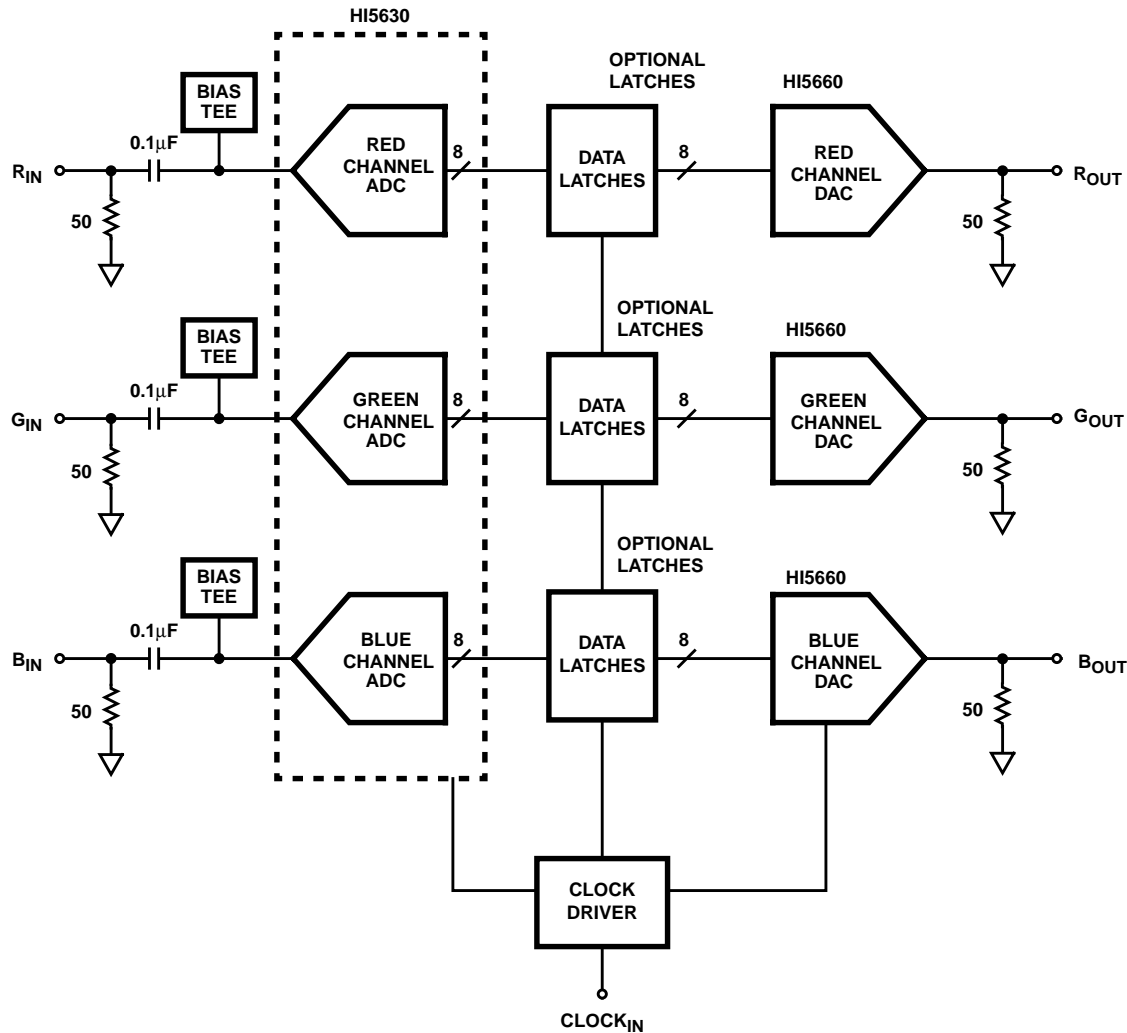


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

## Buffered Clock Driver

In order to ensure rated performance of the HI5630, the duty cycle of the sample clock should be set to 50%. It must also have low phase noise and operate at standard TTL logic levels.

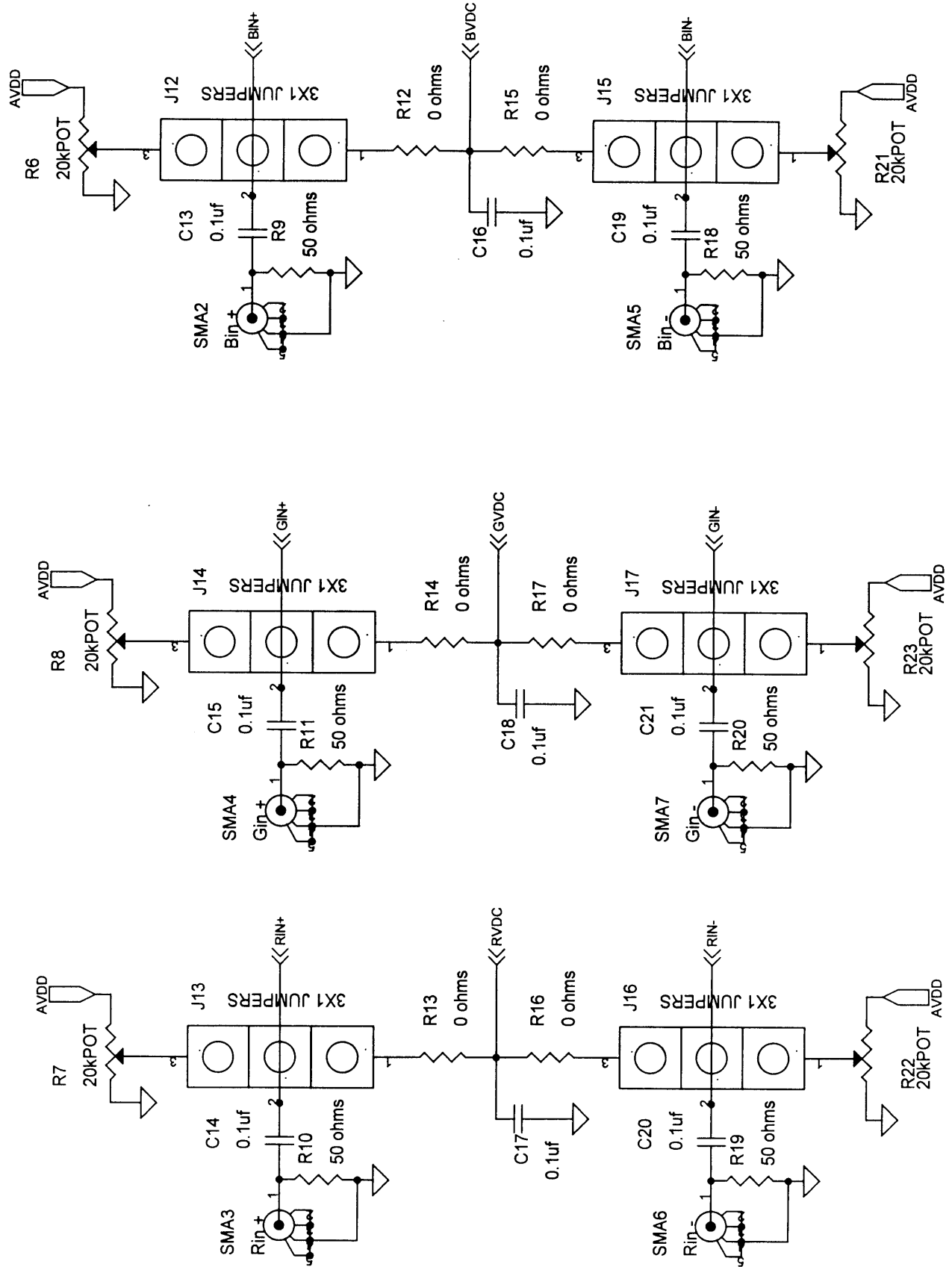
It can be difficult to find a low phase noise generator that will provide a 80MHz squarewave at TTL logic levels. Consequently, the evaluation board is designed with a logic buffer (U7) acting as a voltage comparator to generate the sampling clock for the HI5630 when a sinewave ( $\leq \pm 1.5V$ ) is applied to the CLK input of the evaluation board. The sample clock sinewave is AC coupled into the input of the inverter and a discrete bias tee is used to bias the sinewave around the trigger level of the inverter's input. The variable resistor (R35) varies the DC bias voltage added to the sinewave input allowing the user to adjust the duty cycle of the sampling clock to obtain the best performance from the ADC

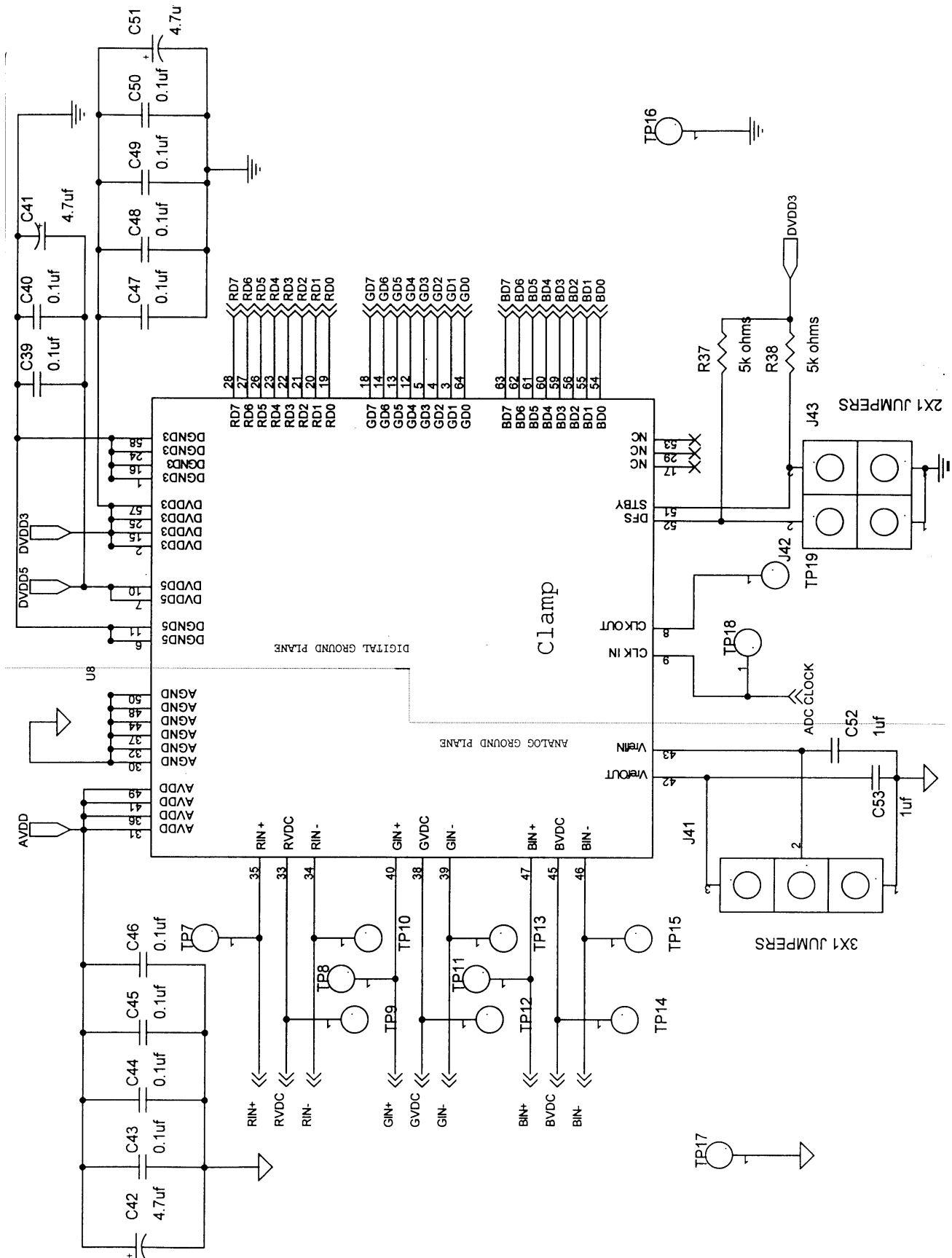
and to evaluate the effects of sample clock duty cycle on the performance of the converter. The sinewave to logic level comparator drives a series of additional buffers that provides isolation between the three sample clocks used on the evaluation board. One clock drives the ADC clock input pin (ADC CLK), a second clock drives output data latches (LATCH CLK), and the last clock provides the DAC reconstruct clock (DAC CLK).

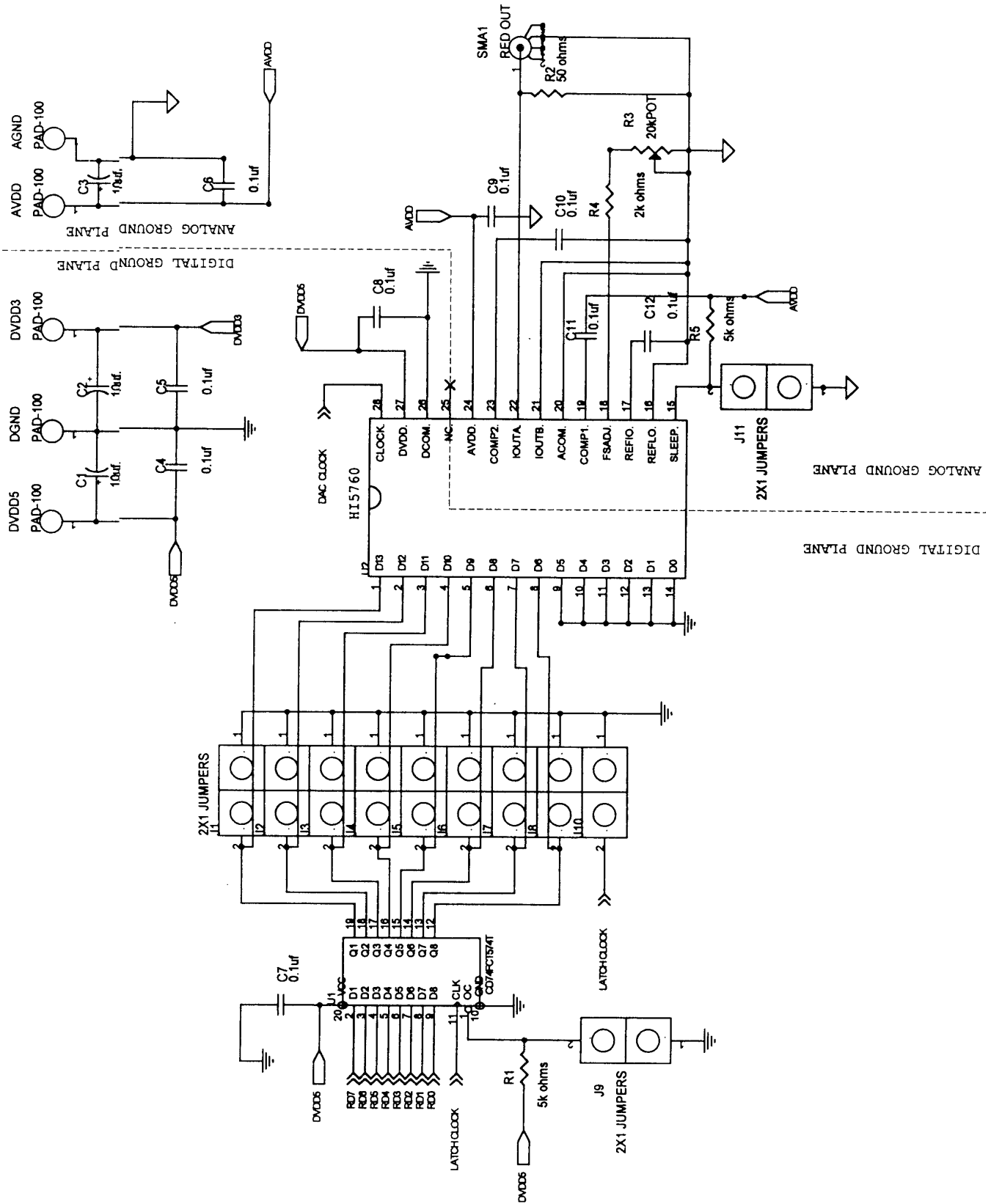
## Reconstruction DAC

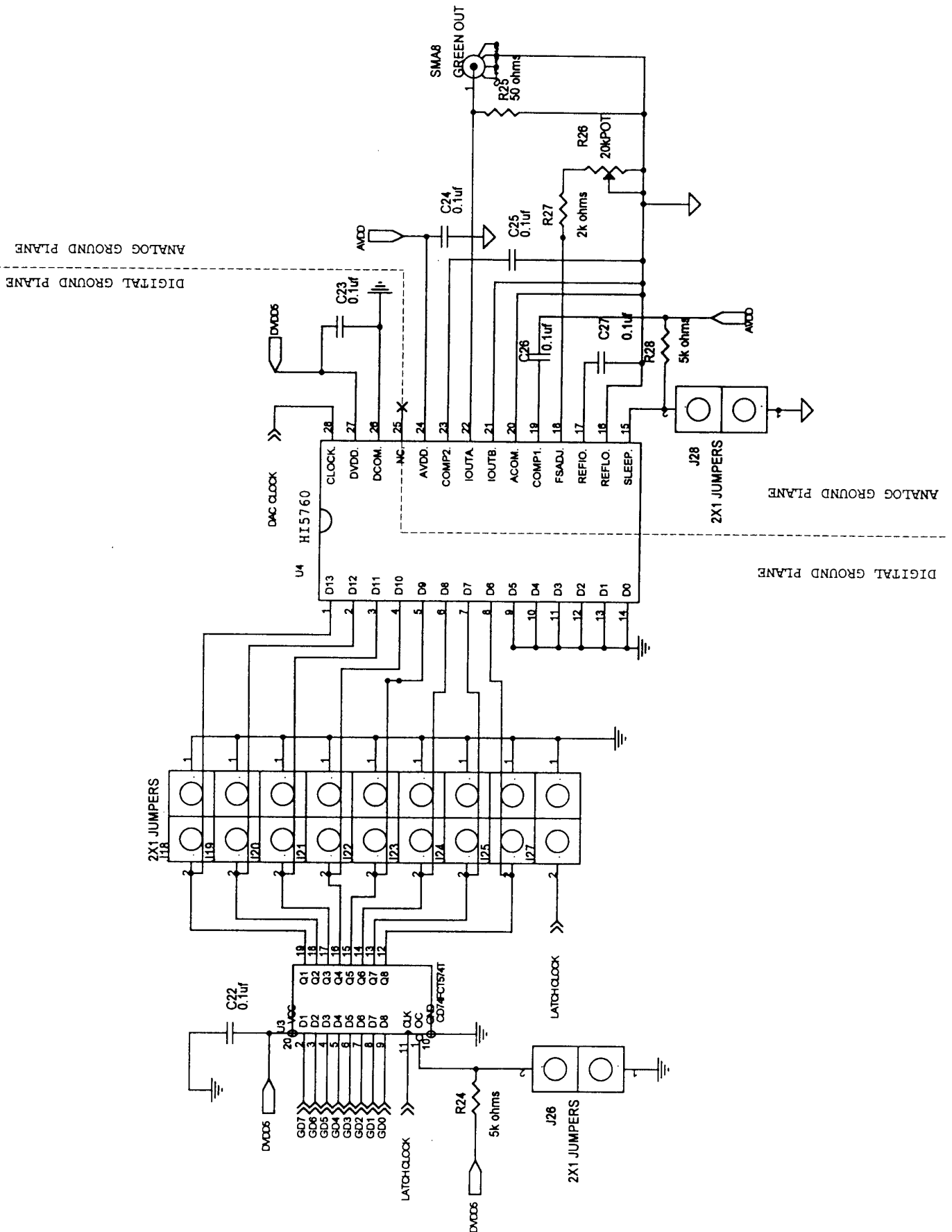
To easily verify the performance of the ADC a reconstruction DAC is provided. The 8-bit HI5660 triple DAC was selected to ensure the user measures the real ADC performance without any degradation from the reconstruct DAC. The DAC is configured to convert the latched data into a 1V fullscale output. The fullscale output can be adjusted via R3, R26 and R31.

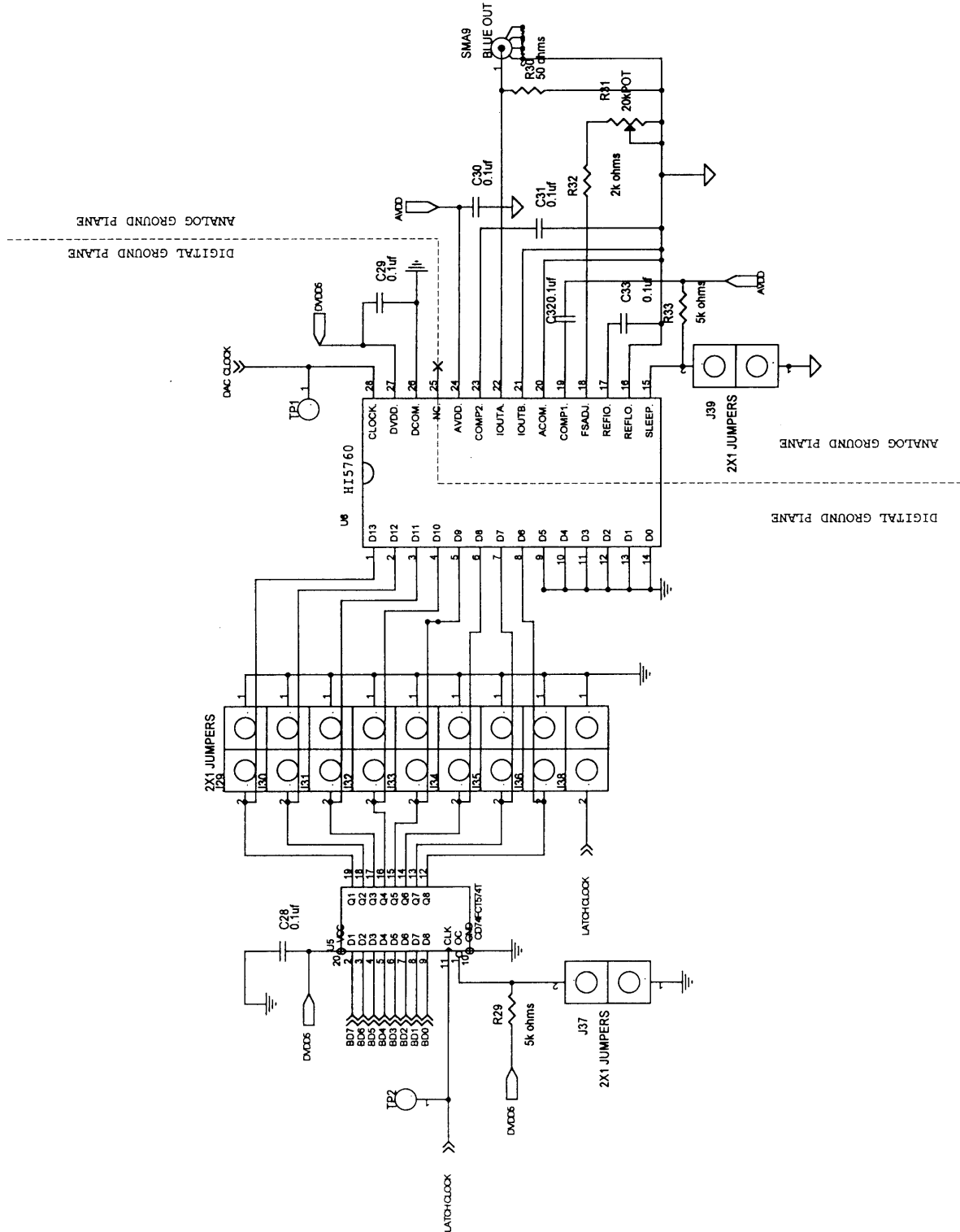
Schematic Diagrams

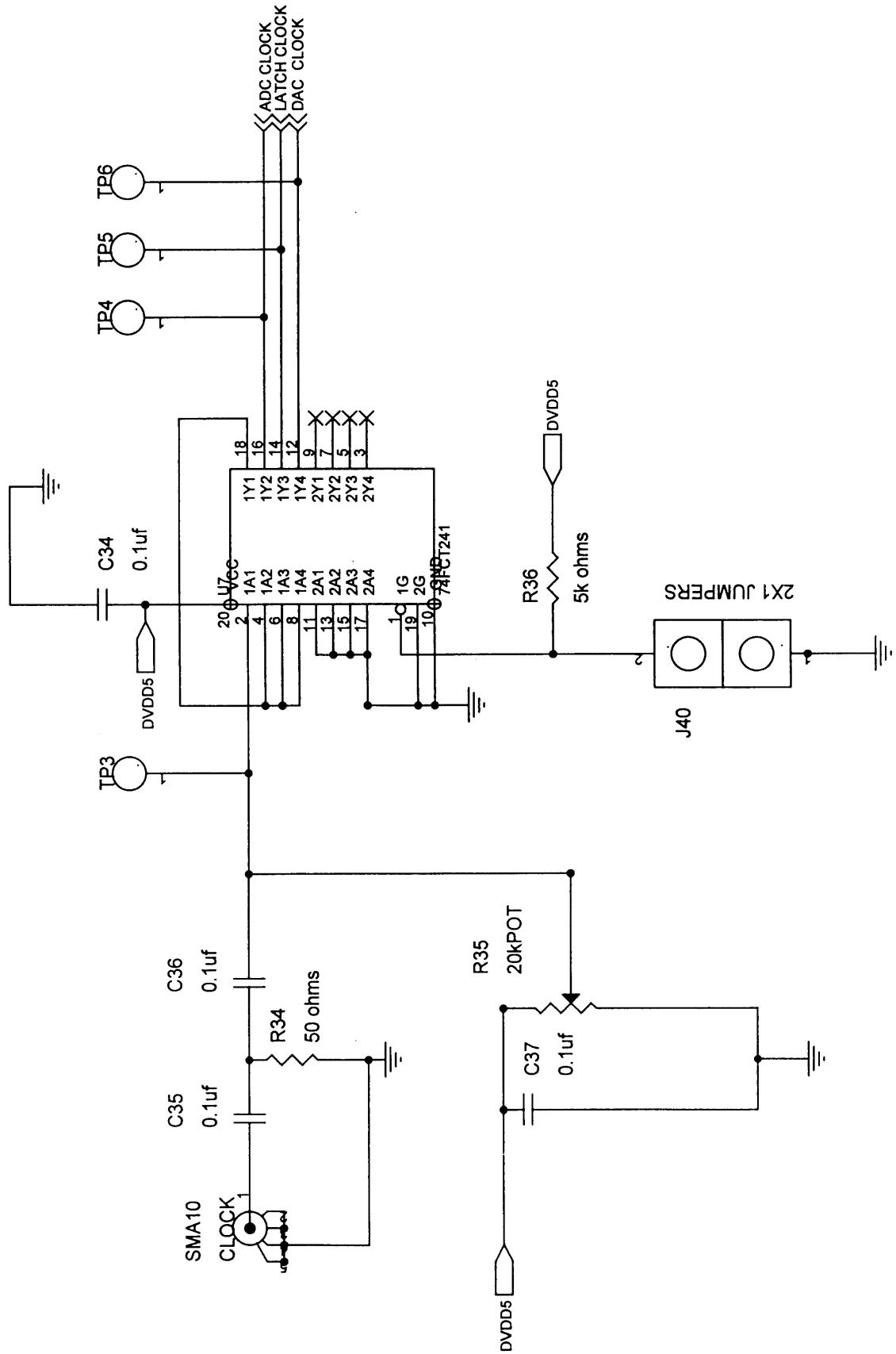














## Evaluation Board Test Procedure

1. Review this entire user manual and HI5630 data sheet.
2. If not installed at board house, affix “twisted pair” power supply wires for AVDD, AGND, DVDD and DGND. Shrink wrap three inches from the end of the power wires to prevent untwisting.
3. Check to ensure ALL jumpers are inserted per the “Golden” board. ENSURE that J2-J10, J19-J27 and J30-J38 are NOT inserted! The 2x1 header is for the DAS test head. If the jumpers are inserted the HI5630 and Clock buffer digital outputs will be shorted to ground and device damage may result.
4. Apply AVDD (5V), DVDD (5V) and Clock input (80MHz, 0.5V).
5. Check power supply current and compare to application note. (AVDD ~240mA DVDD ~ 80mA.)
6. Voltage Adjustments
  - a. Clock duty cycle via R35 to 50% (ADC CLK TP4, by U7).
  - b. If capturing the digital output data with logic analyzer (DAS), apply 0V input and adjust each input bias tee to produce the mid-scale code of 128.
  - c. Apply a 1V<sub>P-P</sub> 1MHz sine wave to each of the inputs (SMA3, SMA4 and SMA2). Adjust the D/A full scale voltage for each DAC via R3, R26 and R31 to 0.5V (SMA1, SMA8 and SMA9).
7. Red Channel (without DAS):

Apply a 1V<sub>P-P</sub> 1MHz sine wave to R<sub>IN+</sub> (SMA3).

Observe the DAQ reconstruct output to verify a clean sine wave (SMA1, by U2).

You may adjust the input bias tee voltage via R7 to center the DA sine wave.
8. Green Channel (without DAS):

Apply a 1V<sub>P-P</sub> 1MHz sine wave to G<sub>IN+</sub> (SMA4).

Observe the DAQ reconstruct output to verify a clean sine wave (SMA8, by U4).

You may adjust the input bias tee voltage via R8 to center the DA sine wave.
9. Blue Channel (without DAS):

Apply a 1V<sub>P-P</sub> 1MHz sine wave to B<sub>IN+</sub> (SMA2).

Observe the DAQ reconstruct output to verify a clean sine wave (SMA9, by U6).

You may adjust the input bias tee voltage via R6 to center the DA sine wave.
10. If the DAS system is available perform the following tests.
  - a) Adjust the input voltage until “raw code” is between 4-252.
  - b) Acquire the “loop FFT” with a minimum ENOB of 7.2 bits.

### Notes/Problems

The first boards had a hookup error on U7, the clock buffer. The error consisted of not powering the device via pin 20. The rework involves a wire between the top of C37 to the left side of C34. This applies power to the decoupling capacitor on pin 20. In addition C38 should not be installed.

**Notes**

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