

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

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To all our customers

Regarding the change of names mentioned in the document, such as Hitachi Electric and Hitachi XX, to Renesas Technology Corp.

The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Differences between the H8S/2195 Evaluation Chip and H8S/2199 Series, H8S/2199R Series

(1) Timer-J

Item	Evaluation Chip	H8S/2199 Series F-ZTAT, MASK	H8S/2199R Series F-ZTAT, MASK	Notes
Expansion function (adding the specification for bit 3 of the timer J control register (TMJC))	None*	Added	Added	H8S/2199R Hardware Manual pp. 272, 273, and 282

Note: Do not write the timer with the evaluation chip. When reading, 1 is read.

(2) Servo circuit

Item	Evaluation Chip	H8S/2199 Series F-ZTAT, MASK	H8S/2199R Series F-ZTAT, MASK	Notes
TBC selection bit (adding the specification for bit 7 of reference period mode register 2 (RFM2) in the reference signal generator)	None*	Added	Added	H8S/2199R Hardware Manual pp. 580 and 581

Note: Do not write the timer with the evaluation chip. When reading, 1 is read.

(3) OSD

Item	Evaluation Chip	H8S/2199 Series F-ZTAT, MASK	H8S/2199R Series F-ZTAT, MASK	Notes
Initial value of bit 0 of the digital output specification register (DOUT)	1 ¹	0	0	H8S/2199R Hardware Manual pp. 880 and 881
Countermeasure for malfunction of blinking target	Cursor/half tone + character + border	Character + border	Character + border	Refer to detail 1
Countermeasure for malfunction of button-frame misalignment to display the double-size character	Only button frames are shifted left by one dot.	Not shifted	Not shifted	Refer to detail 2
Countermeasure for malfunction of CVout amplitude level in the text display mode	Larger by about 20 IRE than the register setting value	Same as the register setting value	Same as the register setting value	H8S/2199R Hardware Manual p. 870

(3) OSD (cont)

Item	Evaluation Chip	H8S/2199 Series F-ZTAT, MASK	H8S/2199R Series F-ZTAT, MASK	Notes
Countermeasure for malfunction of the display when the half-tone display is out of the display area	Malfunction that the screen display is pulled horizontally	Without display malfunction	Without display malfunction	
Clearing condition of the OSDV interrupt flag	0 is written without reading 1	0 is written after reading 1	0 is written after reading 1	H8S//2199R Hardware Manual pp. 874, 875, and 876
Border display in the SECAM mode	Unnecessary color is displayed on the right of the character	Unnecessary color is not displayed on the right of the character	Unnecessary color is not displayed on the right of the character	
Initialization mode of bits 11 and 12 of the OSD register (DFORM)	Initialized at reset or low-power consumption mode (module stop, sleep, standby, watch, subactive, or subsleep)	Initialized at reset or low-power consumption mode (module stop, sleep, standby, watch, subactive, or subsleep)	Initialized at reset	H8S/2199R Hardware Manual p. 872
The number of displayed horizontal characters at double height x double width	16 characters	16 characters	32 characters	
4/2 fsc clock in the superimposed mode	Necessary	Necessary	Not necessary	
Mask area for outputting the horizontal direction display in the superimposed mode	Before the internal synchronous H (AFCH): about 3.0 μ s, after the internal synchronous H (AFCH): about 8.0 μ s	Before the internal synchronous H (AFCH): about 3.0 μ s, after the internal synchronous H (AFCH): about 8.0 μ s	Before the internal synchronous H (AFCH): about 4.0 μ s, after the internal synchronous H (AFCH): about 7.0 μ s	

(3) OSD (cont)

Item	Evaluation Chip	H8S/2199 Series F-ZTAT, MASK	H8S/2199R Series F-ZTAT, MASK	Notes
Mask area for outputting the vertical direction display in the superimposed mode	After external V detection: NTSC, 4.43 NTSC, MPAL = 16 lines, PAL, SECAM, NPAL = 22 lines	After external V detection: NTSC, 4.43 NTSC, MPAL = 16 lines, PAL, SECAM, NPAL = 22 lines	After external V detection: NTSC, 4.43 NTSC, MPAL, PAL, SECAM, NPAL = 6 lines	
Starting position of horizontal direction when HCKSEL = 1 is selected (bit 3 of the sync separation control register (SEPCR))	For the position when selecting HCKSEL = 0, shifted left about 1.7 μ s when AFC = 9 MHz, and shifted left about 1.1 μ s when AFC = 7 MHz	For the position when selecting HCKSEL = 0, shifted left about 1.7 μ s when AFC = 9 MHz, and shifted left about 1.1 μ s when AFC = 7 MHz	Same starting position as selecting HCKSEL = 0	H8S/2199R Hardware Manual pp. 775 and 776
Dot-clock source in the text display mode (adding the specification for bit 1 of the sync separation AFC control register (SEPACR))	AFC reference clock ²	AFC reference clock ²	AFC reference clock or 4/2 fsc clock	H8S/2199R Hardware Manual pp. 778 and 779

- Notes: 1. When the program is developed with the evaluation chip and this register is written, write 0 to bit 0 to maintain the program compatibility with the F-ZTAT and MASK versions.
2. Do not write 1.

(4) Sync separation circuits for OSD/data slicer

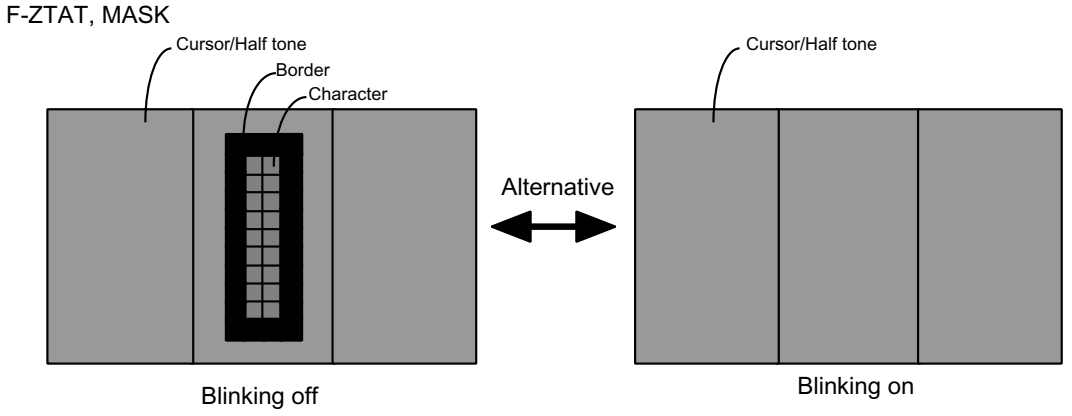
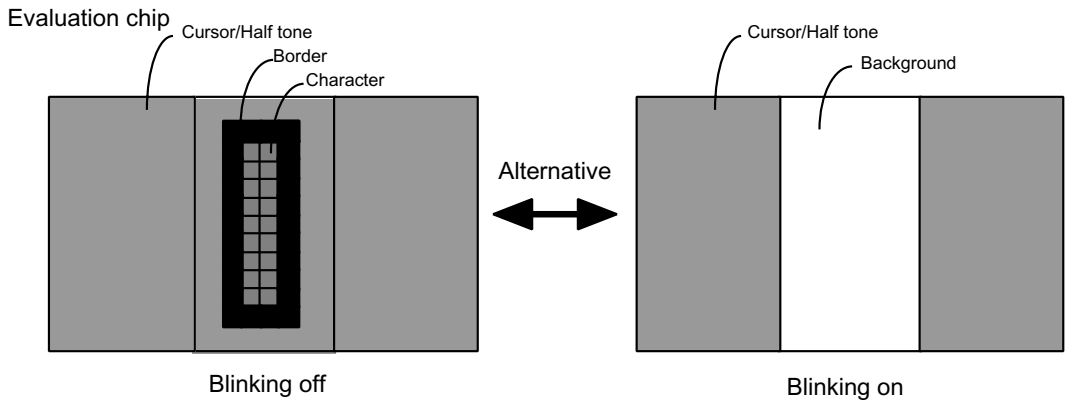
Item	Evaluation Chip	H8S/2199 Series F-ZTAT, MASK	H8S/2199R Series F-ZTAT, MASK	Notes
Internal sync frequency register (INFRQR)	None	Included	Included	H8S/2199R Hardware Manual pp. 794 and 795
Mask operation period for V complement and mask counter	NTSC, PAL: 85%	NTSC: 85%, PAL: 72%	NTSC: 85%, PAL: 72%	H8S/2199R Hardware Manual p. 801
Detecting external Vsync when the VCKSL bit is set to 1 at AFC = 7 MHz (bit 5 of the sync separation control register (SEPCR))	External Vsync cannot be detected	External Vsync can be detected	External Vsync can be detected	H8S/2199R Hardware Manual pp. 774 and 775
Initialization mode of the sync separation circuit	Initialized at reset	Initialized at reset	Initialized at reset or low-power consumption mode (module stop, sleep, standby, watch, subactive, or subsleep) (Bit 5 of SEPIMR is only initialized at reset)	
Countermeasure for malfunction when an image signal is switched in the superimposed mode	Characters are displayed three lines below of the specified line (bit 4 of SEPCR = 1), and disappeared (bit 4 of SEPCR = 0)	Characters are displayed three lines below of the specified line (bit 4 of SEPCR = 1), and disappeared (bit 4 of SEPCR = 0)	No problems	H8S/2199R Hardware Manual pp. 774 and 775
AFC operation when the ARST bit is set to 1	AFC may not be locked at power on	AFC may not be locked at power on	AFC is locked at power on	H8S/2199R Hardware Manual pp. 777 and 778
AFC operation while the unrecorded tape is being run in the text display mode	AFC is locked	AFC may not be locked	AFC is locked	

(5) Data slicer

Item	Evaluation Chip	H8S/2199 Series F-ZTAT, MASK	H8S/2199R Series F-ZTAT, MASK	Notes
Operating frequency of the data slicer (AFC reference clock)	9 MHz	9 MHz	7 MHz/9 MHz	
Bit length of the slice data (adding the specification for bit 0 of the sync separation AFC control register (SEPACR))	16 bits*	16 bits*	16 bits/32 bits	H8S/2199R Hardware Manual p. 831
Slicer operation during displaying a text (adding the specification for bit 1 of the sync separation AFC control register (SEPACR))	Cannot operate*	Cannot operate*	Operates	H8S/2199R Hardware Manual pp. 778 and 779

Note: Do not write 1.

Detail 1 Bug countermeasure for blinking target



Detail 2 Bug countermeasure for button-frame misalignment

