ClockMatrix TDC

This document explains how to use the Input and Output Time-to-Digital Converters (TDCs) in ClockMatrix devices. It is intended to complement the *ClockMatrix TDC Application Note*.

Contents

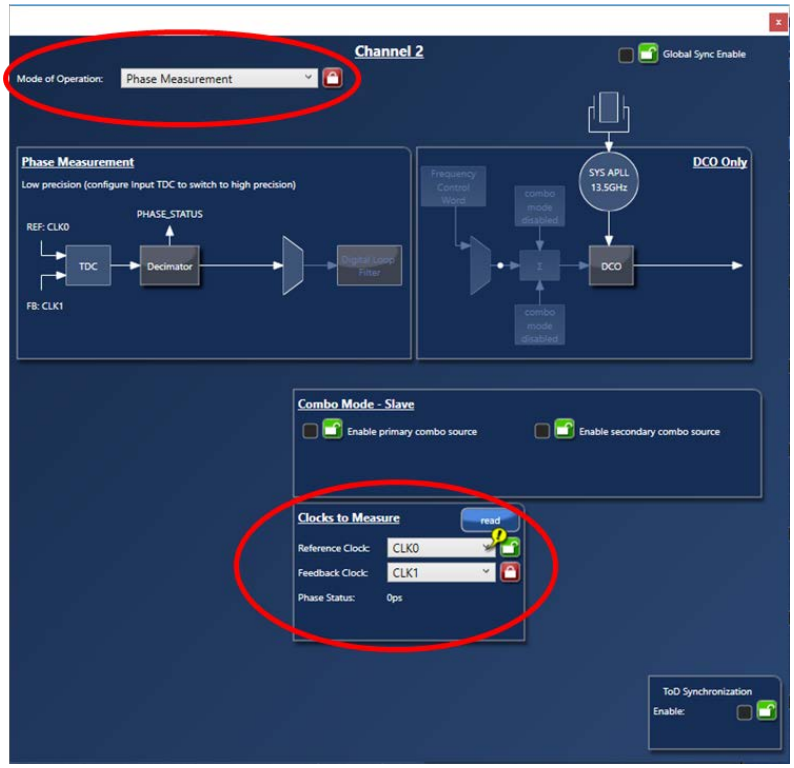
1. Input TDC

1.1 Main Screen

- Any channel can be used for Phase Measurement mode (i.e., to measure the phase between two different inputs).
- Outputs are still useable for Synthesizer or DCO (FCW) mode when in Phase Measurement mode.

1.2 CH2 Phase Measurement Mode

- Clk0 and CLK1 are used for Phase Measurement mode and must be the same frequency.
- Two types:
  - Phase Status has a resolution of 50ps.
  - Filter Status has a resolution of less than 1ps.
- Resolution is the step size.
- Filter Status is only activated when High Precision mode is enabled (see section 1.3).
- The “read” button gives the phase difference between CLK0 and CLK1.

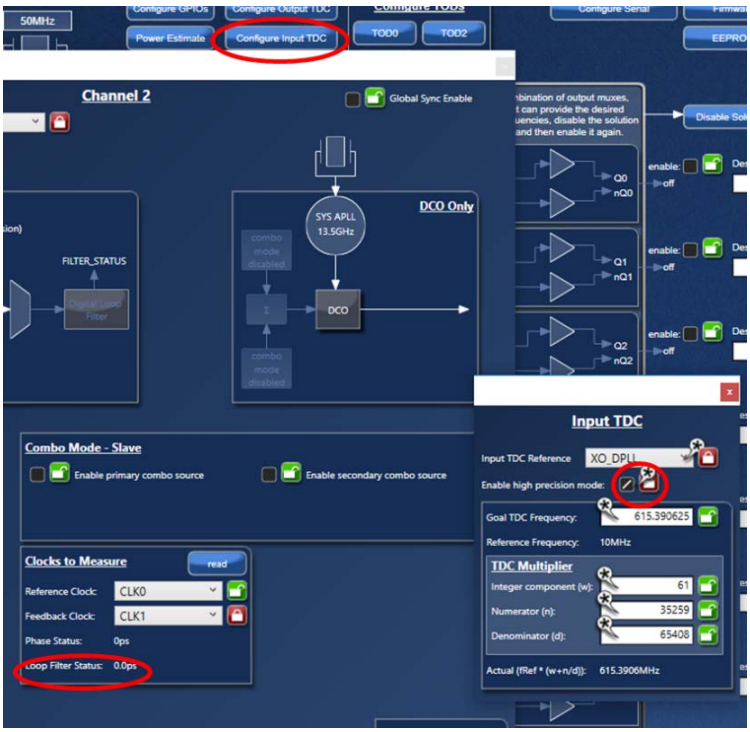


1.3 Registers

- Input TDC Reference source can use the XTAL or the XO_DPLL (if available).
- The TDC source determines the accuracy.
- For small phase offsets using phase measurement such as 1ns or 1ps, XTAL or XO_DPLL does not make a difference.
- For large phase offsets such as 1us or 1ms, XTAL or XO_DPLL makes a difference

	XTAL	XO_DPLL
Phase Offset	50 ppm	5 ppm
1.00E-03	5.00E-08	5.00E-09
1.00E-06	5.00E-11	5.00E-12
1.00E-09	5.00E-14	5.00E-15
1.00E-12	5.00E-17	5.00E-18

- Enabling High Precision mode activates Loop Filter Status for increased resolution (50ps to < 1ps).
- Resolution is the step size.
- If High Precision mode is OFF, TDC frequency is 625MHz by default.
- If High Precision mode is ON, TDC frequency is skewed such that it is not an integer multiple of the input frequency (for more information, see the *ClockMatrix TDC Application Note*).
- Enabling High Precision mode prevents DCO (FCW) access, but Synthesizer still available.



1.4 Reading a Measurement

- Enabling High Precision mode activates Loop Filter Status for increased resolution (50ps to < 1ps).
- Resolution is the step size.
- If High Precision mode is OFF, TDC frequency is 625MHz by default.
- If High Precision mode is ON, TDC frequency is skewed such that it is not an integer multiple of the input frequency (for more information, see the *ClockMatrix TDC Application Note*).
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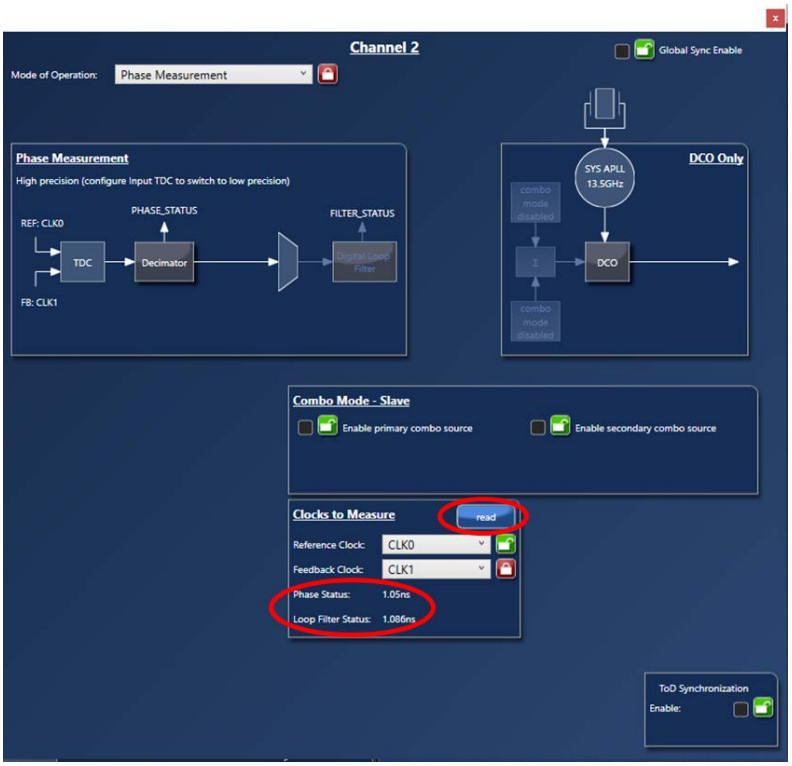
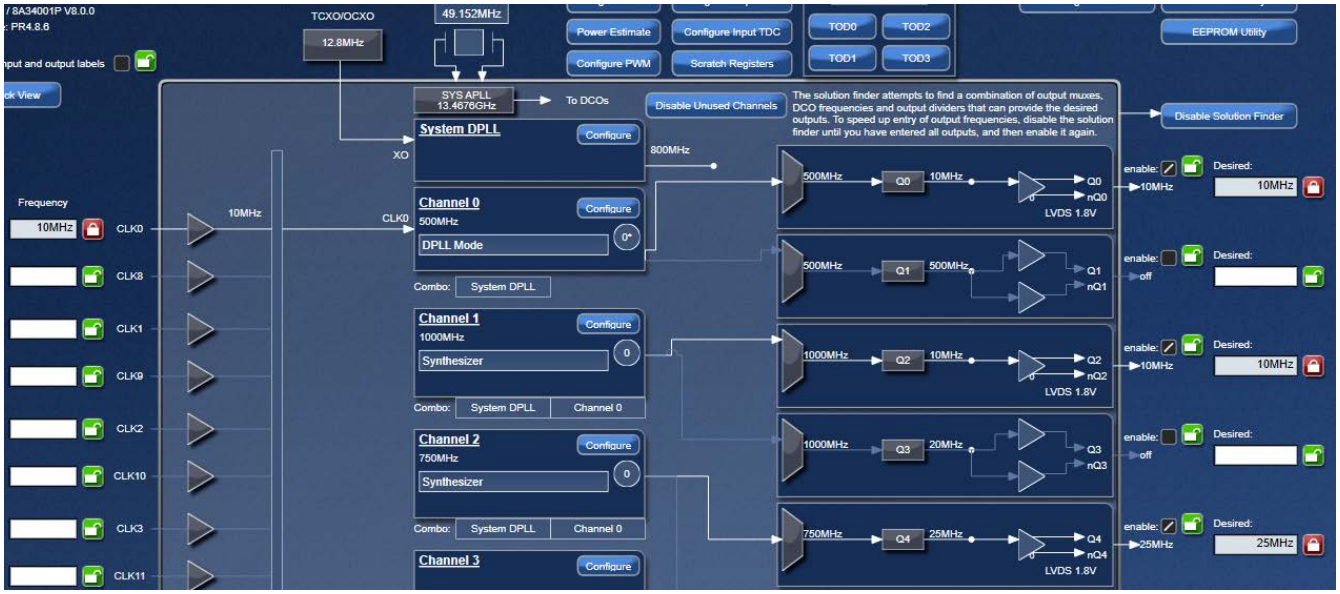


2. Output TDC

2.1 Main Screen



- Output TDCs enable output alignment of outputs from different channels.
- The example below aligns Q0, Q2, and Q4.
- Outputs from the same channel are obviously aligned and do not require a TDC: Q0 and Q1 or Q2 and Q3.

2.2 Masters and Slaves

- Master and slave satellites are assumed and are connected through the combo bus.
- Master normally has an input (Ch0):
  - DPLL mode
- Satellite slaves (Ch1 and CH2) follow the master (Ch0):
  - Synthesizer, DCO (FCW/PCW), or Phase Measurement mode
- Any stimulus on the master is propagated to the slaves through the combo mode.
- Combo mode passes only frequency (change in phase).
- Combo mode does not pass edge information.

2.3 Combo Bus

- All three Channel Combo configs are shown above.
- Ch0 has one master: sysDPLL.
- Ch1 and Ch2 have two masters each: Ch0 and sysDPLL.
- Slaves always inherit the master of its master (since Ch0 has sysDPLL as its master, Ch1 and Ch2 must also have sysDPLL as their master as well as Ch0).

2.4 Master Divider Frequency

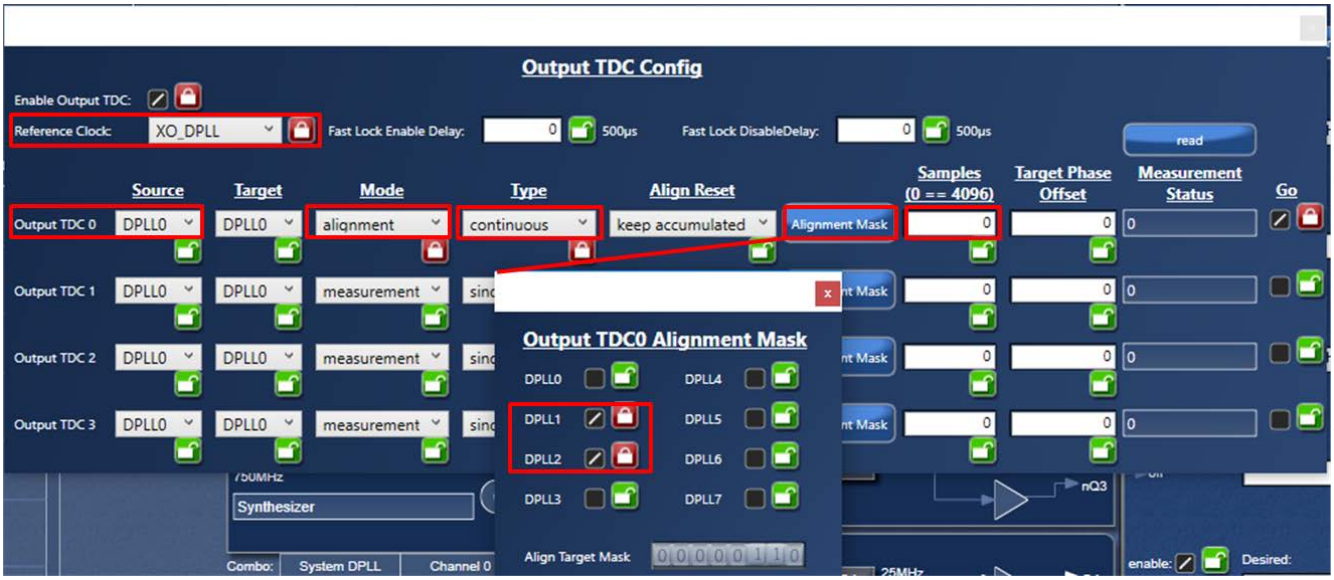
- For alignment to occur, the output of the master divider must all be the same frequency for every channel involved:
  - Ch0 MD frequency = 500MHz/100 = 5MHz
  - Ch1 MD frequency = 1000MHz/200 = 5MHz
  - Ch2 MD frequency = 750MHz/150 = 5MHz
- The higher the master divider frequency, the faster the alignment.
- The master divider frequency must be a common factor of each output frequency:
  - 5MHz is a factor of Q0 = 10MHz, Q2 = 10MHz, and Q4 = 25MHz

2.5 Global Sync Enable (GSE)

- GSE must be enabled for all channels involved.
- GSE performs the initial snap to align all outputs (coarse phase alignment).

2.6 Configuration

- Up to four different Output TDCs can be used individually.
- Output TDCs perform fine phase alignment.
- The Enable and Go buttons must be checked. Order is not important if saving to a TCS file. If connected to a device, the Go button must be last button clicked in entire box.



- Reference clock: XO_DPLL or XTAL. Select XO_DPLL for better accuracy, if possible.
- Source: DPLL0 is the Source (master) in this example.
- Mode: choose Alignment ode to align all slaves.
- When Alignment mode is chosen, Target is ignored and Alignment Mask selects the slaves.
- Measurement mode is for measuring the phase between the Source and Target.
- Type: Select continuous for continuous alignment instead of a single alignment.
- Samples: 0 selects 4096 samples.
  Note: More samples means more averaging.

2.7 Visuals

- 0* indicates the Source for Output TDC 0.
- 0 indicates the Alignment Mask Slaves for Output TDC 0.

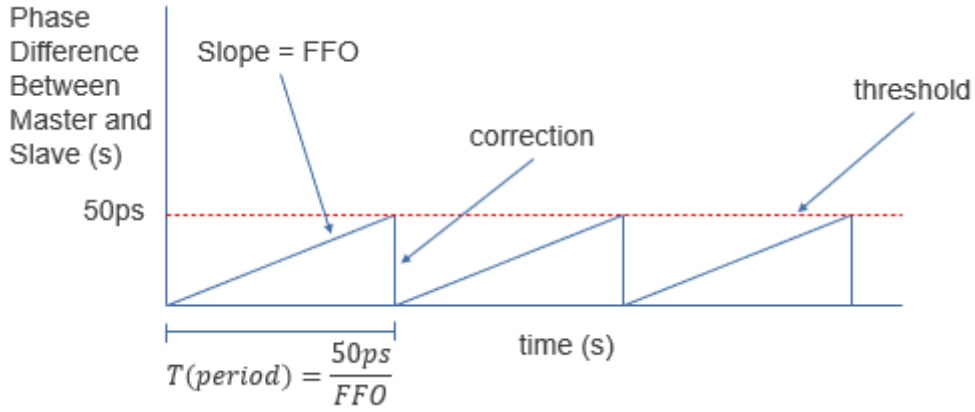
2.8 Initial Alignment Time (Single Shot)

$$Time_{Output\ TDCAlign} = \frac{N_{samples}N_{slaves}}{\min(10kHz, MDF)}$$

The equation calculates the initial alignment time (single shot mode):

- Subsequent alignments (continuous mode) are not included
- $N_{samples}$ is the number of samples used for averaging
- MDF is the Master Divider Frequency
- N_{slaves} is the number of slaves or satellites being used
- Global Sync Enable (GSE) is assumed to be enabled
- GSE performs initial coarse phase adjustment (large output jumps)
- Output TDC performs fine phase adjustment (small output jumps)
- Output TDC Status Register will report when the alignment is done, but that time may be 2x the above time if samples have an average above the threshold of 50ps

2.9 Phase Correction



- TDC mechanism only adjusts the phase of the satellite channel when it drifts by more than 50ps.
- The 50ps threshold is fixed
- Truncation error when DCO frequencies are different can be up to 0.0032ppt, which would mean a correction every 4.3 hours. In reality the truncation error can be smaller depending on actual DCO frequencies.
- The correction happens at a maximum speed of 244ppm or 244 us/s.

3. Revision History

Revision	Date	Description
1.00	Nov 23, 2022	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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