8V19N88x Hardware Design

This document provides general board-level design guidelines for the 8V19N88x JESD204B/C jitter attenuator family (see Table 1). The guidelines use the 8V19N882 device as an example and can be applied to other members of the family.

Table 1. 8V19N88x JESD204B/C Jitter Attenuator Family

Part Number	Built-in VCO Frequency	External VCO Frequency Range	Number of Input	Number of Output	Package
8V19N880	~3.93216GHz	700MHz to 6GHz	4	18	100-CABGA
8V19N882	~3.93216GHz	700MHz to 6GHz	2	16	76-VFQFN

This document will recommend the power rail handling, loop filter calculations, and input/output termination. A general schematic example is shown in Figure 2.

Contents

Figure 1 shows a simplified block diagram of the 8V19N882: it represents the core functionality of all devices in the family. More detailed and individual block diagrams and device descriptions are available in the respective device datasheets.

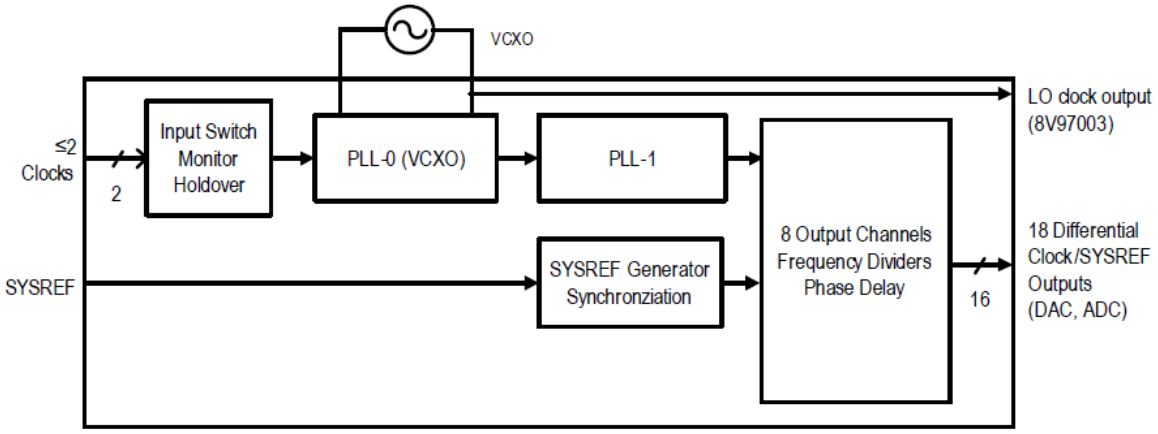

Figure 1. 8V19N882 Simplified Block Diagram

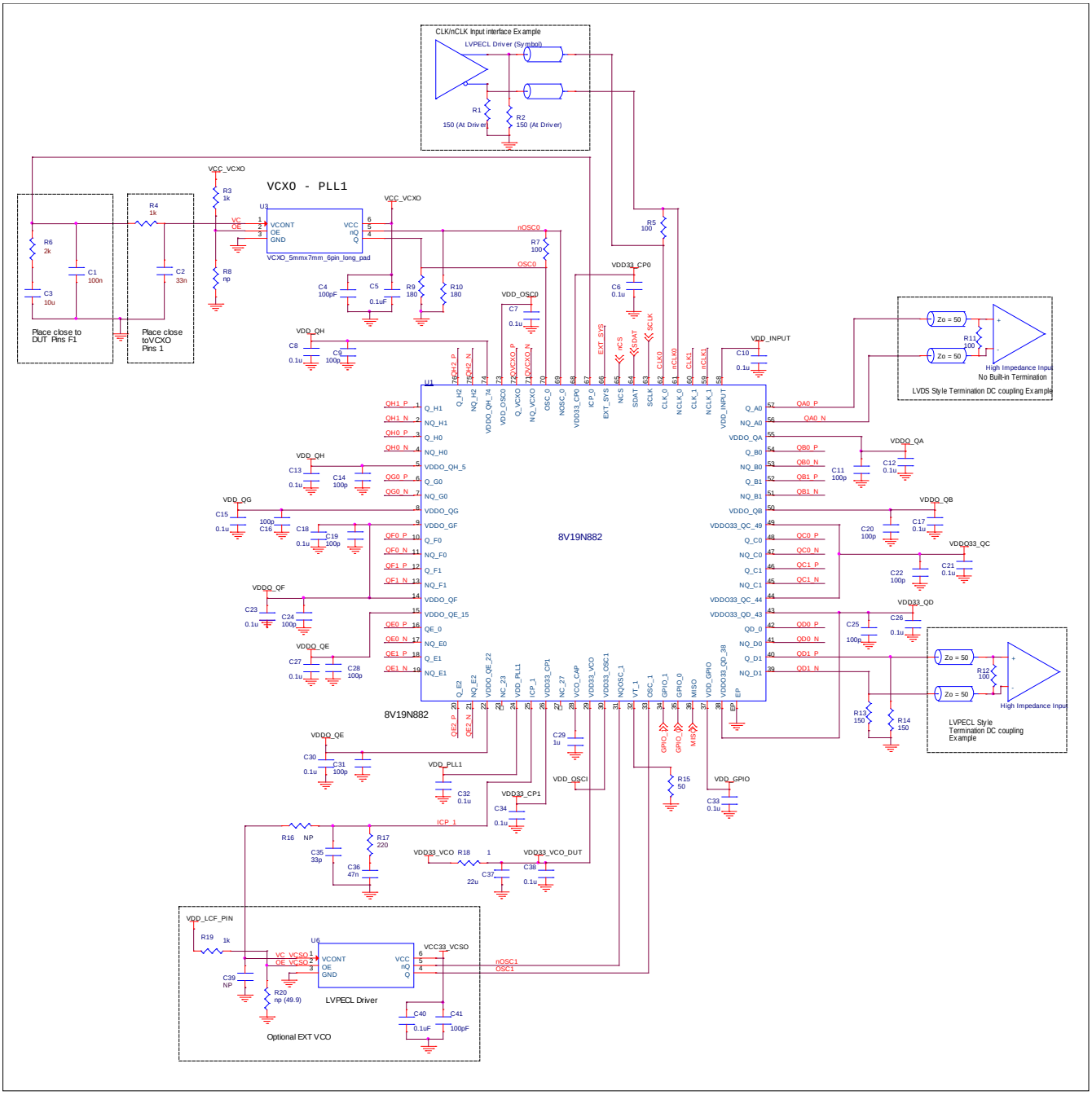

Figure 2. 8V19N882 Reference Schematic Example

Note: PCB layout files and schematics files will be provided upon request.

1. Power Rails

1.1 Bypass capacitors

Bypass capacitors are required to filter noise from switching power supplies and from other devices in the system to avoid signal interference. Figure 2 shows examples of bypass capacitors on the schematic. The type of bypass capacitor will depend on the noise level and noise frequencies on the application board. The device output driver switching can also cause power rail noise and interference with noise signals from other devices on the board, causing unwanted spurious tones in output signals. The bypass capacitors minimize these noise sources.

The bypass capacitor values are usually in the range from 0.01µF to 0.1µF. Other values can also be used. Typical capacitor sizes are 0603, 0402, or 0201 with a low ESR. The dielectric types are typically X5R or X7R. A smaller size allows the capacitor to be placed closer to the power pin of the device with a reduced trace length.

To minimize ESR between power pins and the bypass capacitors, it is recommended to place at least one bypass capacitor at each VDD power pin, with a placement as near as possible to the respective power pin of the device. A thick trace width between the bypass capacitor and the power pin helps to reduce ESR. It is recommended to combine multiple capacitors at different resonance frequencies to achieve a band pass filter characteristics at the critical noise frequencies.

1.2 Power Supply Isolation

The power rails should be as noise free as possible to support the low-phase noise performance of the device PLLs. The 8V19N88x devices also integrate LDOs for additional noise filtering. An external ultra-low noise LDO may not be required but is recommended for reducing power supply noise further. The power pins with the highest noise sensitivity is VDD_LCF. The power supply for the external VCXO must also be filtered as much as possible. An LDO should have a noise level of less than 6.5uVrms from 10Hz to100kHz. The Renesas RAA214020 is a suitable LDO and has been verified as a power supply circuit for the 8V19N88x and for the external VCXO.

It is recommended to isolate the analog power rail from other high-noise power rails, VDDO_x and VDD_INPUT. The isolation can be implemented through an RC low-pass filter. The larger RC component values can reduce the cutoff frequency further and clean up lower frequency noise. For the output supplies VDDO_x, to reduce output frequency interference, the power rails between the output banks that operate at different output frequencies can be isolated using separate LDOs or using 1 to 2 ohm resistors if they share the same power source. Additional smaller value capacitors (e.g., 100pF) in parallel with the existing 0.1µF near the power pins can provide additional higher frequency noise filtering.

2. Loop Filter

2.1 2nd Order Loop Filter

This section discusses design information for a 2nd order loop filter for PLL. Figure 3 shows a typical 2nd order loop filter. It also provides a step-by-step calculation to determine Rs, Cs, and Cp values. The required parameters for this part are also provided. A spreadsheet or software tool for calculating the loop filter values are also available.

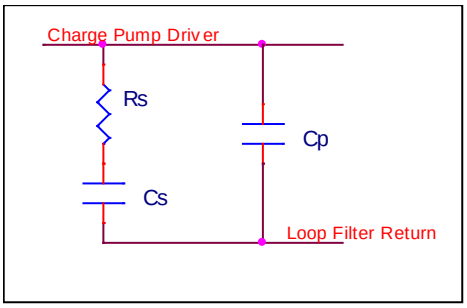

Figure 3. Typical 2nd Order Loop Filter

1. Determine desired loop bandwidth fc. The fc must satisfy the following condition:

$$\frac{Fpd}{fc} >> 20$$

Where, Fpd is phase detector input frequency.

2. Calculate Rs

$$Rs = \frac{2 * \pi * fc * N}{Icp * Kvco}$$

Where,

Icp is charge pump current.

Kvco is VCO gain.

N is effective feedback divider.

$$N = \frac{Fvco}{Fpd}$$

Fvco is vco frequency.

Fpd is the phase detector input frequency.

3. Calculate Cs

$$Cs = \frac{\alpha}{2 * \pi * fc * Rc}$$

Where,

α is ratio between loop bandwidth and the zero frequency at zero, α = fc / fz, recommend α greater than 3.

fz is frequency at zero.

4. Calculate Cp

$$Cp = \frac{Cs}{\alpha * \beta}$$

Where,

β is ratio between frequency at pole and loop bandwidth, β = fp / fc, recommend β greater than 3.

fp is frequency at pole.

5. Verify maximum Phase Margin, PM

$$PM = \arctan(\frac{b-1}{2*\sqrt{b}})$$

Where,

$$b = 1 + \frac{Cs}{Cp}$$

PM should be greater than 50 degrees.

2.2 3rd Order Loop Filter

This section provides design information for a 3rd order loop filter. A typical 3rd order loop filter is shown in Figure 4.

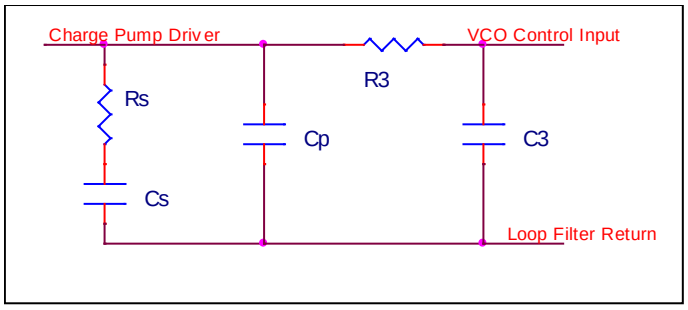

Figure 4. Typical 3rd Order Loop Filter

The Rs, Cs, and Cp can be the actual value used in the 2nd order loop filter. The following equation helps determine the 3rd order loop filter R3 and C3.

Pick an R3 value. Suggest R3 ~ 1.5xRs

$$C3 = \frac{Rs * Cp}{R3 * \gamma}$$

Where,

γ is ratio between the 1st pole frequency and the 2nd pole frequency. Suggest γ greater than 3.

The Timing Commander software tool is provided to calculate the loop filter component values. To use the spreadsheet, you can enter the follow parameters:

fc, Fpd, fvco, α, and β.

The software tool will provide the component values, Rs, Cs, and Cp as result. The spreadsheet will also calculate maximum phase margin for verification.

The 3rd order loop filter R3 and C3 is also calculated using the actual 2nd order loop filter components values.

2.3 Loop Filter Calculation Examples

2.3.1. Loop Filter for VCXO PLL

2.3.1.1. Second Order Loop Filter for the VCXO PLL

This section provides a calculation example for the VCXO PLL loop filter value. The 8V19N88x VCXO phase lock loop block diagram is displayed in Figure 5. A 2nd order loop filter for VCXO is displayed in Figure 6. In this example, the reference CLK input frequency is 30.72MHz and a VCXO with output frequency of 122.88MHz is used.

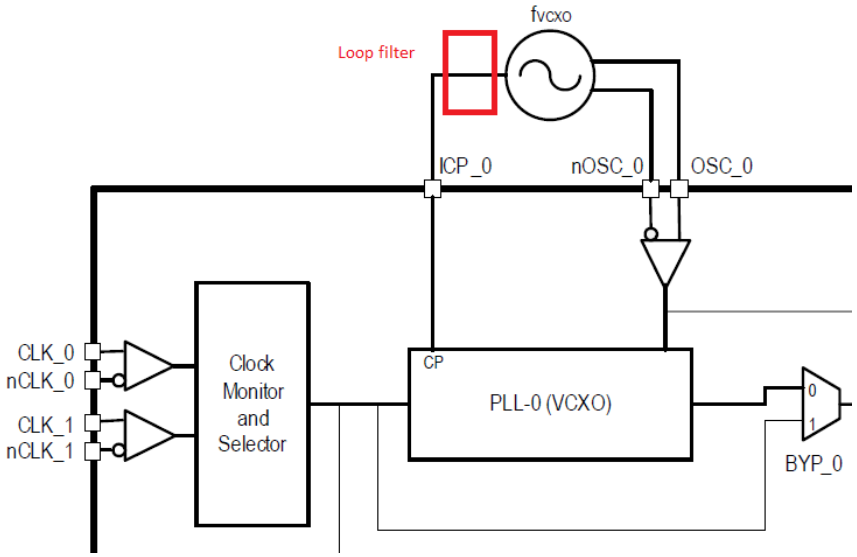

Figure 5. 8V19N88X VCXO Phase Lock Loop Block Diagram

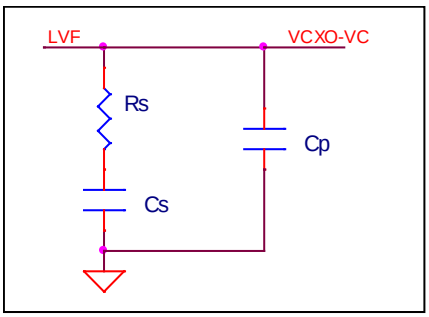

Figure 6. Typical 2nd Order Loop Filter

To calculate loop filter component values for loop bandwidth Fc = 40Hz with the reference CLK input frequency equals to 30.72MHz, set input pre-divider Pv = 16. The phase detector input frequency Fpd = 0.96MHz. This satisfies the condition of:

Fpd/Fc >> 20.

The VCXO frequency Fvcxo=122.88MHz, the effective feedback divider

N = Mv = Fvcxo / Fpd = 128

Rs can be calculated from the equation,

$$Rs = \frac{2 * \pi * fc * N}{Icp * Kvco}$$

Rs = 2.2k Ohm

Kvco VCO gain can be found or derived from the VCXO datasheet. The VCO gain can also be measured from lab experiment. In this example, we use Kvco = 10kHz/V.

The 8V19N88x charge pump current can be set up to 3mA from 100uA or 200uA and I_ICP0_OFFSET registers. In this example, assume the charge pump current is programmed to Icp0 = 1.5mA.

Cs can be calculated from the following equation,

$$Cs = \frac{\alpha}{2 * \pi * fc * Rc}$$

For α = 3, Cs is calculated to be 5.6µF. Cs greater than this value can be used to assure that the α is greater than 3. For example, the actual chosen value can be 10µF from a standard capacitor value.

Cp can be calculated from the equation,

$$Cp = \frac{Cs}{\alpha * \beta}$$

For β = 4, Cp is calculated to be 463nF. Less than this value can be used for Cp to guarantee that the β is greater than 4 (e.g., actual chosen value Cp can be 330nF).

2.3.1.2. Third Order Loop Filter for the VCXO PLL

This section helps design a 3rd order loop filter for 8V19N88x VCXO PLL. A general 3rd order loop filter is displayed in Figure 7.

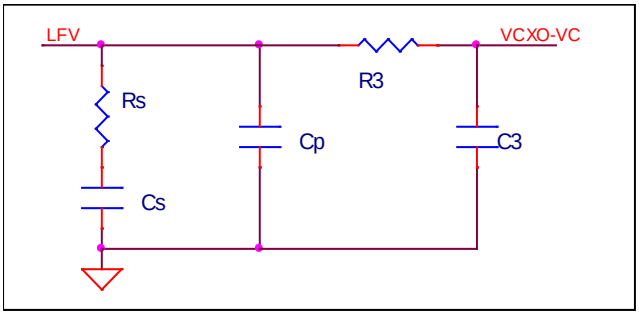

Figure 7. Typical 3rd Order Loop Filter

The Rs, Cs, and Cp are actual chosen standard values from the 2nd order loop filter. In this example, the actual chosen values are Rs = 2.2k Ohm, Cs = 10µF, and Cp = 330nF. The following equation will help determine the 3rd order loop filter R3 and C3.

Pick an R3 value. Suggest R3 ~ 0.5xRs to ~2.5xRs or greater (e.g., R3 = 2.2k Ohm is used in this example). C3 can be calculated using the following equation,

$$C3 = \frac{Rs * Cp}{R3 * \gamma}$$

Pick γ = 4 in this example

C3 is calculated to be 82.5nF. A smaller standard capacitor value can be used.

Table 2 shows some VCXO PLL Loop Filter examples for different VCXO frequencies. Other values can also be used to meet other specific conditions and requirements.

Table 2. VCXO PLL Loop Filter Examples

VCXO Frequency[1]	122.88MHz	30.72MHz
VCXO Made/Model examples	Epson,VG4513CA/CB Epson VG3225EFN Crystek CVPD922 Crystek CHPD950 Crystek CVPD-037 Rakon RVX7050M TXC Vectron	Epson, TXC, Rakon
Typical VCXO gain, Kvco	10k Hz/V	2.5k Hz/V
Loop Band width, Fc	~40Hz	~40Hz
PDF, Phase Detector input Frequency	960kHz	960 kHz
Feedback Divider (N or Mv)	128	32
Charge pump current setting **(Can be slightly Adjusted to change the loop band width)**	1500uA	1500uA
Rs	2.2k Ohm	2.2k Ohm
Cs	6.8µF	6.8µF
Cp	330nF	330nF
R3	2.2k Ohm	2.2k Ohm
C3	33nF	33nF

1. Other VCXO frequencies can also be used with proper loop filter and parameter settings. The following list are examples of VCXO order information:
   * 122.88MHz - Epson VG3225EFN 122.88M-CJHHBA
   * 245.76MHz - Epson VG3225ENN 245.76M-CJHHMA
   * 491.52MHz - Epson VG3225ENN 491.52M-CJGHSA

2.3.2. Loop Filter for VCO PLL

The 8V19N88x VCO phase lock loop diagram is displayed in Figure 8. The internal VCO frequency Fvco is 3.93216GHz. In this example, the 3.93216GHz VCO is used. A 2nd order loop filter for the VCO is displayed in Figure 9.

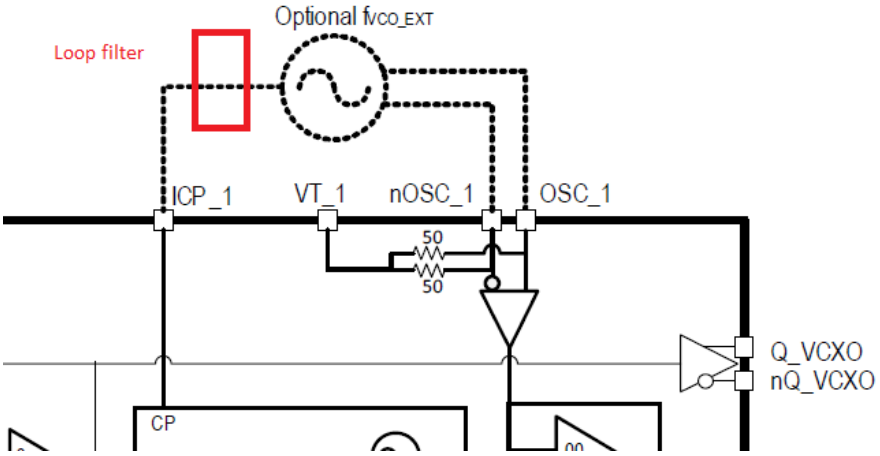

Figure 8. VCO PLL Block Diagram

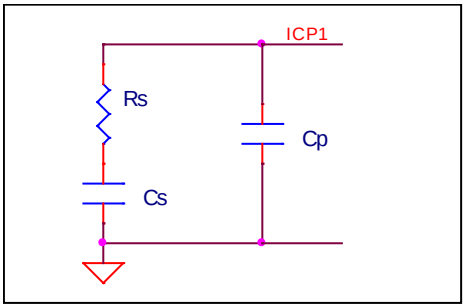

Figure 9. 2nd Order Loop Filter for the VCO

The board-level VCO 2nd order loop filter works in conjunction with the internal circuitries. A traditional loop filter calculation method cannot be used. The external 2 pole loop filter value examples are provided in Table 3.

Table 3. VCO PLL 2nd Order Loop Filter Example

VCXO used in the VCXO PLL	122.88MHz	30.72MHz
PDF, Phase detector input frequency with doubler on	245.76MHz	61.44MHz
Feedback divider	16	64
Suggest Charge pump current setting	~ 1.5 ma (typical) Suggest range setting 400ua to 3 ma	~1.5ma (typical) Suggest range setting 400ua to 3 ma
Rs	220 Ohm Suggest range (100 – 1k Ohm)	560 Ohm Suggest range (100 to 1k Ohm)
Cs	47nF	47nF
Cp	~ 33pF	~ 33pF

3. Input Output Interface

3.1 Input Termination for Reference Clock Input

The 8V19N882 reference clock input CLK/nCLK is a high-impedance differential receiver. The inverting input nCLK has weak bias to 1.2V. The input can accept a signal from a standard 3.3V LVPECL or an LVDS driver directly without AC coupling. The board-level termination at the CLK/nCLK input is determined by the driver type. Figure 10 and Figure 11 provide examples of input interface without AC coupling. Figure 12 and Figure 13 provide examples of input driven by a differential driver with AC coupling. This section provides only few examples. Other termination topologies can also be used.

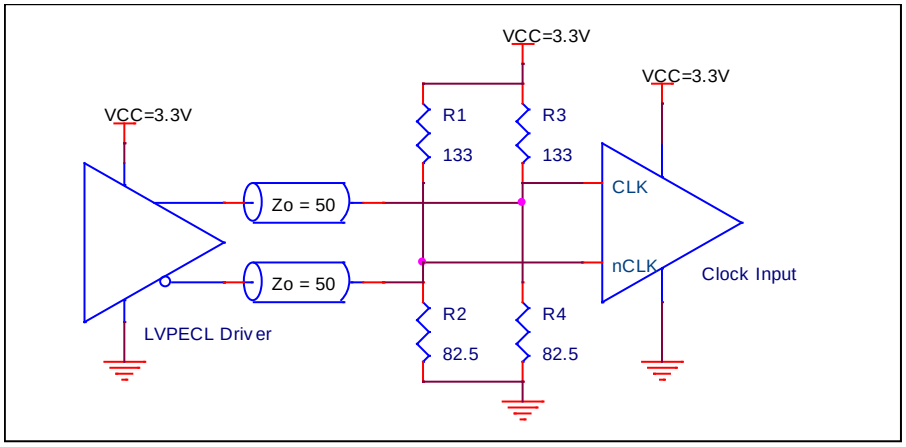

Figure 10. Input Termination Example – 8V19N882 Reference Clock Input CLK/nCLK, Driven by a 3.3V LVPECL Driver

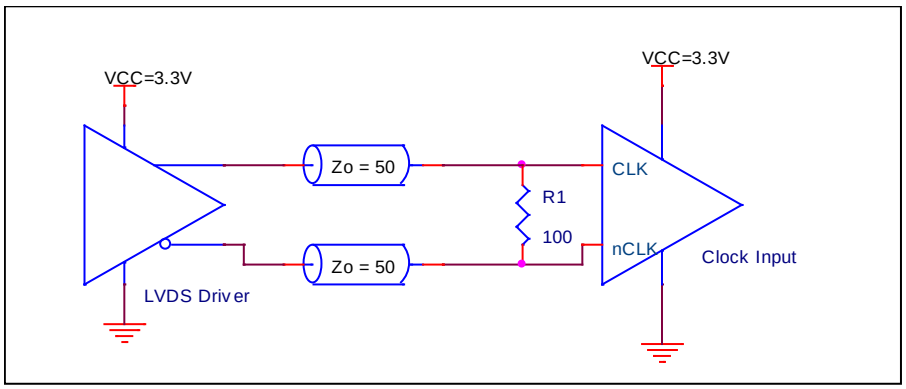

Figure 11. Input Termination Example – 8V19N882 Reference Clock Input CLK/nCLK Driven by a 3.3V LVDS Driver

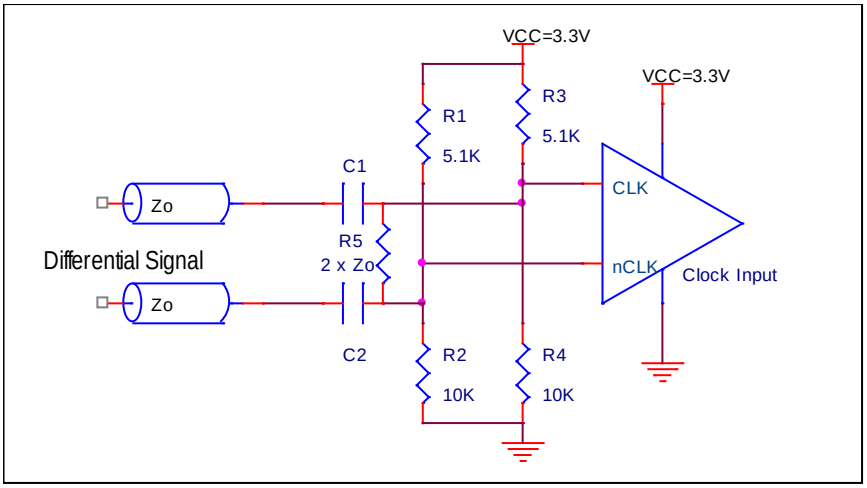

Figure 12. 8V19N882 Reference Clock Input CLK/nCLK AC Coupling Termination Example 1

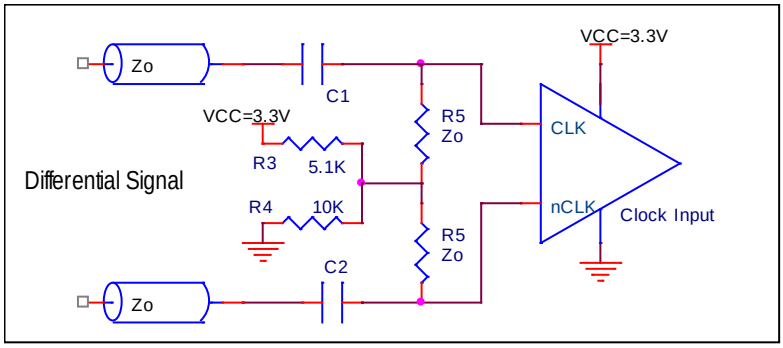

Figure 13. 8V19N882 Reference Clock Input CLK/nCLK AC Coupling Termination Example 2

3.2 OSC_1 Input Termination (External VCO)

The differential OSC_1/nOSC_1 input is used in applications with an external VCO as oscillator for PLL-1. For signal termination of the external VCO, the OSC_1/nOSC_1 input has two built-in 50Ohm termination resistors with its junction connected to the VT_1 pin. The external VCO can have a differential LVPECL, LVDS, or single-ended sinusoidal waveform output driver. See below for recommended interfaces.

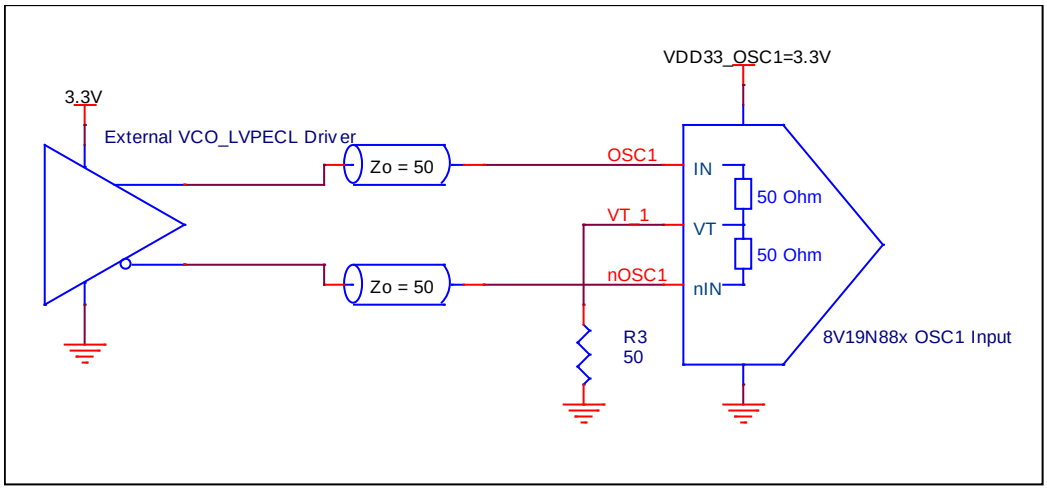

Figure 14. External VCO 3.3V LVPECL Driver to OSC_1/nOSC_1 Input Interface

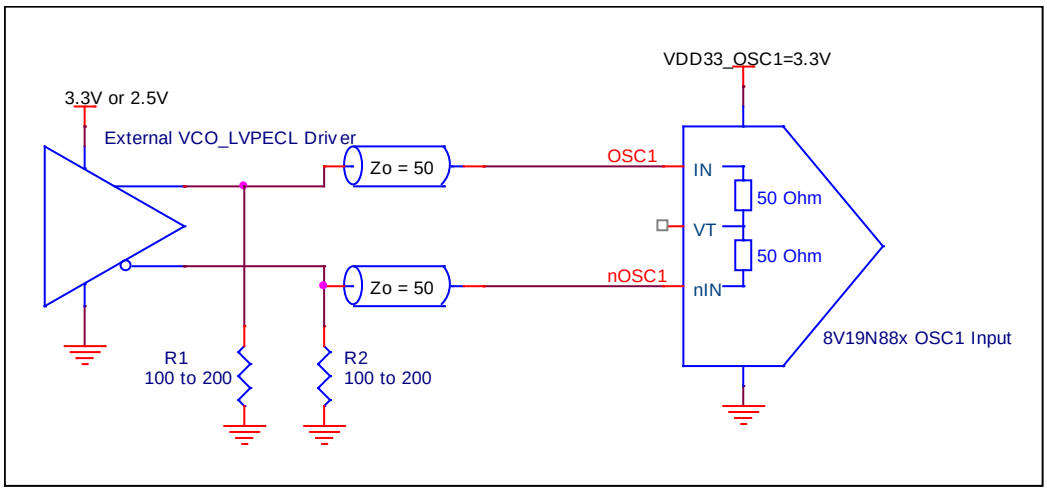

Figure 15. External VCO 3.3V LVPECL Driver to OSC_1/nOSC_1 Input, Alternative Interface

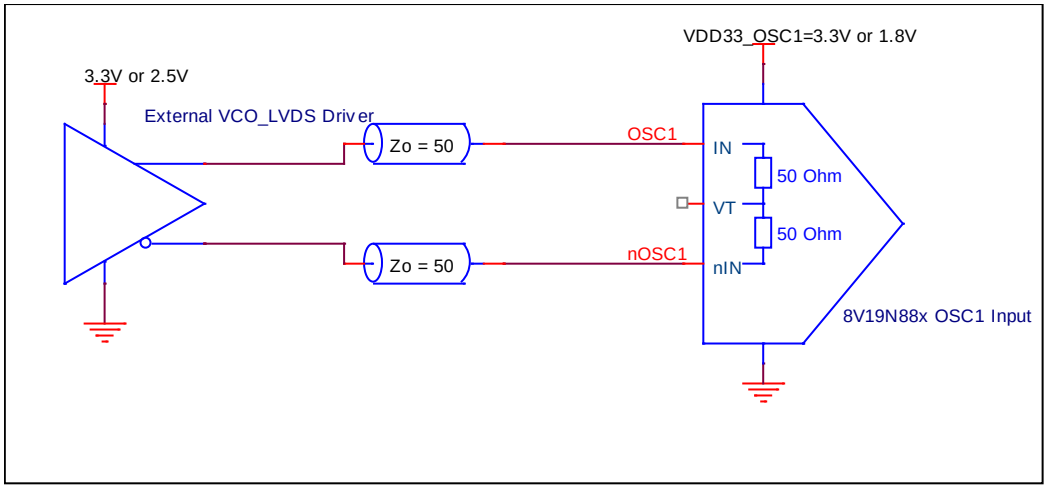

Figure 16. External VCO LVDS Driver to OSC_1/nOSC_1 Input Interface

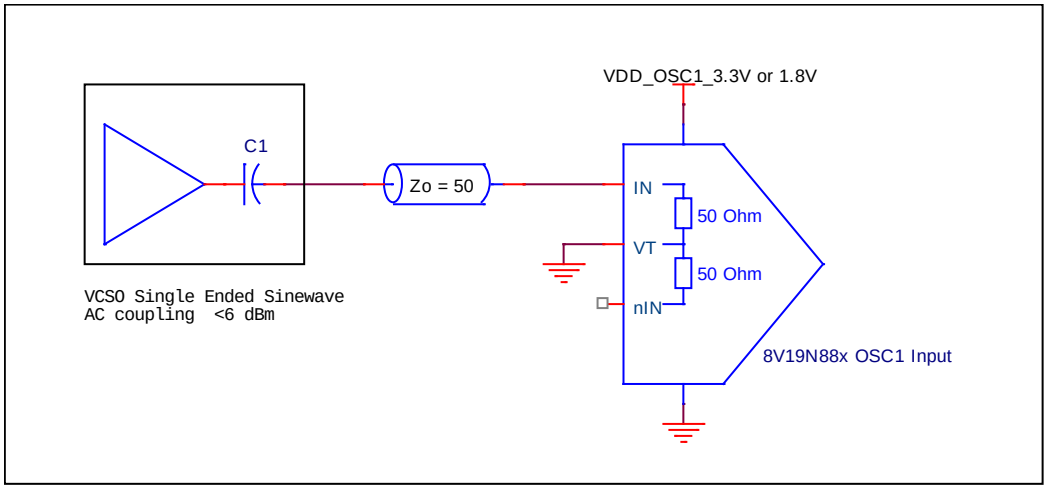

Figure 17. External VCO Single-ended Sinusoidal-Driver to OSC_1/nOSC_1 Input Interface

3.3 Output Terminations for QCLK and QREF Drivers

The output stage of the 8V19N882 QCLK drivers can be configured to LVPECL Style driver or LVDS Style driver.

3.3.1. LVPECL Type Driver Terminations

When the output is configured to LVPECL, the driver is an open emitter type requiring a DC current path to the termination voltage V_T through the pull-down resistor. A standard LVPECL driver termination is shown in Figure 18; Figure 19 to Figure 21 show alternative terminations. The LVPECL output driver is configurable and the applicable termination voltage V_T depends on the output amplitude setting and output supply voltage V_{DDO_v}. Refer to the V_T and termination resistor value tables below each diagram.

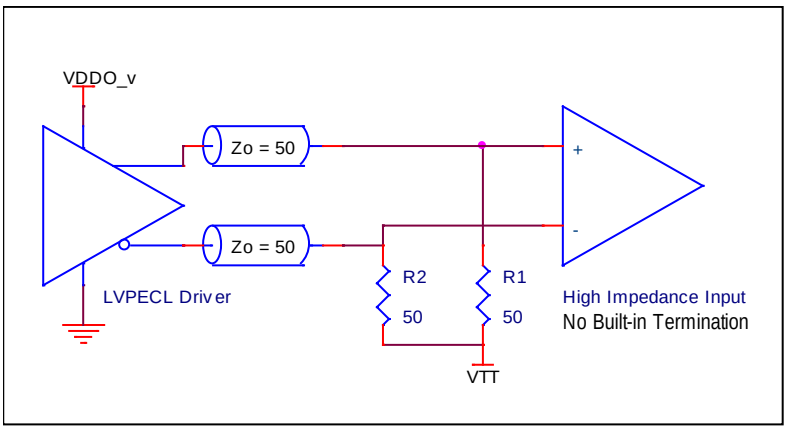

Figure 18. LVPECL Style Termination

Table 4. V_T Values for Output Termination in Figure 18

Output Supply Voltage	Output Amplitude	V_T
V_{DDO_v} = 1.8V	300mV	V_{DDO_v} – 1.55V
	400mV	V_{DDO_v} – 1.65V
	550mV	GND
	700mV	GND
V_{DDO_v} = 2.5V	300mV	V_{DDO_v} – 1.55V
	400mV	V_{DDO_v} – 1.65V
	550mV	V_{DDO_v} – 1.8V
	700mV	V_{DDO_v} – 1.95V
V_{DDO_v} = 3.3V	300mV	V_{DDO_v} – 1.55V
	400mV	V_{DDO_v} – 1.65V
	550mV	V_{DDO_v} – 1.8V
	700mV	V_{DDO_v} – 1.95V

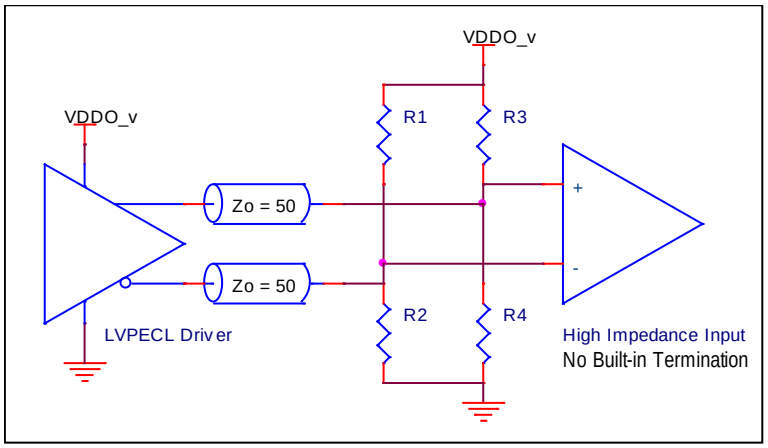

Figure 19. Alternative LVPECL Style Termination

Table 5. Resistor Values for Output Termination in Figure 19

Output Supply Voltage	Output Amplitude	R1, R3	R2, R4
V_{DDO_V} = 1.8V	300mV	360Ω	58.1Ω
	400mV	600Ω	54.5Ω
	550mV	No-pop	50Ω
	700mV	No-pop	50Ω
V_{DDO_V} = 2.5V	300mV	131.6Ω	80.6Ω
	400mV	147.1Ω	75.8Ω
	550mV	178.6Ω	69.4Ω
	700mV	227.3Ω	64.1Ω
V_{DDO_V} = 3.3V	300mV	94.2Ω	106.5Ω
	400mV	100Ω	100Ω
	550mV	110Ω	91.7Ω
	700mV	122.2Ω	84.6Ω

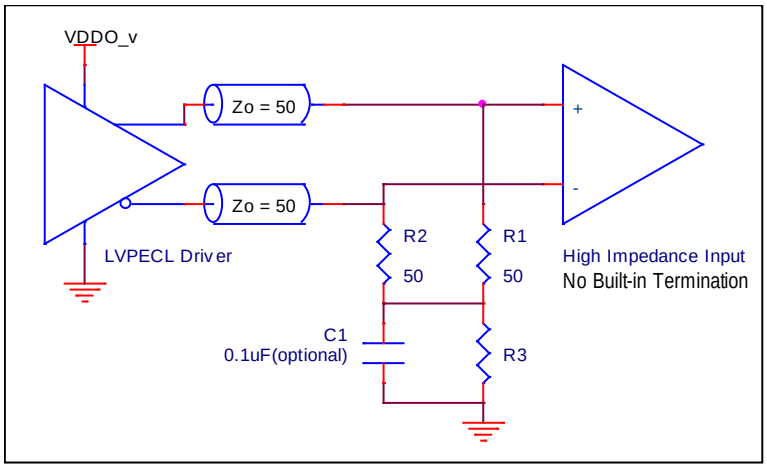

Figure 20. Alternative LVPECL Style Termination

Table 6. Resistor Values for Output Termination in Figure 20

Output Supply Voltage	Amplitude	R3
V_{DDO_V} = 1.8V	300mV	14Ω
	400mV	7.6Ω
	550mV	0Ω
	700mV	0Ω
V_{DDO_V} = 2.5V	300mV	53.1Ω
	400mV	43.8Ω
	550mV	27.9Ω
	700mV	22.4Ω
V_{DDO_V} = 3.3V	300mV	80.6Ω
	400mV	73.3Ω
	550mV	61.2Ω
	700mV	50Ω

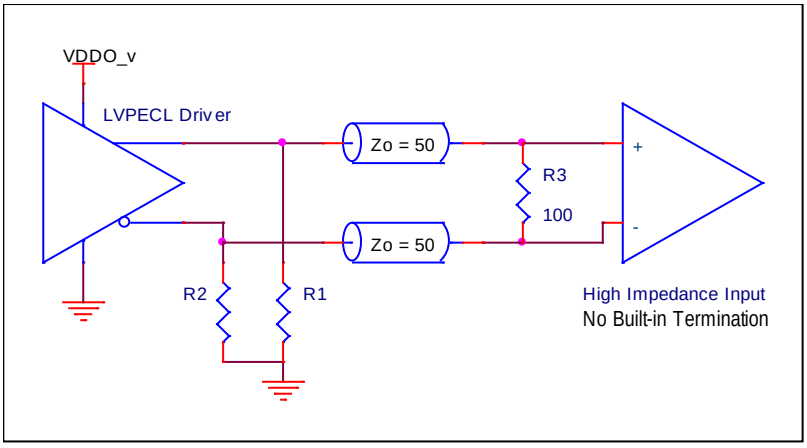

Figure 21. Alternative LVPECL Style Termination

Table 7. Resistor Values for Output Termination in Figure 21

Output Supply Voltage	Amplitude	R1, R2 (Ohm)
V_{DDO_V} = 1.8V	300mV	77.9Ω
	400mV	65.3Ω
	550mV	50Ω
	700mV	50Ω
V_{DDO_V} = 2.5V	300mV	156Ω
	400mV	138Ω
	550mV	116Ω
	700mV	94.9Ω
V_{DDO_V} = 3.3V	300mV	211Ω
	400mV	196Ω
	550mV	172Ω
	700mV	150Ω

3.3.2. LVDS Type Driver Terminations

Unlike the LVPECL style driver, the LVDS style driver does not require a board-level pull-down resistor. Figure 22 and Figure 23 show typical termination examples with DC coupling for the LVDS style driver. A termination example with AC coupling is shown in Figure 24. The following figures are for LVDS receivers with a high-input impedance (no built-in 100Ω termination). For receivers with built-in 100Ω termination, see the note below Figure 24.

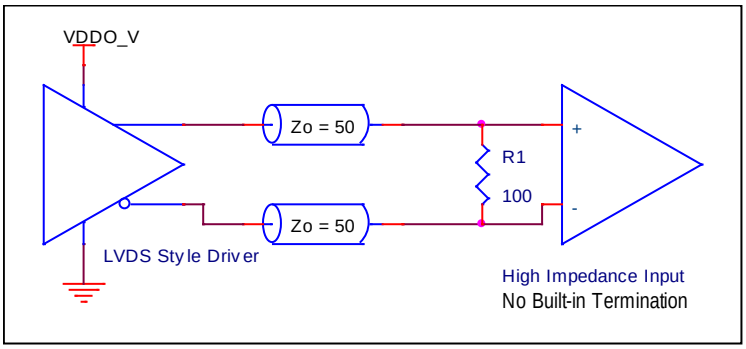

Figure 22. LVDS Style Driver Termination (DC Coupled)

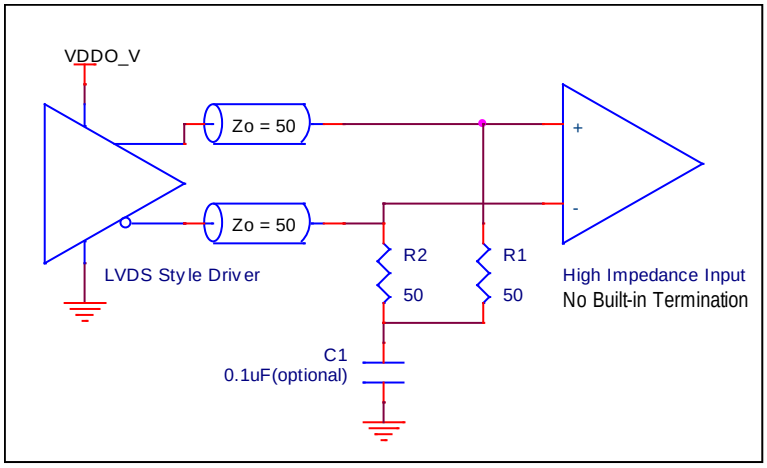

Figure 23. LVDS Style Alternative Driver Termination (DC Coupled)

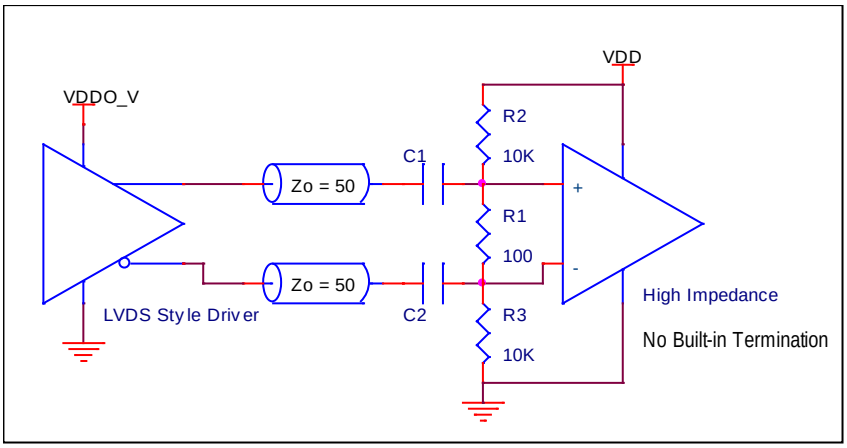

Figure 24. LVDS Style Alternative Driver Termination (AC Coupled)

For receivers with built-in 100Ω termination that provide their own DC offset (self-bias): Apply the AC-coupled termination displayed in Figure 24 and do not populate the resistors R1, R2, and R3.

4. Schematic Example

Reference demo board schematic and the board layout are available upon request

- 8V19N882 EVB schematic
- 8V19N882 EVB board layout

5. Revision History

Revision	Date	Description
1.1	Jun 1, 2021	Added VCXO order information to Table 2 (see footnote 1).
1.0	Mar 31, 2021	Initial release.

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