Introduction

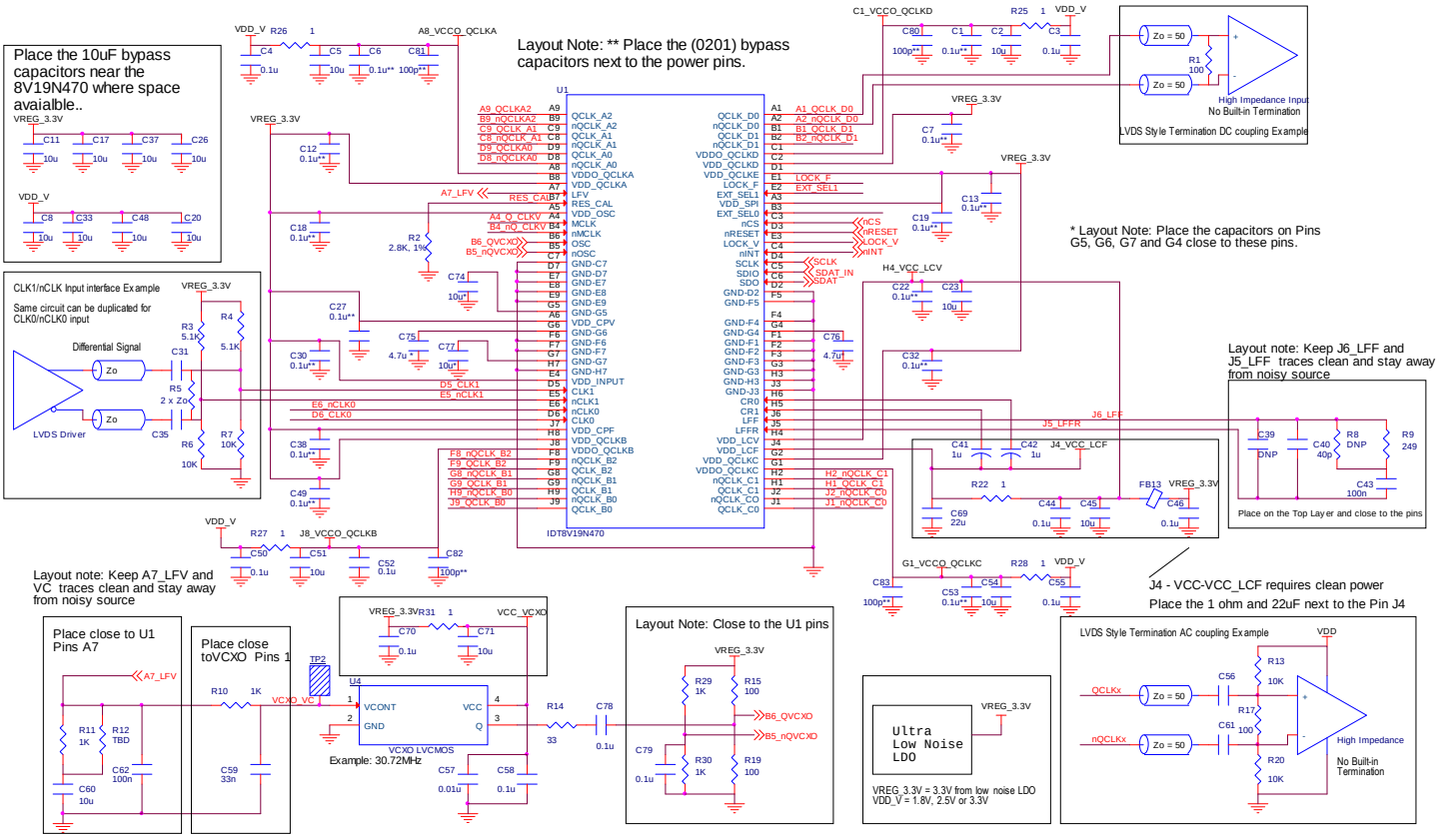
This document provides a general board-level hardware design guide for the 8V19N470, 8V19N472 and 8V19N474 devices. The main difference between these devices is the VCO frequency (see Table 1). The IDT8V19N470 is used for demonstration purposes in this document.

Table 1. VCO Frequencies

Part Number	VCO Frequency
8V19N470	~2.94912GHz and ~2.4576 GHz
8V19N472	~2.94912GHz and ~2.4576 GHz
8V19N474	~2.4G to ~2.5GHz

This document recommends power rail handling, loop filter calculation, and input/output termination for the 8V19N47x devices. A general schematic example for the 8V19N470 is shown in Figure 1. A larger schematic version is available upon request.

Figure 1. 8V19N470 Schematic Example



Power Rails

Bypass Capacitors

Bypass capacitors are required to filter out the system noise from switching power supplies, and switching signal interference from other parts of the system. Examples of bypass capacitors on the schematic are shown in Figure 1. The type of bypass capacitor will depend on the noise level and noise frequencies in the system environment. The synthesizer's output driver switching can cause power rail noise. These noises can also interfere with other parts of the circuit, or cause spurs on other output channels. A PCB layout example will be provided upon request.

The bypass capacitor values usually range from 0.01uF to 0.1uF. Other values can also be used. Typical capacitor sizes with low ESR are: 0603, 0402, or 0201. The typical dielectric types are: X5R or X7R. A smaller size allows the capacitor to be placed close to the power pin to reduce the trace length. Some capacitor vendors such as AVX provide online tools and models to provide the frequency response of the capacitors. Figure 2 to Figure 5 show the frequency response of various value capacitors, provided by the capacitor supplier AVX. The frequency response plot shows that the smaller value capacitor can filter out high frequency noise, and a larger value capacitor can filter out lower frequency noise. Typical power supply switching frequencies can be approximately 50kHz to 2MHz. Switching noise from other parts of the system can be varied. IDT suggests a combination of various values to cover low-frequency and high-frequency noise, if necessary.

To minimize ESR between power pins and the bypass capacitors, IDT suggests at least one bypass cap per power pin, and to place the capacitors as close to the power pins as possible. A thicker trace width between the bypass capacitor and power pin can also help reduce the ERS.

Figure 2. Example of a 100nF Bypass Capacitor Frequency Response

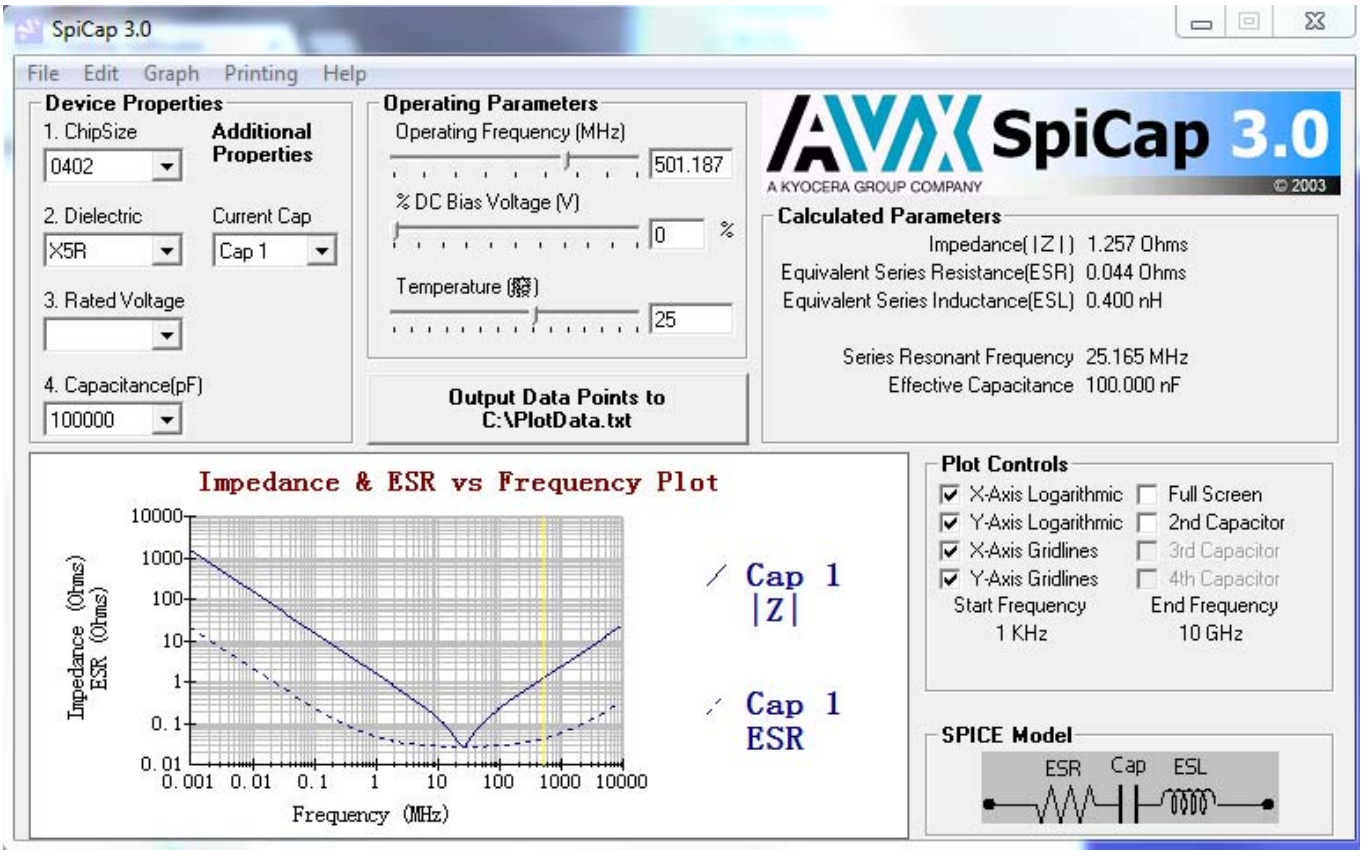


Figure 3. Example of a 10nF Bypass Capacitor Frequency Response

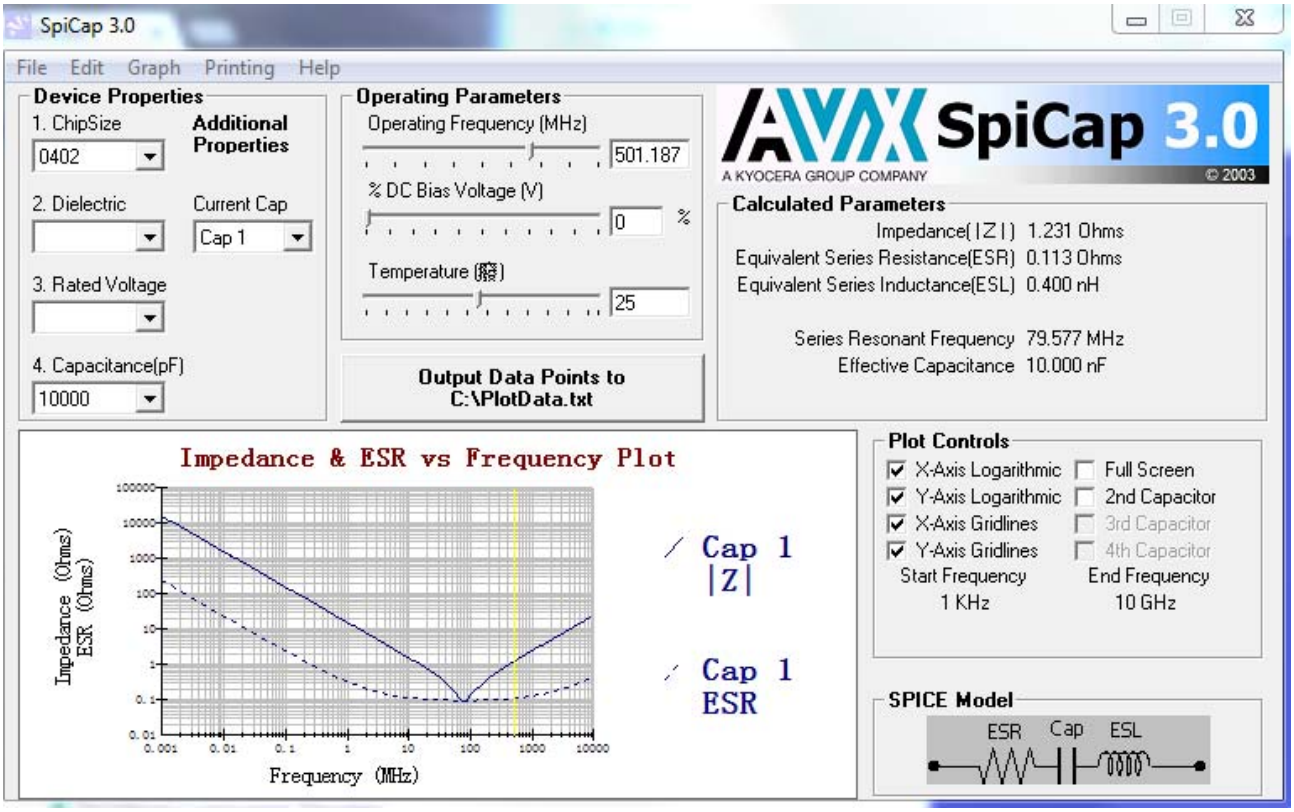


Figure 4. Example of a Larger Value (4.7µF) Bypass Capacitor Frequency Response

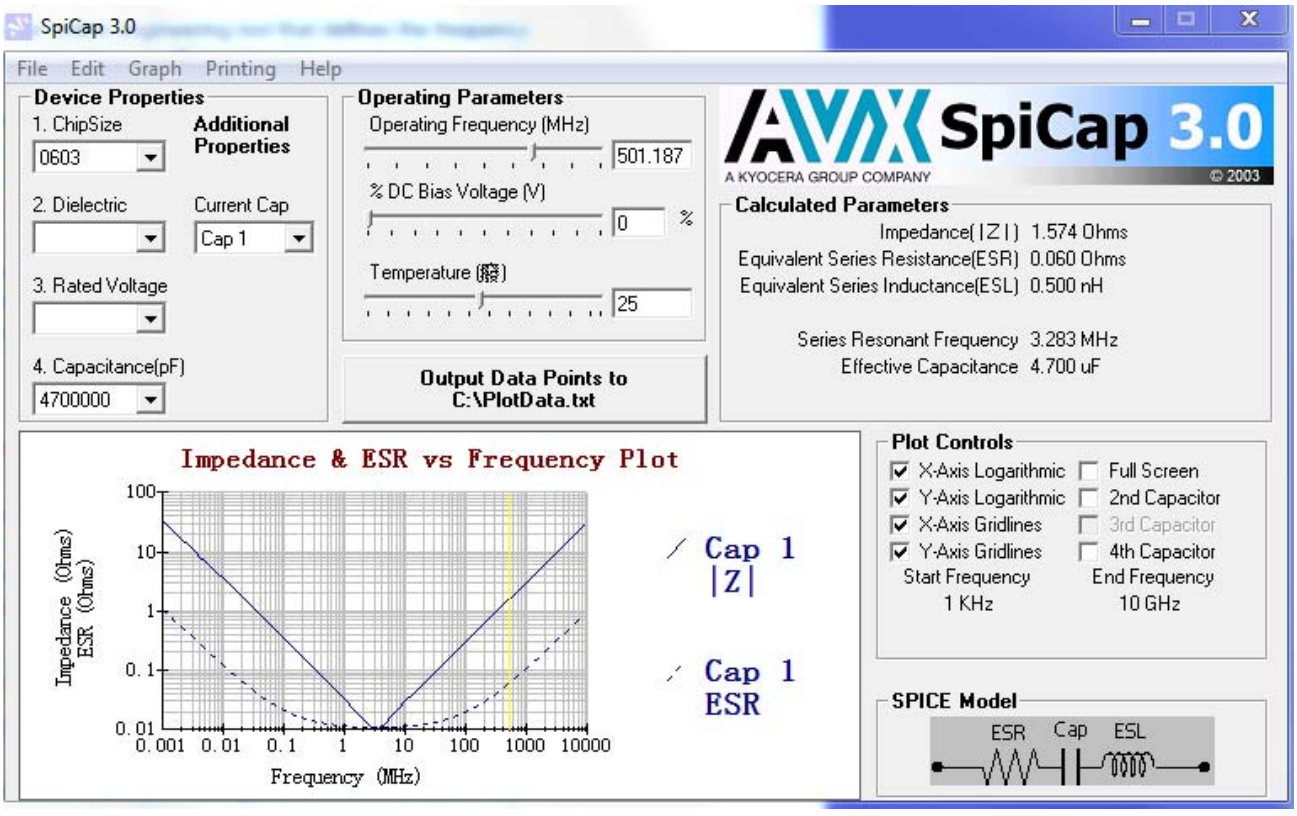
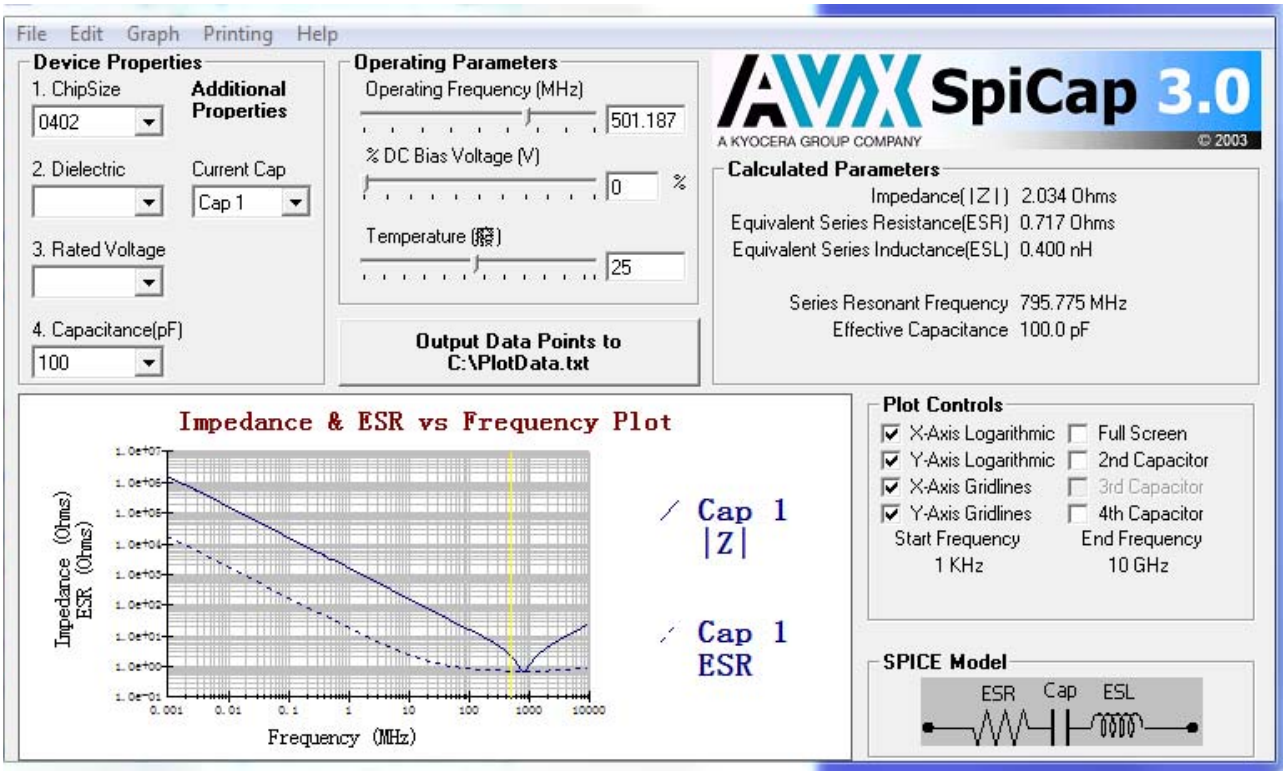


Figure 5. Example of a Smaller Value (100pF) Bypass Capacitor Frequency Response



Power Supply Isolation

An analog power rail requires cleaner power to optimize the jitter performance of the PLL. IDT suggests to isolate the analog power rail from other high noise power rails. The isolation can be implemented through an RC low-pass filter. The larger RC component values can further reduce the cutoff frequency and clean up lower frequency noise.To isolate a clean power rail from noise power, an ultra-low noise LDO is required for reducing power supply noise to a noise sensitive power line such as VDD_LCV and the external VCXO. IDT suggests an ultra-low noise LDO for the VDD_LCV pin noise level of less than 6uVrms from 10Hz to100kHz.

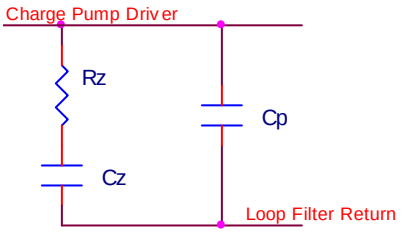
To reduce output frequency interference for V_{DDO} output supplies, the power rails between the output banks that operate at different output frequencies can be isolated using a separate 1Ω resistor if they share the same power source. Additional smaller value capacitors (e.g. 100pF) in parallel with the existing 0.1uF near the power pins can provide additional higher frequency noise filtering.

Loop Filter

2nd Order Loop Filter

This section provides information about designing a 2nd order loop filter for the PLL. A typical 2nd order loop filter is shown in Figure 6. The following equations show a step-by-step calculation to determine Rz, Cz, and Cp values. The required parameters for this device are also provided. A spreadsheet for calculating the loop filter values is also available upon request.

Figure 6. Typical 2nd Order Loop Filter



1. The desired loop bandwidth, *fc*, must satisfy the following condition: $\frac{Fpd}{fc} \gg 20$

   Where, Fpd is the phase detector input frequency.

2. Calculate Rz: $$Rz = \frac{2 \times \pi \times fc \times N}{Icp \times Kvco}$$

   Where:

   Icp = Charge pump current

   Kvco = VCO gain

   N = Effective feedback divider

   $$N = \frac{Fvco}{Fpd}$$

   Where:

   Fvco = VCO frequency

   Fpd = Phase detector input frequency

3. Calculate Cz: $$Cz = \frac{\alpha}{2 \times \pi \times fc \times Rz}$$

   Where:

   fz = Frequency at zero

   α = Ratio between the loop bandwidth and the zero frequency at zero; α = fc ÷ fz (α > 3 is recommended)

4. Calculate Cp: $$Cp = \frac{Cz}{\alpha \times \beta}$$

   Where:

   fp = Frequency at pole

   β = Ratio between frequency at pole and loop bandwidth; β = fp ÷ fc (β > 3 is recommended)

5. Verify maximum Phase Margin (PM): $$PM = \arctan\left(\frac{b-1}{2 \times \sqrt{b}}\right)$$

   Where:

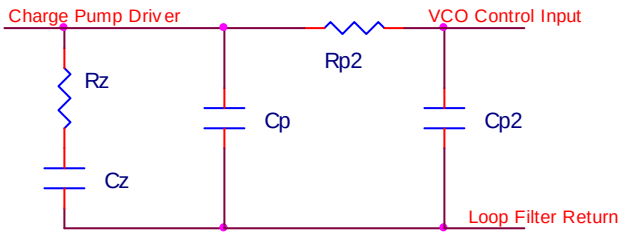
$$b = 1 + \frac{Cz}{Cp}$$

   Note: the PM should be > 50°.

3rd Order Loop Filter

This section provides an example of a 3rd order loop filter. A typical 3rd order loop filter is shown in Figure 7.

Figure 7. Typical 3rd Order Loop Filter



The Rz, Cz, and Cp can be the actual values used in the 2nd order loop filter. To determine the 3rd order loop filter, Rp2 and Cp2, refer to the following equation:

Select an Rp2 value (Rp2 ~ 1.5xRz is used in the example below).

$$Cp2 = \frac{Rz \times Cp}{Rp2 \times y}$$

Where:

γ = Ratio between the 1st pole frequency and the 2nd pole frequency (γ > 3 is recommended).

A spreadsheet is provided to calculate the loop filter component values. To use the spreadsheet, the user can enter the following parameters: fc, Fpd, fvco, α, and β.

The spreadsheet will provide the component values, Rz, Cz, and Cp, as a result. The spread sheet can also calculate the maximum phase margin for verification. The 3rd order loop filter Rp2 and Cp2 is also calculated using the actual 2nd order loop filter components values.

Loop Filter Calculation Examples

Loop Filter for VCXO PLL

Second Order Loop Filter for the VCXO PLL

This section provides calculation examples for the VCXO PLL loop filter value. The 8V19N470 VCXO phase lock loop block diagram is shown in Figure 8. A 2nd order loop filter for VCXO is shown in Figure 9. In this example, the reference CLK input frequency = 30.72MHz and a VCXO with output frequency of 122.88MHz is used.

Figure 8. 8V19N470 VCXO Phase Lock Loop Block Diagram

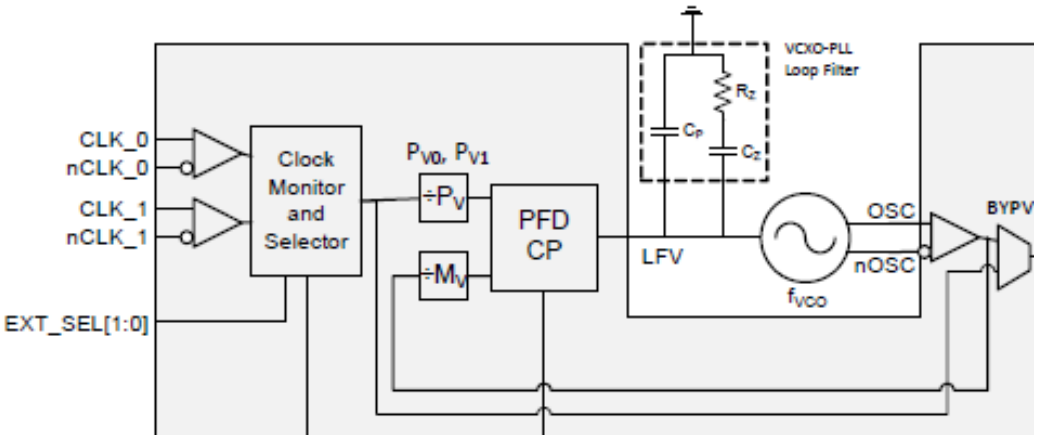
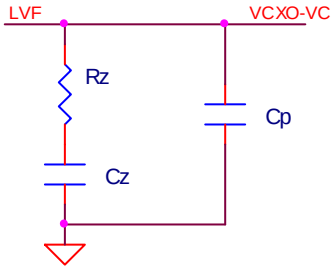


Figure 9. Typical 2nd Order Loop Filter



To calculate the loop filter component value for loop bandwidth, Fc = 40Hz with the reference CLK input frequency equal to 30.72MHz, set the input pre-divider Pv = 256. The phase detector input frequency Fpd = 0.12MHz. This satisfies the condition of Fpd ÷ Fc >> 20.

The VCXO frequency is: Fvcxo = 122.88MHz, and the effective feedback divider is: N = Mv = Fvcxo ÷ Fpd = 1024.

Rz can be calculated from the equation: $$Rz = \frac{2 \times \Pi \times fc \times N}{Icp \times Kvco}$$

Rz = 33kΩ

Kvco VCO gain can be found or derived from the VCXO datasheet. The VCO gain can also be measured from a lab experiment. In this example, Kvco = 10kHz/V was applied.

The 8V19N470 charge pump current can be programmed from 50uA to 1.6mA. In the following example, the charge pump current is programmed to Icp = 800uA.

Cz can be calculated from the following equation:

$$Cz = \frac{\alpha}{2 \times \pi \times fc \times Rz}$$

For α = 8, Cz is calculated to be 0.99uF. Cz greater than this value can be used to assure that the α is > 12. For example, the actual determined value can be, 1uF from a standard capacitor value.

Cp can be calculated from the following equation:

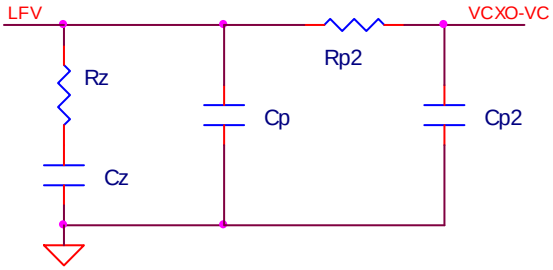
$$Cp = \frac{Cz}{\alpha \times \beta}$$

For β = 4, Cp = 31nF. Less than this value can be used for Cp to assure, β is > 4 (e.g. the actual determined value Cp can be 27nF).

Third Order Loop Filter for the VCXO PLL

This section provides information about designing a 3rd order loop filter for the 8V19N470 VCXO PLL. A general 3rd order loop filter is shown in Figure 10.

Figure 10. Typical 3rd Order Loop Filter



The Rz, Cz, and Cp are actual standard values from the 2nd order loop filter. In this example, the actual values are: Rz = 33kΩ, Cz = 1uF, and Cp = 27nF. The 3rd order loop filter, Rp2 and Cp2, is determined in the following equation.

Select an Rp2 value (Rp2 ~ 1.5xRz to ~2.5xRz or greater is recommended; e.g. Rp2 = 51kHz is used in this example).
Cp2 can be calculated using the following equation:

$$Cp2 = \frac{Rz \times Cp}{Rp2 \times y}$$

In this example, γ = 4 was selected.

Cp2 is calculated at 4.37nF. A closer standard capacitor value can be used.

Loop Filter for VCO PLL

The 8V19N470 VCO phase lock loop diagram is shown in Figure 11. The Fvco frequency is 2.94912GHz. In this example, the 2949.12MHz VCO is used. A 2nd order loop filter for VCXO is shown in Figure 12.

Figure 11. VCO PLL Block Diagram

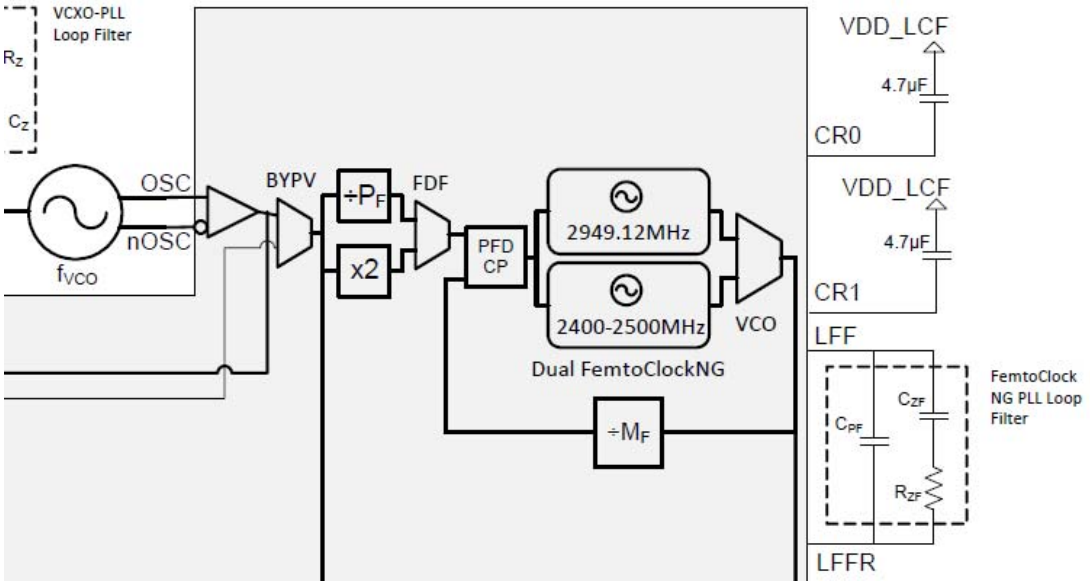
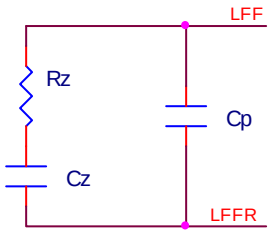


Figure 12. 2nd Order Loop Filter for VCO



In this example, the VCO phase detector input frequency is: Fpd = 122.88MHz, which is driven from the VCXO output.
The effective feedback divider is: N = MF = 20.

Calculate the loop filter component values for loop bandwidth, Fc = 80kHz.
The phase detector input frequency is: Fpd = 122.88MHz. This satisfies the condition of Fpd ÷ Fc >> 20.

The VCO gain for this part is: Kvco = 30MHz/V

The charge pump current is: Icp = 2mA

Rz can be calculated from the following equation: $Rz = \frac{2 \times \Pi \times fc \times N}{Icp \times Kvco}$

Rz = 201Ω

For α = 10, the Cz is calculated from the following equation: $Cz = \frac{\alpha}{2 \times \Pi \times fc \times Rz}$

Select an α value, where α must be greater than 3. In this example, α = 10 is selected and Cz is calculated at 99nF. A capacitor greater than this value should be used for Cz to ensure α is greater than 10 (e.g. the selected value, Cp, can be 100nF from a standard capacitor value). For Cp capacitor value, since this is compensated by the internal partial loop filtering, suggest install Cp = 40pF.

Input Output Interface

Input Termination for Reference Clock Input

The 8V19N470 reference clock input CLK, nCLK is a high impedance differential receiver. The inverting input nCLK has weak bias to 1.2V. The input can accept a signal from a standard 3.3V LVPECL or an LVDS driver directly without AC coupling. The board-level termination at the CLK, nCLK input, is determined by the driver type. Figure 13 and Figure 14 provide examples of an input interface without AC coupling. Figure 15 and Figure 16 provide examples of an input driven by a differential driver with AC coupling. This section provides only a few examples; other termination topologies can also be used.

Figure 13. Input Termination Example – 8V19N470 Input Reference Clock CLK, nCLK Driven by a 3.3V LVPECL Driver

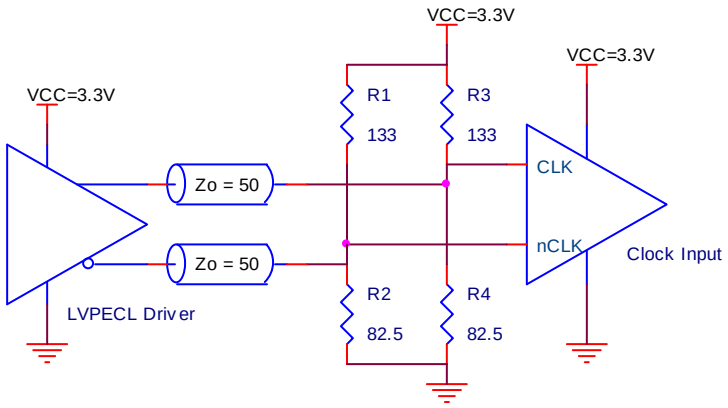


Figure 14. Input Termination Example – 8V19N470 Input Reference Clock CLK, nCLK Driven by a 3.3V LVDS Driver

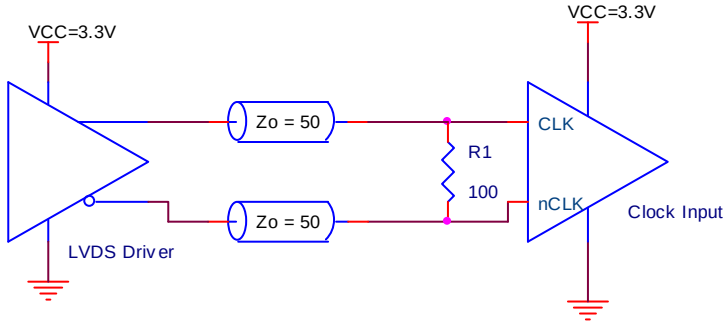


Figure 15. 8V19N470 Input Reference Clock CLK, nCLK AC Coupling Termination Example 1

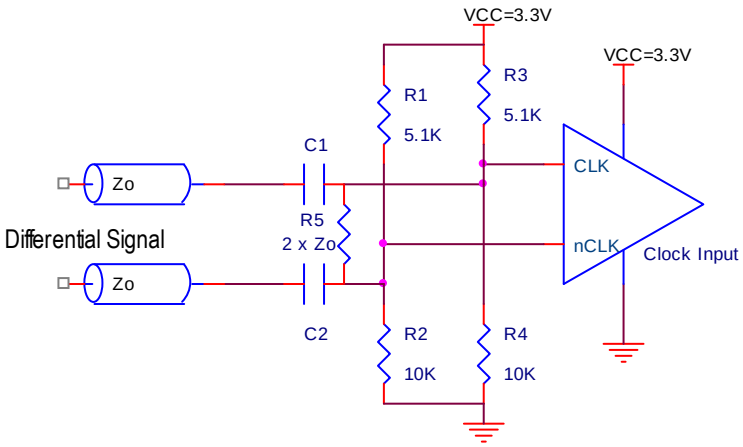
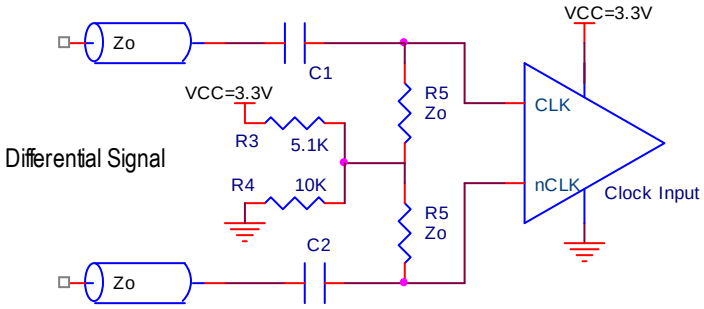


Figure 16. 8V19N470 Input Reference Clock CLK, nCLK AC Coupling Termination Example 2



Output Terminations for QCLK and QREF Drivers

The output stage of the 8V19N470 QCLK drivers can be configured to an LVPECL-style driver or an LVDS-style driver.The output power supply VDD_v can also be ranged from 1.8V to 3.3V.

LVEPCL Driver Terminations

When the 8V19N470 output is configured to LVPECL-style driver, the driver is an open emitter type and requires pull-down resistors to provide DC current path in order for the output to switch. A typical standard LVPECL style driver termination for characterization is shown in Figure 17. The VTT value will depend on the programmed amplitude and the VDD_v power supply voltage. Table 2 shows the recommend VTT values for the amplitudes setting. There are various ways to terminate the LVEPCL driver. Examples of LVPECL-style driver terminations are shown in Figure 18 to Figure 21. Table 3 to Table 5 show recommend component values for each amplitude setting and VDD_v power supply voltages.

Figure 17. Standard LVEPCL Driver Termination

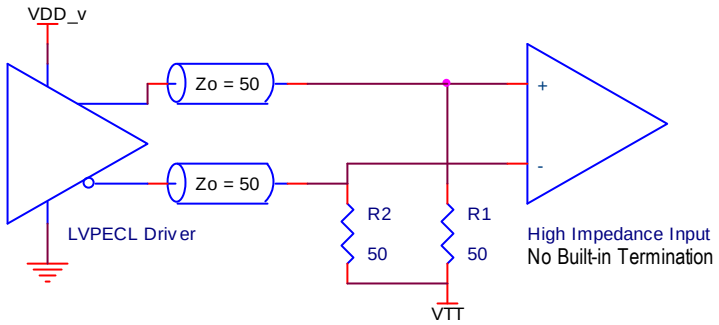


Table 2. VTT Values for Figure 17

Amplitude	VTT
850mV	VDD_v – 2.10V
700mV	VDD_v – 1.95V
500mV	VDD_v – 1.75V
350mV	VDD_v – 1.60V

Figure 18. LVPECL Termination Example 1

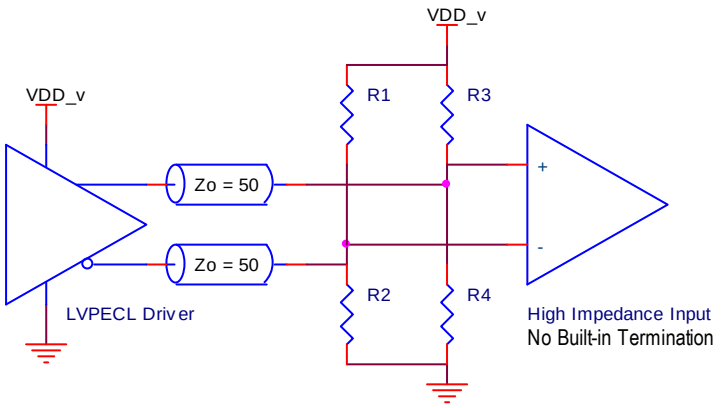


Table 3. Suggested Component Values for Figure 18

VDD_v	Amplitude	R1, R3 (Ohm)	R2, R4 (Ohm)
3.3V	850mV	137.5	78.6
3.3V	750mV	122	84.6
3.3V	500mV	106.5	94.3
3.3V	350mV	97.1	103.1
2.5V	850mV	312.5	59.5
2.5V	750mV	227.3	64.1
2.5V	500mV	166.7	71.4
2.5V	350mV	138.8	78.1
1.8V	500mV	No-Pop	50
1.8V	250mV	450	56.3

Figure 19. LVPECL Termination Example 2

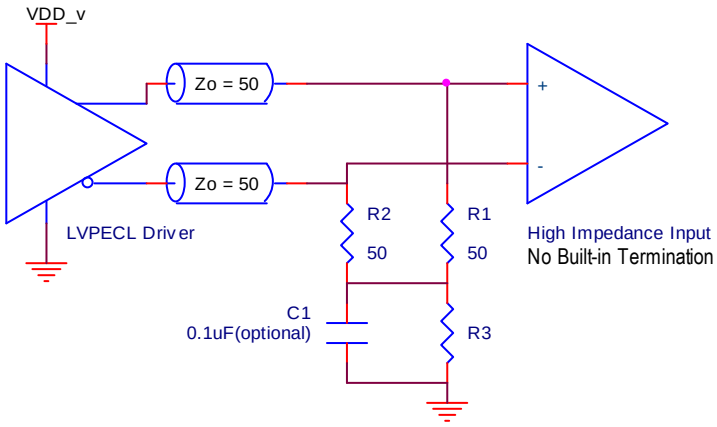


Table 4. Suggested Component Values for Figure 19

VDD_v	Amplitude	R3 (Ohm)
3.3V	850mV	50
3.3V	750mV	50
3.3V	500mV	50
3.3V	350mV	50
2.5V	850mV	18
2.5V	750mV	18
2.5V	500mV	18
2.5V	350mV	18
1.8V	500mV	0
1.8V	350mV	0

Figure 20. LVPECL Termination Example 3

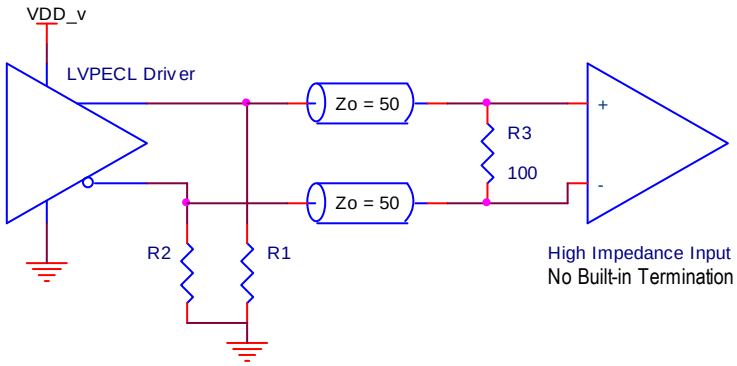


Table 5. Suggested Component Values for Figure 20

VDD_v	Amplitude	R1, R2 (Ohm)
3.3V	850mV	100 to 200
3.3V	750mV	100 to 200
3.3V	500mV	100 to 200
3.3V	350mV	100 to 200
2.5V	850mV	80 to 150
2.5V	750mV	80 to 150
2.5V	500mV	80 to 150
2.5V	350mV	80 to 150
1.8V	500mV	50 to 100
1.8V	350mV	50 to 100

Figure 21. LVPECL Driver DC Coupling Termination for the Receiver with Built-in 100Ω Termination

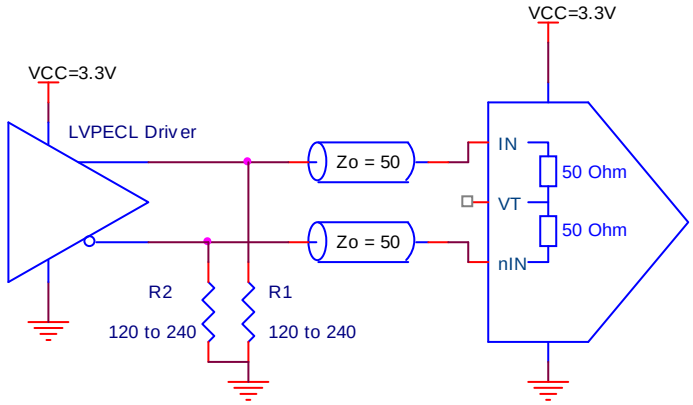
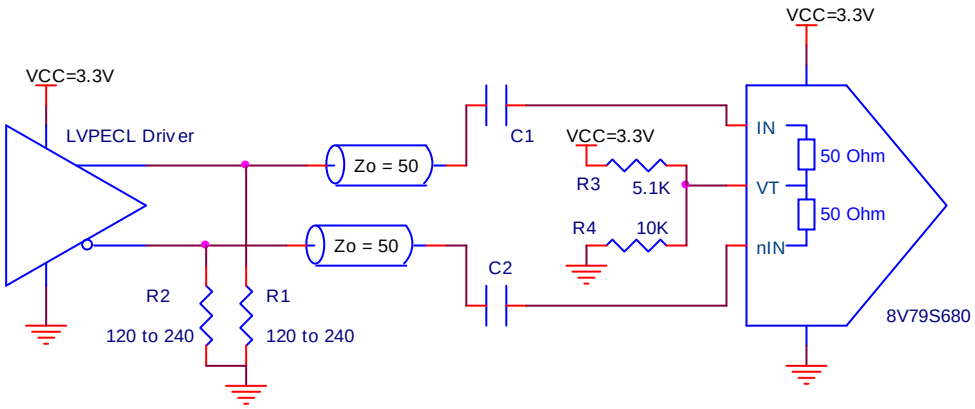


Figure 22. LVPECL Driver AC Coupling Termination for the Receiver with Built-in Termination



LVDS-type Driver Terminations

An LVDS-type driver does not require a board-level pull-down resistor. A typical termination with DC coupling for the LVDS-type driver is shown in Figure 23. A termination example with AC coupling is shown in Figure 24.

Figure 23. Typical LVDS-style Driver Termination

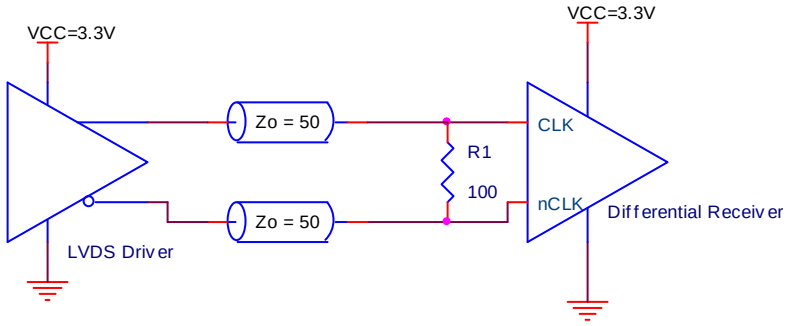
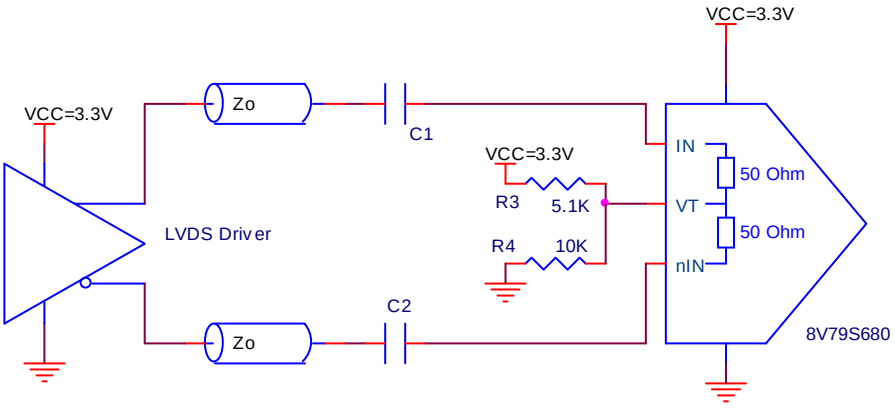


Figure 24. 8V19N470 LVDS Driver Driving a Receiver with Built-in Termination (e.g. 8V79S680 CLK, nCLK and REF, nREF Inputs)



Schematic Example

The reference demo board schematic and board layout example are available upon request.

Revision History

Revision Date	Description of Change
May 28, 2017	Initial release.

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