8A3xxxx Firmware Version v4.9.1

Overview

This document describes changes in the functionality and register map between firmware version 4.8.8 and version 4.9.1. This optional firmware update provides support for sending Asynchronous information over a carrier using PWM. There are related documents listed in Table 1 that describe specific functions or details that would overly burden this document.

Table 1. Related Documents

Document Title Document Description	Document Title Document Description
8A3xxxx Device Datasheet	Contains a functional overview of a specific 8A3xxxx Family device and hardware-design related details including pinouts, AC & DC specifications and applications information related to power filtering and terminations.
8A3xxxx Family Programming Guide v4.9.1	Contain detailed register descriptions and address maps for all members of the family of devices. All devices use some subset of this register map.

Compatibility with Earlier Firmware Versions

Registers for Firmware 4.8.8 are compatible with 4.9.1. However, there have been some documentation changes, which are described in Issue Number – BRMBXR-3338 later in this document.

Firmware Version Number

The firmware version can be read from the GENERAL_STATUS registers as shown in the following table.

Register Module Base Address – C014h			Firmware Version – v4.9.1
Offset Address (Hex)	**Individual Register Name**	**Register Description**	**Default Value**
010h	GENERAL_STATUS.MAJ_REL	Major release number	09h
011h	GENERAL_STATUS.MIN_REL	Minor release number	09h
012h	GENERAL_STATUS.HOTFIX_REL	Hotfix release number	01h

New Features Implemented Between 4.8.8 and 4.9.1

Async Clock over PWM. For more information, see application note Multi-Clock Distribution using Timing Commander for FW4.9.1.

TOD over PWM transmission. For more information, see application note Multi-Clock Distribution using Timing Commander for FW4.9.1.

Functional Differences

The following tables describe the functional differences between firmware version 4.8.8 and 4.9.1.

Issue Number – BRMBXR-3256	
Firmware	**Functional Difference**
4.8.8	Behavior mismatch in master/Slave hitless switch between marketing expectations and implementation. Changes related to this item: ▪ If the DPLL is in slave mode, then an instant reference switch must be applied even if the hitless switch is enabled. The condition “Is DPLL in slave mode” was limited to “if SCSR_DPLL_REF_MODE.mode = 3 (slave)”. Now it is OR'ed with “if SCSR_DPLL_REF_MODE.mode = 4 (GPIO_slave) and the slave mode is selected by the GPIO”. ▪ TIE reset applies when switching into slave mode.
4.9.1	A hitless switch is applied if SCSR_DPLL_REF_MODE.mode = 4 (GPIO_slave) and the slave mode is selected by the GPIO. TIE reset is applied when switching into the slave mode.

Issue Number – BRMBXR-3301	
Firmware	**Functional Difference**
4.8.8	PWM user data is limited to 37 bytes at 10kHz carrier speed. The timeout for PWM user data reception is too short and therefore, the maximum number of bytes depends on the PWM carrier frequency.
4.9.1	A complete burst of 128 bytes can be transmitted over PWM even if the carrier frequency is 8kHz.

Issue Number – BRMBXR-3302	
Firmware	**Functional Difference**
4.8.8	When the output sync is disabled, the output clock is delayed a few seconds. This problem occurs randomly after power cycle. In order to fix it, the output divider must be always reset at start up regardless of OUT_SYNC_DISABLE setting.
4.9.1	The output clock is not delayed when OUT_SYNC_DISABLED = 1.

Issue Number – BRMBXR-3431	
Firmware	**Functional Difference**
4.8.8	Reference switching may be blocked. This problem might be caused by a race condition between the DPLL events and the external DPLL configuration via serial interface.
4.9.1	The reference switch state machine parameters are reset properly when a new reference switch is initiated.

Issue Number – BRMBXR-3403	
Firmware	**Functional Difference**
4.8.8	Decimator value may be affected by the fine phase measurement algorithm. This problem might occur when register FILTER_STATUS_SELECT_CNFG is set to 1.
4.9.1	The decimator value is not affected by the continuous filter status update.

Issue Number – BRMBXR-3406	
Firmware	**Functional Difference**
4.8.8	Fix PWM async phase jump issue. ▪ The PWM decoder-to-encoder alignment experienced an unexpected periodic phase jump.
4.9.1	This problem could be reproduced with controlled frequency offset between the PWM Encoder XO and the PWM Decoder XO. The same test conditions were used to prove that the phase jump was fixed.

Issue Number – BRMBXR-3416	
Firmware	**Functional Difference**
4.8.8	In Phase Measurement mode, it takes 10s to switch inputs. ▪ This problem occurs only when the DPLL is in Phase Measurement mode and the FOD frequency is set to zero. ▪ The delay is caused by the feedback divider initialization, which in this case it should not be initialized.
4.9.1	The phase measurement mode works properly after the inputs are changed. The result is updated immediately after the measurement is finished, without any additional delay.

Issue Number – BRMBXR-3427	
Firmware	**Functional Difference**
4.8.8	Fix the feedback divider misalignment. ▪ This problem might affect the feedback-to-input alignment when the DPLL is configured for the first time after power up and the selected input reference is qualified.
4.9.1	After the DPLL is initialized, the feedback divider is aligned with the input reference as expected.

Issue Number – BRMBXR-3338
Documentation update. No functional change.

- Remove TEMPERATURE from the programming guide.
- Set the default value of PR_BUILD = 1.
- Change the name of TOD_OUT_SYNC_ENABLE to TOD_OUT_SYNC_DISABLE.
- Fix inconsistent use of INPUT and CLK in the description of MUX_GPIO_IN, EXT_FB_REF_SELECT, and IN_DIFF.
- Change FBD_INTEGER_MODE_EN to FBD_USER_CONFIG_EN. Update the description of FBD_USER_CONFIG_EN.
- In register GPIO_FUNCTION, replace the option “OTP CONFIGURATION Select” with “reserved”.
- Fix the description of OTP_STATUS. The status is (1 << 24) | error code.
- Expose all INPUT_TDC registers to programming guide.
- Add more options to registers FORCE_LOCK_INPUT and MANUAL_REFERENCE:
  - 0x13 = fb clk of DPLL 0
  - 0x14 = fb clk of DPLL 1
  - 0x15 = fb clk of DPLL 2
  - 0x16 = fb clk of DPLL 3
  - 0x17 = fb clk of DPLL 4
  - 0x18 = fb clk of DPLL 5
  - 0x19 = fb clk of DPLL 6
  - 0x1A = fb clk of DPLL 7
  - 0x1B = fb clk of SYS DPLL
- Fix the description of IN_DIV: “Maximum speed for the references sent to the DPLL is 150 MHz.”
- Improve the description of the following registers:
  - GPIO_DPLL_INDICATOR
  - DPLL_MASTER_DIV
  - PHASE_LOCK_MAX_ERROR
  - FB_SELECT_REF
  - DPLLx_FILTER_STATUS
  - DPLL_SYS_FILTER_STATUS
  - SDM_FRAC

Revision History

Revision	Date	Description
1.0	Jun 15, 2021	Initial release.

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