RENESAS RZ

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BIG IDEAS FOR EVERY SPACE

Entry Level MPU with the AI accelerator (DRP-AI)

RENESAS RZ/V2L EMBEDDED AI MPU

More Cost-Efficient Vision AI solution

In order to utilize embedded AI, it is necessary to overcome various issues such as heat dissipation, shortening of development period, and cost, as well as the performance of AI accelerators and CPUs.

We have released a new product RZ/V2L for the entry class of the Renesas RZ/V series that solves such problems. Equipped with Renesas' original AI accelerator DRP-AI (Dynamically Reconfigurable Processor for AI), It realizes high-precision AI inference and industry-leading power efficiency.

Artificial Intelligence

AI Accelerator

DRP-AI

- Realizes AI inference with high power efficiency without costly heat dissipation like heat sink

Image Signal Processing

ISP function by DRP library

Simple ISP

- Improves recognition accuracy by image pre-processing
- Makes using low-cost CMOS sensor without ISP possible

Scalability for Vison AI

Compatibility of RZ/V2L & RZ/G2L

Scalability for Vision AI

- Provides easy migration from RZ/G2L to RZ/V2L by package full compatibility and S/W reusability

Target Application

Embedded AI on various use cases

Target Application

- Home appliances with AI
- Surveillance camera with recognition function
- Retail POS
- Smart doorbell

etc.

Key Features

- 64-bit Arm® Cortex®-A55 (1.2GHz, dual or single core) and Cortex®-M33
- DRP-AI (1TOPS/W class) capable of running the Tiny YOLOv2 program at 28 frames per second (fps)
- Simple ISP functions required for machine vision are provided in the DRP library
- 16-bit, single-channel DDR memory interface
- 3-D graphics functions (Arm® Mali™-G31 GPU)
- Video codec (H.264)
- CMOS sensor interfaces (MIPI-CSI and Parallel) for camera input
- Display interfaces (MIPI-DSI and Parallel)
- Memory with error checking and correction (ECC)
- Available in 15mm square or 21mm square BGA packages that are pin-compatible with the RZ/G2L
- Provides a single-chip PMIC solution (RAA215300) optimized for the RZ/V2L group
- Released a Winning Combination HMI SoM with AI Accelerator provided by RZ/V2L and powerful Power&Timing ICs of Renesas

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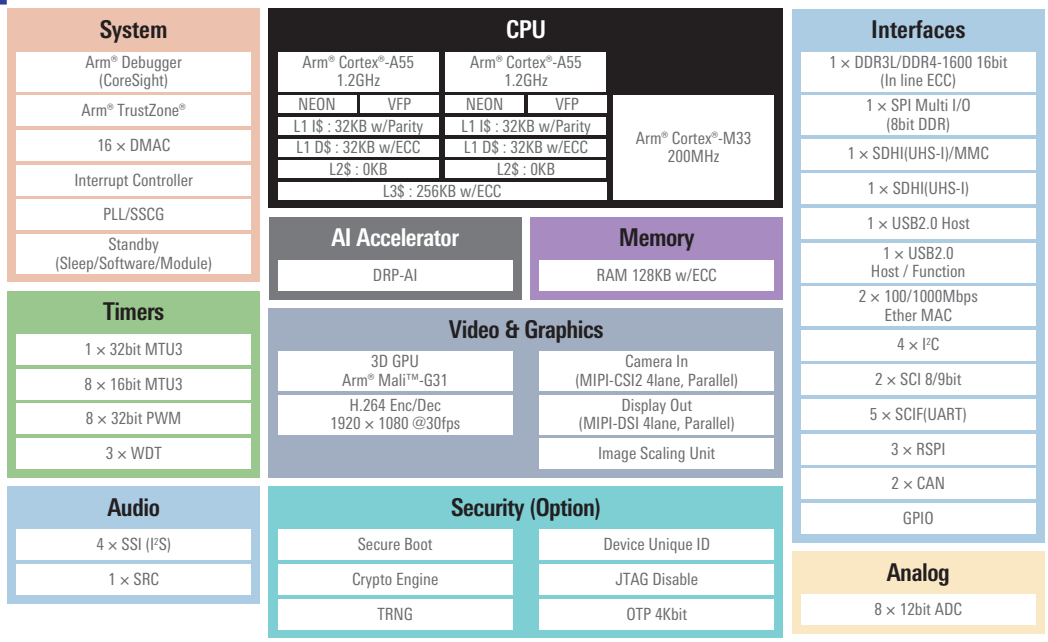
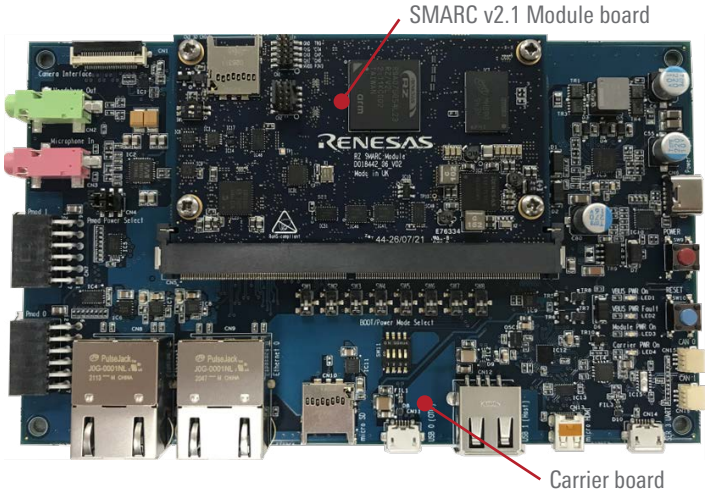
Block Diagram



- AI Accelerator; DRP-AI
- 2× Cortex®-A55 (1.2GHz), Cortex®-M33 (200MHz)
- 16bit DDR3L/DDR4-1600 (in line ECC)
- Simple ISP (provided in the DRP library)
- Camera IF; MIPI-CSI2 (4 lanes) and Parallel
- H.264 codec
- 3D graphics function (Arm® Mali™-G31)
- Display IF; MIPI-DSI (4 lanes) and Parallel
- 2× Gigabit Ethernet
- 2× CAN (CAN-FD)
- 2× USB2.0 (Host, Host/Peripheral)
- 2× SDHI (UHS-I, UHS-I/MMC)
- Equipped with hardware security engine
- Package;
  –15mm × 15mm, 0.5mm pitch 456pins BGA
  –21mm × 21mm, 0.8mm pitch 551pins BGA

Reference Board (Evaluation Kit)

The reference board of RZ/V2L has a SMARC v2.1 Module board + Carrier board configuration.



- Module board (Dimension: 82mm × 50mm)
  –Processor: RZ/V2L
  –Main Memory: 2GB DDR4 (2GB ×1)
  –QSPI NOR FLASH: 64MB
  –eMMC Memory: 64GB
  –External Storage: micro SD ×1
  –A/D Converter Interface x6
  –JTAG connector
  –PMIC (RAA215300) for RZ/V2L
- Carrier board (Dimension: 160mm × 100mm)
  –Gigabit Ethernet ×2
  –USB2.0 × 2ch (OTG ×1ch, Host ×1ch)
  –MIPI-CSI Camera connector
  (can connect to Google Coral Camera)
  –Micro HDMI (output) connector
  –CAN-FD ×2
  –External Storage: micro SD ×1
  –Audio Line in ×1
  –Audio Line out ×1
  –PMOD ×2
  –USB-Type C for Power Input

For More Information

For more details on RZ/V2L Group MPUs, please visit:
RZ/V2L: https://www.renesas.com/rzv2l

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Document No.: R01PF0214EJ0200