Platform for Embedded System in Package

PfESiP EP – 3

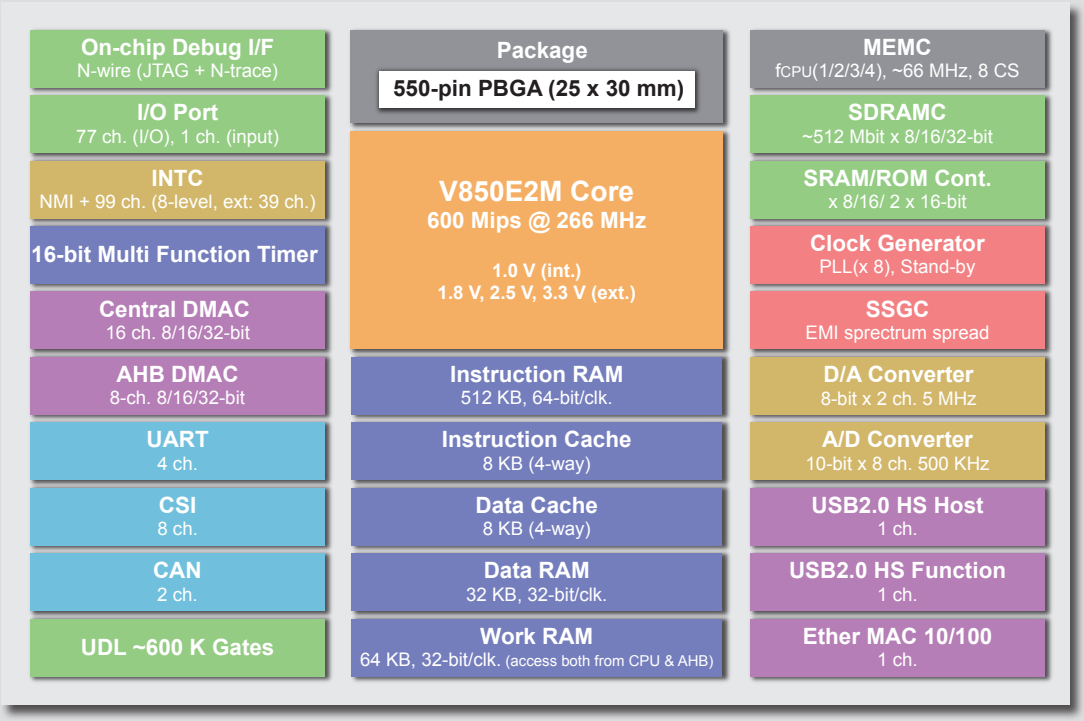
The PfESiP EP-3 is the new member of the Renesas PfESiP family. Conjuging the very high performances a V850E2M, which family is leader in 32-bit CPU, and a gate-array to aggregate application specific peripherals to the MCU thus allowing to spare space, costs and gain overall efficiency.

Result is a MCU build with the latest technologies to achieve high performances and calibrated to allow a high degree of customization in the most efficient way. Its embedded V850E2M is designed for high end application with performances up to 600 Mips. With this platform Renesas is proposing the 32-bit world leader CPU with an unmatched flexibility.

Features

- V850E2 CPU core, 600 Mips in operation
- CPU in 90 nm technology (CB-90)
- 1.0 V core voltage
- Low power consumption MCU: 1.5 W
- Internal AHB multilayer bus system
- USB2.0 HS (host and function)
- 10/100 Ethernet MAC
- On-board CAN, memory controller, UARTs, ADC, DAC…
- 32-bit external bus
- Large instruction RAM 512 KB
- Up to 600 K customizable gates
- 0.35 um embedded user defined logic (EA9HD)
- I/O voltage options: 1.8 V, 2.5 V, 3.3 V
- Low noise

Block Diagram



Product Outline

PfESiP – EP3	V850E2M	User Defined Logic (Default)
Technology	90 nm	0.35 µm (EA9HD technology)
Size	–	up to 600 K gates
Performance	600 MIPS	up to 100 MHz system frequency
External bus	32-bit	
Core V_{DD}	1.0 ± 0.1 V	3.3 V
Power consumption	1.5 W*	0.048 µW/MHz/gate**
I/O level	1.8 V, 2.5 V, 3.3 V	
Package	550 PBGA (Standard)	

* MCU in normal conditions ** 0.1 operation rate

Features

Technology (architecture). The EP3 offers a MCU based on V850E2M giving high real-time performances while having very low power consumption. The 90 nm technology used for the MCU allows both high integration rate, performances and low power consumption. Associated to the V850E2 architecture build around a main pipeline, it allows the system to work at 266 MHz for more than 600 Mips.

Meanwhile thanks to this excellent MHz/Mips ratio and the 90 nm technology, the power consumption for this MCU does not exceed 1.5 W in typical conditions.

High integration. In addition to the V850E2M, Renesas Electronics' PfESiP–EP3 embeds various functions: Memory controller, DMAC, UART, USB host & function, ADC, DAC, Ethernet MAC, CAN.

Furthermore, in order to be more flexible and provide even more integration, EP3 also includes a customizable part ready to receive any user defined logic. This part going up to 600 K gates can easily be used to integrate additional features such as more RAMs, I²C, PWM, or more simply some glue logic needed.

Thus the EP3 is completely adaptable to every applications needs. Result of this strategy for the final product is higher integration rate, smaller boards and lower unit cost than with standards products buy.

Low power consumption and low noise. Renesas' 90 nm technology allows mixing optimum transistors in order to reach targeted performance while lowering to the max power consumption. Thanks to this technology and an optimized design, power consumption of this embedded MCU (V850E2M) has been cut down to 1 W.

The standard technology chosen to receive the additional function is the famous Renesas' EA9HD (0.35 µm) which in addition to its flexibility also provides low noise performances.

Easy development. Versatile development boards embedding FPGA and peripherals (USB connector, Ethernet, RAM, ROM…) allow very simple and fast development phase. Once the FPGA is developed, Renesas Electronics will take care of the transfer into the PfESiP's UDL.

A large collection of pre-developed IPs is available in Renesas' libraries, allowing thus easy integration in the UDL and its fast development.

In addition complete support is provided by Renesas Electronics in a local fashion for both hardware and software development.

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