EMMA Mobile EV2 Data Sheet

Multimedia Processor for Mobile Applications

R19DS0010EJ1200
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DESCRIPTION

EMMA MobileTM EV2 (EM/EV2) is an application processor for mobile multimedia handset devices. EM/EV2 utilizes two ARM® Cortex-A9 cores with two Neon extensions, an integrated audio video engine (AV engine), and a 3D graphics block to enable high-class processing in a range of applications. The processor contains a wide variety of interfaces for cameras, displays, mass storage devices, memory devices, and many other peripherals.
EM/EV2 achieves high-performance multimedia processing of up to HD-level decoding by means of hardware acceleration, while consuming minimal power..

FEATURES

- CPU: ARM Cortex-A9 (Frequency: 533 MHz, I-cache: 32 KB, D-cache: 32 KB, L2 cache : 256KB)
- AV engine: High-performance multimedia processor
  - Video:
    - Decoder: Multi decoder (H.264, VC-1, MPEG 1/2, H.263, MPEG-4: up to 1080p 30fps), other decoders/encoders may be implemented by software using CPU resources
  - Audio:
    - Decoder: MPEG-4 HE-AAC decoder, enhanced aacPlus decoder
- 3D Graphics accelerator (A3D)
  - 3D: 14.7 Mpix/sec
    Supporting Open-GL-ES2.0, OpenGL-ES1.x
- Image processor: Resizing, rotating, image composing with alpha blending and key color masking
- Image composer: Image composing with alpha blending and key color masking, gamma correction
  - Direct connection to LCD interface
- Security functions: Secure boot function, secure timer, secure watchdog timer, secure DMA
- Internal memories: SRAM: 128 KB, ROM: 64 KB
- DMA controller: 8 channels
- Timers: Interval timers and watchdog timers: 15 channels
- DRAM interface:
  - LPDDR-SDRAM interface: Max 200 MHz DDR (DDR400), 32 bits, up to 1.6 GB/s
  - DDR2-SDRAM interface: Max 266 MHz DDR (DDR533), 32 bits, up to 2.1 GB/s
- NOR-Flash interface: 16-bit data bus
- Peripheral interfaces:
  - Memory card interface: SD card (with CPRM [Note]) × 1, SDIO × 3, CF card interface (Note : Option)
  - Image interfaces:
    - LCD interface → Parallel interface
    - ITU-R BT.656 interface
    - Camera interface → Parallel interface
  - Other serial interfaces:
    - USB 2.0 host × 1 and peripheral × 1 (with PHY)
    - UART × 4
    - I2C × 2
    - Unified serial interface × 6 (SPI, I2S)

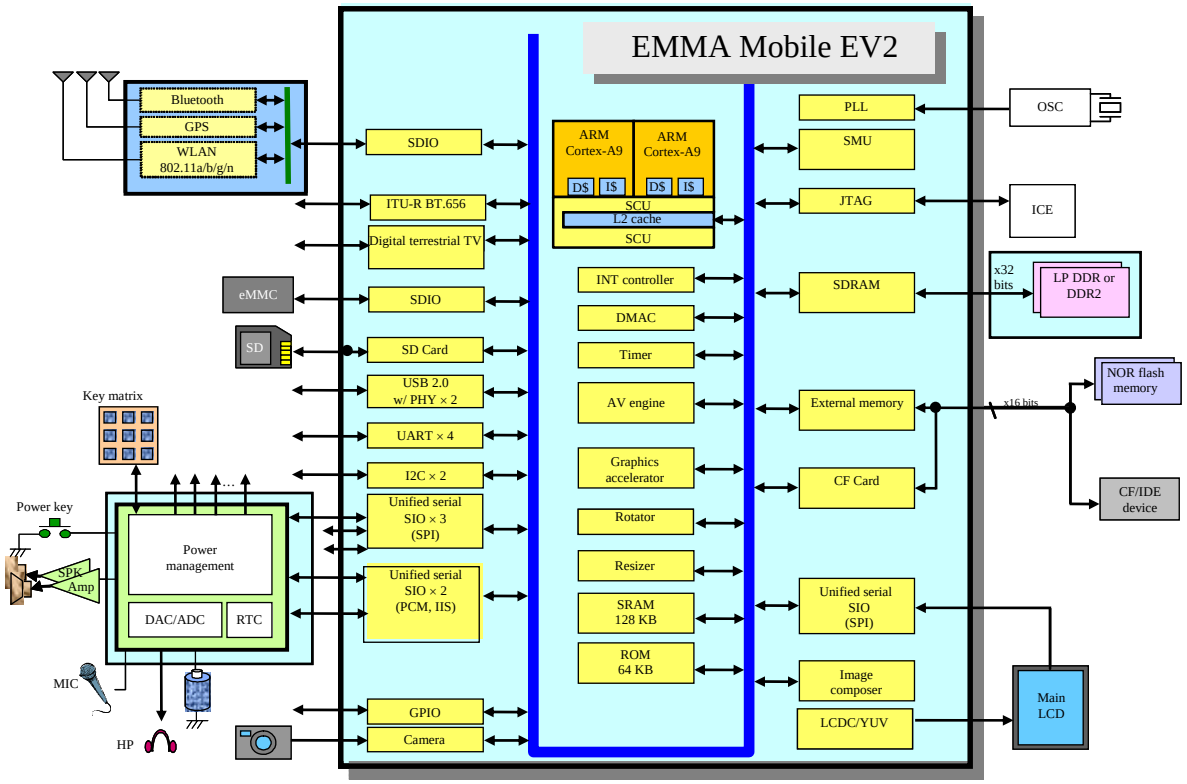
  - General-purpose I/O port interface × 159
- Testing and debugging: ARM CoreSight, JTAG

- Power supply voltage
  - Core Logic: 1.1V to 1.2 V
  - PLL: 1.1 V to 1.2V
  - IO power supply: 1.8 V, 3.3 V
- Power management
  Several power saving operation modes are supported.
- Package
  393-pin FPBGA package (16 × 16 mm), ball pitch: 0.65 mm

Order Information

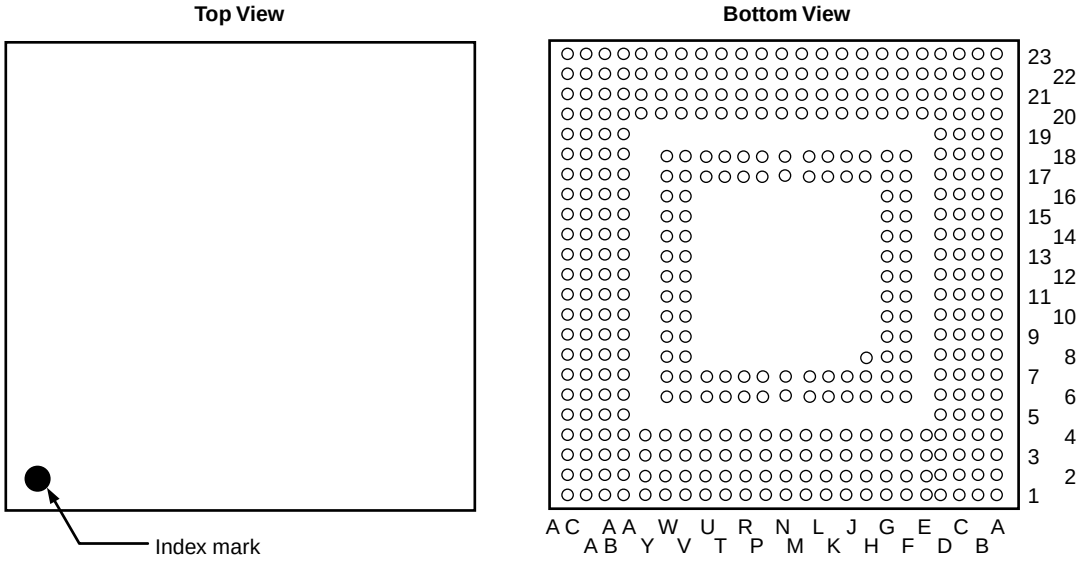
Part No.	Package Type
μPD77642BF1-GA9-A	393pin FPBGA (16mm×16mm, 0.65mm pitch)

BLOCK DIAGRAM



PIN LAYOUT

393-pin FPBGA (16×16mm, 0.65mm pitch)



PIN ASSIGNMENT

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Pin No.	Pin Name
A1	GND
A2	GND
A3	VDD33D
A4	AVDD
A5	C32K
A6	GND
A7	GND
A8	OSC0_XT2
A9	OSC0_XT1
A10	GND
A11	JT_TCK
A12	LOWPWR
A13	PONDET
A14	GND
A15	LCD3_B1
A16	LCD3_B0
A17	LCD3_G1
A18	LCD3_G0
A19	LCD3_R2
A20	LCD3_R0
A21	LCD3_CLK_I
A22	GND
A23	GND
B1	GND
B2	GND
B3	AFS_ARSTB
B4	AVDD
B5	GND
B6	USI0_CLK
B7	USI0_CS0
B8	USI0_CS1
B9	USI0_CS2
B10	USI0_DI
B11	USI0_DO
B12	SRESETB
B13	VDD18
B14	LCD3_B5
B15	LCD3_B2
B16	LCD3_G5

Pin No.	Pin Name
B17	LCD3_G2
B18	LCD3_R5
B19	LCD3_R3
B20	LCD3_R1
B21	LCD3_HS
B22	LCD3_PXCLK
B23	GND
C1	DDR_DQ7
C2	DDR_DQ0
C3	DDR_DQ2
C4	AGND
C5	NECTESTIO
C6	UTEST (When being unused, ”L” is fixed.)
C7	GND
C8	GND
C9	USI1_CLK
C10	USI1_DI
C11	JT_TRSTB
C12	NC (leave open)
C13	JT_TDI
C14	LCD3_B6
C15	LCD3_B3
C16	LCD3_G6
C17	LCD3_G3
C18	LCD3_R6
C19	LCD3_R4
C20	LCD3_VS
C21	GPIO_019
C22	AB_AD1
C23	AB_AD0
D1	DDR_DM0
D2	DDR_DQ4
D3	DDR_DQ6
D4	DDR_DQ1
D5	AGND
D6	TE1
D7	TE2
D8	GND
D9	GND

Pin No.	Pin Name
D10	USI1_DO
D11	USI1_CS0
D12	JT_DBG_EN
D13	JT_TDO
D14	LCD3_B7
D15	LCD3_B4
D16	LCD3_G7
D17	LCD3_G4
D18	LCD3_R7
D19	LCD3_DE
D20	GPIO_024
D21	AB_CSB0
D22	AB_AD3
D23	AB_AD2
E1	DDR_DQS0
E2	DDR_DQS0B
E3	DDR_DQ3
E4	DDR_DQ5
E20	GPIO_025
E21	AB_CSB1
E22	AB_AD5
E23	AB_AD4
F1	DDR_DQS1
F2	DDR_DQS1B
F3	DDR_GND
F4	DDR_VREFL
F6	DDR_VDDIO
F7	VDD33
F8	TRSTB
F9	VDD11
F10	VDD11
F11	BOOTSEL2
F12	BOOTSEL0
F13	JT_TDOEN
F14	JT_TMS
F15	VDD18
F16	GPIO_026
F17	GPIO_027
F18	GPIO_028

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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
F20	AB_CSB2	H20	AB_WRB	L17	AB_A27
F21	AB_AD8	H21	AB_AD14	L18	AB_A24
F22	AB_AD7	H22	AB_AD13	L20	AB_WAIT
F23	AB_AD6	H23	AB_AD12	L21	AB_A19
G1	DDR_DQ11	J1	DDR_A0	L22	HSI_ACREADY Note1
G2	DDR_DQ8	J2	DDR_A2	L23	HSI_CAFLAG Note1
G3	DDR_DM1	J3	DDR_GND	M1	DDR_CK
G4	DDR_DQ9	J4	DDR_DQ14	M2	DDR_CKB
G6	VDD11	J6	DDR_CS1B	M3	DDR_GND
G7	GND	J7	VDD11	M4	DDR_WEB
G8	VDD18	J17	VDD11	M6	DDR_ODT Note2
G9	GND	J18	GPIO_031	M7	GND
G10	GND	J20	AB_RDB	M17	AB_A28
G11	BOOTSEL1	J21	AB_A17	M18	AB_A25
G12	VDD33M	J22	AB_AD15	M20	AB_A22
G13	VDD11	J23	AB_CLK	M21	AB_A20
G14	GND	K1	DDR_BA2	M22	HSI_CAREADY Note1
G15	VDD33	K2	DDR_BA0	M23	HSI_ACFLAG Note1
G16	VDD11	K3	DDR_A3	N1	DDR_CKE1
G17	GND	K4	DDR_A10	N2	DDR_GND
G18	GPIO_029	K6	DDR_CASB	N3	DDR_A11
G20	AB_CSB3	K7	DDR_VDDIO	N4	DDR_A13
G21	AB_AD11	K17	VDD33	N6	DDR_CKERSTB
G22	AB_AD10	K18	VDD11	N7	DDR_VDDIO
G23	AB_AD9	K20	AB_ADV	N17	VDD18
H1	DDR_DQ12	K21	AB_A18	N18	AB_A26
H2	DDR_DQ15	K22	HSI_CAWAKE Note1	N20	AB_A23
H3	DDR_DQ13	K23	HSI_CADATA Note1	N21	AB_A21
H4	DDR_DQ10	L1	DDR_CKE0	N22	HSI_ACWAKE Note1
H6	DDR_VDDIO	L2	DDR_A14	N23	HSI_ACDATA Note1
H7	GND	L3	DDR_A1	P1	DDR_A12
H8	GND	L4	DDR_BA1	P2	DDR_A7
H17	VDD33	L6	DDR_RASB	P3	DDR_A8
H18	GPIO_030	L7	DDR_CS0B	P4	DDR_A6

Note1 The HSI function is not available.

Note2 The on die termination function for DDR-ODT is not available.

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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
P6	VDD11	U11	GND	Y1	DDR_DM3
P7	GND	U12	GND	Y2	DDR_DQ27
P17	VDD11	U13	VDD11	Y3	DDR_DQ25
P18	NTSC_DATA1	U14	VDD33	Y4	DDR_DQ29
P20	NTSC_DATA0	U15	VDD33	Y5	PWM1
P21	GND	U16	GND	Y6	USI2_CS2
P22	IC	U17	VDD18	Y7	USI2_CS0
P23	IC	U18	NTSC_DATA7	Y8	IIC1_SDA
R1	DDR_A9	U20	NTSC_DATA6	Y9	IIC1_SCL
R2	DDR_A5	U21	CAM_YUV3	Y10	UART1_TX
R3	DDR_A4	U22	CAM_YUV4	Y11	UART1_RX
R4	DDR_DQ20	U23	CAM_YUV5	Y12	SDI0_CMD
R6	DDR_VDDIO	V1	DDR_DQS2	Y13	SDI0_DATA1
R7	GND	V2	DDR_DQS2B	Y14	SDI0_DATA3
R17	VDD33	V3	DDR_GND	Y15	SDI0_DATA5
R18	NTSC_DATA3	V4	DDR_VREFH	Y16	SDI0_DATA7
R20	NTSC_DATA2	V6	VDD18	Y17	SD_DATA2
R21	GND	V7	VDD33M	Y18	SD_DATA0
R22	IC	V8	GPIO_004	Y19	GPIO_015
R23	IC	V9	GPIO_002	Y20	GPIO_014
T1	DDR_DQ16	V10	GPIO_000	Y21	GPIO_013
T2	DDR_DQ17	V11	VDD18	Y22	GND
T3	DDR_DQ22	V12	UART0_TX	Y23	CAM_CLKI
T4	DDR_DQ19	V13	UART0_RX	AA1	DDR_DQ24
T6	DDR_VDDIO	V14	VDD11	AA2	DDR_DQ28
T7	GND	V15	GPIO_009	AA3	DDR_DQ26
T17	VDD11	V16	GPIO_008	AA4	PWM0
T18	NTSC_DATA5	V17	GPIO_007	AA5	USI2_DO
T20	NTSC_DATA4	V18	GPIO_006	AA6	USI2_DI
T21	CAM_YUV0	V20	NTSC_CLK	AA7	USI2_CS1
T22	CAM_YUV1	V21	CAM_HS	AA8	IIC0_SDA
T23	CAM_YUV2	V22	CAM_YUV6	AA9	IIC0_SCL
U1	DDR_DQ21	V23	CAM_YUV7	AA10	UART1_CTSB
U2	DDR_DQ18	W1	DDR_DQS3	AA11	USB_GND11
U3	DDR_DQ23	W2	DDR_DQS3B	AA12	USB_VBUS
U4	DDR_DM2	W3	DDR_DQ31	AA13	SDI0_DATA0
U6	VDD11	W4	DDR_DQ30	AA14	SDI0_DATA2
U7	GND	W20	GPIO_017	AA15	SDI0_DATA4
U8	GPIO_005	W21	GPIO_016	AA16	SDI0_DATA6
U9	GPIO_003	W22	CAM_VS	AA17	SD_DATA3
U10	GPIO_001	W23	CAM_CLKO	AA18	SD_DATA1

Remark IC : Internally-connected pins (pull it down)

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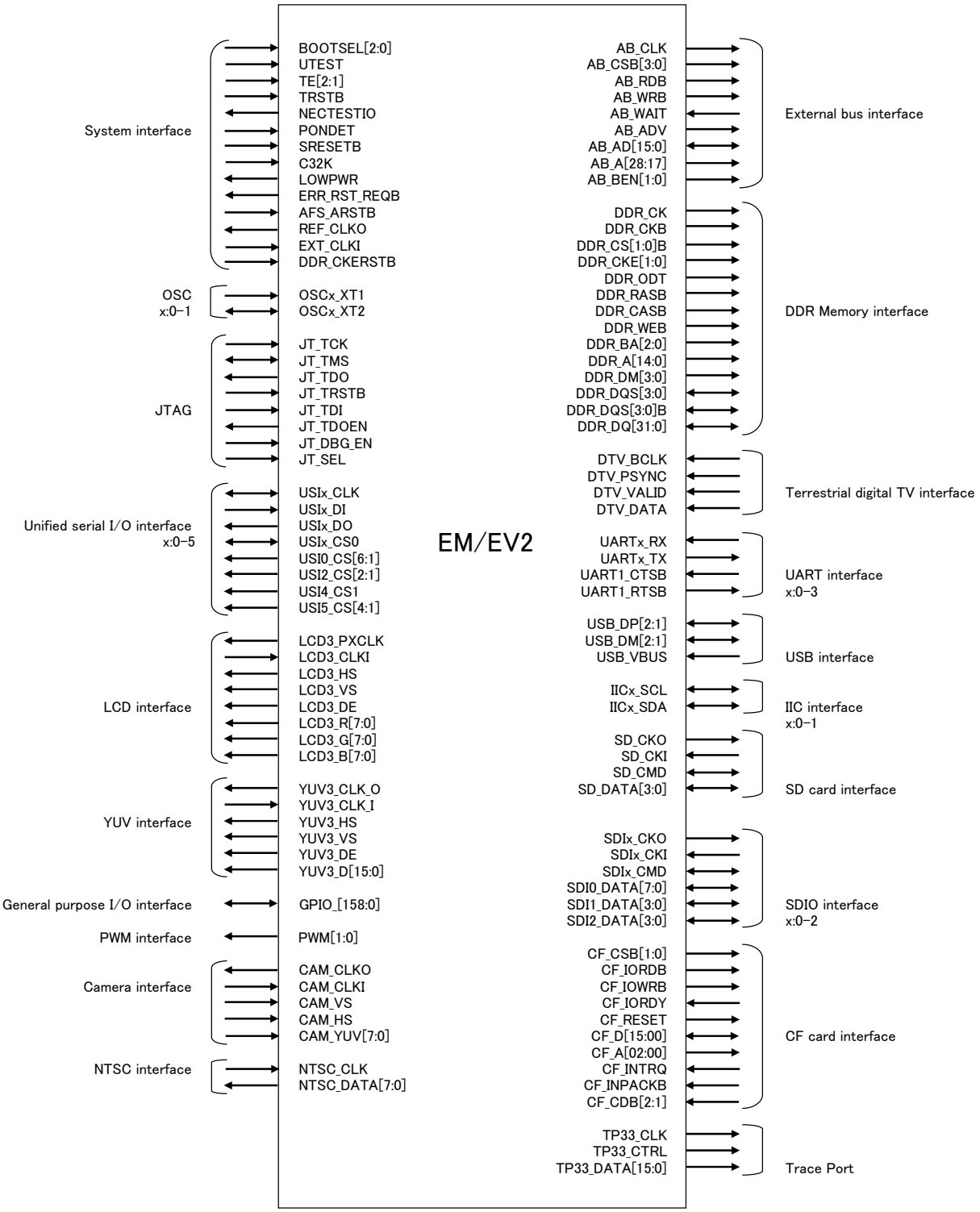
Pin No.	Pin Name
AA19	SDI1_DATA3
AA20	GPIO_012
AA21	GPIO_011
AA22	GPIO_010
AA23	SDI1_CKI
AB1	GND
AB2	GND
AB3	GPIO_119
AB4	USI3_CS0
AB5	USI2_CLK
AB6	USB_AVSS2
AB7	USB_PVSS2
AB8	USB_VD3312
AB9	USB_DP2
AB10	UART1_RTSB
AB11	USB_AVDD1
AB12	USB_AVSS1
AB13	USB_DP1
AB14	USB_VD3311
AB15	GND
AB16	GPIO_049
AB17	SD_CMD
AB18	SDI0_CKO
AB19	SDI1_DATA2
AB20	SDI1_DATA1
AB21	SDI1_DATA0
AB22	SDI1_CKO
AB23	GND
AC1	GND
AC2	GND
AC3	USI3_DO
AC4	USI3_DI
AC5	USI3_CLK
AC6	USB_AVDD2
AC7	USB_RREF2
AC8	USB_GND12
AC9	USB_DM2

Pin No.	Pin Name
AC10	USB_GND22
AC11	USB_RREF1
AC12	USB_PVSS1
AC13	USB_DM1
AC14	USB_GND21
AC15	OSC1_XT1
AC16	OSC1_XT2
AC17	GND
AC18	SDI0_CKI
AC19	SD_CKI
AC20	SD_CKO
AC21	SDI1_CMD
AC22	GND
AC23	GND

CONTENTS

1. PIN FUNCTIONS

1.1 Pin Configuration



1.2 Pin Functions

1.2.1 Boot select signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function	Buffer Type	Handling when not used
BOOTSEL2	F11	Input	Boot mode selection 2	VDD18	–	A	–
BOOTSEL1	G11	Input	Boot mode selection 1	VDD18	–	A	–
BOOTSEL0	F12	Input	Boot mode selection 0	VDD18	–	A	–

1.2.2 System control signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
UTEST	C6	Input	Test	VDD18	–	A	"L" level hold
TE1	D6	Input	Test	VDD18	–	N	Leave open
TE2	D7	Input	Test	VDD18	–	O	Leave open
TRSTB	F8	Input	Test	VDD18	–	C	Leave open
NECTESTIO	C5	Output	Test	VDD33	–	–	Leave open
PONDET	A13	Input	Power-on reset	VDD18	–	M	–
SRESETB	B12	Input	System reset	VDD18	–	D	–
C32K Note	A5	Input	32.768 kHz clock	VDD18	–	A	–
ERR_RST_REQB	U9	Output	Error reset request	VDD33M	**GPIO_003**	L	Leave open
LOWPWR	A12	Output	Low power control signal	VDD18	GPIO_154	E	Leave open
AFS_ARSTB	B3	Input	Antifuse asynchronous reset	VDD18	–	A	–
REF_CLKO	V8	Output	Reference clock input	VDD33M	**GPIO_004**	L	Leave open
EXT_CLKI	U8	Input	Reference clock output	VDD33M	**GPIO_005**	L	Leave open
DDR_CKERSTB	N6	Input	Clock reset input	DDR_VDDIO	–	U	–

Note input : schmitt

Remark AFS_ARSTB, DDR_CKERSTB : The same signal as PONDET is connected.

1.2.3 OSC signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function	Buffer Type	Handling when not used
OSC0_XT1	A9	Input	OSC input	VDD18	–	P	Leave open
OSC0_XT2	A8	I/O	OSC output	VDD18	–	P	Leave open
OSC1_XT1	AC15	Input	OSC input	VDD18	–	P	Leave open
OSC1_XT2	AC16	I/O	OSC output	VDD18	–	P	Leave open

1.2.4 JTAG signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function	Buffer Type	Handling when not used
JT_TCK	A11	Input	JTAG clock input	VDD18	–	C	Leave open
JT_TRSTB	C11	Input	JTAG reset input	VDD18	–	C	Leave open
JT_TMS	F14	I/O	JTAG test mode	VDD18	–	B	Leave open
JT_TDI	C13	Input	JTAG data input	VDD18	–	B	Leave open
JT_TDO	D13	Output	JTAG data output	VDD18	GPIO_151	E	Leave open
JT_TDOEN	F13	Output	JTAG data output enable	VDD18	GPIO_152	E	Leave open
JT_DBG_EN	D12	Input	JTAG debug enable	VDD18	–	C	Leave open
JT_SEL	V9	Input	JTAG select	VDD33M	GPIO_002	L	Leave open

1.2.5 External memory interface signals

(1/2)

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
AB_AD15	J22	I/O	Address/data bus bit 15	VDD33	SDI2_DATA3, CF_D15, **GPIO_092**	L2	Leave open
AB_AD14	H21	I/O	Address/data bus bit 14	VDD33	SDI2_DATA2, CF_D14, **GPIO_091**	L2	Leave open
AB_AD13	H22	I/O	Address/data bus bit 13	VDD33	SDI2_DATA1, CF_D13, USI5_CS2, **GPIO_090**	L2	Leave open
AB_AD12	H23	I/O	Address/data bus bit 12	VDD33	SDI2_DATA0, CF_D12, USI5_CS1, **GPIO_089**	L2	Leave open
AB_AD11	G21	I/O	Address/data bus bit 11	VDD33	DTV_DATA, CF_D11, USI5_CS0, **GPIO_088**	L2	Leave open
AB_AD10	G22	I/O	Address/data bus bit 10	VDD33	DTV_VALID, CF_D10, USI5_DO, **GPIO_087**	L2	Leave open
AB_AD9	G23	I/O	Address/data bus bit 9	VDD33	DTV_PSYNC, CF_D09, USI5_DI, **GPIO_086**	L2	Leave open
AB_AD8	F21	I/O	Address/data bus bit 8	VDD33	DTV_BCLK, CF_D08, USI5_CLK, **GPIO_085**	L2	Leave open
AB_AD7	F22	I/O	Address/data bus bit 7	VDD33	CF_D07, **GPIO_084**	L2	Leave open
AB_AD6	F23	I/O	Address/data bus bit 6	VDD33	CF_D06, **GPIO_083**	L2	Leave open
AB_AD5	E22	I/O	Address/data bus bit 5	VDD33	CF_D05, **GPIO_082**	L2	Leave open
AB_AD4	E23	I/O	Address/data bus bit 4	VDD33	CF_D04, **GPIO_081**	L2	Leave open
AB_AD3	D22	I/O	Address/data bus bit 3	VDD33	CF_D03, **GPIO_080**	L2	Leave open
AB_AD2	D23	I/O	Address/data bus bit 2	VDD33	CF_D02, **GPIO_079**	L2	Leave open
AB_AD1	C22	I/O	Address/data bus bit 1	VDD33	CF_D01, **GPIO_078**	L2	Leave open
AB_AD0	C23	I/O	Address/data bus bit 0	VDD33	CF_D00, **GPIO_077**	L2	Leave open
AB_A28	M17	Output	Address bus bit 26	VDD33	AB_BEN1, **GPIO_104**	H	Leave open
AB_A27	L17	Output	Address bus bit 26	VDD33	AB_BEN0, **GPIO_103**	H	Leave open
AB_A26	N18	Output	Address bus bit 26	VDD33	CF_CDB2, **GPIO_102**	H	Leave open
AB_A25	M18	Output	Address bus bit 25	VDD33	CF_CDB1, **GPIO_101**	H	Leave open

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Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
AB_A24	L18	Output	Address bus bit 24	VDD33	CF_INPACKB, **GPIO_100**	H	Leave open
AB_A23	N20	Output	Address bus bit 23	VDD33	SDI2_CMD, **GPIO_099**	H	Leave open
AB_A22	M20	Output	Address bus bit 22	VDD33	SDI2_CKI, **GPIO_098**	H	Leave open
AB_A21	N21	Output	Address bus bit 21	VDD33	SDI2_CKO, CF_INTRQ, **GPIO_097**	H	Leave open
AB_A20	M21	Output	Address bus bit 20	VDD33	**GPIO_096**	H	Leave open
AB_A19	L21	Output	Address bus bit 19	VDD33	CF_A02, **GPIO_095**	L	Leave open
AB_A18	K21	Output	Address bus bit 18	VDD33	CF_A01, **GPIO_094**	L	Leave open
AB_A17	J21	Output	Address bus bit 17	VDD33	CF_A00, **GPIO_093**	L	Leave open
AB_RDB	J20	Output	Read strobe	VDD33	CF_IORDB, **GPIO_073**	H	Leave open
AB_WRB	H20	Output	Write strobe	VDD33	CF_IOWRB, **GPIO_074**	H	Leave open
AB_ADV	K20	Output	Address valid	VDD33	CF_RESET, **GPIO_076**	H	Leave open
AB_WAIT	L20	Input	Wait	VDD33	CF_IORDY, **GPIO_075**	H	Leave open
AB_CSB3	G20	Output	Chip select 3	VDD33	CF_CSB1, **GPIO_072**	H	Leave open
AB_CSB2	F20	Output	Chip select 2	VDD33	CF_CSB0, **GPIO_071**	H	Leave open
AB_CSB1	E21	Output	Chip select 1	VDD33	**GPIO_070**	F	Leave open
AB_CSB0	D21	Output	Chip select 0	VDD33	**GPIO_069**	F	Leave open
AB_CLK	J23	Output	Bus clock output	VDD33	**GPIO_068**	L	Leave open
AB_BEN1	M17	Output	Byte enable	VDD33	**GPIO_104**	H	Leave open
AB_BEN0	L17	Output	Byte enable	VDD33	**GPIO_103**	H	Leave open

1.2.6 DDR SDRAM interface signals

(1/2)

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function	Buffer Type	Handling when not used
DDR_A14	L2	Output	Command/address bit 14	DDR_VDDIO	–	Q	Leave open
DDR_A13	N4	Output	Command/address bit 13	DDR_VDDIO	–	Q	Leave open
DDR_A12	P1	Output	Command/address bit 12	DDR_VDDIO	–	Q	Leave open
DDR_A11	N3	Output	Command/address bit 11	DDR_VDDIO	–	Q	Leave open
DDR_A10	K4	Output	Command/address bit 10	DDR_VDDIO	–	Q	Leave open
DDR_A9	R1	Output	Command/address bit 9	DDR_VDDIO	–	Q	Leave open
DDR_A8	P3	Output	Command/address bit 8	DDR_VDDIO	–	Q	Leave open
DDR_A7	P2	Output	Command/address bit 7	DDR_VDDIO	–	Q	Leave open
DDR_A6	P4	Output	Command/address bit 6	DDR_VDDIO	–	Q	Leave open
DDR_A5	R2	Output	Command/address bit 5	DDR_VDDIO	–	Q	Leave open
DDR_A4	R3	Output	Command/address bit 4	DDR_VDDIO	–	Q	Leave open
DDR_A3	K3	Output	Command/address bit 3	DDR_VDDIO	–	Q	Leave open
DDR_A2	J2	Output	Command/address bit 2	DDR_VDDIO	–	Q	Leave open
DDR_A1	L3	Output	Command/address bit 1	DDR_VDDIO	–	Q	Leave open
DDR_A0	J1	Output	Command/address bit 0	DDR_VDDIO	–	Q	Leave open
DDR_CS0B	L7	Output	Chip select 0	DDR_VDDIO	–	Q	Leave open
DDR_CS1B	J6	Output	Chip select 1	DDR_VDDIO	–	Q	Leave open
DDR_CK	M1	Output	Clock +	DDR_VDDIO	–	R	Leave open
DDR_CKB	M2	Output	Clock –	DDR_VDDIO	–	R	Leave open
DDR_CKE0	L1	Output	Clock enable 0	DDR_VDDIO	–	Q	Leave open
DDR_CKE1	N1	Output	Clock enable 1	DDR_VDDIO	–	Q	Leave open
DDR_DM3	Y1	I/O	Data mask bit 3	DDR_VDDIO	–	S	Leave open
DDR_DM2	U4	I/O	Data mask bit 2	DDR_VDDIO	–	S	Leave open
DDR_DM1	G3	I/O	Data mask bit 1	DDR_VDDIO	–	S	Leave open
DDR_DM0	D1	I/O	Data mask bit 0	DDR_VDDIO	–	S	Leave open
DDR_DQ31	W3	I/O	Data bit 31	DDR_VDDIO	–	S	Leave open
DDR_DQ30	W4	I/O	Data bit 30	DDR_VDDIO	–	S	Leave open
DDR_DQ29	Y4	I/O	Data bit 29	DDR_VDDIO	–	S	Leave open
DDR_DQ28	AA2	I/O	Data bit 28	DDR_VDDIO	–	S	Leave open
DDR_DQ27	Y2	I/O	Data bit 27	DDR_VDDIO	–	S	Leave open
DDR_DQ26	AA3	I/O	Data bit 26	DDR_VDDIO	–	S	Leave open
DDR_DQ25	Y3	I/O	Data bit 25	DDR_VDDIO	–	S	Leave open
DDR_DQ24	AA1	I/O	Data bit 24	DDR_VDDIO	–	S	Leave open
DDR_DQ23	U3	I/O	Data bit 23	DDR_VDDIO	–	S	Leave open
DDR_DQ22	T3	I/O	Data bit 22	DDR_VDDIO	–	S	Leave open
DDR_DQ21	U1	I/O	Data bit 21	DDR_VDDIO	–	S	Leave open
DDR_DQ20	R4	I/O	Data bit 20	DDR_VDDIO	–	S	Leave open
DDR_DQ19	T4	I/O	Data bit 19	DDR_VDDIO	–	S	Leave open
DDR_DQ18	U2	I/O	Data bit 18	DDR_VDDIO	–	S	Leave open

(2/2)

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function	Buffer Type	Handling when not used
DDR_DQ17	T2	I/O	Data bit 17	DDR_VDDIO	–	S	Leave open
DDR_DQ16	T1	I/O	Data bit 16	DDR_VDDIO	–	S	Leave open
DDR_DQ15	H2	I/O	Data bit 15	DDR_VDDIO	–	S	Leave open
DDR_DQ14	J4	I/O	Data bit 14	DDR_VDDIO	–	S	Leave open
DDR_DQ13	H3	I/O	Data bit 13	DDR_VDDIO	–	S	Leave open
DDR_DQ12	H1	I/O	Data bit 12	DDR_VDDIO	–	S	Leave open
DDR_DQ11	G1	I/O	Data bit 11	DDR_VDDIO	–	S	Leave open
DDR_DQ10	H4	I/O	Data bit 10	DDR_VDDIO	–	S	Leave open
DDR_DQ9	G4	I/O	Data bit 9	DDR_VDDIO	–	S	Leave open
DDR_DQ8	G2	I/O	Data bit 8	DDR_VDDIO	–	S	Leave open
DDR_DQ7	C1	I/O	Data bit 7	DDR_VDDIO	–	S	Leave open
DDR_DQ6	D3	I/O	Data bit 6	DDR_VDDIO	–	S	Leave open
DDR_DQ5	E4	I/O	Data bit 5	DDR_VDDIO	–	S	Leave open
DDR_DQ4	D2	I/O	Data bit 4	DDR_VDDIO	–	S	Leave open
DDR_DQ3	E3	I/O	Data bit 3	DDR_VDDIO	–	S	Leave open
DDR_DQ2	C3	I/O	Data bit 2	DDR_VDDIO	–	S	Leave open
DDR_DQ1	D4	I/O	Data bit 1	DDR_VDDIO	–	S	Leave open
DDR_DQ0	C2	I/O	Data bit 0	DDR_VDDIO	–	S	Leave open
DDR_DQS3	W1	I/O	Data strobe bit 3 +	DDR_VDDIO	–	T	Leave open
DDR_DQS3B	W2	I/O	Data strobe bit 3 –	DDR_VDDIO	–	T	Leave open
DDR_DQS2	V1	I/O	Data strobe bit 2 +	DDR_VDDIO	–	T	Leave open
DDR_DQS2B	V2	I/O	Data strobe bit 2 –	DDR_VDDIO	–	T	Leave open
DDR_DQS1	F1	I/O	Data strobe bit 1 +	DDR_VDDIO	–	T	Leave open
DDR_DQS1B	F2	I/O	Data strobe bit 1 –	DDR_VDDIO	–	T	Leave open
DDR_DQS0	E1	I/O	Data strobe bit 0 +	DDR_VDDIO	–	T	Leave open
DDR_DQS0B	E2	I/O	Data strobe bit 0 –	DDR_VDDIO	–	T	Leave open
DDR_RASB	L6	Output	RAS	DDR_VDDIO	–	Q	Leave open
DDR_CASB	K6	Output	CAS	DDR_VDDIO	–	Q	Leave open
DDR_WEB	M4	Output	Write enable	DDR_VDDIO	–	Q	Leave open
DDR_BA2	K1	Output	Bank address bit 2	DDR_VDDIO	–	Q	Leave open
DDR_BA1	L4	Output	Bank address bit 1	DDR_VDDIO	–	Q	Leave open
DDR_BA0	K2	Output	Bank address bit 0	DDR_VDDIO	–	Q	Leave open
DDR_ODT Note	M6	Output	On-die termination	DDR_VDDIO	–	Q	Leave open

Note : The on die termination function for DDR-ODT is not available.

1.2.7 Unified serial interface port 0 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
USI0_DI	B10	Input	Port 0 data input	VDD33M	–	L	Leave open
USI0_DO	B11	Output	Port 0 data output	VDD33M	–	L	Leave open
USI0_CLK	B6	I/O	Port 0 clock input/output	VDD33M	–	L	Leave open
USI0_CS6	AB4	Output	Port 0 CS6	VDD33M	USI3_CS0, **GPIO_118**	L	Leave open
USI0_CS5	AC3	Output	Port 0 CS5	VDD33M	USI3_DO, **GPIO_117**	L	Leave open
USI0_CS4	AC4	Output	Port 0 CS4	VDD33M	USI3_DI, **GPIO_116**	L	Leave open
USI0_CS3	AC5	Output	Port 0 CS3	VDD33M	USI3_CLK, **GPIO_115**	L	Leave open
USI0_CS2	B9	Output	Port 0 CS2	VDD33M	**GPIO_106**	L	Leave open
USI0_CS1	B8	Output	Port 0 CS1	VDD33M	**GPIO_105**	L	Leave open
USI0_CS0	B7	I/O	Port 0 CS0	VDD33M	–	L	Leave open

1.2.8 Unified serial interface port 1 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function	Buffer Type	Handling when not used
USI1_DI	C10	Input	Port 1 data input	VDD33M	GPIO_107	J	Leave open
USI1_DO	D10	Output	Port 1 data output	VDD33M	GPIO_108	J	Leave open
USI1_CLK	C9	I/O	Port 1 clock input/output	VDD33M	–	J	Leave open
USI1_CS0	D11	I/O	Port 1 CS0	VDD33M	–	J	Leave open

1.2.9 Unified serial interface port 2 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
USI2_DI	AA6	Input	Port 2 data input	VDD33M	DTV_PSYNC, GPIO_110	L	Leave open
USI2_DO	AA5	Output	Port 2 data output	VDD33M	DTV_VALID, GPIO_111	L	Leave open
USI2_CLK	AB5	I/O	Port 2 clock input/output	VDD33M	DTV_BCLK, GPIO_109	L	Leave open
USI2_CS2	Y6	Output	Port 2 CS2	VDD33M	USI4_CS1, **GPIO_114**	L	Leave open
USI2_CS1	AA7	Output	Port 2 CS1	VDD33M	USI4_CS0, **GPIO_113**	L	Leave open
USI2_CS0	Y7	I/O	Port 2 CS0	VDD33M	DTV_DATA, GPIO_112	L	Leave open

1.2.10 Unified serial interface port 3 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
USI3_DI	AC4	Input	Port 3 data input	VDD33M	USI0_CS4, **GPIO_116**	L	Leave open
USI3_DO	AC3	Output	Port 3 data output	VDD33M	USI0_CS5, **GPIO_117**	L	Leave open
USI3_CLK	AC5	I/O	Port 3 clock input/output	VDD33M	USI0_CS3, **GPIO_115**	L	Leave open
USI3_CS0	AB4	I/O	Port 3 CS0	VDD33M	USI0_CS6, **GPIO_118**	L	Leave open

1.2.11 Unified serial interface port 4 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
USI4_DI	AA4	Input	Port 4 data input	VDD33M	PWM0, **GPIO_120**	L	Leave open
USI4_DO	Y5	Output	Port 4 data output	VDD33M	PWM1, **GPIO_121**	L	Leave open
USI4_CLK	AB3	I/O	Port 4 clock input/output	VDD33M	**GPIO_119**	L	Leave open
USI4_CS1	Y6	Output	Port 4 CS1	VDD33M	USI2_CS2, **GPIO_114**	L	Leave open
USI4_CS0	AA7	I/O	Port 4 CS0	VDD33M	USI2_CS1, **GPIO_113**	L	Leave open

1.2.12 Unified serial interface port 5 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
USI5_DI	G23	Input	Port 5 data input	VDD33	AB_AD9, DTV_PSYNC, CF_D09, **GPIO_086**	L2	Leave open
	M22			VDD18	**GPIO_150**	C	Leave open
USI5_DO	G22	Output	Port 5 data output	VDD33	AB_AD10, DTV_VALID, CF_D10, **GPIO_087**	L2	Leave open
	K23			VDD18	**GPIO_144**	C	Leave open
USI5_CLK	F21	I/O	Port 5 clock input/output	VDD33	AB_AD8, DTV_BCLK, CF_D08, **GPIO_085**	L2	Leave open
	K22			VDD18	**GPIO_143**	C	Leave open
USI5_CS4	M23	Output	Port 5 CS4	VDD18	**GPIO_149**	C	Leave open
USI5_CS3	N23	Output	Port 5 CS3	VDD18	**GPIO_148**	C	Leave open
USI5_CS2	H22	Output	Port 5 CS2	VDD33	AB_AD13, SDI2_DATA1, CF_D13, **GPIO_090**	L2	Leave open
	N22			VDD18	**GPIO_147**	C	Leave open
USI5_CS1	H23	Output	Port 5 CS1	VDD33	AB_AD12, SDI2_DATA0, CF_D12, **GPIO_089**	L2	Leave open
	L22			VDD18	**GPIO_146**	C	Leave open
USI5_CS0	G21	I/O	Port 5 CS0	VDD33	AB_AD11, DTV_DATA, CF_D11, **GPIO_088**	L2	Leave open
	L23			VDD18	**GPIO_145**	C	Leave open

1.2.13 Digital terrestrial TV interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
DTV_BCLK	F21	Input	DTV clock input	VDD33	AB_AD8, CF_D08, USI5_CLK, **GPIO_085**	L2	Leave open
	AB5			VDD33M	**USI2_CLK**, GPIO_109	L	Leave open
DTV_PSYNC	G23	Input	DTV sync.	VDD33	AB_AD9, CF_D09, USI5_DI, **GPIO_086**	L2	Leave open
	AA6			VDD33M	**USI2_DI,** GPIO_110	L	Leave open
DTV_VALID	G22	Input	DTV valid	VDD33	AB_AD10, CF_D10, USI5_DO, **GPIO_087**	L2	Leave open
	AA5			VDD33M	**USI2_DO**, GPIO_111	L	Leave open
DTV_DATA	G21	Input	DTV data input	VDD33	AB_AD11, CF_D11, USI5_CS0, **GPIO_088**	L2	Leave open
	Y7			VDD33M	**USI2_CS0**, GPIO_112	L	Leave open

1.2.14 UART interface port 0 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function	Buffer Type	Handling when not used
UART0_RX	V13	Input	Port 0 SIN	VDD33M	–	J	Leave open
UART0_TX	V12	Output	Port 0 SOUT	VDD33M	–	I	Leave open

1.2.15 UART interface port 1 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
UART1_RX	Y11	Input	Port 1 SIN	VDD33M	**GPIO_155**	J	Leave open
UART1_TX	Y10	Output	Port 1 SOUT	VDD33M	**GPIO_156**	K	Leave open
UART1_RTSB	AB10	Output	Port 1 RTS	VDD33M	UART2_TX,**GPIO_158**	K	Leave open
UART1_CTSB	AA10	Input	Port 1 CTS	VDD33M	UART2_RX,**GPIO_157**	J	Leave open

1.2.16 UART interface port 2 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
UART2_RX	AA10	Input	Port 2 SIN	VDD33M	UART1_CTSB, **GPIO_157**	J	Leave open
UART2_TX	AB10	Output	Port 2 SOUT	VDD33M	UART1_RTSB, **GPIO_158**	K	Leave open

1.2.17 UART interface port 3 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
UART3_RX	Y9	Input	Port 3 SIN	VDD33M	**IIC1_SCL**, GPIO_046	K	Leave open
UART3_TX	Y8	Output	Port 3 SOUT	VDD33M	**IIC1_SDA**, GPIO_047	K	Leave open

1.2.18 USB interface port1 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function	Buffer Type	Handling when not used
USB_DP1	AB13	I/O	USB port1 data input/output	USB_VD3311	–	Note	Leave open
USB_DM1	AC13	I/O	USB port 1data input/output	USB_VD3311	–	Note	Leave open

Note : Refer to USB Specification Revision 2.0.

1.2.19 USB interface port2 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function	Buffer Type	Handling when not used
USB_DP2	AB9	I/O	USB port2 data input/output	USB_VD3312	–	Note	Leave open
USB_DM2	AC9	I/O	USB port 2data input/output	USB_VD3312	–	Note	Leave open
USB_VBUS	AA12	Input	USB VBUS	USB_VD3312	GPIO_153	H	Leave open

Note : Refer to USB Specification Revision 2.0.

1.2.20 I2C interface port 0 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function	Buffer Type	Handling when not used
IIC0_SCL	AA9	I/O	IIC0 clock	VDD33M	GPIO_044	K	Leave open
IIC0_SDA	AA8	I/O	IIC0 data	VDD33M	GPIO_045	K	Leave open

1.2.21 I2C interface port 1 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function	Buffer Type	Handling when not used
IIC1_SCL	Y9	I/O	IIC1 clock	VDD33M	UART3_RX, GPIO_046	K	Leave open
IIC1_SDA	Y8	I/O	IIC1 data	VDD33M	UART3_TX, GPIO_047	K	Leave open

1.2.22 LCD interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
LCD3_PXCLK	B22	Output	Pixel clock	VDD33	YUV3_CLK_O, **GPIO_018**	L	Leave open
LCD3_CLK_I	A21	Input	Clock input	VDD33	YUV3_CLK_I, **GPIO_020**	L	Leave open
LCD3_HS	B21	Output	H sync	VDD33	YUV3_HS, **GPIO_021**	L	Leave open
LCD3_VS	C20	Output	V sync	VDD33	YUV3_VS, **GPIO_022**	L	Leave open
LCD3_DE	D19	Output	Enable	VDD33	YUV3_DE, **GPIO_023**	L	Leave open
LCD3_R7	D18	Output	Red 7	VDD33	TP33_CTRL, **GPIO_039**	L	Leave open
LCD3_R6	C18	Output	Red 6	VDD33	TP33_CLK, **GPIO_038**	L	Leave open
LCD3_R5	B18	Output	Red 5	VDD33	**GPIO_037**	L	Leave open
LCD3_R4	C19	Output	Red 4	VDD33	**GPIO_036**	L	Leave open
LCD3_R3	B19	Output	Red 3	VDD33	**GPIO_035**	L	Leave open
LCD3_R2	A19	Output	Red 2	VDD33	**GPIO_034**	L	Leave open
LCD3_R1	B20	Output	Red 1	VDD33	**GPIO_033**	L	Leave open
LCD3_R0	A20	Output	Red 0	VDD33	**GPIO_032**	L	Leave open
LCD3_G7	D16	Output	Green 7	VDD33	YUV3_D7, TP33_DATA7	L	Leave open
LCD3_G6	C16	Output	Green 6	VDD33	YUV3_D6, TP33_DATA6	L	Leave open
LCD3_G5	B16	Output	Green 5	VDD33	YUV3_D5, TP33_DATA5	L	Leave open
LCD3_G4	D17	Output	Green 4	VDD33	YUV3_D4, TP33_DATA4	L	Leave open
LCD3_G3	C17	Output	Green 3	VDD33	YUV3_D3, TP33_DATA3	L	Leave open
LCD3_G2	B17	Output	Green 2	VDD33	YUV3_D2, TP33_DATA2	L	Leave open
LCD3_G1	A17	Output	Green 1	VDD33	YUV3_D1, TP33_DATA1, **GPIO_041**	L	Leave open
LCD3_G0	A18	Output	Green 0	VDD33	YUV3_D0, TP33_DATA0, **GPIO_040**	L	Leave open
LCD3_B7	D14	Output	Blue 7	VDD33	YUV3_D15, TP33_DATA15	L	Leave open
LCD3_B6	C14	Output	Blue 6	VDD33	YUV3_D14, TP33_DATA14	L	Leave open
LCD3_B5	B14	Output	Blue 5	VDD33	YUV3_D13, TP33_DATA13	L	Leave open
LCD3_B4	D15	Output	Blue 4	VDD33	YUV3_D12, TP33_DATA12	L	Leave open
LCD3_B3	C15	Output	Blue 3	VDD33	YUV3_D11, TP33_DATA11	L	Leave open
LCD3_B2	B15	Output	Blue 2	VDD33	YUV3_D10, TP33_DATA10	L	Leave open
LCD3_B1	A15	Output	Blue 1	VDD33	YUV3_D9, TP33_DATA9, **GPIO_043**	L	Leave open
LCD3_B0	A16	Output	Blue 0	VDD33	YUV3_D8, TP33_DATA8, **GPIO_042**	L	Leave open

1.2.23 YUV interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
YUV3_D15	D14	Output	Data bit 15	VDD33	**LCD3_B7**, TP33_DATA15	L	Leave open
YUV3_D14	C14	Output	Data bit 14	VDD33	**LCD3_B6**, TP33_DATA14	L	Leave open
YUV3_D13	B14	Output	Data bit 13	VDD33	**LCD3_B5**, TP33_DATA13	L	Leave open
YUV3_D12	D15	Output	Data bit 12	VDD33	**LCD3_B4**, TP33_DATA12	L	Leave open
YUV3_D11	C15	Output	Data bit 11	VDD33	**LCD3_B3**, TP33_DATA11	L	Leave open
YUV3_D10	B15	Output	Data bit 10	VDD33	**LCD3_B2**, TP33_DATA10	L	Leave open
YUV3_D9	A15	Output	Data bit 9	VDD33	LCD3_B1, TP33_DATA9, **GPIO_043**	L	Leave open
YUV3_D8	A16	Output	Data bit 8	VDD33	LCD3_B0, TP33_DATA8, **GPIO_042**	L	Leave open
YUV3_D7	D16	Output	Data bit 7	VDD33	**LCD3_G7**, TP33_DATA7	L	Leave open
YUV3_D6	C16	Output	Data bit 6	VDD33	**LCD3_G6**, TP33_DATA6	L	Leave open
YUV3_D5	B16	Output	Data bit 5	VDD33	**LCD3_G5**, TP33_DATA5	L	Leave open
YUV3_D4	D17	Output	Data bit 4	VDD33	**LCD3_G4**, TP33_DATA4	L	Leave open
YUV3_D3	C17	Output	Data bit 3	VDD33	**LCD3_G3**, TP33_DATA3	L	Leave open
YUV3_D2	B17	Output	Data bit 2	VDD33	**LCD3_G2**, TP33_DATA2	L	Leave open
YUV3_D1	A17	Output	Data bit 1	VDD33	LCD3_G1, TP33_DATA1, **GPIO_041**	L	Leave open
YUV3_D0	A18	Output	Data bit 0	VDD33	LCD3_G0, TP33_DATA0, **GPIO_040**	L	Leave open
YUV3_CLK_O	B22	Output	Clock	VDD33	LCD3_PXCLK, **GPIO_018**	L	Leave open
YUV3_CLK_I	A21	Input	Clock	VDD33	LCD3_CLK_I, **GPIO_020**	L	Leave open
YUV3_HS	B21	Output	Hsync	VDD33	LCD3_HS, **GPIO_021**	L	Leave open
YUV3_VS	C20	Output	Vsync	VDD33	LCD3_VS, **GPIO_022**	L	Leave open
YUV3_DE	D19	Output	Enable	VDD33	LCD3_DE, **GPIO_023**	L	Leave open

1.2.24 SD card interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function	Buffer Type	Handling when not used
SD_CKO	AC20	Output	SD card clock output	VDD33	–	L	Leave open
SD_CKI	AC19	Input	SD card clock input	VDD33	GPIO_048	L	Leave open
SD_CMD	AB17	I/O	SD card command	VDD33	–	L	Leave open
SD_DATA3	AA17	I/O	SD card data bit 3	VDD33	–	L	Leave open
SD_DATA2	Y17	I/O	SD card data bit 2	VDD33	–	L	Leave open
SD_DATA1	AA18	I/O	SD card data bit 1	VDD33	–	L	Leave open
SD_DATA0	Y18	I/O	SD card data bit 0	VDD33	–	L	Leave open

1.2.25 SDIO interface port 0 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
SDI0_CMD	Y12	I/O	SDIO0 command	VDD33	GPIO_052	L	Leave open
SDI0_DATA7	Y16	I/O	SDIO0 data bit 7	VDD33	**GPIO_060**	L	Leave open
SDI0_DATA6	AA16	I/O	SDIO0 data bit 6	VDD33	**GPIO_059**	L	Leave open
SDI0_DATA5	Y15	I/O	SDIO0 data bit 5	VDD33	**GPIO_058**	L	Leave open
SDI0_DATA4	AA15	I/O	SDIO0 data bit 4	VDD33	**GPIO_057**	L	Leave open
SDI0_DATA3	Y14	I/O	SDIO0 data bit 3	VDD33	GPIO_056	L	Leave open
SDI0_DATA2	AA14	I/O	SDIO0 data bit 2	VDD33	GPIO_055	L	Leave open
SDI0_DATA1	Y13	I/O	SDIO0 data bit 1	VDD33	GPIO_054	L	Leave open
SDI0_DATA0	AA13	I/O	SDIO0 data bit 0	VDD33	GPIO_053	L	Leave open
SDI0_CKO	AB18	Output	SDIO0 clock output	VDD33	**GPIO_050**	L	Leave open
SDI0_CKI	AC18	Input	SDIO0 clock input	VDD33	GPIO_051	L	Leave open

1.2.26 SDIO interface port 1 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
SDI1_CMD	AC21	I/O	SDIO1 CMD	VDD33	GPIO_063	L	Leave open
SDI1_DATA3	AA19	I/O	SDIO1 data bit 3	VDD33	GPIO_067	L	Leave open
SDI1_DATA2	AB19	I/O	SDIO1 data bit 2	VDD33	GPIO_066	L	Leave open
SDI1_DATA1	AB20	I/O	SDIO1 data bit 1	VDD33	GPIO_065	L	Leave open
SDI1_DATA0	AB21	I/O	SDIO1 data bit 0	VDD33	GPIO_064	L	Leave open
SDI1_CKO	AB22	Output	SDIO1 clock output	VDD33	**GPIO_061**	L	Leave open
SDI1_CKI	AA23	Input	SDIO1 clock input	VDD33	GPIO_062	L	Leave open

1.2.27 SDIO interface port 2 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
SDI2_CMD	N20	I/O	SDIO2 command	VDD33	AB_A23, **GPIO_099**	H	Leave open
SDI2_DATA3	J22	I/O	SDIO2 data bit 3	VDD33	AB_AD15, CF_D15, **GPIO_092**	L2	Leave open
SDI2_DATA2	H21	I/O	SDIO2 data bit 2	VDD33	AB_AD14, CF_D14, **GPIO_091**	L2	Leave open
SDI2_DATA1	H22	I/O	SDIO2 data bit 1	VDD33	AB_AD13, CF_D13, USI5_CS2, **GPIO_090**	L2	Leave open
SDI2_DATA0	H23	I/O	SDIO2 data bit 0	VDD33	AB_AD12, CF_D12, USI5_CS1, **GPIO_089**	L2	Leave open
SDI2_CKO	N21	Output	SDIO2 clock output	VDD33	AB_A21, CF_INTRQ, **GPIO_097**	H	Leave open
SDI2_CKI	M20	Input	SDIO2 clock input	VDD33	AB_A22, **GPIO_098**	H	Leave open

1.2.28 CF card interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
CF_D15	J22	I/O	CF data bit 15	VDD33	AB_AD15, SDI2_DATA3, **GPIO_092**	L2	Leave open
CF_D14	H21	I/O	CF data bit 14	VDD33	AB_AD14, SDI2_DATA2, **GPIO_091**	L2	Leave open
CF_D13	H22	I/O	CF data bit 13	VDD33	AB_AD13, SDI2_DATA1, USI5_CS2, **GPIO_090**	L2	Leave open
CF_D12	H23	I/O	CF data bit 12	VDD33	AB_AD12, SDI2_DATA0, USI5_CS1, **GPIO_089**	L2	Leave open
CF_D11	G21	I/O	CF data bit 11	VDD33	AB_AD11, DTV_DATA, USI5_CS0, **GPIO_088**	L2	Leave open
CF_D10	G22	I/O	CF data bit 10	VDD33	AB_AD10, DTV_VALID, USI5_DO, **GPIO_087**	L2	Leave open
CF_D09	G23	I/O	CF data bit 9	VDD33	AB_AD9, DTV_PSYNC, USI5_DI, **GPIO_086**	L2	Leave open
CF_D08	F21	I/O	CF data bit 8	VDD33	AB_AD8, DTV_BCLK, USI5_CLK, **GPIO_085**	L2	Leave open
CF_D07	F22	I/O	CF data bit 7	VDD33	AB_AD7, **GPIO_084**	L2	Leave open
CF_D06	F23	I/O	CF data bit 6	VDD33	AB_AD6, **GPIO_083**	L2	Leave open
CF_D05	E22	I/O	CF data bit 5	VDD33	AB_AD5, **GPIO_082**	L2	Leave open
CF_D04	E23	I/O	CF data bit 4	VDD33	AB_AD4, **GPIO_081**	L2	Leave open
CF_D03	D22	I/O	CF data bit 3	VDD33	AB_AD3, **GPIO_080**	L2	Leave open
CF_D02	D23	I/O	CF data bit 2	VDD33	AB_AD2, **GPIO_079**	L2	Leave open
CF_D01	C22	I/O	CF data bit 1	VDD33	AB_AD1, **GPIO_078**	L2	Leave open
CF_D00	C23	I/O	CF data bit 0	VDD33	AB_AD0, **GPIO_077**	L2	Leave open
CF_CSB1	G20	Output	CF chip select 1	VDD33	AB_CSB3, **GPIO_072**	H	Leave open
CF_CSB0	F20	Output	CF chip select 0	VDD33	AB_CSB2, **GPIO_071**	H	Leave open
CF_RESET	K20	Output	CF reset output	VDD33	AB_ADV, **GPIO_076**	H	Leave open
CF_A02	L21	Output	CF address bit 2	VDD33	AB_A19, **GPIO_095**	L	Leave open
CF_A01	K21	Output	CF address bit 1	VDD33	AB_A18, **GPIO_094**	L	Leave open
CF_A00	J21	Output	CF address bit 0	VDD33	AB_A17, **GPIO_093**	L	Leave open
CF_IOWRB	H20	Output	CF write strobe	VDD33	AB_WRB, **GPIO_074**	H	Leave open
CF_IORDB	J20	Output	CF read strobe	VDD33	AB_RDB, **GPIO_073**	H	Leave open
CF_IORDY	L20	Input	CF I/O ready	VDD33	AB_WAIT, **GPIO_075**	H	Leave open
CF_INTRQ	N21	Input	CF INT request	VDD33	AB_A21, SDI2_CKO, **GPIO_097**	H	Leave open
CF_INPACKB	L18	Input	IO read reply input (asynchronous)	VDD33	AB_A24, **GPIO_100**	H	Leave open
CF_CDB1	M18	Input	CF card detection 1	VDD33	AB_A25, **GPIO_101**	H	Leave open
CF_CDB2	N18	Input	CF card detection 2	VDD33	AB_A26, **GPIO_102**	H	Leave open

1.2.29 GPIO interface signals

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Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
GPIO_158	AB10	I/O	General-purpose I/O	VDD33M	UART1_RTSB, UART2_TX	K	Leave open
GPIO_157	AA10	I/O	General-purpose I/O	VDD33M	UART1_CTSB, UART2_RX	J	Leave open
GPIO_156	Y10	I/O	General-purpose I/O	VDD33M	UART1_TX	K	Leave open
GPIO_155	Y11	I/O	General-purpose I/O	VDD33M	UART1_RX	J	Leave open
GPIO_154	A12	I/O	General-purpose I/O	VDD18	**LOWPWR**	E	Leave open
GPIO_153	AA12	I/O	General-purpose I/O	USB_VD3312	**USB_VBUS**	H	Leave open
GPIO_152	F13	I/O	General-purpose I/O	VDD18	**JT_TDOEN**	E	Leave open
GPIO_151	D13	I/O	General-purpose I/O	VDD18	**JT_TDO**	E	Leave open
GPIO_150	M22	I/O	General-purpose I/O	VDD18	USI5_DI	C	Leave open
GPIO_149	M23	I/O	General-purpose I/O	VDD18	USI5_CS4	C	Leave open
GPIO_148	N23	I/O	General-purpose I/O	VDD18	USI5_CS3	C	Leave open
GPIO_147	N22	I/O	General-purpose I/O	VDD18	USI5_CS2	C	Leave open
GPIO_146	L22	I/O	General-purpose I/O	VDD18	USI5_CS1	C	Leave open
GPIO_145	L23	I/O	General-purpose I/O	VDD18	USI5_CS0	C	Leave open
GPIO_144	K23	I/O	General-purpose I/O	VDD18	USI5_DO	C	Leave open
GPIO_143	K22	I/O	General-purpose I/O	VDD18	USI5_CLK	C	Leave open
GPIO_142	V23	I/O	General-purpose I/O	VDD33	CAM_YUV7	L2	Leave open
GPIO_141	V22	I/O	General-purpose I/O	VDD33	CAM_YUV6	L2	Leave open
GPIO_140	U23	I/O	General-purpose I/O	VDD33	CAM_YUV5	L2	Leave open
GPIO_139	U22	I/O	General-purpose I/O	VDD33	CAM_YUV4	L2	Leave open
GPIO_138	U21	I/O	General-purpose I/O	VDD33	CAM_YUV3	L2	Leave open
GPIO_137	T23	I/O	General-purpose I/O	VDD33	CAM_YUV2	L2	Leave open
GPIO_136	T22	I/O	General-purpose I/O	VDD33	CAM_YUV1	L2	Leave open
GPIO_135	T21	I/O	General-purpose I/O	VDD33	CAM_YUV0	L2	Leave open
GPIO_134	V21	I/O	General-purpose I/O	VDD33	CAM_HS	L	Leave open
GPIO_133	W22	I/O	General-purpose I/O	VDD33	CAM_VS	H	Leave open
GPIO_132	Y23	I/O	General-purpose I/O	VDD33	CAM_CLKI	H	Leave open
GPIO_131	W23	I/O	General-purpose I/O	VDD33	CAM_CLKO	L	Leave open
GPIO_130	U18	I/O	General-purpose I/O	VDD33	NTSC_DATA7	H	Leave open
GPIO_129	U20	I/O	General-purpose I/O	VDD33	NTSC_DATA6	H	Leave open
GPIO_128	T18	I/O	General-purpose I/O	VDD33	NTSC_DATA5	L	Leave open
GPIO_127	T20	I/O	General-purpose I/O	VDD33	NTSC_DATA4	L	Leave open
GPIO_126	R18	I/O	General-purpose I/O	VDD33	NTSC_DATA3	L	Leave open
GPIO_125	R20	I/O	General-purpose I/O	VDD33	NTSC_DATA2	L	Leave open
GPIO_124	P18	I/O	General-purpose I/O	VDD33	NTSC_DATA1	L	Leave open
GPIO_123	P20	I/O	General-purpose I/O	VDD33	NTSC_DATA0	L	Leave open
GPIO_122	V20	I/O	General-purpose I/O	VDD33	NTSC_CLK	L	Leave open

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Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
GPIO_121	Y5	I/O	General-purpose I/O	VDD33M	PWM1, USI4_DO	L	Leave open
GPIO_120	AA4	I/O	General-purpose I/O	VDD33M	PWM0, USI4_DI	L	Leave open
GPIO_119	AB3	I/O	General-purpose I/O	VDD33M	USI4_CLK	L	Leave open
GPIO_118	AB4	I/O	General-purpose I/O	VDD33M	USI3_CS0, USI0_CS6	L	Leave open
GPIO_117	AC3	I/O	General-purpose I/O	VDD33M	USI3_DO, USI0_CS5	L	Leave open
GPIO_116	AC4	I/O	General-purpose I/O	VDD33M	USI3_DI, USI0_CS4	L	Leave open
GPIO_115	AC5	I/O	General-purpose I/O	VDD33M	USI3_CLK, USI0_CS3	L	Leave open
GPIO_114	Y6	I/O	General-purpose I/O	VDD33M	USI2_CS2, USI4_CS1	L	Leave open
GPIO_113	AA7	I/O	General-purpose I/O	VDD33M	USI2_CS1, USI4_CS0	L	Leave open
GPIO_112	Y7	I/O	General-purpose I/O	VDD33M	**USI2_CS0**, DTV_DATA	L	Leave open
GPIO_111	AA5	I/O	General-purpose I/O	VDD33M	**USI2_DO**, DTV_VALID	L	Leave open
GPIO_110	AA6	I/O	General-purpose I/O	VDD33M	**USI2_DI**, DTV_PSYNC	L	Leave open
GPIO_109	AB5	I/O	General-purpose I/O	VDD33M	**USI2_CLK**, DTV_BCLK	L	Leave open
GPIO_108	D10	I/O	General-purpose I/O	VDD33M	**USI1_DO**	J	Leave open
GPIO_107	C10	I/O	General-purpose I/O	VDD33M	**USI1_DI**	J	Leave open
GPIO_106	B9	I/O	General-purpose I/O	VDD33M	USI0_CS2	L	Leave open
GPIO_105	B8	I/O	General-purpose I/O	VDD33M	USI0_CS1	L	Leave open
GPIO_104	M17	I/O	General-purpose I/O	VDD33	AB_A28, AB_BEN1	H	Leave open
GPIO_103	L17	I/O	General-purpose I/O	VDD33	AB_A27, AB_BEN0	H	Leave open
GPIO_102	N18	I/O	General-purpose I/O	VDD33	AB_A26, CF_CDB2	H	Leave open
GPIO_101	M18	I/O	General-purpose I/O	VDD33	AB_A25, CF_CDB1	H	Leave open
GPIO_100	L18	I/O	General-purpose I/O	VDD33	AB_A24, CF_INPACKB	H	Leave open
GPIO_099	N20	I/O	General-purpose I/O	VDD33	AB_A23, SDI2_CMD	H	Leave open
GPIO_098	M20	I/O	General-purpose I/O	VDD33	AB_A22, SDI2_CKI	H	Leave open
GPIO_097	N21	I/O	General-purpose I/O	VDD33	AB_A21, SDI2_CKO, CF_INTRQ	H	Leave open
GPIO_096	M21	I/O	General-purpose I/O	VDD33	AB_A20	H	Leave open
GPIO_095	L21	I/O	General-purpose I/O	VDD33	AB_A19, CF_A02	L	Leave open
GPIO_094	K21	I/O	General-purpose I/O	VDD33	AB_A18, CF_A01	L	Leave open
GPIO_093	J21	I/O	General-purpose I/O	VDD33	AB_A17, CF_A00	L	Leave open
GPIO_092	J22	I/O	General-purpose I/O	VDD33	AB_AD15, SDI2_DATA3, CF_D15	L2	Leave open
GPIO_091	H21	I/O	General-purpose I/O	VDD33	AB_AD14, SDI2_DATA2, CF_D14	L2	Leave open
GPIO_090	H22	I/O	General-purpose I/O	VDD33	AB_AD13, SDI2_DATA1, CF_D13, USI5_CS2	L2	Leave open
GPIO_089	H23	I/O	General-purpose I/O	VDD33	AB_AD12, SDI2_DATA0, CF_D12, USI5_CS1	L2	Leave open
GPIO_088	G21	I/O	General-purpose I/O	VDD33	AB_AD11, DTV_DATA, CF_D11, USI5_CS0	L2	Leave open
GPIO_087	G22	I/O	General-purpose I/O	VDD33	AB_AD10, DTV_VALID, CF_D10, USI5_DO	L2	Leave open

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Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
GPIO_086	G23	I/O	General-purpose I/O	VDD33	AB_AD9, DTV_PSYNC, CF_D09, USI5_DI	L2	Leave open
GPIO_085	F21	I/O	General-purpose I/O	VDD33	AB_AD8, DTV_BCLK, CF_D08, USI5_CLK	L2	Leave open
GPIO_084	F22	I/O	General-purpose I/O	VDD33	AB_AD7, CF_D07	L2	Leave open
GPIO_083	F23	I/O	General-purpose I/O	VDD33	AB_AD6, CF_D06	L2	Leave open
GPIO_082	E22	I/O	General-purpose I/O	VDD33	AB_AD5, CF_D05	L2	Leave open
GPIO_081	E23	I/O	General-purpose I/O	VDD33	AB_AD4, CF_D04	L2	Leave open
GPIO_080	D22	I/O	General-purpose I/O	VDD33	AB_AD3, CF_D03	L2	Leave open
GPIO_079	D23	I/O	General-purpose I/O	VDD33	AB_AD2, CF_D02	L2	Leave open
GPIO_078	C22	I/O	General-purpose I/O	VDD33	AB_AD1, CF_D01	L2	Leave open
GPIO_077	C23	I/O	General-purpose I/O	VDD33	AB_AD0, CF_D00	L2	Leave open
GPIO_076	K20	I/O	General-purpose I/O	VDD33	AB_ADV, CF_RESET	H	Leave open
GPIO_075	L20	I/O	General-purpose I/O	VDD33	AB_WAIT, CF_IORDY	H	Leave open
GPIO_074	H20	I/O	General-purpose I/O	VDD33	AB_WRB, CF_IOWRB	H	Leave open
GPIO_073	J20	I/O	General-purpose I/O	VDD33	AB_RDB, CF_IORDB	H	Leave open
GPIO_072	G20	I/O	General-purpose I/O	VDD33	AB_CSB3, CF_CSB1	H	Leave open
GPIO_071	F20	I/O	General-purpose I/O	VDD33	AB_CSB2, CF_CSB0	H	Leave open
GPIO_070	E21	I/O	General-purpose I/O	VDD33	AB_CSB1	F	Leave open
GPIO_069	D21	I/O	General-purpose I/O	VDD33	AB_CSB0	F	Leave open
GPIO_068	J23	I/O	General-purpose I/O	VDD33	AB_CLK	L	Leave open
GPIO_067	AA19	I/O	General-purpose I/O	VDD33	**SDI1_DATA3**	L	Leave open
GPIO_066	AB19	I/O	General-purpose I/O	VDD33	**SDI1_DATA2**	L	Leave open
GPIO_065	AB20	I/O	General-purpose I/O	VDD33	**SDI1_DATA1**	L	Leave open
GPIO_064	AB21	I/O	General-purpose I/O	VDD33	**SDI1_DATA0**	L	Leave open
GPIO_063	AC21	I/O	General-purpose I/O	VDD33	**SDI1_CMD**	L	Leave open
GPIO_062	AA23	I/O	General-purpose I/O	VDD33	**SDI1_CKI**	L	Leave open
GPIO_061	AB22	I/O	General-purpose I/O	VDD33	SDI1_CKO	L	Leave open
GPIO_060	Y16	I/O	General-purpose I/O	VDD33	SDI0_DATA7	L	Leave open
GPIO_059	AA16	I/O	General-purpose I/O	VDD33	SDI0_DATA6	L	Leave open
GPIO_058	Y15	I/O	General-purpose I/O	VDD33	SDI0_DATA5	L	Leave open
GPIO_057	AA15	I/O	General-purpose I/O	VDD33	SDI0_DATA4	L	Leave open
GPIO_056	Y14	I/O	General-purpose I/O	VDD33	**SDI0_DATA3**	L	Leave open
GPIO_055	AA14	I/O	General-purpose I/O	VDD33	**SDI0_DATA2**	L	Leave open
GPIO_054	Y13	I/O	General-purpose I/O	VDD33	**SDI0_DATA1**	L	Leave open
GPIO_053	AA13	I/O	General-purpose I/O	VDD33	**SDI0_DATA0**	L	Leave open
GPIO_052	Y12	I/O	General-purpose I/O	VDD33	**SDI0_CMD**	L	Leave open
GPIO_051	AC18	I/O	General-purpose I/O	VDD33	**SDI0_CKI**	L	Leave open
GPIO_050	AB18	I/O	General-purpose I/O	VDD33	SDI0_CKO	L	Leave open
GPIO_049	AB16	I/O	General-purpose I/O	VDD33	–	L	Leave open
GPIO_048	AC19	I/O	General-purpose I/O	VDD33	**SD_CKI**	L	Leave open

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Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
GPIO_047	Y8	I/O	General-purpose I/O	VDD33M	**IIC1_SDA**, UART3_TX	K	Leave open
GPIO_046	Y9	I/O	General-purpose I/O	VDD33M	**IIC1_SCL**, UART3_RX	K	Leave open
GPIO_045	AA8	I/O	General-purpose I/O	VDD33M	**IIC0_SDA**	K	Leave open
GPIO_044	AA9	I/O	General-purpose I/O	VDD33M	**IIC0_SCL**	K	Leave open
GPIO_043	A15	I/O	General-purpose I/O	VDD33	LCD3_B1, YUV3_D9, TP33_DATA9	L	Leave open
GPIO_042	A16	I/O	General-purpose I/O	VDD33	LCD3_B0, YUV3_D8, TP33_DATA8	L	Leave open
GPIO_041	A17	I/O	General-purpose I/O	VDD33	LCD3_G1, YUV3_D1, TP33_DATA1	L	Leave open
GPIO_040	A18	I/O	General-purpose I/O	VDD33	LCD3_G0, YUV3_D0, TP33_DATA0	L	Leave open
GPIO_039	D18	I/O	General-purpose I/O	VDD33	LCD3_R7, TP33_CTRL	L	Leave open
GPIO_038	C18	I/O	General-purpose I/O	VDD33	LCD3_R6, TP33_CLK	L	Leave open
GPIO_037	B18	I/O	General-purpose I/O	VDD33	LCD_R5	L	Leave open
GPIO_036	C19	I/O	General-purpose I/O	VDD33	LCD_R4	L	Leave open
GPIO_035	B19	I/O	General-purpose I/O	VDD33	LCD_R3	L	Leave open
GPIO_034	A19	I/O	General-purpose I/O	VDD33	LCD_R2	L	Leave open
GPIO_033	B20	I/O	General-purpose I/O	VDD33	LCD_R1	L	Leave open
GPIO_032	A20	I/O	General-purpose I/O	VDD33	LCD_R0	L	Leave open
GPIO_031	J18	I/O	General-purpose I/O	VDD33	–	H	Leave open
GPIO_030	H18	I/O	General-purpose I/O	VDD33	–	H	Leave open
GPIO_029	G18	I/O	General-purpose I/O	VDD33	–	H	Leave open
GPIO_028	F18	I/O	General-purpose I/O	VDD33	–	H	Leave open
GPIO_027	F17	I/O	General-purpose I/O	VDD33	–	H	Leave open
GPIO_026	F16	I/O	General-purpose I/O	VDD33	–	L	Leave open
GPIO_025	E20	I/O	General-purpose I/O	VDD33	–	L	Leave open
GPIO_024	D20	I/O	General-purpose I/O	VDD33	–	L	Leave open
GPIO_023	D19	I/O	General-purpose I/O	VDD33	LCD3_DE, YUV3_DE	L	Leave open
GPIO_022	C20	I/O	General-purpose I/O	VDD33	LCD3_VS, YUV3_VS	L	Leave open
GPIO_021	B21	I/O	General-purpose I/O	VDD33	LCD3_HS, YUV3_HS	L	Leave open
GPIO_020	A21	I/O	General-purpose I/O	VDD33	LCD3_CLK_I, YUV3_CLK_I	L	Leave open
GPIO_019	C21	I/O	General-purpose I/O	VDD33	–	L	Leave open
GPIO_018	B22	I/O	General-purpose I/O	VDD33	LCD3_PXCLK, YUV3_CLK_O	L	Leave open
GPIO_017	W20	I/O	General-purpose I/O	VDD33	–	L2	Leave open
GPIO_016	W21	I/O	General-purpose I/O	VDD33	–	L2	Leave open
GPIO_015	Y19	I/O	General-purpose I/O	VDD33	–	L2	Leave open
GPIO_014	Y20	I/O	General-purpose I/O	VDD33	–	L2	Leave open
GPIO_013	Y21	I/O	General-purpose I/O	VDD33	–	L2	Leave open
GPIO_012	AA20	I/O	General-purpose I/O	VDD33	–	H1	Leave open
GPIO_011	AA21	I/O	General-purpose I/O	VDD33	–	H1	Leave open

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Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
GPIO_010	AA22	I/O	General-purpose I/O	VDD33	–	L2	Leave open
GPIO_009	V15	I/O	General-purpose I/O	VDD33	–	L	Leave open
GPIO_008	V16	I/O	General-purpose I/O	VDD33	–	H	Leave open
GPIO_007	V17	I/O	General-purpose I/O	VDD33	–	H	Leave open
GPIO_006	V18	I/O	General-purpose I/O	VDD33	–	L	Leave open
GPIO_005	U8	I/O	General-purpose I/O	VDD33M	EXT_CLKI	L	Leave open
GPIO_004	V8	I/O	General-purpose I/O	VDD33M	REF_CLKO	L	Leave open
GPIO_003	U9	I/O	General-purpose I/O	VDD33M	ERR_RST_REQB	L	Leave open
GPIO_002	V9	I/O	General-purpose I/O	VDD33M	**JT_SEL**	L	Leave open
GPIO_001	U10	I/O	General-purpose I/O	VDD33M	–	L	Leave open
GPIO_000	V10	I/O	General-purpose I/O	VDD33M	–	L	Leave open

1.2.30 PWM interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
PWM0	AA4	Output	PWM output channel 0	VDD33M	USI4_DI, **GPIO_120**	L	Leave open
PWM1	Y5	Output	PWM output channel 1	VDD33M	USI4_DO, **GPIO_121**	L	Leave open

1.2.31 Camera interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
CAM_YUV7	V23	Input	Data bit 7	VDD33	**GPIO_142**	L2	Leave open
CAM_YUV6	V22	Input	Data bit 6	VDD33	**GPIO_141**	L2	Leave open
CAM_YUV5	U23	Input	Data bit 5	VDD33	**GPIO_140**	L2	Leave open
CAM_YUV4	U22	Input	Data bit 4	VDD33	**GPIO_139**	L2	Leave open
CAM_YUV3	U21	Input	Data bit 3	VDD33	**GPIO_138**	L2	Leave open
CAM_YUV2	T23	Input	Data bit 2	VDD33	**GPIO_137**	L2	Leave open
CAM_YUV1	T22	Input	Data bit 1	VDD33	**GPIO_136**	L2	Leave open
CAM_YUV0	T21	Input	Data bit 0	VDD33	**GPIO_135**	L2	Leave open
CAM_VS	W22	Input	Vertical sync.	VDD33	**GPIO_133**	H	Leave open
CAM_HS	V21	Input	Horizontal sync.	VDD33	**GPIO_134**	L	Leave open
CAM_CLKI	Y23	Input	Clock input	VDD33	**GPIO_132**	H	Leave open
CAM_CLKO	W23	Output	Clock output	VDD33	**GPIO_131**	L	Leave open

1.2.32 ITU-R BT.656 interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
NTSC_DATA7	U18	Output	Data bit 7	VDD33	**GPIO_130**	H	Leave open
NTSC_DATA6	U20	Output	Data bit 6	VDD33	**GPIO_129**	H	Leave open
NTSC_DATA5	T18	Output	Data bit 5	VDD33	**GPIO_128**	L	Leave open
NTSC_DATA4	T20	Output	Data bit 4	VDD33	**GPIO_127**	L	Leave open
NTSC_DATA3	R18	Output	Data bit 3	VDD33	**GPIO_126**	L	Leave open
NTSC_DATA2	R20	Output	Data bit 2	VDD33	**GPIO_125**	L	Leave open
NTSC_DATA1	P18	Output	Data bit 1	VDD33	**GPIO_124**	L	Leave open
NTSC_DATA0	P20	Output	Data bit 0	VDD33	**GPIO_123**	L	Leave open
NTSC_CLK	V20	Input	NTSC clock input	VDD33	**GPIO_122**	L	Leave open

1.2.33 Trace port interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Alternate Pin Function (Bold is a default pin.)	Buffer Type	Handling when not used
TP33_DATA15	D14	Output	Trace data bit 15	VDD33	**LCD3_B7**, YUV3_D15	L	Leave open
TP33_DATA14	C14	Output	Trace data bit 14	VDD33	**LCD3_B6**, YUV3_D14	L	Leave open
TP33_DATA13	B14	Output	Trace data bit 13	VDD33	**LCD3_B5**, YUV3_D13	L	Leave open
TP33_DATA12	D15	Output	Trace data bit 12	VDD33	**LCD3_B4**, YUV3_D12	L	Leave open
TP33_DATA11	C15	Output	Trace data bit 11	VDD33	**LCD3_B3**, YUV3_D11	L	Leave open
TP33_DATA10	B15	Output	Trace data bit 10	VDD33	**LCD3_B2**, YUV3_D10	L	Leave open
TP33_DATA9	A15	Output	Trace data bit 9	VDD33	LCD3_B1, YUV3_D9, **GPIO_043**	L	Leave open
TP33_DATA8	A16	Output	Trace data bit 8	VDD33	LCD3_B0, YUV3_D8, **GPIO_042**	L	Leave open
TP33_DATA7	D16	Output	Trace data bit 7	VDD33	**LCD3_G7**, YUV3_D7	L	Leave open
TP33_DATA6	C16	Output	Trace data bit 6	VDD33	**LCD3_G6**, YUV3_D6	L	Leave open
TP33_DATA5	B16	Output	Trace data bit 5	VDD33	**LCD3_G5**, YUV3_D5	L	Leave open
TP33_DATA4	D17	Output	Trace data bit 4	VDD33	**LCD3_G4**, YUV3_D4	L	Leave open
TP33_DATA3	C17	Output	Trace data bit 3	VDD33	**LCD3_G3**, YUV3_D3	L	Leave open
TP33_DATA2	B17	Output	Trace data bit 2	VDD33	**LCD3_G2**, YUV3_D2	L	Leave open
TP33_DATA1	A17	Output	Trace data bit 1	VDD33	LCD3_G1, YUV3_D1, **GPIO_041**	L	Leave open
TP33_DATA0	A18	Output	Trace data bit 0	VDD33	LCD3_G0, YUV3_D0, **GPIO_040**	L	Leave open
TP33_CLK	C18	Output	Trace clock output	VDD33	LCD3_R6, **GPIO_038**	L	Leave open
TP33_CTRL	D18	Output	Trace control	VDD33	LCD3_R7, **GPIO_039**	L	Leave open

1.2.34 Power supply pins

Pin Name	Pin No.	Function
AVDD	A4, B4	PLL power supply
AGND	C4, D5	PLL GND
DDR_VDDIO	F6, H6, K7, N7, R6, T6	DDR IO power supply
DDR_GND	F3, J3, M3, N2, V3	DDR GND
DDR_VREFH	V4	DDR standard reference current generation
DDR_VREFL	F4	DDR standard reference current generation
USB_AVDD1	AB11	Power supply for regulators inside USB PHY 1
USB_AVDD2	AC6	Power supply for regulators inside USB PHY 2
USB_VD3311	AB14	Power supply for USB PHY 1 DP/DM terminals
USB_VD3312	AB8	Power supply for USBPHY 2 DP/DM terminals
USB_GND11	AA11	USB PHY 1 IO GND
USB_GND12	AC8	USB PHY 2 IO GND
USB_GND21	AC14	USB PHY 1 IO GND
USB_GND22	AC10	USB PHY 2 IO GND
USB_AVSS1	AB12	USB PHY 1 regulators GND
USB_AVSS2	AB6	USB PHY 2 regulators GND
USB_PVSS1	AC12	USB PHY 1 PLL GND
USB_PVSS2	AB7	USB PHY 2 PLL GND
USB_RREF1	AC11	USB PHY 1 standard reference current generation
USB_RREF2	AC7	USB PHY 2 standard reference current generation
VDD33D	A3	Anti-fuse power supply (3.3 V)
VDD33	F7, G15, H17, K17, R17, U14, U15	3.3 V IO power supply
VDD33M	G12, V7	1.8V/3.3 V IO power supply Note
VDD18	B13, F15, G8, N17, U17, V6, V11	1.8 V IO power supply
VDD11	F9, F10, G6, G13, G16, J7, J17, K18, P6, P17, T17, U6, U13, V14	Core power supply
GND	A1,A2, A6, A7, A10, A14, A22, A23, B1, B2, B5, B23, C7, C8, D8, D9, G7, G9, G10, G14, G17, H7, H8, M7, P7, P21, R7, R21, T7, U7, U11, U12, U16, Y22, AB1, AB2, AB15, AB23, AC1, AC2, AC17, AC22, AC23	GND

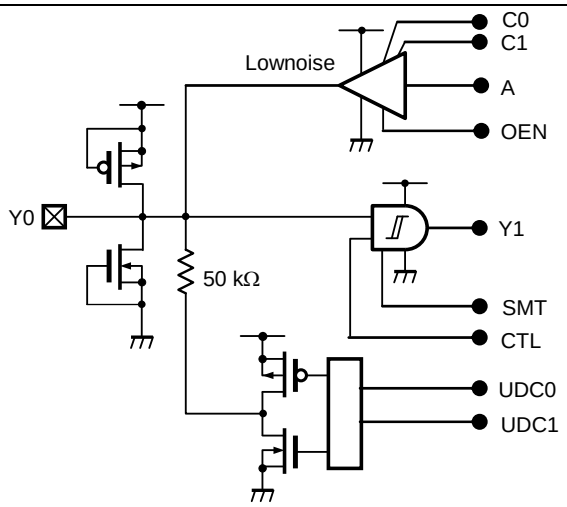
Note One of 1.8V and 3.3V can be chosen and used. It's chosen by setting the voltage supplied to VDD33M to 1.8V or 3.3V.

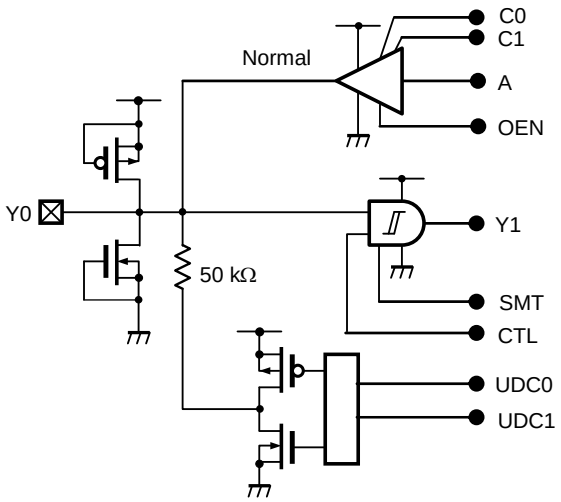
1.3 Pin I/O Circuits

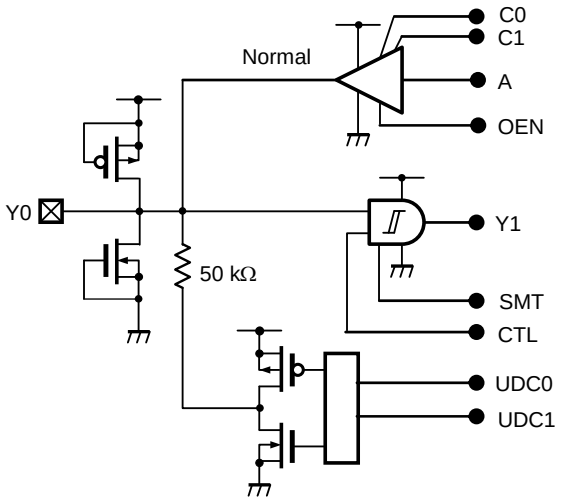
This section shows the types of I/O circuits used in EM/EV2. The correspondence between circuits and pins is shown in the table below.

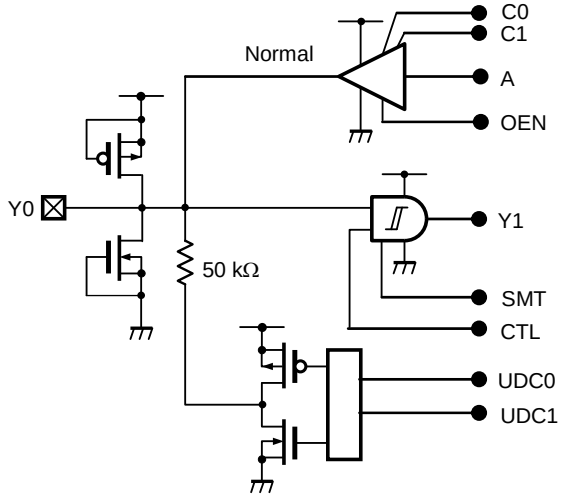
Buffer type	Power	I/O	Low noise	Bus Hold	Input (stand by) (T : Through M : Low mask)	Output condition (stand by)	Normal/Schmitt switch	Pull-up/Pull-down switch (Pull-up50K/Pull-down50K/none)	IOLH switch (4/6/8/12mA)	Description
A	VDD18	IO	√		T	Hi-Z	√	√	√	
B	VDD18	IO			M	Pull-up	√	√	√	
C	VDD18	IO			M	Pull-down	√	√	√	
D	VDD18	IO			M	Hi-Z	√	√	√	
E	VDD18	IO			M	L	√	√	√	
F	VDD33	IO			M	Pull-up	√	√	√	
H	VDD33 USB_VD3312	IO			M	Hi-Z	√	√	√	
H1	VDD33	IO		√	M	Hi-Z	√	√	√	
I	VDD33M	IO	√		M	Pull-up	√	√	√	
J	VDD33M	IO	√		M	Pull-down	√	√	√	
K	VDD33M	IO	√		M	Hi-Z	√	√	√	
L	VDD33M VDD33	IO			M	Pull-down	√	√	√	
L2	VDD33	IO		√	M	Pull-down	√	√	√	
M	VDD18	I			—	–	Schmitt			Standby Control buffer
N	VDD18	I			—	Pull-down	CMOS			Anytime pull-down
O	VDD18	I			—	Pull-down	CMOS			Anytime pull-down
P	VDD18	I			—	–	—			Oscillator

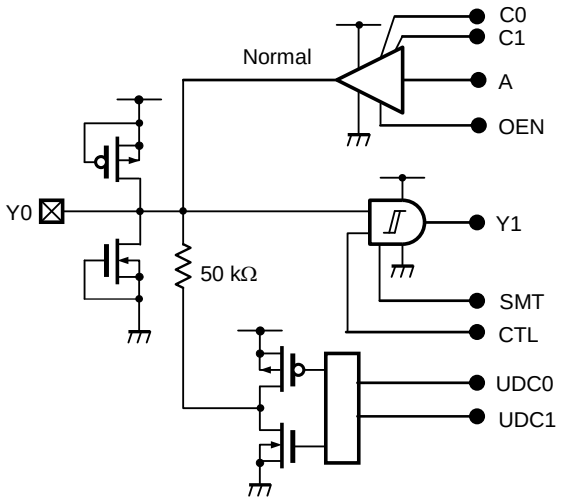
Buffer type	VDD	I/O	CMOS/AMP switch	Termination	Impedance	Description
Q	DDR_VDDIO	IO		√	√	Address, control signals
R	DDR_VDDIO	IO		√	√	Clock
S	DDR_VDDIO	IO	√	√	√	DQ, DM
T	DDR_VDDIO	IO	√	√	√	DQS
U	DDR_VDDIO	I				Clock reset (standby)

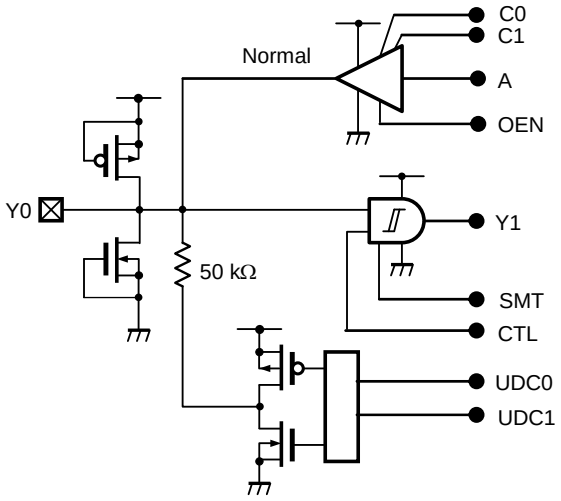
Type A	Description
	Power : VDD18 IO Type : Bidirectional Buffer Input Type : AND, SCHMITT/CMOS Output Type : Lownoise, IOLH control 50K_Pull-up/50K_Pull-down Standby : Hi-Z , Input through Resistance = 50 kΩ (typ.)

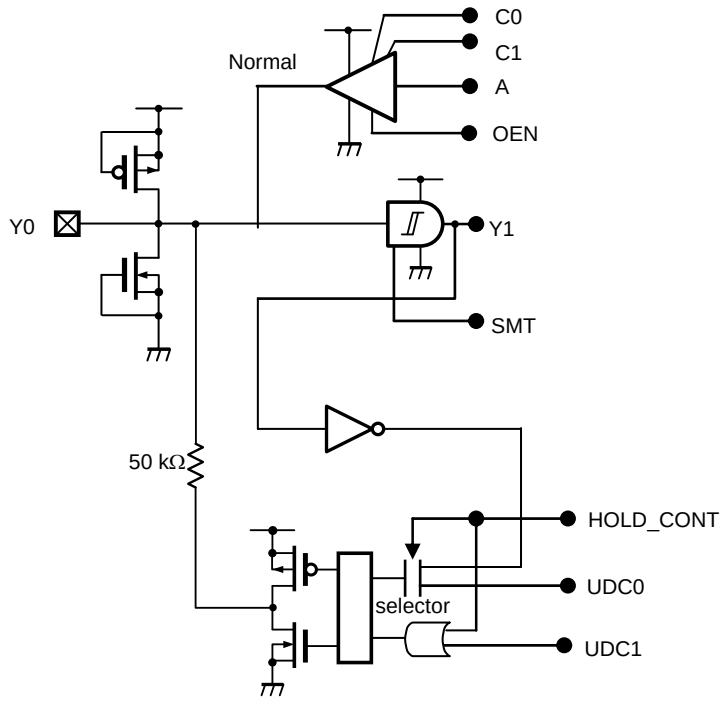
Type B	Description
	Power : VDD18 IO Type : Bidirectional Buffer Input Type : AND, SCHMITT/CMOS Output Type : Normal, IOLH control 50K_Pull-up/50K_Pull-down Standby : Pull-up., Input 0 mask Resistance = 50 kΩ (typ.)

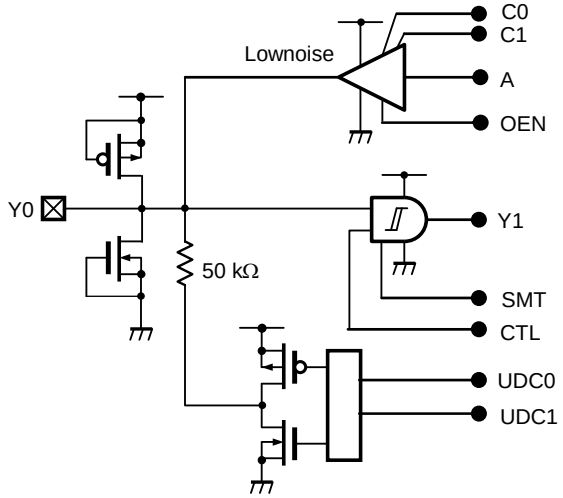
Type C	Description
	Power : VDD18 IO Type : Bidirectional Buffer Input Type : AND, SCHMITT/CMOS Output Type : Normal, IOLH control 50K_Pull-up/50K_Pull-down Standby : Pull-down., Input 0 mask Resistance = 50 kΩ (typ.)

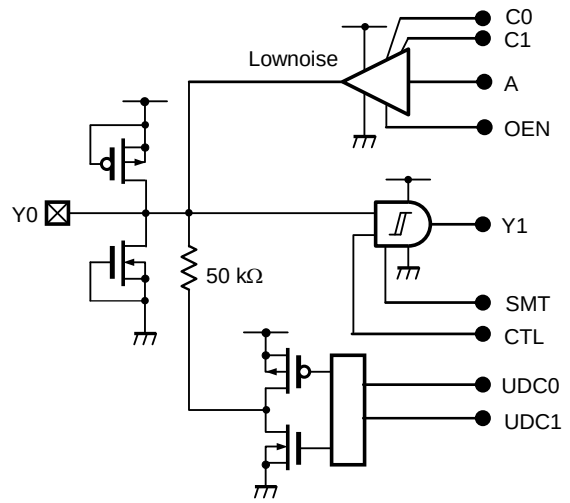
Type D	Description
	Power : VDD18 IO Type : Bidirectional Buffer Input Type : AND, SCHMITT/CMOS Output Type : Normal, IOLH control 50K_Pull-up/50K_Pull-down Standby : Hi-Z, Input 0 mask Resistance = 50 kΩ (typ.)

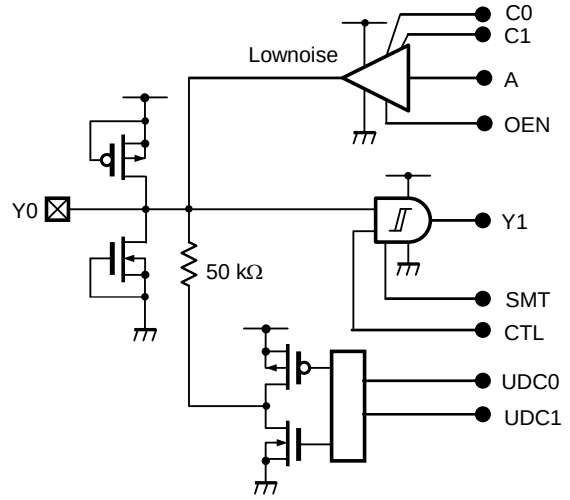
Type E	Description
	Power : VDD18 IO Type : Bidirectional Buffer Input Type : AND, SCHMITT/CMOS Output Type : Normal, IOLH control 50K_Pull-up/50K_Pull-down Standby : Low, Input 0 mask Resistance = 50 kΩ (typ.)

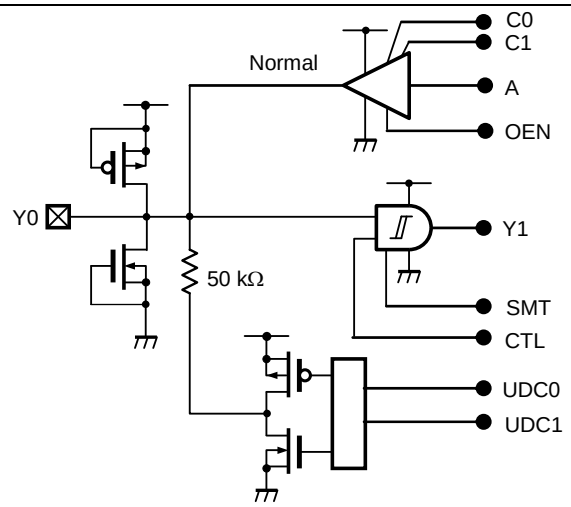
Type F	Description
	Power : VDD33 IO Type : Bidirectional Buffer Input Type : AND, SCHMITT/CMOS Output Type : Normal, IOLH control 50K_Pull-up/50K_Pull-down Standby : Pull-up., Input 0 mask Resistance = 50 kΩ (typ.)

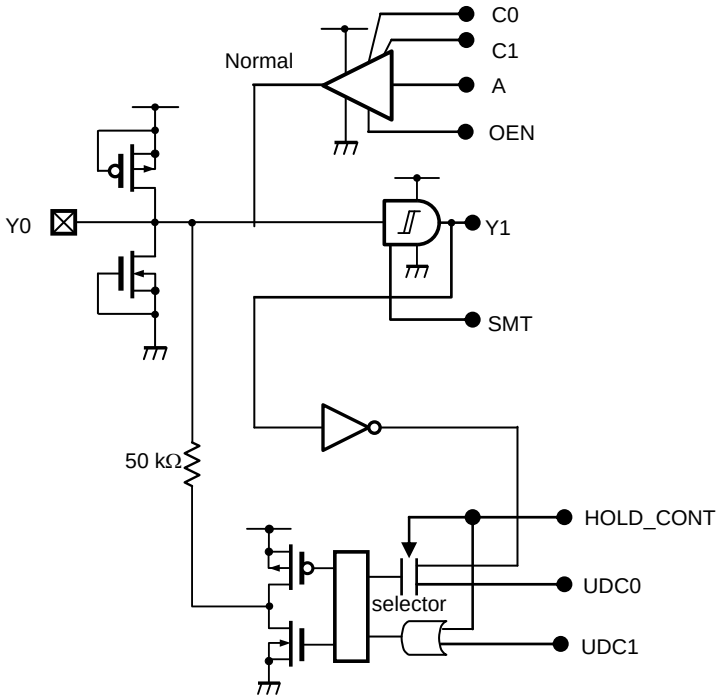
Type H1	Description
	Power : VDD33 IO Type : Bidirectional Buffer Input Type : AND, SCHMITT/CMOS Output Type : Normal, IOLH control bus holder Standby : Hi-Z, Input 0 mask Resistance = 50 kΩ (typ.) CTL,HOLD_CONT is made effective to assume that Bus_Hold is effective.

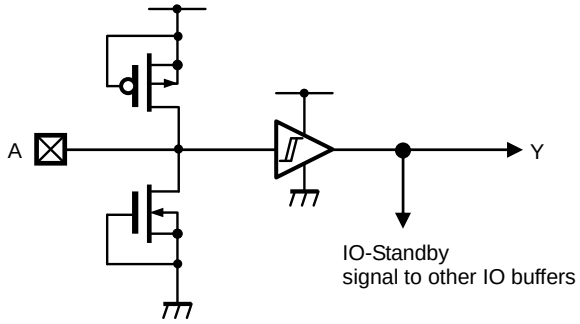
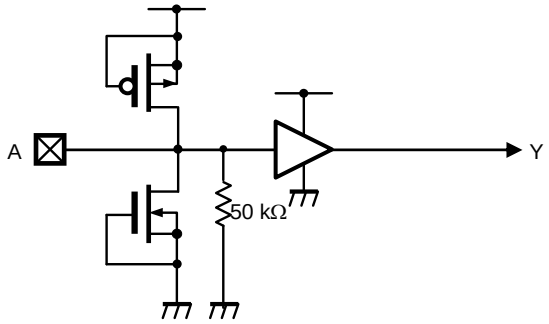
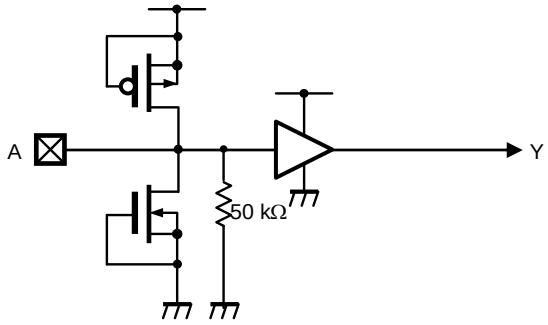
Type I	Description
	Power : VDD33M IO Type : Bidirectional Buffer Input Type : AND, SCHMITT/CMOS Output Type : Lownoise, IOLH control 50K_Pull-up/50K_Pull-down Standby : Pull-up., Input 0 mask Resistance = 50 kΩ (typ.)

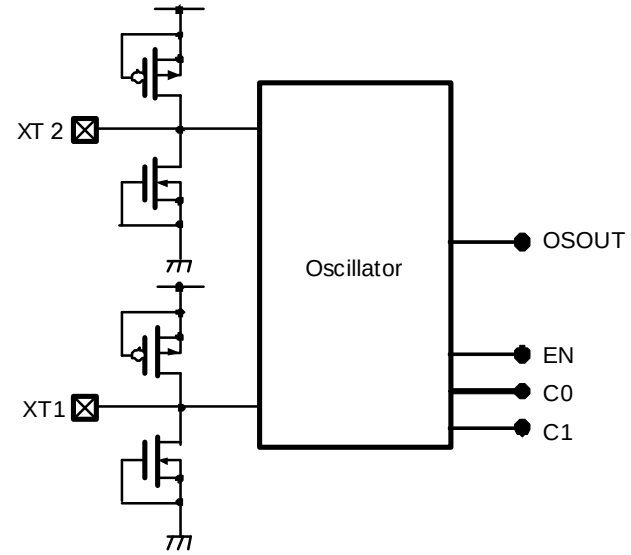
Type J	Description
	Power : VDD33M IO Type : Bidirectional Buffer Input Type : AND, SCHMITT/CMOS Output Type : Lownoise, IOLH control 50K_Pull-up/50K_Pull-down Standby : Pull-down., Input 0 mask Resistance = 50 kΩ (typ.)

Type K	Description
	Power : VDD33M IO Type : Bidirectional Buffer Input Type : AND, SCHMITT/CMOS Output Type : Lownoise, IOLH control 50K_Pull-up/50K_Pull-down Standby : Hi-Z, Input 0 mask Resistance = 50 kΩ (typ.)

Type L	Description
	Power : VDD33M IO Type : Bidirectional Buffer Input Type : AND, SCHMITT/CMOS Output Type : Normal, IOLH control 50K_Pull-up/50K_Pull-down Standby : Pull-down., Input 0 mask Resistance = 50 kΩ (typ.)

Type L2	Description
	Power : VDD33M IO Type : Bidirectional Buffer Input Type : AND, SCHMITT/CMOS Output Type : Normal, IOLH control bus holder Standby : Pull-down., Input 0 mask Resistance = 50 kΩ (typ.) CTL,HOLD_CONT is made effective to assume that Bus_Hold is effective.

Type M	Description
	Power : VDD18 IO Type : Input Input Type : SCHMITT Output Type : — Standby : Standby control (0 : standby, 1 : normal)
Type N	**Description**
	Power : VDD18 IO Type : Input Input Type : CMOS, 50K_Pull-down. Output Type : — Standby : Pull-down. Resistance = 50 kΩ (typ.)
Type O	**Description**
	Power : VDD18 IO Type : Input Input Type : CMOS, 50K_Pull-down Output Type : — Standby : Pull-down. Resistance = 50 kΩ (typ.)

Type P	Description
	Power : VDD18 IO Type : Oscillator Input Type : － Output Type : － Standby : XT1-Pull-down., XT2-Pull-up.

1.4 Pin Multiplex Function

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Pin No.	Default	Mode0	Mode1	Mode2	Mode3	GPIO
A05	C32K	C32K				
A08	OSC0_XT2	OSC0_XT2				
A09	OSC0_XT1	OSC0_XT1				
A11	JT_TCK	JT_TCK				
A12	LOWPWR	LOWPWR				GPIO_154
A13	PONDET	PONDET				
A15	GPIO_043	LCD3_B1	YUV3_D9	TP33_DATA9		GPIO_043
A16	GPIO_042	LCD3_B0	YUV3_D8	TP33_DATA8		GPIO_042
A17	GPIO_041	LCD3_G1	YUV3_D1	TP33_DATA1		GPIO_041
A18	GPIO_040	LCD3_G0	YUV3_D0	TP33_DATA0		GPIO_040
A19	GPIO_034	LCD3_R2				GPIO_034
A20	GPIO_032	LCD3_R0				GPIO_032
A21	GPIO_020	LCD3_CLK_I	YUV3_CLK_I			GPIO_020
B03	AFS_ARSTB	AFS_ARSTB				
B06	USI0_CLK	USI0_CLK				
B07	USI0_CS0	USI0_CS0				
B08	GPIO_105	USI0_CS1				GPIO_105
B09	GPIO_106	USI0_CS2				GPIO_106
B10	USI0_DI	USI0_DI				
B11	USI0_DO	USI0_DO				
B12	SRESETB	SRESETB				
B14	LCD3_B5	LCD3_B5	YUV3_D13	TP33_DATA13		
B15	LCD3_B2	LCD3_B2	YUV3_D10	TP33_DATA10		
B16	LCD3_G5	LCD3_G5	YUV3_D5	TP33_DATA5		
B17	LCD3_G2	LCD3_G2	YUV3_D2	TP33_DATA2		
B18	GPIO_037	LCD3_R5				GPIO_037
B19	GPIO_035	LCD3_R3				GPIO_035
B20	GPIO_033	LCD3_R1				GPIO_033
B21	GPIO_021	LCD3_HS	YUV3_HS			GPIO_021
B22	GPIO_018	LCD3_PXCLK	YUV3_CLK_O			GPIO_018
C01	DDR_DQ7	DDR_DQ7				
C02	DDR_DQ0	DDR_DQ0				
C03	DDR_DQ2	DDR_DQ2				
C05	NECTESTIO	NECTESTIO				
C06	UTEST	UTEST				
C09	USI1_CLK	USI1_CLK				
C10	USI1_DI	USI1_DI				GPIO_107
C11	JT_TRSTB	JT_TRSTB				
C13	JT_TDI	JT_TDI				

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Pin No.	Default	Mode0	Mode1	Mode2	Mode3	GPIO
C14	LCD3_B6	LCD3_B6	YUV3_D14	TP33_DATA14		
C15	LCD3_B3	LCD3_B3	YUV3_D11	TP33_DATA11		
C16	LCD3_G6	LCD3_G6	YUV3_D6	TP33_DATA6		
C17	LCD3_G3	LCD3_G3	YUV3_D3	TP33_DATA3		
C18	GPIO_038	LCD3_R6		TP33_CLK		GPIO_038
C19	GPIO_036	LCD3_R4				GPIO_036
C20	GPIO_022	LCD3_VS	YUV3_VS			GPIO_022
C21	GPIO_019					GPIO_019
C22	GPIO_078	AB_AD1		CF_D01		GPIO_078
C23	GPIO_077	AB_AD0		CF_D00		GPIO_077
D01	DDR_DM0	DDR_DM0				
D02	DDR_DQ4	DDR_DQ4				
D03	DDR_DQ6	DDR_DQ6				
D04	DDR_DQ1	DDR_DQ1				
D06	TE1	TE1				
D07	TE2	TE2				
D10	USI1_DO	USI1_DO				GPIO_108
D11	USI1_CS0	USI1_CS0				
D12	JT_DBG_EN	JT_DBG_EN				
D13	JT_TDO	JT_TDO				GPIO_151
D14	LCD3_B7	LCD3_B7	YUV3_D15	TP33_DATA15		
D15	LCD3_B4	LCD3_B4	YUV3_D12	TP33_DATA12		
D16	LCD3_G7	LCD3_G7	YUV3_D7	TP33_DATA7		
D17	LCD3_G4	LCD3_G4	YUV3_D4	TP33_DATA4		
D18	GPIO_039	LCD3_R7		TP33_CTRL		GPIO_039
D19	GPIO_023	LCD3_DE	YUV3_DE			GPIO_023
D20	GPIO_024					GPIO_024
D21	GPIO_069	AB_CSB0				GPIO_069
D22	GPIO_080	AB_AD3		CF_D03		GPIO_080
D23	GPIO_079	AB_AD2		CF_D02		GPIO_079
E01	DDR_DQS0	DDR_DQS0				
E02	DDR_DQS0B	DDR_DQS0B				
E03	DDR_DQ3	DDR_DQ3				
E04	DDR_DQ5	DDR_DQ5				
E20	GPIO_025					GPIO_025
E21	GPIO_070	AB_CSB1				GPIO_070
E22	GPIO_082	AB_AD5		CF_D05		GPIO_082
E23	GPIO_081	AB_AD4		CF_D04		GPIO_081
F01	DDR_DQS1E	DDR_DQS1E				
F02	DDR_DQS1EB	DDR_DQS1EB				
F04	DDR_VREFL	DDR_VREFL				

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Pin No.	Default	Mode0	Mode1	Mode2	Mode3	GPIO
F08	TRSTB	TRSTB				
F11	BOOTSEL2	BOOTSEL2				
F12	BOOTSEL0	BOOTSEL0				
F13	JT_TDOEN	JT_TDOEN				GPIO_152
F14	JT_TMS	JT_TMS				
F16	GPIO_026					GPIO_026
F17	GPIO_027					GPIO_027
F18	GPIO_028					GPIO_028
F20	GPIO_071	AB_CSB2		CF_CSB0		GPIO_071
F21	GPIO_085	AB_AD8	DTV_BCLK	CF_D08	USI5_CLK	GPIO_085
F22	GPIO_084	AB_AD7		CF_D07		GPIO_084
F23	GPIO_083	AB_AD6		CF_D06		GPIO_083
G02	DDR_DQ8	DDR_DQ8				
G03	DDR_DM1E	DDR_DM1E				
G04	DDR_DQ9	DDR_DQ9				
G11	BOOTSEL1	BOOTSEL1				
G11	DDR_DQ11	DDR_DQ11				
G18	GPIO_029					GPIO_029
G20	GPIO_072	AB_CSB3		CF_CSB1		GPIO_072
G21	GPIO_088	AB_AD11	DTV_DATA	CF_D11	USI5_CS0	GPIO_088
G22	GPIO_087	AB_AD10	DTV_VALID	CF_D10	USI5_DO	GPIO_087
G23	GPIO_086	AB_AD9	DTV_PSYNC	CF_D09	USI5_DI	GPIO_086
H01	DDR_DQ12	DDR_DQ12				
H02	DDR_DQ15	DDR_DQ15				
H03	DDR_DQ13	DDR_DQ13				
H04	DDR_DQ10	DDR_DQ10				
H18	GPIO_030					GPIO_030
H20	GPIO_074	AB_WRB		CF_IOWRB		GPIO_074
H21	GPIO_091	AB_AD14	SDI2_DATA2	CF_D14		GPIO_091
H22	GPIO_090	AB_AD13	SDI2_DATA1	CF_D13	USI5_CS2	GPIO_090
H23	GPIO_089	AB_AD12	SDI2_DATA0	CF_D12	USI5_CS1	GPIO_089
J01	DDR_A0	DDR_A0				
J02	DDR_A2	DDR_A2				
J04	DDR_DQ14	DDR_DQ14				
J06	DDR_CS1B	DDR_CS1B				
J18	GPIO_031					GPIO_031
J20	GPIO_073	AB_RDB		CF_IORDB		GPIO_073
J21	GPIO_093	AB_A17		CF_A00		GPIO_093
J22	GPIO_092	AB_AD15	SDI2_DATA3	CF_D15		GPIO_092
J23	GPIO_068	AB_CLK				GPIO_068
K01	DDR_BA2	DDR_BA2				

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Pin No.	Default	Mode0	Mode1	Mode2	Mode3	GPIO
K02	DDR_BA0	DDR_BA0				
K03	DDR_A3	DDR_A3				
K04	DDR_A10	DDR_A10				
K06	DDR_CASB	DDR_CASB				
K20	GPIO_076	AB_ADV		CF_RESET		GPIO_076
K21	GPIO_094	AB_A18		CF_A01		GPIO_094
K22	GPIO_143	HSI_CAWAKE Note1	USI5_CLK			GPIO_143
K23	GPIO_144	HSI_CADATA Note1	USI5_DO			GPIO_144
L01	DDR_CKE0	DDR_CKE0				
L02	DDR_A14	DDR_A14				
L03	DDR_A1	DDR_A1				
L04	DDR_BA1	DDR_BA1				
L06	DDR_RASB	DDR_RASB				
L07	DDR_CS0B	DDR_CS0B				
L17	GPIO_103	AB_A27		AB_BEN0		GPIO_103
L18	GPIO_100	AB_A24		CF_INPACKB		GPIO_100
L20	GPIO_075	AB_WAIT		CF_IORDY		GPIO_075
L21	GPIO_095	AB_A19		CF_A02		GPIO_095
L22	GPIO_146	HSI_ACREADY Note1	USI5_CS1			GPIO_146
L23	GPIO_145	HSI_CAFLAG Note1	USI5_CS0			GPIO_145
M01	DDR_CK	DDR_CK				
M02	DDR_CKB	DDR_CKB				
M04	DDR_WEB	DDR_WEB				
M06	DDR_ODT Note2	DDR_ODT Note2				
M17	GPIO_104	AB_A28		AB_BEN1		GPIO_104
M18	GPIO_101	AB_A25		CF_CDB1		GPIO_101
M20	GPIO_098	AB_A22	SDI2_CKI			GPIO_098
M21	GPIO_096	AB_A20				GPIO_096
M22	GPIO_150	HSI_CAREADY Note1	USI5_DI			GPIO_150
M23	GPIO_149	HSI_ACFLAG Note1	USI5_CS4			GPIO_149
N01	DDR_CKE1	DDR_CKE1				
N03	DDR_A11	DDR_A11				
N04	DDR_A13	DDR_A13				
N06	DDR_CKERSTB	DDR_CKERSTB				
N18	GPIO_102	AB_A26		CF_CDB2		GPIO_102
N20	GPIO_099	AB_A23	SDI2_CMD			GPIO_099

Note1 : The HSI function is not available.

Note2 : The on die termination function for DDR-ODT is not available.

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Pin No.	Default	Mode0	Mode1	Mode2	Mode3	GPIO
N21	GPIO_097	AB_A21	SDI2_CKO	CF_INTRQ		GPIO_097
N22	GPIO_147	HSI_ACWAKE Note1	USI5_CS2			GPIO_147
N23	GPIO_148	HSI_ACDATA Note1	USI5_CS3			GPIO_148
P01	DDR_A12	DDR_A12				
P02	DDR_A7	DDR_A7				
P03	DDR_A8	DDR_A8				
P04	DDR_A6	DDR_A6				
P18	GPIO_124	NTSC_DATA1				GPIO_124
P20	GPIO_123	NTSC_DATA0				GPIO_123
R01	DDR_A9	DDR_A9				
R02	DDR_A5	DDR_A5				
R03	DDR_A4	DDR_A4				
R04	DDR_DQ20	DDR_DQ20				
R18	GPIO_126	NTSC_DATA3				GPIO_126
R20	GPIO_125	NTSC_DATA2				GPIO_125
T01	DDR_DQ16	DDR_DQ16				
T02	DDR_DQ17	DDR_DQ17				
T03	DDR_DQ22	DDR_DQ22				
T04	DDR_DQ19	DDR_DQ19				
T18	GPIO_128	NTSC_DATA5				GPIO_128
T20	GPIO_127	NTSC_DATA4				GPIO_127
T21	GPIO_135	CAM_YUV0				GPIO_135
T22	GPIO_136	CAM_YUV1				GPIO_136
T23	GPIO_137	CAM_YUV2				GPIO_137
U01	DDR_DQ21	DDR_DQ21				
U02	DDR_DQ18	DDR_DQ18				
U03	DDR_DQ23	DDR_DQ23				
U04	DDR_DM2E	DDR_DM2E				
U08	GPIO_005	EXT_CLKI				GPIO_005
U09	GPIO_003	ERR_RST_REQB				GPIO_003
U10	GPIO_001					GPIO_001
U18	GPIO_130	NTSC_DATA7				GPIO_130
U20	GPIO_129	NTSC_DATA6				GPIO_129
U21	GPIO_138	CAM_YUV3				GPIO_138
U22	GPIO_139	CAM_YUV4				GPIO_139
U23	GPIO_140	CAM_YUV5				GPIO_140
V01	DDR_DQS2E	DDR_DQS2E				
V02	DDR_DQS2EB	DDR_DQS2EB				
V04	DDR_VREFH	DDR_VREFH				
V08	GPIO_004	REF_CLKO				GPIO_004

Note1 : The HSI function is un-installation.

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Pin No.	Default	Mode0	Mode1	Mode2	Mode3	GPIO
V09	JT_SEL	JT_SEL				GPIO_002
V10	GPIO_000					GPIO_000
V12	UART0_TX	UART0_TX				
V13	UART0_RX	UART0_RX				
V15	GPIO_009					GPIO_009
V16	GPIO_008					GPIO_008
V17	GPIO_007					GPIO_007
V18	GPIO_006					GPIO_006
V20	GPIO_122	NTSC_CLK				GPIO_122
V21	GPIO_134	CAM_HS				GPIO_134
V22	GPIO_141	CAM_YUV6				GPIO_141
V23	GPIO_142	CAM_YUV7				GPIO_142
W01	DDR_DQS3	DDR_DQS3				
W02	DDR_DQS3B	DDR_DQS3B				
W03	DDR_DQ31	DDR_DQ31				
W04	DDR_DQ30	DDR_DQ30				
W20	GPIO_017					GPIO_017
W21	GPIO_016					GPIO_016
W22	GPIO_133	CAM_VS				GPIO_133
W23	GPIO_131	CAM_CLKO				GPIO_131
Y01	DDR_DM3	DDR_DM3				
Y02	DDR_DQ27	DDR_DQ27				
Y03	DDR_DQ25	DDR_DQ25				
Y04	DDR_DQ29	DDR_DQ29				
Y05	GPIO_121	PWM1	USI4_DO			GPIO_121
Y06	GPIO_114	USI2_CS2	USI4_CS1			GPIO_114
Y07	USI2_CS0	USI2_CS0	DTV_DATA			GPIO_112
Y08	IIC1_SDA	IIC1_SDA	UART3_TX			GPIO_047
Y09	IIC1_SCL	IIC1_SCL	UART3_RX			GPIO_046
Y10	GPIO_156	UART1_TX				GPIO_156
Y11	GPIO_155	UART1_RX				GPIO_155
Y12	SDI0_CMD	SDI0_CMD				GPIO_052
Y13	SDI0_DATA1	SDI0_DATA1				GPIO_054
Y14	SDI0_DATA3	SDI0_DATA3				GPIO_056
Y15	GPIO_058	SDI0_DATA5				GPIO_058
Y16	GPIO_060	SDI0_DATA7				GPIO_060
Y17	SD_DATA2	SD_DATA2				
Y18	SD_DATA0	SD_DATA0				
Y19	GPIO_015					GPIO_015
Y20	GPIO_014					GPIO_014
Y21	GPIO_013					GPIO_013

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Pin No.	Default	Mode0	Mode1	Mode2	Mode3	GPIO
Y23	GPIO_132	CAM_CLKI				GPIO_132
AA01	DDR_DQ24	DDR_DQ24				
AA02	DDR_DQ28	DDR_DQ28				
AA03	DDR_DQ26	DDR_DQ26				
AA04	GPIO_120	PWM0	USI4_DI			GPIO_120
AA05	USI2_DO	USI2_DO	DTV_VALID			GPIO_111
AA06	USI2_DI	USI2_DI	DTV_PSYNC			GPIO_110
AA07	GPIO_113	USI2_CS1	USI4_CS0			GPIO_113
AA08	IIC0_SDA	IIC0_SDA				GPIO_045
AA09	IIC0_SCL	IIC0_SCL				GPIO_044
AA10	GPIO_157	UART1_CTSB	UART2_RX			GPIO_157
AA12	USB_VBUS	USB_VBUS				GPIO_153
AA13	SDI0_DATA0	SDI0_DATA0				GPIO_053
AA14	SDI0_DATA2	SDI0_DATA2				GPIO_055
AA15	GPIO_057	SDI0_DATA4				GPIO_057
AA16	GPIO_059	SDI0_DATA6				GPIO_059
AA17	SD_DATA3	SD_DATA3				
AA18	SD_DATA1	SD_DATA1				
AA19	SDI1_DATA3	SDI1_DATA3				GPIO_067
AA20	GPIO_012					GPIO_012
AA21	GPIO_011					GPIO_011
AA22	GPIO_010					GPIO_010
AA23	SDI1_CKI	SDI1_CKI				GPIO_062
AB03	GPIO_119		USI4_CLK			GPIO_119
AB04	GPIO_118	USI3_CS0	USI0_CS6			GPIO_118
AB05	USI2_CLK	USI2_CLK	DTV_BCLK			GPIO_109
AB09	USB_DP2	USB_DP2				
AB10	GPIO_158	UART1_RTSB	UART2_TX			GPIO_158
AB13	USB_DP1	USB_DP1				
AB16	GPIO_049					GPIO_049
AB17	SD_CMD	SD_CMD				
AB18	GPIO_050	SDI0_CKO				GPIO_050
AB19	SDI1_DATA2	SDI1_DATA2				GPIO_066
AB20	SDI1_DATA1	SDI1_DATA1				GPIO_065
AB21	SDI1_DATA0	SDI1_DATA0				GPIO_064
AB22	GPIO_061	SDI1_CKO				GPIO_061
AC03	GPIO_117	USI3_DO	USI0_CS5			GPIO_117
AC04	GPIO_116	USI3_DI	USI0_CS4			GPIO_116
AC05	GPIO_115	USI3_CLK	USI0_CS3			GPIO_115
AC09	USB_DM2	USB_DM2				
AC13	USB_DM1	USB_DM1				

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Pin No.	Default	Mode0	Mode1	Mode2	Mode3	GPIO
AC15	OSC1_XT1	OSC1_XT1				
AC16	OSC1_XT2	OSC1_XT2				
AC18	SDI0_CKI	SDI0_CKI				GPIO_051
AC19	SD_CKI	SD_CKI				GPIO_048
AC20	SD_CKO	SD_CKO				
AC21	SDI1_CMD	SDI1_CMD				GPIO_063

2. ELECTRICAL SPECIFICATIONS

2.1 Absolute Maximum Ratings

Parameter	Symbol	Function	Rating	Unit
Power supply voltage	VDD11	Core power supply	–0.45 to +1.8	V
	AVDD	PLL power supply	–0.45 to +1.8	V
	VDD18	1.8 V IO power supply	–0.5 to +2.5	V
	VDD33	3.3 V IO power supply	–0.5 to +4.6	V
	VDD33M	1.8V/3.3 V IO power supply Note	–0.5 to +4.6	V
	VDD33D	Anti-fuse power supply	–0.5 to +4.6	V
	USB_AVDD1	Power supply for regulators inside USB PHY 1	–0.5 to +4.6	V
	USB_AVDD2	Power supply for regulators inside USB PHY 2	–0.5 to +4.6	V
	USB_VDD3311	Power supply for USB PHY 1 DP/DM terminals	–0.5 to +4.6	V
	USB_VDD3312	Power supply for USBPHY 2 DP/DM terminals	–0.5 to +4.6	V
	DDR_VDDIO	DDR IO power supply	–0.5 to +2.5	V
Input voltage	V_{I_18}	1.8 V IO power supply	–0.5 to VDD18 + 0.5	V
	V_{I_33}	3.3 V IO power supply	–0.5 to VDD33 + 0.5	V
	V_{I_33M}	1.8V/3.3 V IO power supply Note	–0.5 to VDD33M + 0.5	V
Output voltage	V_{O_18}	1.8 V IO power supply	–0.5 to VDD18 + 0.5	V
	V_{O_33}	3.3 V IO power supply	–0.5 to VDD33 + 0.5	V
	V_{O_33M}	1.8V/3.3 V IO power supply Note	–0.5 to VDD33M + 0.5	V
Storage temperature	T_{stg}	—	–65 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Note One of 1.8V and 3.3V can be chosen and used. It's chosen by setting the voltage supplied to VDD33M to 1.8V or 3.3V.

2.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	VDD11	Normal operation	1.10	1.15	1.20	V
		Power saving mode Note1	0.75	—	—	V
	AVDD	—	1.10	1.15	1.20	V
	VDD18	—	1.65	1.80	1.95	V
	VDD33	—	3.0	3.3	3.6	V
	VDD33M	1.8V supply	1.65	1.80	1.95	V
		3.3V supply	3.0	3.3	3.6	V
	VDD33D	—	3.0	3.3	3.6	V
	USB_AVDD1	Note2	3.0	3.3	3.6	V
	USB_AVDD2	Note2	3.0	3.3	3.6	V
	USB_VDD3311	Note2	3.0	3.3	3.6	V
	USB_VDD3312	Note2	3.0	3.3	3.6	V
	DDR_VDDIO	Note3	1.7	1.8	1.9	V
OSC oscillation voltage Note4	VOSC	—	1.65	—	—	V
Operating ambient temperature	TA	—	–10	—	+70	°C

Notes 1. The voltage which can guarantee a data-hold of an SRAM at the time of a power-saving mode.

2. Refer to USB Specification Revision 2.0 about DC characteristics of USB port I/F.

3. Refer to JEDEC standards about DC characteristics of DDR2 I/F.

4. The voltage which can guarantee continuation after oscillation starting after turning on the power and oscillation starting.

2.3 Capacitance

(TA = +25°C, f = 1 MHz, unmeasured pins returned to 0 V)

Parameter	Symbol	Buffer type	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	1.8 V IO	1	—	5	pF
		3.3 V IO	2	—	6	pF
		1.8V/3.3V IO	2	—	6	pF
Output capacitance	C_O	1.8 V	1	—	5	pF
		2.8 V	2	—	6	pF
		1.8V/3.3V IO	2	—	6	pF
I/O capacitance	C_{IO}	1.8 V	1	—	5	pF
		2.8 V	2	—	6	pF
		1.8V/3.3V IO	2	—	6	pF

※DDR terminal is non-applicable.

2.4 DC Characteristics

2.4.1 VDD18

(Unless it's designated in particular by the item after this, it'll be the standard under 2.2 recommendation operating condition.)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH}	No DC load Note 1		V_{DD18} – 0.1	—	—	V
Output voltage, low	V_{OL}	No DC load Note 1		—	—	0.1	V
Input voltage, high	V_{IH}	CMOS input		0.65 × V_{DD18}	—	V_{DD18} + 0.3	V
Input voltage, low	V_{IL}	CMOS input		–0.3	—	0.35 × V_{DD18}	V
Output current, high	I_{OH1}	V_{OH}=V_{DD18} -0.45V Note 2	4 mA setting Note 3	3.2	—	—	mA
	I_{OH2}		6 mA setting Note 3	4.8	—	—	mA
	I_{OH3}		8 mA setting Note 3	6.3	—	—	mA
	I_{OH4}		12 mA setting Note 3	7.7	—	—	mA
Output current, low	I_{OL1}	V_{OL}=0.45V Note 2	4 mA setting Note 3	3.2	—	—	mA
	I_{OL2}		6 mA setting Note 3	4.8	—	—	mA
	I_{OL3}		8 mA setting Note 3	6.3	—	—	mA
	I_{OL4}		12 mA setting Note 3	7.7	—	—	mA
Hysteresis voltage	V_H	Schmitt input		0.1 × V_{DD18}	—	0.4 × V_{DD18}	V
Negative trigger voltage	V_N	Schmitt input		0.3 × V_{DD18}	—	0.6 × V_{DD18}	V
Positive trigger voltage	V_P	Schmitt input		0.4 × V_{DD18}	—	0.7 × V_{DD18}	V
Input leakage current, high	I_{LH}	V_I = V_{DD18}		—	—	10	μA
Input leakage current, low	I_{LL}	V_I = GND		—	—	10	μA
Pull-up resistance	R_{PU}	—		37	50	80	kΩ
Pull-down resistance	R_{PD}	—		37	50	80	kΩ

Notes **1.** The parameters V_{OH} and V_{OL} here are the values guaranteed when there is no load when applying the DC current.

2. The parameters V_{OH} and V_{OL} here define the output current.

3. This is the value set to the I/O buffer output current drive switch register. It's established at CHG_DRIVE0-5 register of a CHG module.

2.4.2 VDD33

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH}	No DC load Note 1		V_{DD33} – 0.1	–	–	V
Output voltage, low	V_{OL}	No DC load Note 1		–	–	0.1	V
Input voltage, high	V_{IH}	CMOS input		2.0	–	V_{DD33} + 0.3	V
Input voltage, low	V_{IL}	CMOS input		–0.3	–	0.8	V
Output current, high	I_{OH1}	$V_{OH} = V_{DD33(min)}$ – 0.6 V Note 2	4 mA setting Note 3	4	–	–	mA
	I_{OH2}		6 mA setting Note 3	6	–	–	mA
	I_{OH3}		8 mA setting Note 3	7.8	–	–	mA
	I_{OH4}		12 mA setting Note 3	9.5	–	–	mA
Output current, low	I_{OL1}	V_{OL} = 0.4 V Note 2	4 mA setting Note 3	4	–	–	mA
	I_{OL2}		6 mA setting Note 3	6	–	–	mA
	I_{OL3}		8 mA setting Note 3	7.8	–	–	mA
	I_{OL4}		12 mA setting Note 3	9.5	–	–	mA
Hysteresis voltage	V_H	Schmitt input		0.11 × V_{DD33}	–	0.41 × V_{DD33}	V
Negative trigger voltage	V_N	Schmitt input		0.17 × V_{DD33}	–	0.38 × V_{DD33}	V
Positive trigger voltage	V_P	Schmitt input		0.54 × V_{DD33}	–	0.65 × V_{DD33}	V
Input leakage current, high	I_{L_H}	$V_I = V_{DD33}$		–	–	10	μA
Input leakage current, low	I_{L_L}	V_I = GND		–	–	10	μA
Pull-up resistance	R_{PU}	50 kΩ resistor		37	50	80	kΩ
Pull-down resistance	R_{PD}	50 kΩ resistor		37	50	80	kΩ

Notes **1.** The parameters V_{OH} and V_{OL} here are the values guaranteed when there is no load when applying the DC current.

2. The parameters V_{OH} and V_{OL} here define the output current.

3. This is the value set to the output current drive switch register. It's established at CHG_DRIVE0-5 register of a CHG module.

2.4.3 VDD33M (1.8V supply)

The power-supply voltage when supplying VDD33M with 1.8V, is shown with VDD18M.

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH}	No DC load Note 1		V_{DD18M} – 0.1	–	–	V
Output voltage, low	V_{OL}	No DC load Note 1		–	–	0.1	V
Input voltage, high	V_{IH}	CMOS input		0.65 × V_{DD18M}	–	V_{DD18M} + 0.3	V
Input voltage, low	V_{IL}	CMOS input		–0.3	–	0.35 × V_{DD18M}	V
Output current, high	I_{OH1}	V_{OH} = V_{DD18M} – 0.6 V Note 2	4 mA setting Note 3	2.2	–	–	mA
	I_{OH2}		6 mA setting Note 3	3.3	–	–	mA
	I_{OH3}		8 mA setting Note 3	4.3	–	–	mA
	I_{OH4}		12 mA setting Note 3	5.4	–	–	mA
Output current, low	I_{OL1}	V_{OL} = 0.4 V Note 2	4 mA setting Note 3	2.8	–	–	mA
	I_{OL2}		6 mA setting Note 3	4.1	–	–	mA
	I_{OL3}		8 mA setting Note 3	5.4	–	–	mA
	I_{OL4}		12 mA setting Note 3	6.7	–	–	mA
Hysteresis voltage	V_H	Schmitt input		0.1 × V_{DD18M}	–	0.4 × V_{DD18M}	V
Negative trigger voltage	V_N	Schmitt input		0.2 × V_{DD18M}	–	0.6 × V_{DD18M}	V
Positive trigger voltage	V_P	Schmitt input		0.4 × V_{DD18M}	–	0.7 × V_{DD18M}	V
Input leakage current, high	I_{L_H}	V_I = V_{DD18M}		–	–	10	μA
Input leakage current, low	I_{L_L}	V_I = GND		–	–	10	μA
Pull-up resistance	R_{PU}	50 kΩ resistor		37	50	80	kΩ
Pull-down resistance	R_{PD}	50 kΩ resistor		37	50	80	kΩ

Notes **1.** The parameters V_{OH} and V_{OL} here are the values guaranteed when there is no load when applying the DC current.

2. The parameters V_{OH} and V_{OL} here define the output current.

3. This is the value set to the output current drive switch register. It's established at CHG_DRIVE0-5 register of a CHG module.

2.4.4 VDD33M (3.3V supply)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH}	No DC load Note 1		V_{DD33M} – 0.1	–	–	V
Output voltage, low	V_{OL}	No DC load Note 1		–	–	0.1	V
Input voltage, high	V_{IH}	CMOS input		2.0	–	V_{DD33M} + 0.5	V
Input voltage, low	V_{IL}	CMOS input		–0.3	–	0.8	V
Output current, high	I_{OH1}	V_{OH} = $V_{DD33M(min)}$ – 0.6 V Note 2	4 mA setting Note 3	4	–	–	mA
	I_{OH2}		6 mA setting Note 3	6	–	–	mA
	I_{OH3}		8 mA setting Note 3	7.8	–	–	mA
	I_{OH4}		12 mA setting Note 3	9.5	–	–	mA
Output current, low	I_{OL1}	V_{OL} = 0.4 V Note 2	4 mA setting Note 3	4	–	–	mA
	I_{OL2}		6 mA setting Note 3	6	–	–	mA
	I_{OL3}		8 mA setting Note 3	7.8	–	–	mA
	I_{OL4}		12 mA setting Note 3	9.5	–	–	mA
Hysteresis voltage	V_H	Schmitt input		0.11 × V_{DD33M}	–	0.41 × V_{DD33M}	V
Negative trigger voltage	V_N	Schmitt input		0.17 × V_{DD33M}	–	0.38 × V_{DD33M}	V
Positive trigger voltage	V_P	Schmitt input		0.54 × V_{DD33M}	–	0.65 × V_{DD33M}	V
Input leakage current, high	I_{L_H}	V_I = V_{DD33M}		–	–	10	μA
Input leakage current, low	I_{L_L}	V_I = GND		–	–	10	μA
Pull-up resistance	R_{PU}	50 kΩ resistor		37	50	80	kΩ
Pull-down resistance	R_{PD}	50 kΩ resistor		37	50	80	kΩ

Notes **1.** The parameters V_{OH} and V_{OL} here are the values guaranteed when there is no load when applying the DC current.

2. The parameters V_{OH} and V_{OL} here define the output current.

3. This is the value set to the output current drive switch register. It's established at CHG_DRIVE0-5 register of a CHG module.

2.4.5 Standby state current

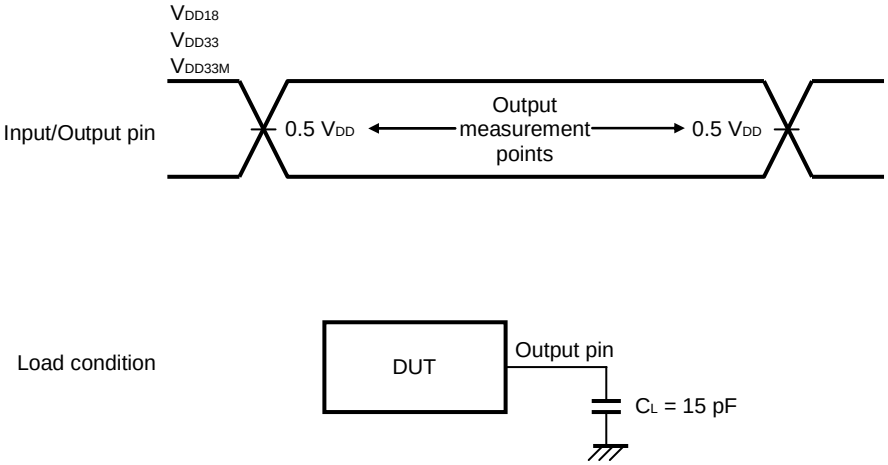
(T_A = 25°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Standby current	I_{DD_PA}	Logic power supply PA, f = 0 Hz, V_{DD11} = 0.75 V	—	0.6	—	mA
	I_{DD_IO18}	IO power supply f = 0 Hz, V_{IO18} = 1.8 V	—	5	—	μA
	I_{DD_IO33}	IO power supply f = 0 Hz, V_{IO3} = 3.3 V	—	5	—	μA
	I_{DD_IO33M}	IO power supply f = 0 Hz, V_{IO3} = 3.3 V	—	5	—	μA

2.5 AC Characteristics

2.5.1 AC test I/O measurement points

Figure 2-1. AC Test I/O Measurement Points



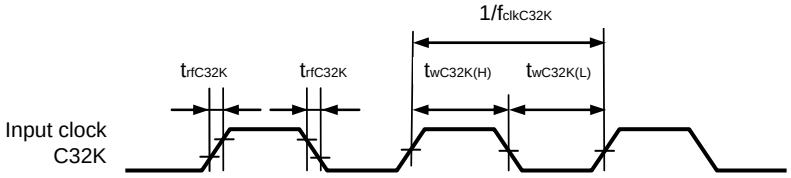
Remark Excluding the OSC pin. Unless specified otherwise, the load of C_L is assumed to be 15 pF.
Unless it's designated in particular by the item after this, it'll be the standard under 2.2 recommendation operating condition

2.5.2 System control

(1) Clock (input timing requirements)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
C32K frequency	$f_{clkC32K}$	–	–	32.768	–	kHz
C32K rise/fall time	t_{rfC32K}	0 to 90%	–	–	1	μs
32 kHz input clock duty ratio	$I_{dutyC32K}$	–	30	–	70	%
32 kHz input clock jitter	$I_{jitterC32K}$	–	–20	–	20	ns

Figure 2-2. Clock Timing



(2) PLL

PLL1 lock up time : 200 μ s max
PLL2 lock up time : 2000 μ s max
PLL3 lock up time : 800 μ s max
PLL4 lock up time : 2000 μ s max

(3) OSC

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
OSC oscillation frequency range	$f_{C(OSC)}$	Internal oscillator OSCx Note1,Note2, Note3 (OSCx_XT1, OSCx_XT2)		1	–	27	MHz
		AMP ability setting Note4	C1=1 / C0=1	20	–	27	MHz
			C1=1 / C0=0	10	–	20	MHz
			C1=0 / C0=1	4	–	10	MHz
			C1=0 / C0=0	1	–	4	MHz

OSC lock up time : 2000 μ s max Note5

Notes **1.** x=0 or 1

2. Use by 10-27MHz is recommended. If you have any question (When using by 1-10MHz), please contact us through

"http://japan.renesas.com/contact/contact_tech.html " (Japanese) or

"http://america2.renesas.com/support/index.html " (English).

3. It's subject to the next restrictions.

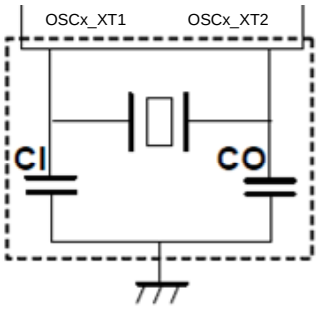
Oscillation frequency ≦ 20MHz : Capacitance is 8pF.

Oscillation frequency > 20MHz : Capacitance is 7pF.

4. It's possible to choose a correspondence frequency by changing the AMP ability. Setting is a OSC_CX register of a SMU module.

5. For lock up time to change by quartz crystal units, estimate by actual environment.

Figure 2-3. Recommended Oscillator



Cautions 1. Keep the wiring length between the oscillator and the OSCx_XT1 and OSCx_XT2 pins as short as possible.

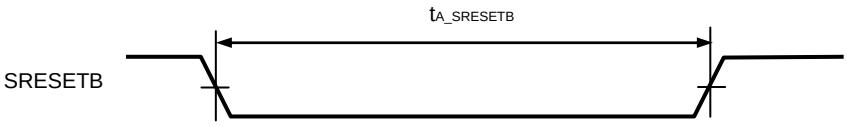
2. Do not cross the wiring with the other signal lines in the area enclosed by the broken lines.

3. Thoroughly evaluate matching of the resonator.

(4) Reset

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SRESETB low-level width	$t_{A\_SRESETB}$	—	6	—	—	ms

Figure 2-4. Reset Timing



2.5.3 Asynchronous bus (AB) interface

（VDD33＝3.3±0.3 V, input pin : Normal , Drive=8mA ） (1/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
AB_CSB[3:0] fall to AB_ADV fall	t_{200}	－	CS_ADV×Tf-5	CS_ADV×Tf+5	ns	
AB_CSB[3:0] active width (at read)	t_{201}	－	(CS_ADV+ADV_WIDTH+1+T0+T1+RDT+1+T2) × Tf-5	(CS_ADV+ADV_WIDTH+1+T0+T1+RDT+1+T2) ×Tf+5	ns	1, 2, 4, 5
AB_CSB[3:0] fall to AB_ADV rise	t_{202}	－	(CS_ADV+ADV_WIDTH+1)×Tf-5	(CS_ADV+ADV_WIDTH+1)×Tf+5	ns	
AB_ADV active width	t_{203}	AB_ADV=Low	(ADV_WIDTH+1)×Tf-5	(ADV_WIDTH+1)×Tf+5	ns	
Lower ADD hold time (at AD-Mux read)	t_{204}	－	See Note6	See Note6	ns	1, 6
AB_ADV rise to AB_RDB fall	t_{205}	Falling edge of AB_RDB	T0×Tf-5	T0×Tf+5	ns	1
AB_RDB active width	t_{206}	AB_RDB=Low	(T1+RDT+1)×Tf-5	(T1+RDT+1)×Tf+5	ns	4, 5
AB_RDB rise to AB_CSB[3:0] rise	t_{207}	Rising edge of AB_RDB	T2×Tf-5	T2×Tf+5	ns	4, 5
AB_CSB[3:0] assert interval time (at read)	t_{208}	－	(CSint+1)×Tf-5	－	ns	4, 5
Read data setup time	t_{209}	Rising edge of AB_RDB	(RDT+1)×Tf + 8	－	ns	4, 5
Read data hold time	t_{210}	Rising edge of AB_RDB	0	－	ns	
Address determination to AB_RDB fall	t_{211}	Falling edge of AB_RDB	(CS_ADV+ADV_WIDTH+1+T0)×Tf-5	(CS_ADV+ADV_WIDTH+1+T0)×Tf-5	ns	1
AB_CSB[3:0] fall to AB_RDB fall	t_{212}	Falling edge of AB_RDB	(CS_ADV+ADV_WIDTH+1+T0)×Tf-5	(CS_ADV+ADV_WIDTH+1+T0)×Tf+5	ns	1
AB_CSB[3:0] fall to lower ADD output delay (at AD-MUX)	t_{213}	－	-5	5	ns	
AB_RDB rise to ADD output transition time	t_{214}	－	(T2+CSint+1)×Tf-5	－	ns	4, 5
AB_CSB[3:0] active width (at write)	t_{220}	－	(CLK_MODE=1 setting) (CS_ADV+ADV_WIDTH+1+T0_W+T1_W+0.5+T2_W)×Tf – 5 (CLK_MODE=0 setting) (CS_ADV+ADV_WIDTH+1+T0_W+T1_W+1+T2_W)×Tf – 5	(CLK_MODE=1 setting) (CS_ADV+ADV_WIDTH+1+T0_W+T1_W+0.5+T2_W)×Tf + 5 (CLK_MODE=0 setting) (CS_ADV+ADV_WIDTH+1+T0_W+T1_W+1+T2_W)×Tf + 5	ns	3, 7

(2/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
AB_ADV rise to AB_WRB fall	t_{221}	Falling edge of AB_WRB	T0_W×Tf-5	T0_W×Tf+5	ns	
AB_WRB active width	t_{222}	AB_WRB=Low	(CLK_MODE=1 setting) (T1_W+0.5)×Tf - 5 (CLK_MODE=0 setting) (T1_W+1)×Tf – 5	(CLK_MODE=1 setting) (T1_W+0.5)×Tf + 5 (CLK_MODE=0 setting) (T1_W+1)×Tf + 5	ns	3, 7
AB_WRB rise to AB_CSB[3:0] rise	t_{223}	Rising edge of AB_WRB	T2_W×Tf-5	T2_W×Tf+5	ns	
AB_WRB rise to AB_AD[15:0] Hi-z transition	t_{224}	Rising edge of AB_WRB	T2_W×Tf-5	T2_W×Tf+5	ns	
Address determination to AB_WRB fall	t_{225}	Falling edge of AB_WRB	(CS_ADV+ADV_WIDTH+1+T0_W)×Tf-5	(CS_ADV+ADV_WIDTH+1+T0_W)×Tf+5	ns	
AB_CSB[3:0] fall to AB_WRB fall	t_{226}	Falling edge of AB_WRB	(CS_ADV+ADV_WIDTH+1+T0_W)×Tf-5	(CS_ADV+ADV_WIDTH+1+T0_W)×Tf+5	ns	
AB_CSB[3:0] assert interval time (at write)	t_{227}	–	(CLK_MODE=1 setting) (CSint+1+0.5)×Tf - 5 (CLK_MODE=0 setting) (CSint+1+1)×Tf – 5	–	ns	4, 5, 7
AB_WRB to Data output start time (at AD non Mux)	t_{228}	–	-5	5	ns	
AB_ADV rise to AB_AD[15:0] ADD-Data transition (at AD-Mux write)	t_{229}	–	T0_W×Tf-5	T0_W×Tf+5	ns	8
AB_WRB rise to ADD transition time	t_{230}	–	(CLK_MODE=1 setting) (T2_W+CSint+1+0.5)×Tf - 5 (CLK_MODE=0 setting) (T2_W+CSint+1+1)×Tf – 5	–	ns	7
AB_WAIT rise to T1 section end	t_{240}	–	(CLK_MODE=1 setting) 1×Tf+8 (CLK_MODE=0 setting) 2×Tf+8	–	ns	7,9
AB_WAIT fall to AB_RDB rise	t_{241}	–	–	(CLK_MODE=1 setting) (2+RDT+1)×Tf+12 (CLK_MODE=0 setting) (3+RDT+1)×Tf+12	ns	7

(3/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
AB_WAIT rise to T1_W+1 section end or (AB_WAIT rise to T1_W+0.5 section end)	t_{242}	−	(CLK_MODE=1 setting) 1×Tf+8 (CLK_MODE=0 setting) 2×Tf+8	−	ns	7, 10
AB_WAIT fall to AB_WRB rise	t_{243}	−	−	(CLK_MODE=1 setting) 2×Tf+12 (CLK_MODE=0 setting) 3×Tf+12	ns	7

Remark Tf = AB_CLK 2clocks (CLK_MODE=1 setting)
AB_CLK 1 clock (CLK_MODE=0 setting) AB_CLK is HFB domain clock.
Refer to SMU User's manual (R19UH0037EJ) for a setting method of AB_CLK frequency.
ex) In case of PLL2=500MHz, a frequency of AB_CLK can be set as 125MHz by the following setting.
DMSRC_PLLSEL_NRM = 4 (CKMODE_PLLSEL register)
HFBDOMAIN_DIV_NRA = 3 (NORMALA_DIV register)
MODE_SEL = 1 (CLK_MODE_SEL register)

T0, T1, T2, CSInt : AB0_CSxWAITCTRL setting value
T0_W, T1_W, T2_W : AB0_CSxWAITCTRL_W setting value
RDT : AB0_CSxREADCTRL setting value
CS_ADV, ADV_WIDTH : AB0_CSxCONTROL setting value
x : 0-5

Note 1. Setting of T0 operates as setting of "1" in case of "0" at the time of AD-MUX.
2. Setting of T1 operates as setting of "1" in case of "0".
3. Setting of T1_W operates as setting of "1" in case of "0".
4. It's necessary to make the total of the set value of RDT,T2,CSINT more than 1 at the time of CLK_MODE=1 setting.
5. It's necessary to make the total of the set value of RDT,T2,CSINT more than 2 at the time of CLK_MODE=0 setting.
6. t204 is in combination of AD_OE bit (AB0_CSxCONTROL) and CLK_MODE, and 4 ways of timing can be established. (the following).

Lower ADD hold time (min)

	CLK_MODE=0	CLK_MODE=1
AD_OE=0	-5	-5
AD_OE=1	(T0-1)×Tf-5	(T0-0.5)×Tf-5

Lower ADD hold time (max)

	CLK_MODE=0	CLK_MODE=1
AD_OE=0	5	5
AD_OE=1	(T0-1)×Tf+5	(T0-0.5)×Tf+5

When it's CLK_MODE=0, T0=1 setting it changes into Hi-Z by the same timing as a fall of AB_RDB.

7. It's possible to set CLK_MODE at the AB_FLASHCLKCTRL register.
8. Only when setting of T0_W is 0 at the time of AD-Mux, refer to following Min,Max.

t229 = Min : 0.5×Tf-5, Max : 0.5×Tf+5 (CLK_MODE=1 setting, AD-Mux, T0_W=0)

t229 = Min : 1×Tf-5, Max : 1×Tf+5 (CLK_MODE=0 setting, AD-Mux, T0_W=0)

9. Condition to use WAIT function

Active AB_WAIT signal by the minimum time before the end of T1 section. Data latch will stop till inactivating AB_WAIT.

In case of inactivating AB_WAIT signal by the minimum time before the end of T1 section, Wait function will not work.

10. Condition to use WAIT function

Active AB_WAIT signal by the minimum time before the end of T1 section. Data latch will stop till inactivating AB_WAIT.

In case of inactivating AB_WAIT signal by the minimum time before the end of T1 section, Wait function will not work.

(At the time of CLK_MODE=1 is “T1_W+0.5”)

Figure 2-5. Single Read Timing (AD-Mux)

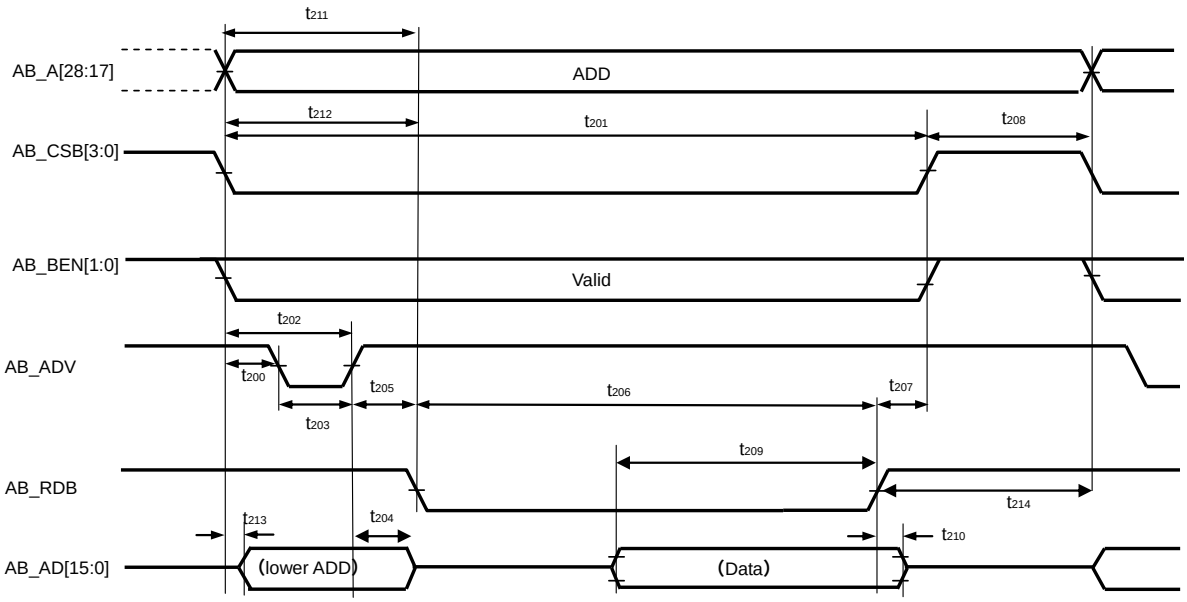


Figure 2-6. Single Write Timing (AD-Mux)

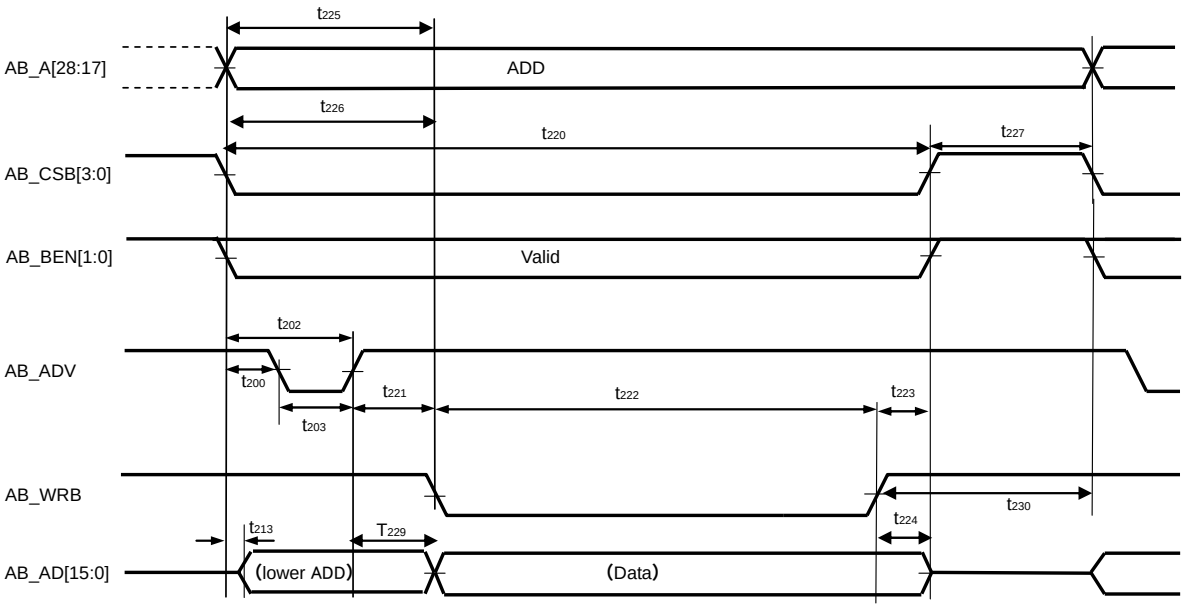


Figure 2-7. Single Read Timing (AD non Mux)

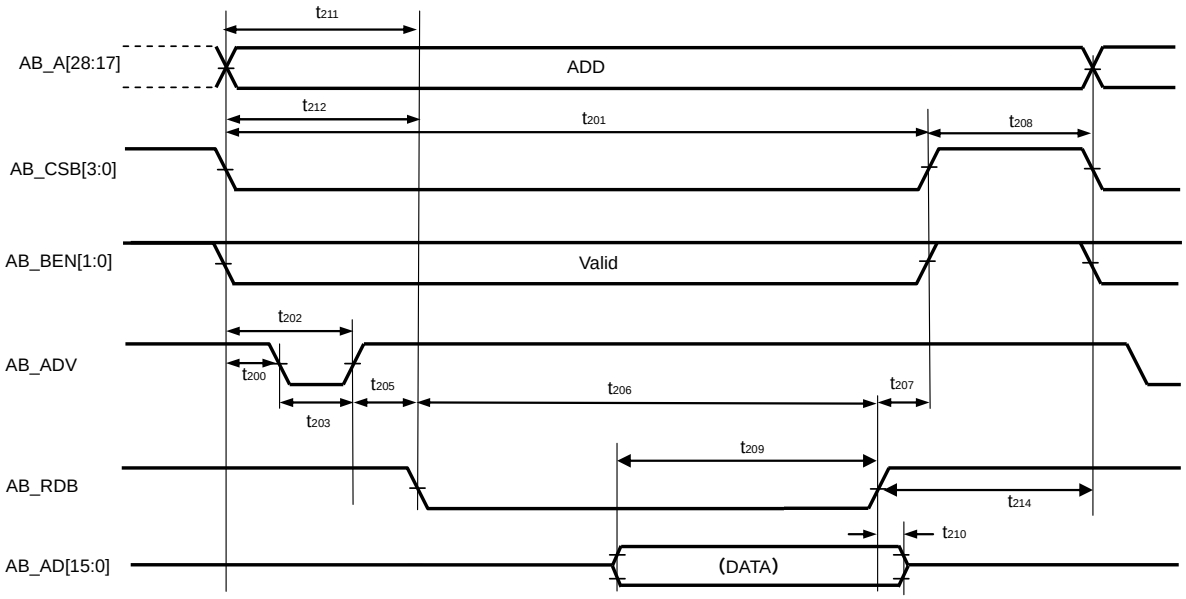


Figure 2-8. Single Write Timing (AD non Mux)

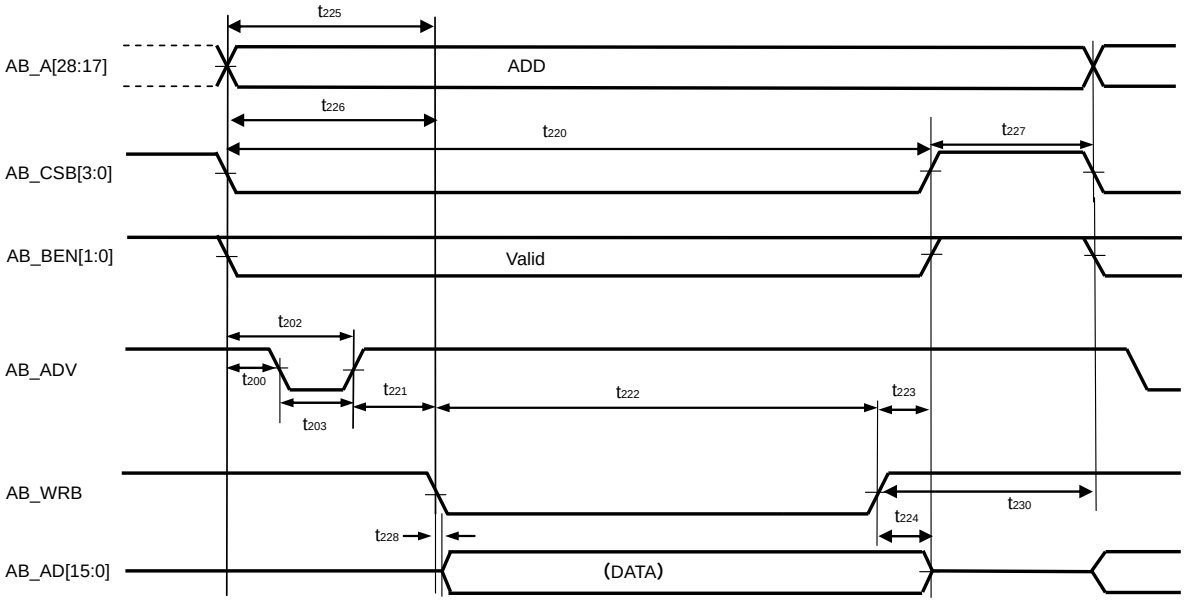


Figure 2-9. Single Read Timing (Wait)

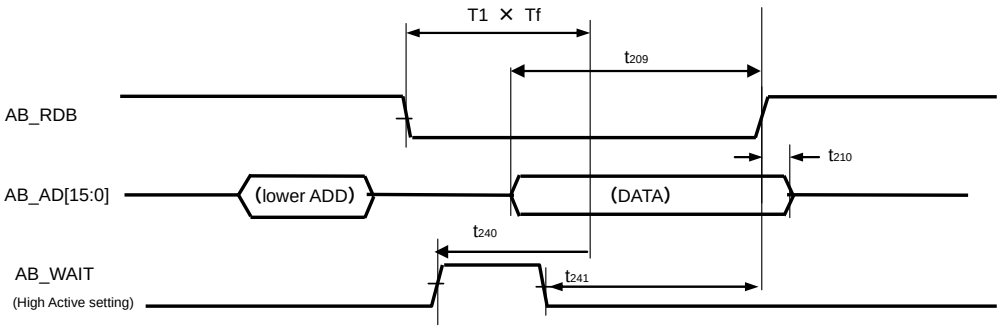
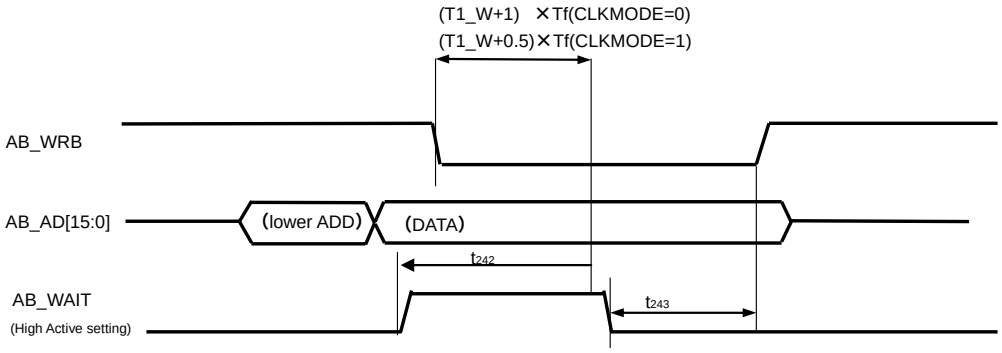


Figure 2-10. Single Write Timing (Wait)



2.5.4 IIC interface

Parameter	Symbol	Conditions	Standard Mode[Note 1]		Fast Mode[Note 1]		Unit
			MIN.	MAX.	MIN.	MAX.	
IIC_SCL clock frequency	f_C	—	0	100	0	400	kHz
IIC bus free time	t_{BF}	Interval between stop and start conditions	4.7	–	1.3	–	μs
IIC hold time[Note 2]	t_{H1}	—	4.0	–	0.6	–	μs
IIC hold time (SCL clock)	t_{WL}	"Low" state	4.7	–	1.3	–	μs
	t_{WH}	"Hi" state	4.0	–	0.6	–	μs
IIC setup time	t_{SU1}	Start condition Restart condition	4.7	–	0.6	–	μs
IIC data setup time	t_{SU2}	—	250	–	100[Note 3]	–	ns
IIC rise time	t_R	SDA and SCL signals	–	–	–	300[Note 4]	ns
IIC fall time	t_F	SDA and SCL signals	–	–	–	300[Note 4]	ns
IIC setup time	t_{SU3}	Stop condition	4.0	–	0.6	–	μs
IIC data hold time	t_{H2}	Clock fall output	5.0	–	—	–	μs
		Clock fall input	0	3.45	0[Note 5]	0.9[Note 6]	μs
Capacitance load of each IIC bus line	C_b	—	–	400	–	400	pF

Notes 1. Select the standard mode or fast mode by using the SMC0 bit of the IIC0 clock select register (IICCL0).

2. At the start condition, the first clock pulse is generated after the hold time.

3. The fast mode I^2C bus can be used in the standard-mode I^2C bus system. In this case, set the fast mode I^2C bus so that it meets the following conditions.

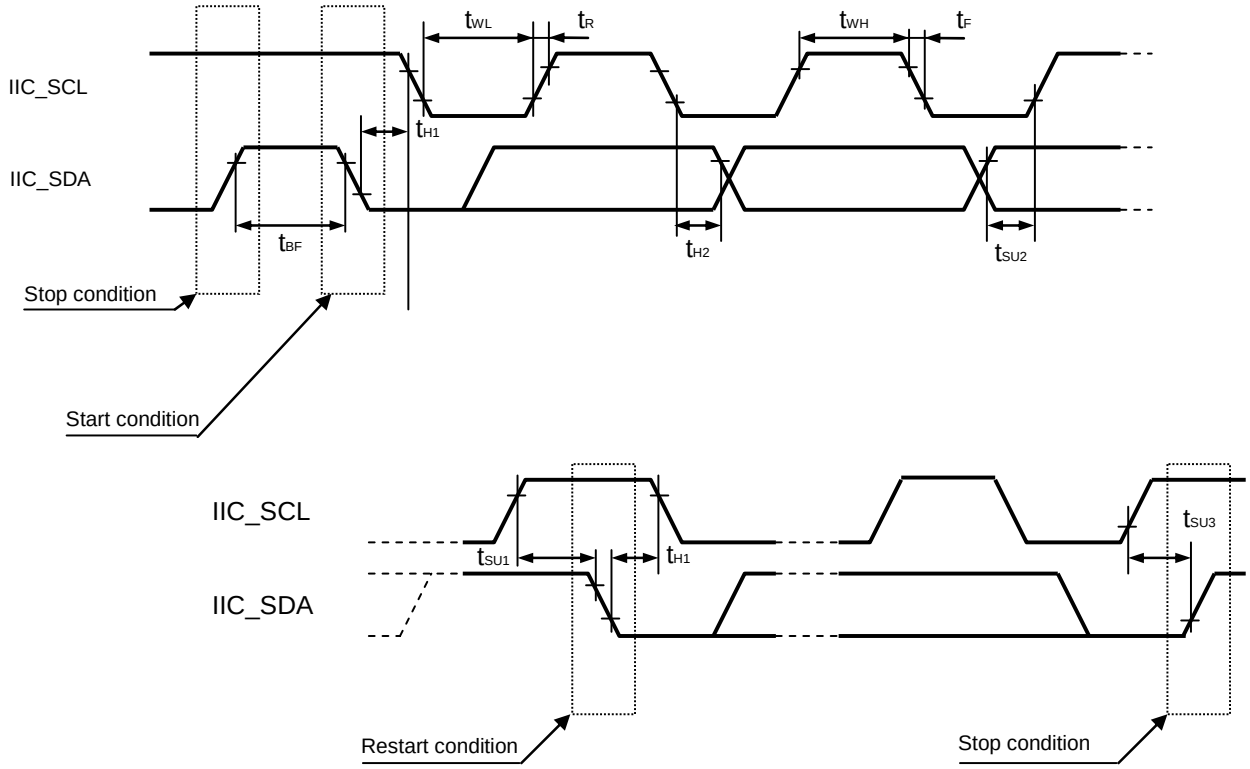
- If the system does not extend the IIC_SCL signal's low state hold time: $t_{SU2} \geq 250$ ns

4. Do not input noise exceeding the hysteresis width of the 1.8 V system IO Schmitt buffer during a rise or fall time.

5. The system requires a minimum of 300 ns hold time internally for the SDA signal (at V_{IH} (MIN.) [0.7 V_{DD2}] of IIC_SCL signal) in order to occupy the undefined area at the falling edge of IIC_SCL.

6. If the system does not extend the IIC_SCL signal low hold time (t_{WL}), only the maximum data hold time (t_{H2}) needs to be satisfied.

Figure 2-11. IIC Bus Interface Timing



2.5.5 Unified Serial Interface

(1) Audio/Voice interface

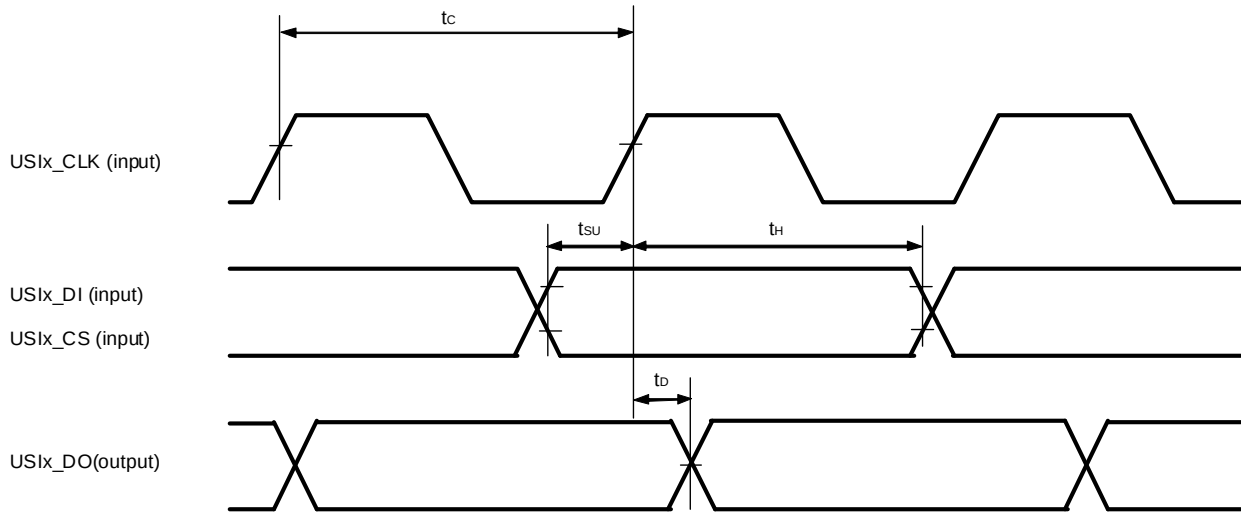
(a) Slave mode

(VDD33＝3.3±0.3 V, input pin : schmitt , Drive=4mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USIx_CLK cycle time	t_C	–	50	—	—	ns
USIx_DI, USIx_CS setup time	t_{SU}	Rise or fall of USI_xCLK	20	—	—	ns
USIx_DI, USIx_CS hold time	t_H	Rise or fall of USI_xCLK	20	—	—	ns
USIx_DO output delay time	t_D	Rise or fall of USI_xCLK	0	—	20	ns

Remark Time from the valid edge
x = 0-5

Figure 2-12. Audio/Voice Interface Timing (Slave Mode)



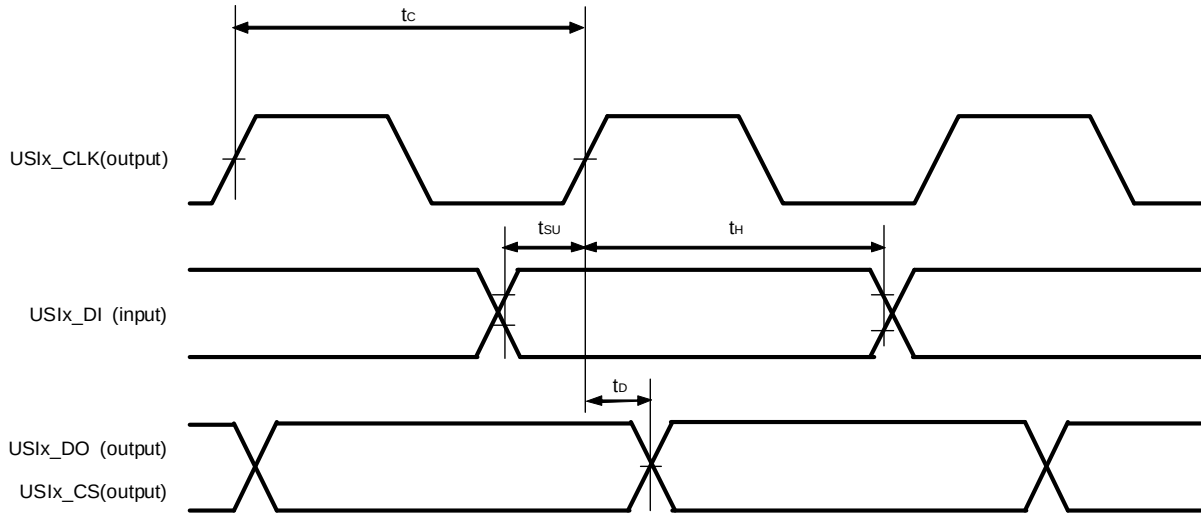
(b) Master mode

(VDD33＝3.3±0.3 V, input pin : schmitt , Drive=4mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USIx_CLK cycle time	t_C	–	50	—	—	ns
USIx_DI setup time	t_{SU}	–	20	—	—	ns
USIx_DI hold time	t_H	–	20	—	—	ns
USIx_DO, USIx_CS output delay time	t_D	–	–5	—	20	ns

Remark Time from the valid edge
x = 0-5

Figure 2-13. Audio/Voice Interface Timing (Master Mode)



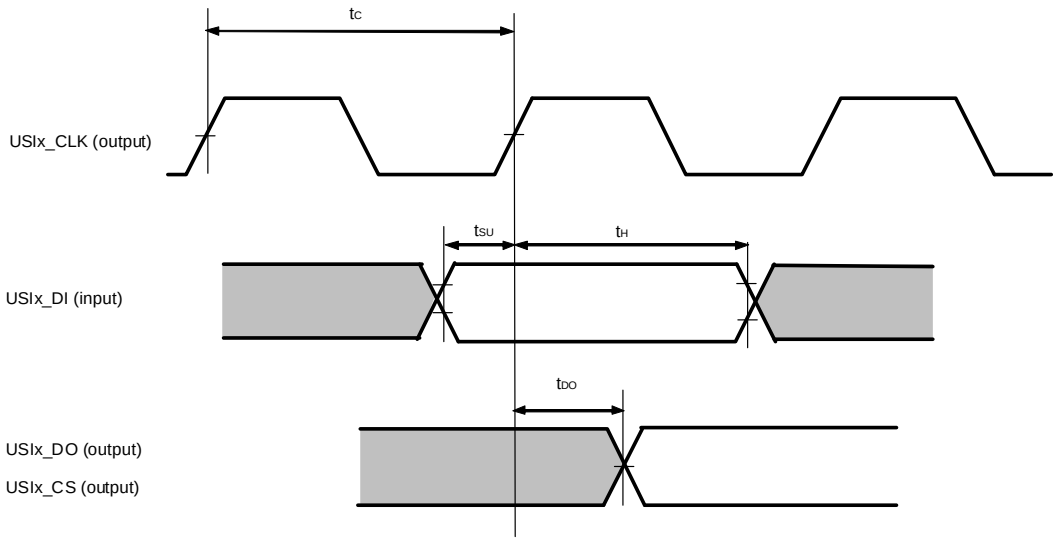
(2) SPI interface

(a) Master mode

(VDD33＝3.3±0.3 V, input pin : Normal , Drive=4mA (USI0, USI1) 6mA (USI2))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
<USI0-1, 3-5> x=0-1, 3-5						
USIx_CLK output cycle	t_C	—	33	—	—	ns
USIx_DI setup time	t_{SU0}	Rise or fall of USI_xCLK	12	—	—	ns
USIx_DI hold time	t_{H0}	Rise or fall of USI_xCLK	0	—	—	ns
USIx_DO, USIx_CS output delay time	t_{DO}	Rise or fall of USI_xCLK	0	—	12	ns
<USI2> x=2						
USIx_CLK output cycle	t_C	—	16.6	—	—	ns
USIx_DI setup time	t_{SU0}	Rise or fall of USI_xCLK	8	—	—	ns
USIx_DI hold time	t_{H0}	Rise or fall of USI_xCLK	0	—	—	ns
USIx_DO, USIx_CS output delay time	t_{DO}	Rise or fall of USI_xCLK	0	—	6	ns

Figure 2-14. SPI Interface Timing (Master Mode)



Notes 1. USIx_CLK can output reverse by register setting.

2. USIx_CLK doesn't output USIx_CLK inactive period (It'll be inactive level fixing.)

3. When the read latency of the connection device is long, it's an input/output phase switch function of DI/DO (rising/falling of SCLK) and is applicable.

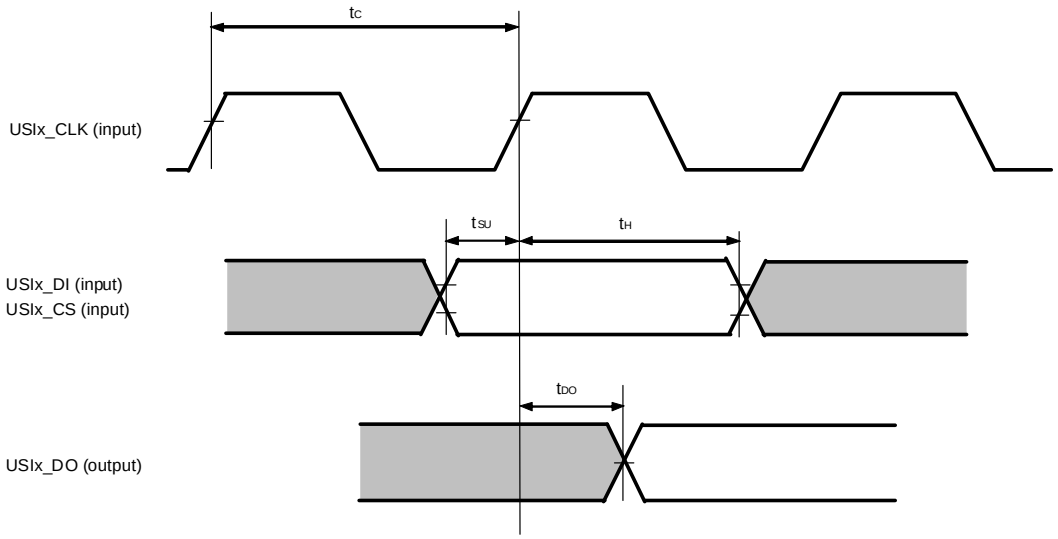
(b) Slave mode

（VDD33＝3.3±0.3 V, input pin : Normal , Drive=4mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USIx_CLK input cycle	t_C	–	50	–	–	ns
USIx_DI, USIx_CS setup time	t_{SU}	Rise or fall of USI_xCLK	5	–	–	ns
USIx_DI, USIx_CS hold time	t_H	Rise or fall of USI_xCLK	15	–	–	ns
USIx_DO delay time	t_{DO}	Rise or fall of USI_xCLK	3	–	20	ns

Remark Time from the valid edge
x = 0-5

Figure 2-15. SPI Interface Timing (Slave Mode)



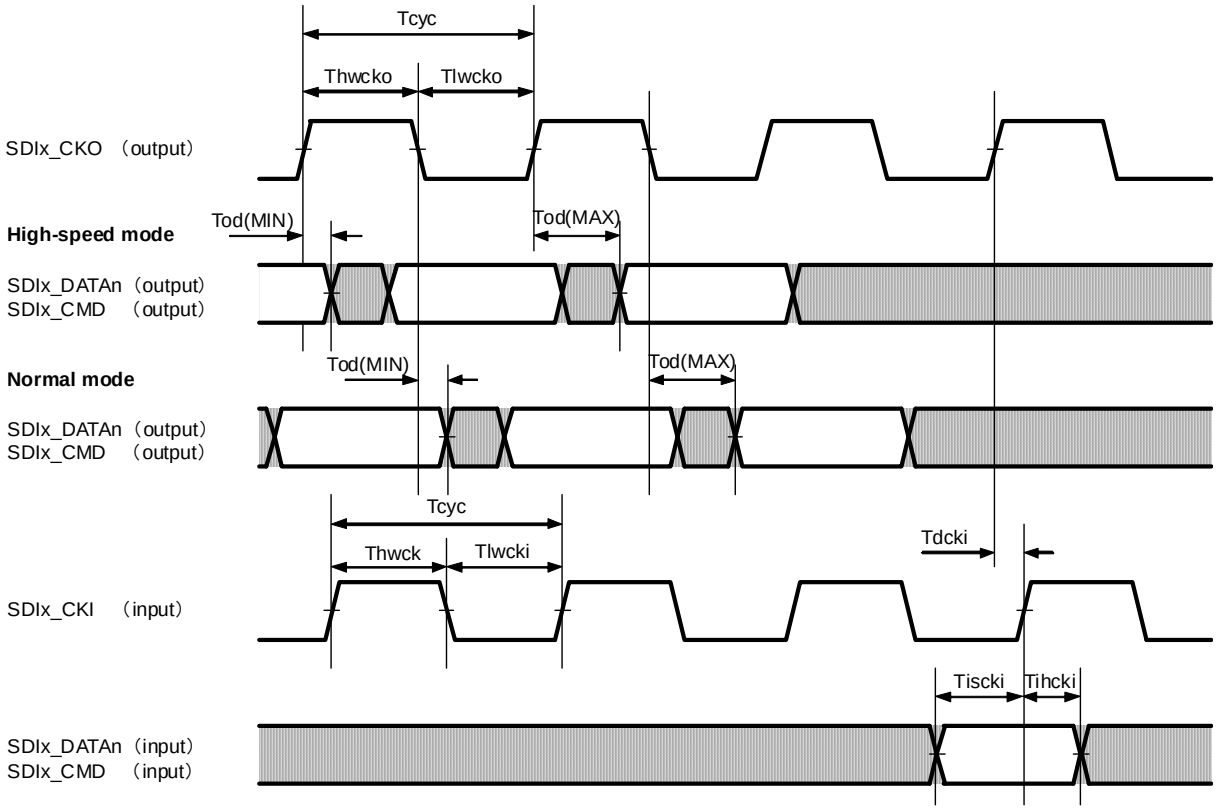
2.5.6 SDIO interface

SDIO1, 2 is MMC non-correspondence.

(VDD33=3.3±0.3 V, input pin : Schmitt, Drive=8mA, outside loop, CMD and Data is pull-up.)

Parameter	Symbol	Conditions	SD0 (SDIA), SD1 (SDIB), SD2 (SDIC)			
			MIN.	TYP.	MAX.	Unit
Clock cycle	T_{cyc}	–	19.2	–	–	ns
Output clock high-level width	T_{hwcko}	@52MHz	8.1	9.6	11.1	ns
Output clock low-level width	T_{lwcko}	@52MHz	8.1	9.6	11.1	ns
Output delay	T_{od}	SDIO	3	–	14	ns
Output delay	T_{od}	SDI1, SDI2	2	–	14	ns
Input clock high-level width	T_{hwcki}	–	7.6	9.6	11.6	ns
Input clock low-level width	T_{lwcki}	–	7.6	9.6	11.6	ns
Input clock delay time	T_{dcki}	–	0	–	10	ns
Setup time	T_{iscki}	–	2	–	–	ns
Hold time	T_{ihcki}	–	1	–	–	ns

Figure 2-16. SDIO Interface Timing



Remark x = 0 to 2

n = 0 to 7 (SDI0)

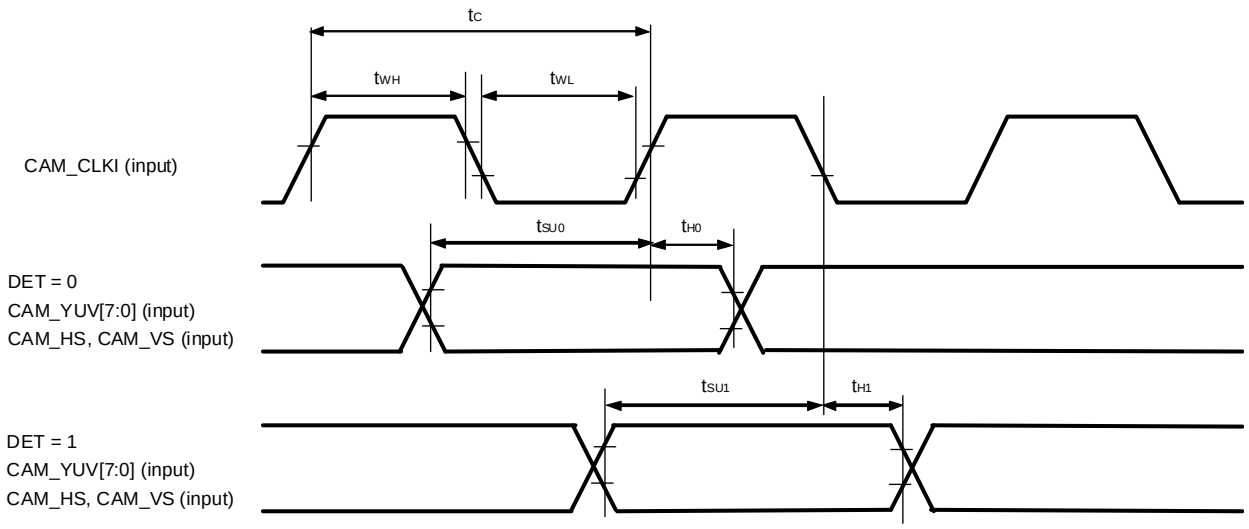
0 to 3 (SDI1, SDI2)

2.5.7 Camera interface

(VDD33＝3.3±0.3 V, input pin : Normal)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CAM_CLKI input cycle	t_C	—	10	—	—	ns
CAM_CLKI high-level width	t_{WH}	—	4	—	—	ns
CAM_CLKI low-level width	t_{WL}	—	4	—	—	ns
CAM_YUV[7:0], CAM_HS, CAM_VS setup time	t_{SU0}	DET = 0	5	—	—	ns
CAM_YUV[7:0], CAM_HS, CAM_VS hold time	t_{H0}	DET = 0	0	—	—	ns
CAM_YUV[7:0], CAM_HS, CAM_VS setup time	t_{SU1}	DET = 1	5	—	—	ns
CAM_YUV[7:0], CAM_HS, CAM_VS hold time	t_{H1}	DET = 1	0	—	—	ns

Figure 2-17. Camera Interface Timing



2.5.8 LCD interface

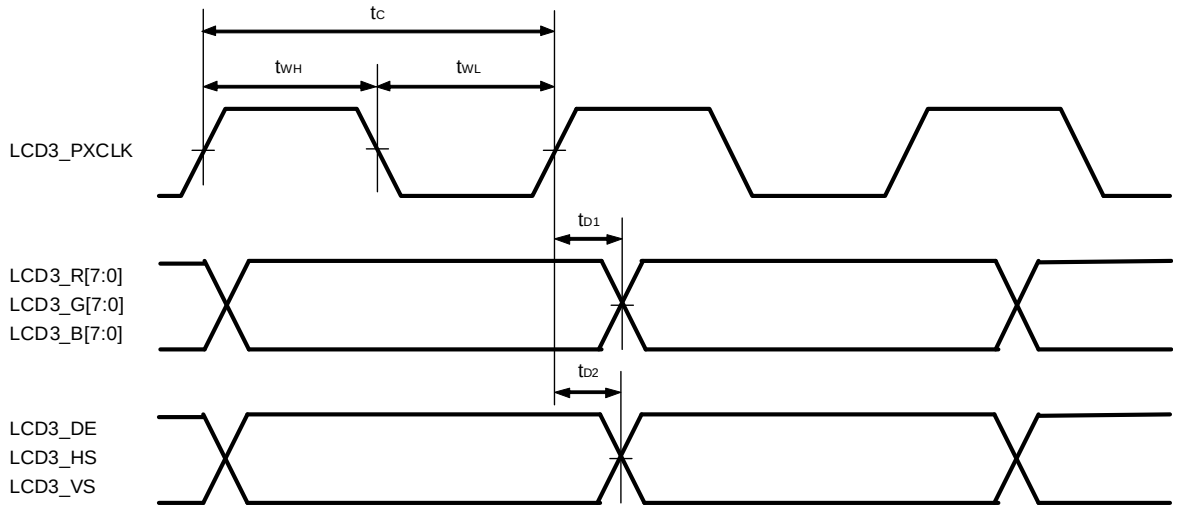
(1) LCD interface

(VDD33＝3.3±0.3 V, input pin : Normal , Drive=8mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD3_PXCLK output cycle	t_C	—	10	—	—	ns
LCD3_PXCLK high-level width	t_{WH}	—	4	—	—	ns
LCD3_PXCLK low-level width	t_{WL}	—	4	—	—	ns
LCD3_R/G/B[7:0], LCD3_HS, LCD3_VS and LCD3_DE data delay time	t_{D1}	LCD3_R/G/B[7:0]	1	—	6	ns
	t_{D2}	LCD3_HS, LCD3_VS, LCD3_DE	1	—	6	ns

Remark The setting of the rise and fall timing for LCD3_PXCLK is based on the valid edge set by the CLKPOL value in the LCD control register (rising: CLKPOL = 0, falling: CLKPOL = 1).

Figure 2-18. LCD Interface Timing



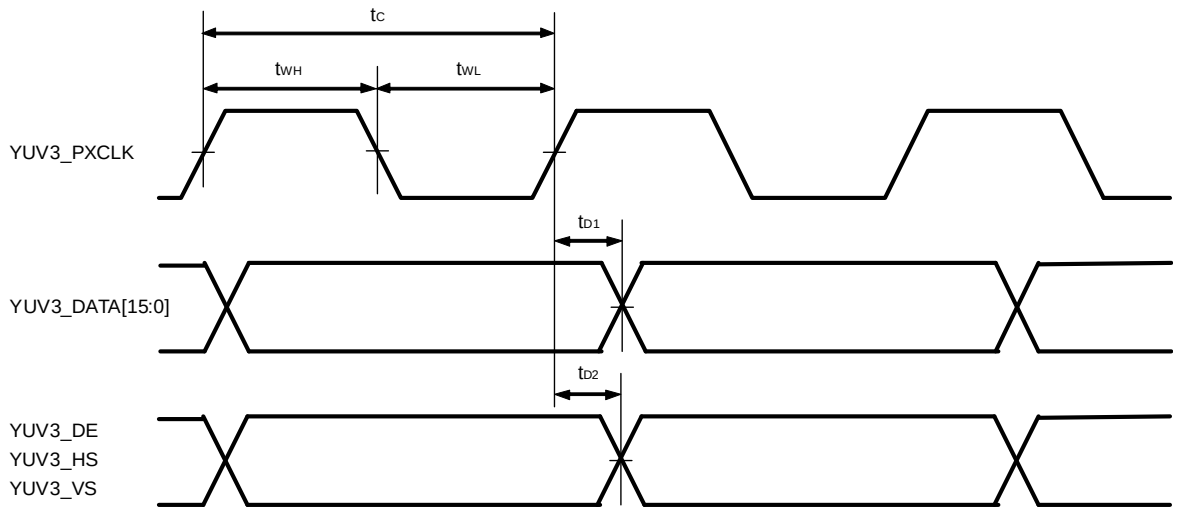
(2) YUV interface

(VDD33＝3.3±0.3 V, input pin : Normal , Drive=8mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
YUV3_PXCLK output cycle	t_C	—	10	—	—	ns
YUV3_PXCLK high-level width	t_{WH}	—	4	—	—	ns
YUV3_PXCLK low-level width	t_{WL}	—	4	—	—	ns
YUV3_DATA[15:0], YUV3_HS, YUV3_VS, YUV3_DE data delay time	t_{D1}	YUV3_DATA[15:0]	1	—	6	ns
	t_{D2}	YUV3_HS, YUV3_VS, YUV3_DE	1	—	6	ns

Remark The setting of the rise and fall timing for YUV3_PXCLK is based on the valid edge set by the CLKPOL value in the LCD control register (rising: CLKPOL = 0, falling: CLKPOL = 1).

Figure 2-19. YUV Interface Timing



2.5.9 USB interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USB_CLK cycle (24MHz)	$T_{cycUCLK24}$	—	—	24	—	MHz

Note ±500 ppm (± 100ppm recommendation)

Refer to USB Specification Revision2.0 about AC and DC characteristics in a USB port.

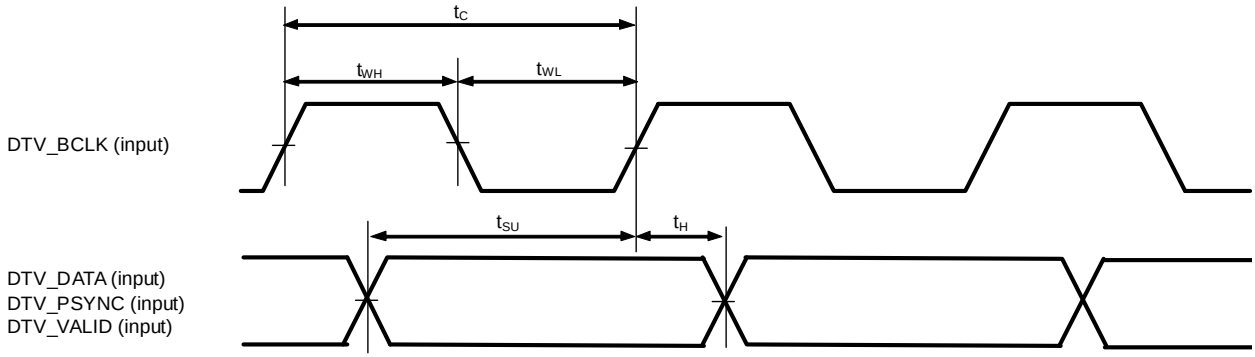
2.5.10 Digital terrestrial TV interface

(VDD33＝3.3±0.3 V, input pin : schmitt , Drive=4mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
DTV_BCLK input cycle	t_C	－	25	－	－	ns
DTV_BCLK high-level width	t_{WH}	－	10	－	－	ns
DTV_BCLK low-level width	t_{WL}	－	10	－	－	ns
DTV_DATA, DTV_PSYNC, DTV_VALID setup time	$t_{SU\ (AB)}$ Note	－	6	－	－	ns
DTV_DATA, DTV_PSYNC, DTV_VALID hold time	$t_{H\ (AB)}$ Note	－	6	－	－	ns
DTV_DATA, DTV_PSYNC, DTV_VALID setup time	$t_{SU\ (USI2)}$ Note	－	8	－	－	ns
DTV_DATA, DTV_PSYNC, DTV_VALID hold time	$t_{H\ (USI2)}$ Note	－	8	－	－	ns

Note (AB) : AB_AD9, AB_AD10, AB_AD11, and AB_AD12 terminal used.
(USI2) : USI2_DI, USI2_DO, and USI2_CS terminal used.

Figure 2-20. DTV Interface Timing



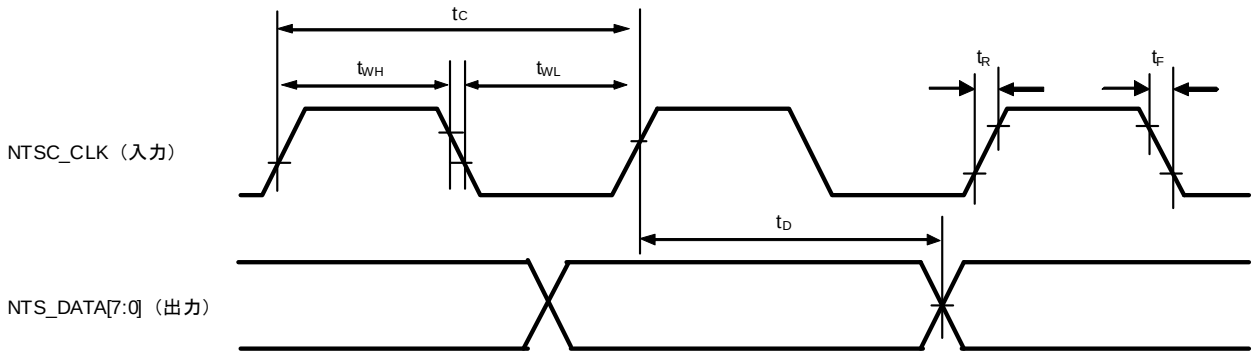
2.5.11 ITU-R BT.656 interface

（VDD33＝3.3±0.3 V, input pin : Normal (only clock is Schmitt) , Drive=8mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
NTSC_CLK input cycle	t_C	—	—	37[Note]	—	ns
NTSC_CLK high-level width	t_{WH}	—	13	—	—	ns
NTSC_CLK low-level width	t_{WL}	—	13	—	—	ns
NTSC_CLK rise time	t_R	—	—	—	5	ns
NTSC_CLK fall time	t_F	—	—	—	5	ns
NTSC_DATA output delay time	t_D	Rising edge of NTSC_CLK	4	_	18	ns

Note NTSC_CLK = 27 MHz

Figure 2-21. NTSC Interface Timing

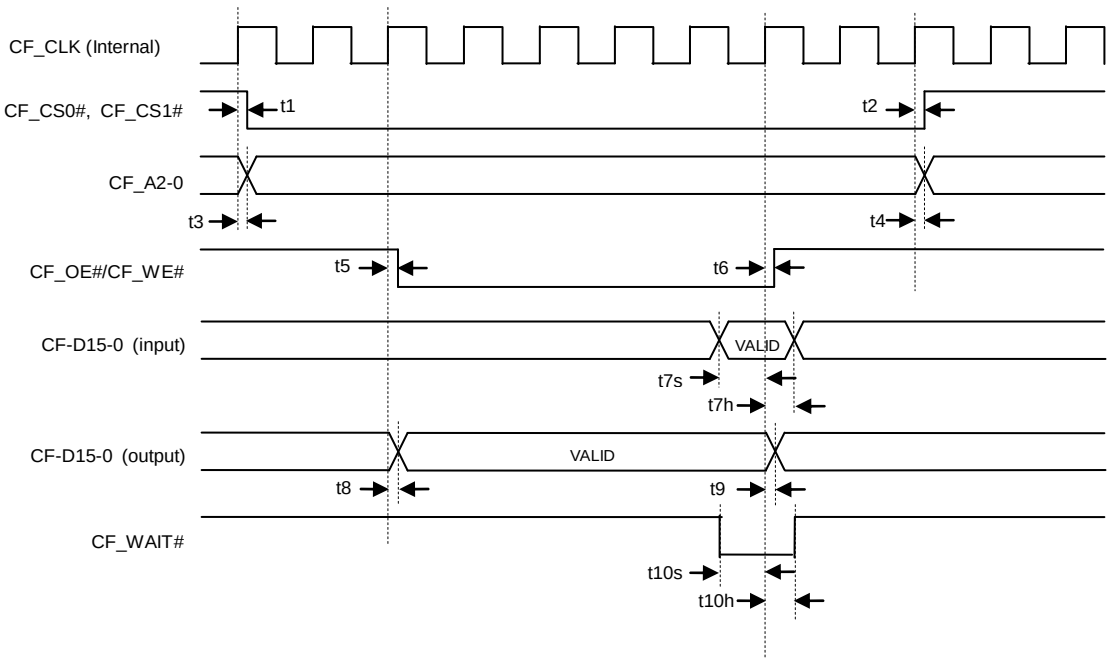


2.5.12 CF card interface (PIO mode)

（VDD33＝3.3±0.3 V, input pin : schmitt , Drive=4mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CF_CLK frequency	–	–	–	–	100	MHz
CF CLK cycle	–	–	10	–	–	ns
Until CF_CS0#, CF_CS1# becomes active	t1	–	–	–	11	ns
Until CF_CS0#, CF_CS1# becomes inactive.	t2	–	–	–	11	ns
The delay until CF_A2-0 becomes effective	t3	–	–	–	12	ns
The delay until CF_A2-0 becomes invalid	t4	–	–	–	12	ns
Until CF_OE#, CF_WE# becomes active	t5	–	–	–	12	ns
Until CF_OE#, CF_WE# becomes inactive.	t6	–	–	–	12	ns
Data setup time	t7s	–	8	–	–	ns
Data hold time	t7h	–	0	–	–	ns
The delay until data becomes effective	t8	–	–	–	11	ns
The delay until data becomes invalid	t9	–	–	–	11	ns
CF_WAIT# setup time	t10s	–	9	–	–	ns
CF_WAIT# hold time	t10h	–	0	–	–	ns

Figure 2-22. CF card Interface Timing (PIO mode)

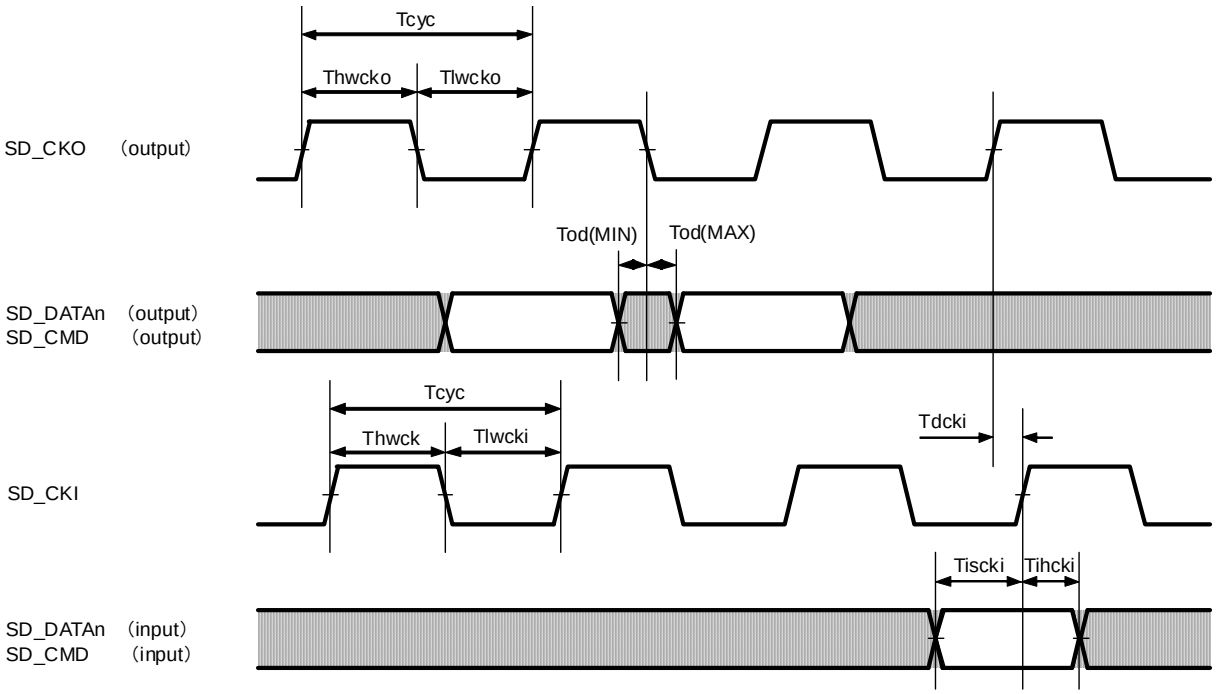


2.5.13 SD card interface

（VDD33＝3.3±0.3 V, input pin : schmitt, Drive=8mA, outside loop, CMD and Data is pull-up ）

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock cycle	Tcyc	—	20	—	—	ns
Output clock high-level width	Thwcko	@50MHz	8.5	10	11.5	ns
Output clock low-level width	Tlwcko	@50MHz	8.5	10	11.5	ns
Output delay	Tod	—	-3	—	2	ns
Input clock high-level width	Thwcki	@50MHz	8	—	11	ns
Input clock low-level width	Tlwcki	@50MHz	8	—	11	ns
Input clock delay time	Tdcki	—	0	—	6	ns
Setup time	Tiscki	—	2	—	—	ns
Hold time	Tihcki	—	1	—	—	ns

Figure 2-23. SD card Interface Timing



Remark n = 0 to 3

2.5.14 SDRAM Interface

(1) DDR2-533

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
DDR_CK, DDR_CKB cycle time	t_{CK}	—	3.75	—	8	ns
DDR_CK, DDR_CKB high level width	t_{CKH}	—	0.45	—	0.55	t_{CK}
DDR_CK, DDR_CKB low level width	t_{CKL}	—	0.45	—	0.55	t_{CK}
Address/Command terminal delay time	t_{CKSQ}	Note1	-1	—	1	ns
DDR_DQx, DDR_DMy output valid time Note2	t_{DQSDQ}	From DDR_DQSy	—	—	$0.25t_{ck}$-0.5	ns
DDR_DQx, DDR_DMy output skew time Note2	t_{DQSQO}	—	—	—	0.35	ns
DDR_DQSy output delay time	t_{DQSS}	—	-0.20	—	0.20	t_{CK}
DDR_DQx hold time Note2	t_{QH}	—	1.27	—	—	ns
DDR_DQx input skew time	t_{DQSQI}	From DDR_DQSy	—	—	0.32	ns
DDR_DQSy input access time	t_{DQSCK}	From CK	—	—	1	ns

Remark x = 0 to 31, y = 0 to 3

Register setting can adjust the delay time to DDR_CK/DDR_CKB, DQ/DM output, DQS output and DQS input.

Note 1 : DDR_A[14:0], DDR_BA[2:0], DDR_CSB[1:0], DDR_CKE[1:0], DDR_RASB, DDR_CASB, DDR_WEB

2 : The specification during a signal in the following each group.

1) DDR_DM[0], DDR_DQ[7:0]
2) DDR_DM[1], DDR_DQ[15:8]
3) DDR_DM[2], DDR_DQ[23:16]
4) DDR_DM[3], DDR_DQ[31:24]

Figure 2-24. DDR2 Output Timing

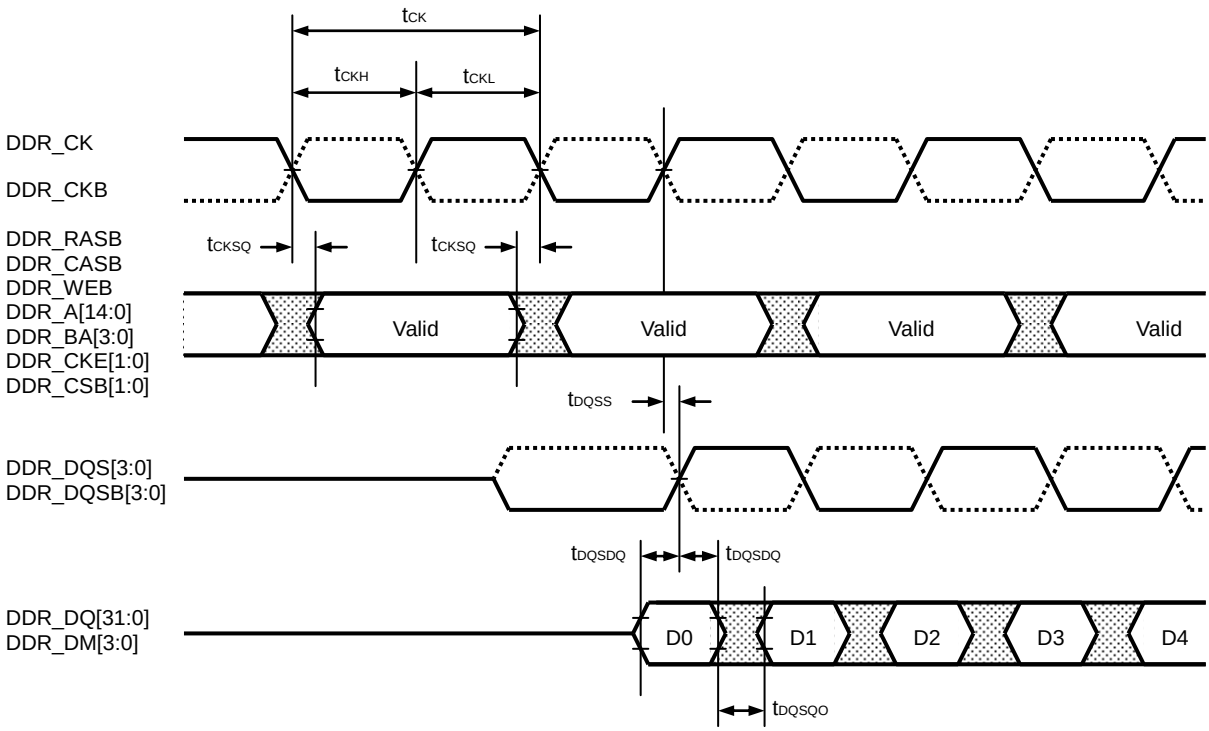
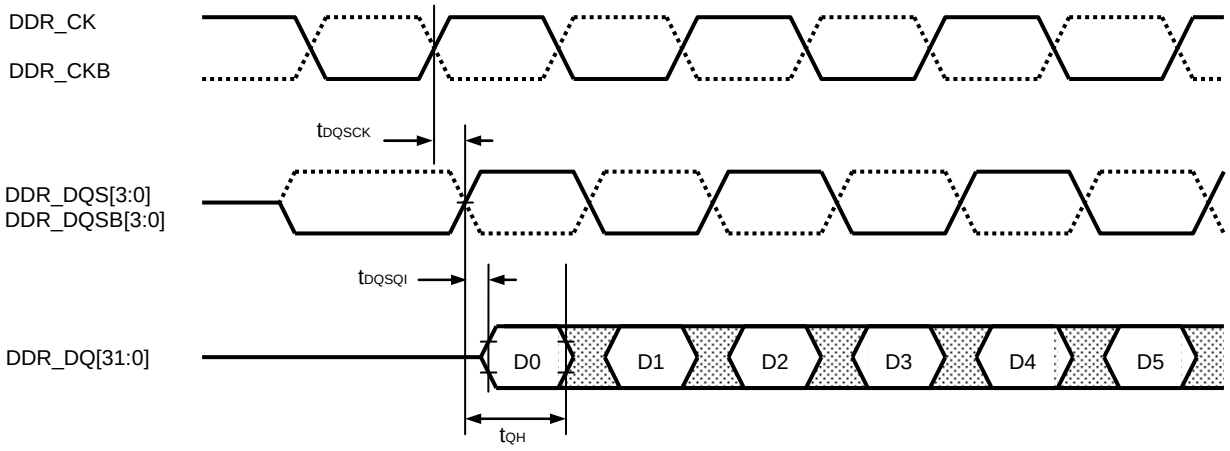


Figure 2-25. DDR2 Input Timing



(2) LPDDR-400

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
DDR_CK, DDR_CKB cycle time	t_{CK}	—	5	—	100	ns
DDR_CK, DDR_CKB high level width	t_{CKH}	—	0.45	—	0.55	t_{CK}
DDR_CK, DDR_CKB low level width	t_{CKL}	—	0.45	—	0.55	t_{CK}
Address/command terminal delay time Note1	t_{CKSQ}	From DDR_CK	-0.8	—	0.8	ns
DDR_DQx, DDR_DMy output valid time Note2	t_{DQSDQ}	From DDR_DQSy	$0.25t_{ck}$-0.6	—	—	ns
DDR_DQx, DDR_DMy output skew time Note2	t_{DQSQO}	—	—	—	0.8	ns
DDR_DQSy output delay time	t_{DQSS}	—	0.8	—	1.2	t_{CK}
DDR_DQSy input delay time	t_{DQSCK}	From DDR_CK	2.0	—	5.2	ns
DDR_DQx input skew time	t_{DQSQI}	From DDR_DQSy	—	—	0.5	ns
DDR_DQx hold time Note2	t_{QH}	From DDR_DQSy	1.7	—	—	ns

Remark x = 0 to 31, y = 0 to 3

Register setting can adjust the delay time to DDR_CK/DDR_CKB, DQ/DM output, DQS output and DQS input. The specification after a delayed adjustment is prescribed.

Note 1 : DDR_A[14:0], DDR_BA[2:0], DDR_CSB[1:0], DDR_CKE[1:0], DDR_RASB, DDR_CASB, DDR_WEB

2 : The specification during a signal in the following each group.

1) DDR_DM[0], DDR_DQ[7:0]
2) DDR_DM[1], DDR_DQ[15:8]
3) DDR_DM[2], DDR_DQ[23:16]
4) DDR_DM[3], DDR_DQ[31:24]

Figure 2-26. LP-DDR Output Timing

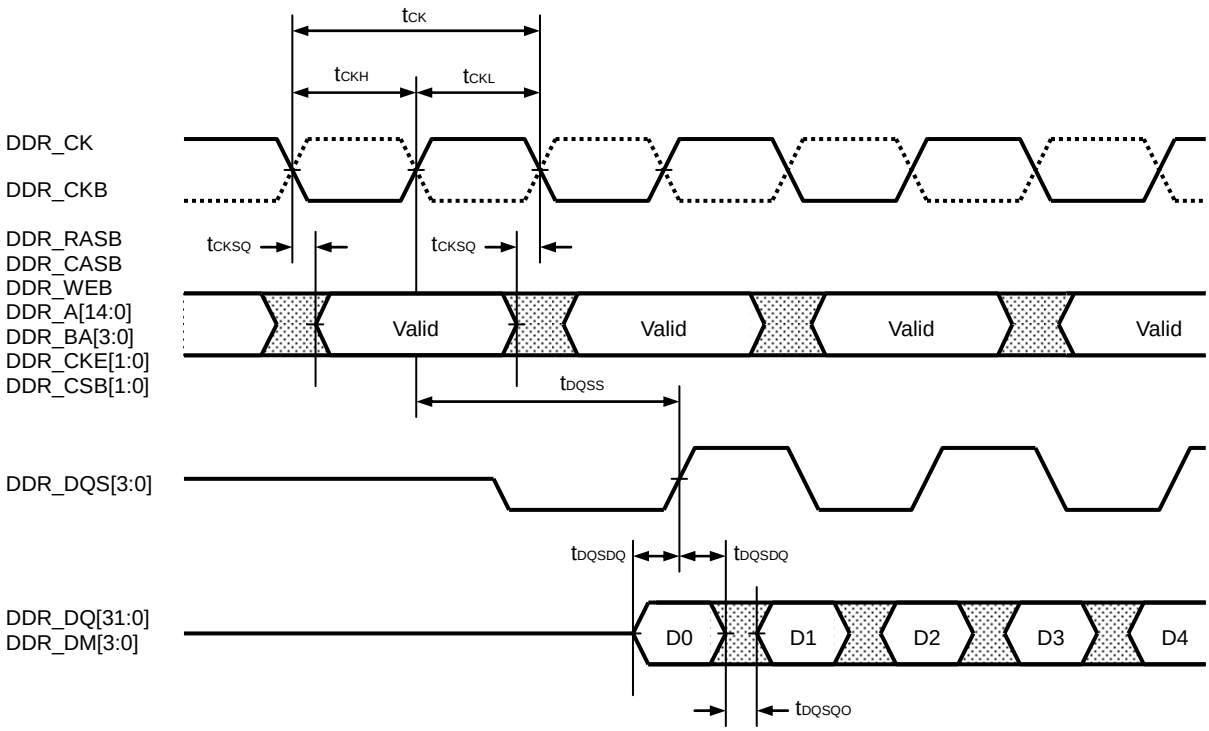
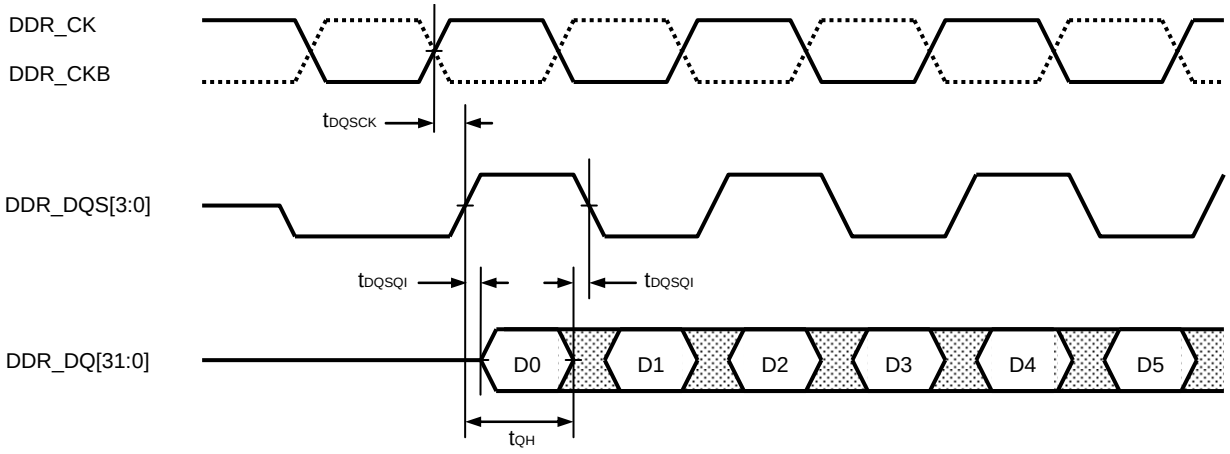


Figure 2-27. LP-DDR Input Timing

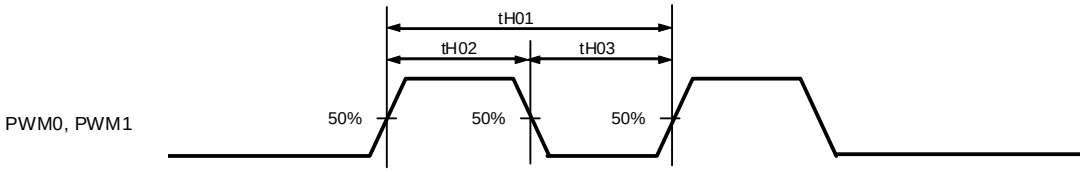


2.5.15 PWM Interface

（VDD33＝3.3±0.3 V,input pin : normal, Drive=4mA)

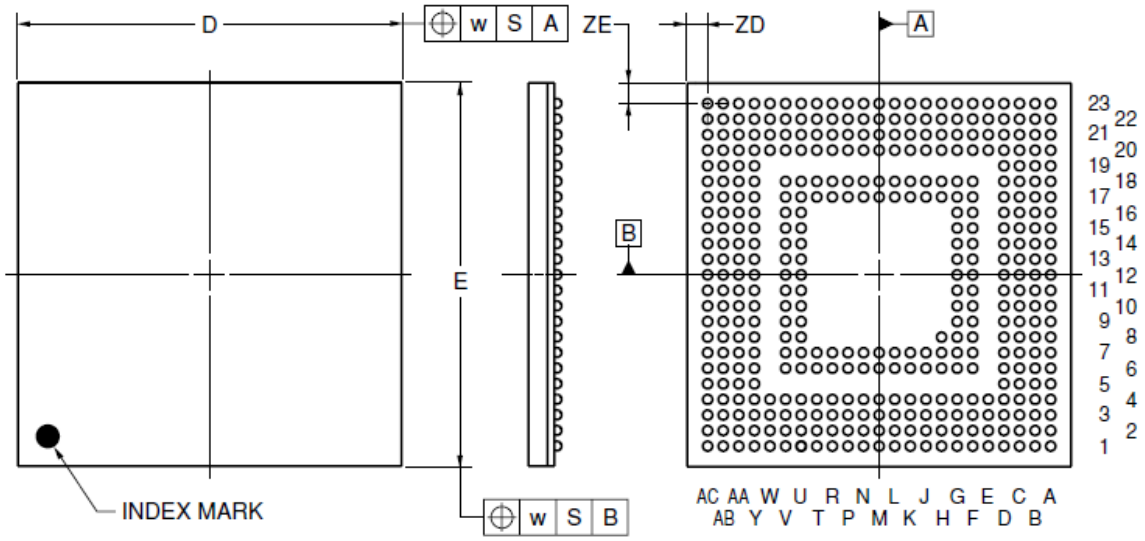
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output cycle	tH01	－	50	－	1000	ns
High level width	tH02	－	25	－	500	ns
Low level width	tH03	－	25	－	500	ns

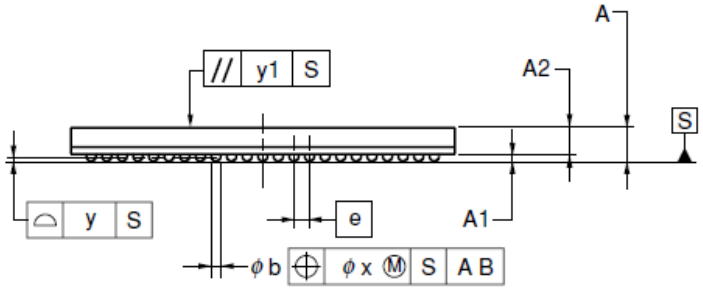
Figure 2-28. PWM Interface Timing (Transmission)



3. PACKAGE DRAWING

393-PIN PLASTIC FBGA (16x16)





(UNIT:mm)

ITEM	DIMENSIONS
D	16.00±0.10
E	16.00±0.10
w	0.20
A	1.41±0.10
A1	0.30±0.05
A2	1.11
e	0.65
b	0.40±0.05
x	0.08
y	0.10
y1	0.20
ZD	0.85
ZE	0.85

P393F1-65-GA9

REVISION HISTORY	EMMA Mobile EV2 Data Sheet

Rev.	Date	Description	
		Page	Summary
1.0	February 8, 2010	—	—
2.0	February 18, 2010	—	2.5.6 SDIO interface specification modified. 2.5.14 SD card interface specification modified. 2.5.15 DDR2 SDRAM interface specification is added.
Provisional 3rd	February 26, 2010	—	1.2 Pin functions Buffer type added. 1.3 Pin I/O circuits added.
Provisional 4th	March 19, 2010	—	2.1 Absolute Maximum Ratings added. 2.2 Recommended Operating Conditions added. 2.3 Capacitance added. 2.4 DC Characteristics added. 2.5.1 AC test I/O measurement points added. 2.5.2 System control added. Incremental update from comments to the provisional 3rd.
Provisional 5th	July 23, 2010	—	2.5.13 Memory stick interface deleted. EM/EV1 is added. (The difference with EM/EV2 is mentioned.) Incremental update from comments to the provisional 4th. (A change part from the old revision is "★" marked in the page left end.)
Provisional 6th	August 4, 2010	—	Order Information added. 2.5.14(2) LP-DDR SDRAM Interface specification added. Incremental update from comments to the provisional 5th. (A change part from the old revision is "★" marked in the page left end.)
Provisional 7th	August 6, 2010	—	2.5.15 PWM Interface Specification added. Incremental update from comments to the provisional 6th. (A change part from provisional 4th is "★" marked in the page left end.)
3.0	August 23, 2010	—	Regular version issue
4.0	September 30, 2010	—	ARM logo added. (Face page) Incremental update from comments to the provisional 3.0. (A change part from 3.0 is "★" marked in the page left end.)
5.0	February 10, 2011	—	Order Information changed. AC Characteristics changed. (IIC, SDIO, SDC, SDRAM) Incremental update from comments to the provisional 4.0. (A change part from 4.0 is "★" marked in the page left end.)
6.0	April 15, 2011	—	AC Characteristics changed. (Asynchronous bus, SDRAM Interface) Incremental update from comments to the provisional 5.0. (A change part from 5.0 is "★" marked in the page left end.)

Rev.	Date	Description	
		Page	Summary
7.0	May 31, 2010	—	Incremental update from comments to the provisional 6.0.
8.0	September 30, 2011	—	Incremental update from comments to the provisional 7.0.
		11-29	Chapter 1.2 corrected. (Buffer type and Handling when not used added.)
		31-38	Chapter 1.3 corrected.
		39-46	Chapter 1.4 added.
		76	Chapter 2.5.10 corrected.
9.0	December 21, 2011	—	Incremental update from comments to the provisional 8.0.
		31, 35	Chapter 1.3 corrected. (Buffer type “I” added.)
10.00	April 19, 2012	—	Incremental update from comments to the provisional 9.0.
11.00	May 25, 2012	—	Incremental update from comments to the provisional 10.0.
12.00	Jun 22, 2012	57	Chapter 2.5.2 Notes1 x=1 or 2 → x=0 or 1

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

Notice

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