Analog IP

ADPLL For Spread Spectrum Clock

Overview

This core is ADPLL(All Digital PLL) with SSCG(Spread Spectrum Clock Generator). This core is not able to adjust the output clock delay using the external delay.

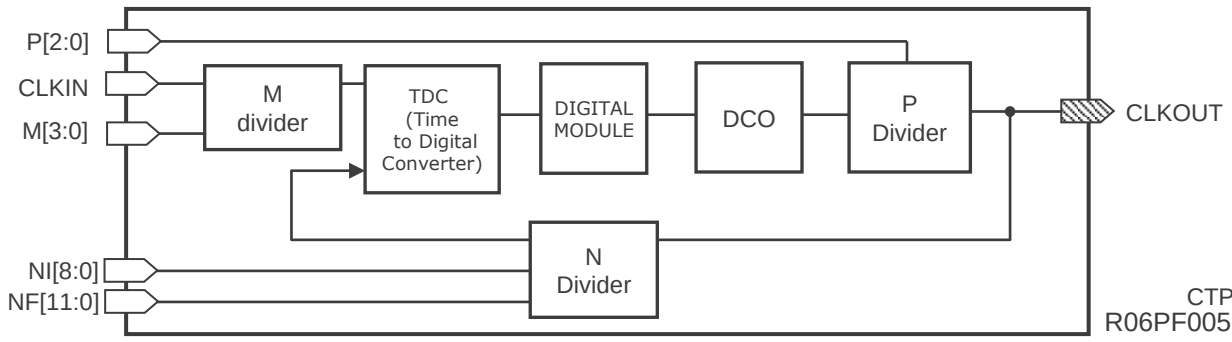
Technology

Process: TSMC T22ULP
Available metallization technologies: 5X2Y2R

Features

- Supply voltage : min=0.81V, typ=0.9V, max=1.05V
- Operating temperature (Tj) : -40 - +125°C
- DCO frequency range : 900MHz - 3000MHz
- Output frequency range : 56.25MHz - 3000MHz
- Input frequency range : 8MHz - 192MHz
- Multiplying
  Output frequency / Input frequency : 0.293 - 375
- Fractional multiplying available
- SSC Modulation frequency : 3kHz - 30kHz(target) (Dithered frequency mode)
- SSC modulation depth :
  - 0.25% - 3.0% down spread (Dithered frequency mode)
  - +/-0.125% - +/-1.5% center spread (Dithered frequency mode)
- Divider
  - 21bit feedback divider (N divider)
  - 4bit input divider (M divider)
  - 3bit output divider (P divider)
- No external device is needed.

Block diagram



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