Using the Reference Layout

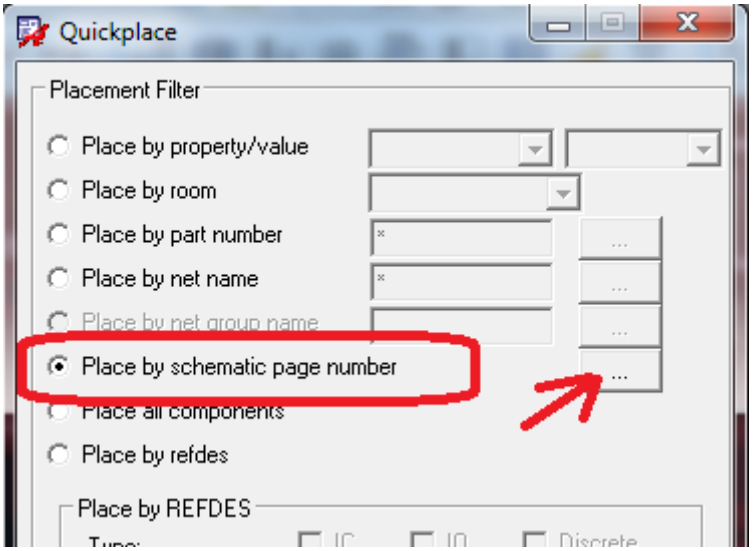
The P9027LP-R-EVK reference layout is a full feature four-layer design optimized for high-performance, small-size, and ease-of-use. The purpose is to minimize design-in effort and risk by providing a proven solution that can be imported into an existing system design. The P9027LP-R-EV board layout can be divided into two parts; the main function layout (core layout) and the layout for test purpose. When imported into an existing system, only the core layout is necessary. The core layout follows the design rules for wearable devices with minimum space and trace width of 4 mils. The minimum finished VIA size is 4 mils, assuming 1 mil plating thickness. The minimum spacing between components is 0.2 mm. Only through hole VIAs are used. There are no blind or buried VIAs. When circumstances permit, it is highly recommended to copy the reference layout.

Importing the Reference Layout

The P9027LP-R-EVK reference design was created using Cadence PCB design software. This software has been used to generate the layout modules, which can be rapidly deployed onto PCB designs, using Cadence, OrCAD, CIS and Cadence Allegro PCB Editor. The P9027LP-R layout module is labeled P9027LP-R-EVK.mdd and may be loaded into an existing or new PCB design file by following these instructions:

1. Use or copy the P9027LP-R-EVK schematic file (.dsn) and export the netlist to a PCB file.
2. Move the file P9027LP-R-EVK.mdd to the same directory as the PCB design file.
3. Import the netlist into the PCB file (.brd).
4. Open the PCB design file (.brd) and click on the menu Place→Quickplace…
    a. Select Place by Page Number and select the page the P9027LP-R circuitry resides on
    b. Click Place. Click Ok..

Figure 1. Cadence Quickplace option box used for placing the IDT Layout module by Page Number.



5. Select the parts that were placed from the schematic that matches the schematic used from the P9027LP-R-EVK.
    a. In the Find Filter, select Symbols, then left click and drag to highlight all of the components that were just placed.
    b. Right click on any of the highlighted parts and select “Place Replicate Apply→Browse…”.
    c. Select the P9027LP-R-EVK.mdd file and select Ok.
    d. Components should now be matched; if unmatched, manually identify and match component reference designators based on schematic location.
6. Enter the coordinates(x,y location) in the command window where the P9027LP-R circuit should be located at, or left click where the P9027LP-R should be placed.

Connecting a Load

The reference board layout has been designed such that the DC output is easily accessible when being imported on to a system board. Traces should be connected directly to the OUT and GND VIAs on the top or bottom layer, and routed to the load. Wide, low-impedance traces are recommended to minimize the DC voltage drop on its way to and from the load. To reduce ripple voltages, or improve transient performance, increase the capacitance on Vrect and OUT nodes.

Connecting Inputs / Outputs

All input and outputs on the reference board have been placed near the edges of the reference layout such that they can be easily connected to other parts of the system board. After placing the module in the specific design, use the labeled VIAs as connection points for new traces on either the top or bottom layer.

Manufacturing Notes

The PCB should be made with a minimum of 1oz copper foil weight per square foot or heavier.

Additional Resources

All support files and collateral for the P9027LP-R-EVK reference board can be found at www.IDT.com/WP3W-RK. Files include: schematics, layout files, datasheets, user manual, etc.

Custom Layout Guidelines

The P9027L-R wireless power receiver is an integrated device consisting of multiple high-power blocks along with noise sensitive circuits all controlled by a state-machine with some programmability. When designing the printed circuit board (PCB), there are multiple considerations, and often some tradeoffs, associated with managing the critical current paths. In order to optimize the design, components should be placed based on circuit function, to guarantee the best performance when the schematic is implemented in a PCB design. Furthermore the thermal management of the application is important to the product's performance and should be optimized during PCB design. By following the guidelines set forth in this document, efficient operation will be obtained for each circuit function.

At the time that the layout is started the following guidance should be used to place the most critical parts in order of priority. There are three main categories of circuitry: Power Circuits, Sensitive Circuits, and Non-Sensitive Circuits.

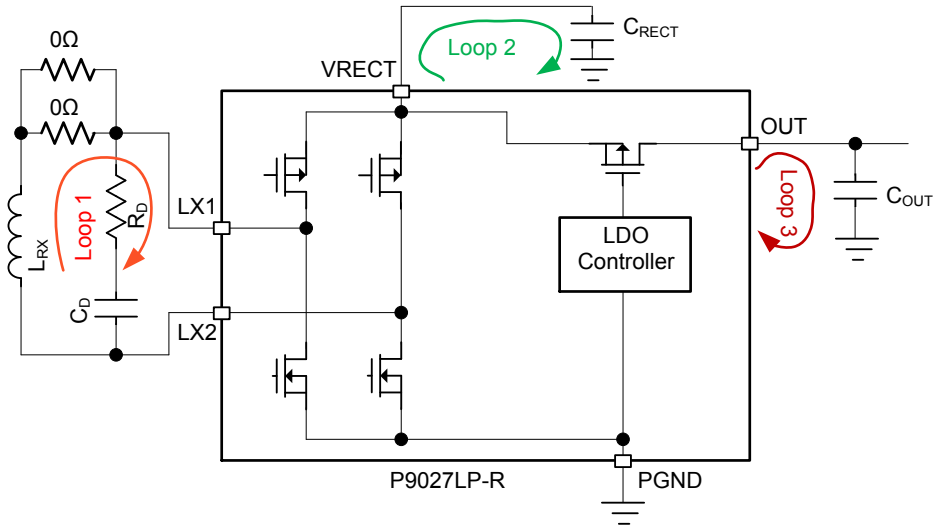
Layout Priority Checklist:

1. Route the power connections sufficiently wide depending on the load current. 15 mils is recommended for a 400 mA load current with less than 20°C temperature rise. These connections are Vrect, LX1, LX2, OUT, LC node, and PGND.
2. Use the next closest layer to the P9027LP-R device as a solid GND plane.
3. Avoid unnecessary layer transitions of the power connections (Vrect, LX1, LX2, OUT, LC node, and PGND). Use at least 4 mil-finished size VIAs for any layer transitions of these connections for a 400 mA load current.
4. Attempt to place the P9027LP-R as close as possible to the center of the allocated layout area.
5. Connect at least five 8mil finished VIAs under the PGND Bumps and nearby area. Use multiple PGND planes to connect to these VIAs. Have a solid, continuous PGND plane under these PGND Bumps on the bottom layer. This helps tremendously to spread the heat to rest of the PCB to reduce any hot spots in the P9027LP-R IC.
6. Follow the placement and routing suggestions outlined in the remainder of this document.
7. Use low ESR resonance capacitors (Cs) to decrease losses in the LC and LX1 current path. IDT recommends using components with less than 300 mΩ of ESR at 100k Hz operating frequency.

Power Circuits

Error! Reference source not found. shows the simplified circuit with key external components of the power circuits inside the P9027LP-R IC. As mentioned in the above layout priority checklist, these three loops, formed by the key external components, need to be taken care first to achieve the best performance.

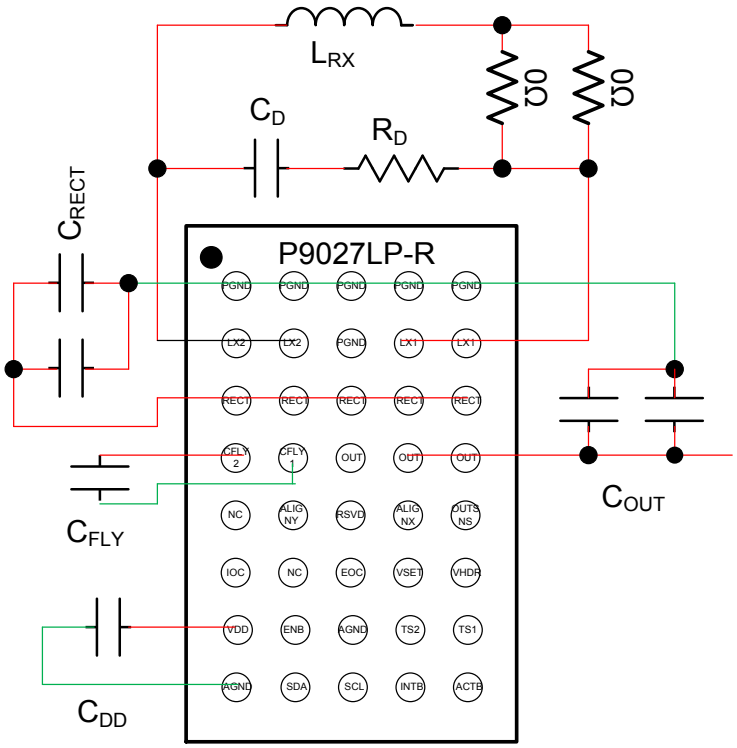
Figure 2. Three main loops of P9027LP-R.



As soon as the final shape of the PCB has been determined (based on system constraints), the connection points for the receiver coil (L_{RX}) should be determined. Next, the P9027LP-R should be placed as close to the center of the allocated PCB area as possible. The orientation of the device should be determined based on the ability to route connections and place the necessary components in the following order of priority: Rectifier capacitors (C_{RECT}: C1,C2), the resonance Capacitors (C_S:C5,C8, C_d: C9), VDD capacitor (C4), , OUT capacitors (C_{OUT}: C6,C7), and these capacitors should be placed with equal precedence (LX1, LX2).

The main power current path is considered the connection from the RX coil to LX2, the Cs capacitors to LX1, GND, V_{RECT}, and OUT connections. The optimal P9027LP-R orientation relative to the receiver coil (L_{RX}) and output connector physical locations are presented in **Error! Reference source not found.**:

Figure 3. P9027LP-R Recommended orientation based on Rx coil location and generic placement guide for some critical components (Note, not all necessary connections are shown in this figure, refer to the P9027LP-R datasheet Typical Application Drawing for a complete diagram of recommended connections). Trace widths not to scale. All GND pins should be connected to GND.



This layout guideline will address four critical layout areas for the best performance. Figure 4 shows the P9027LP-R schematics with full features and **Error! Reference source not found.** shows the recommend P9027LP-R layout image.

Figure 4. 9027LP-R full feature schematic.

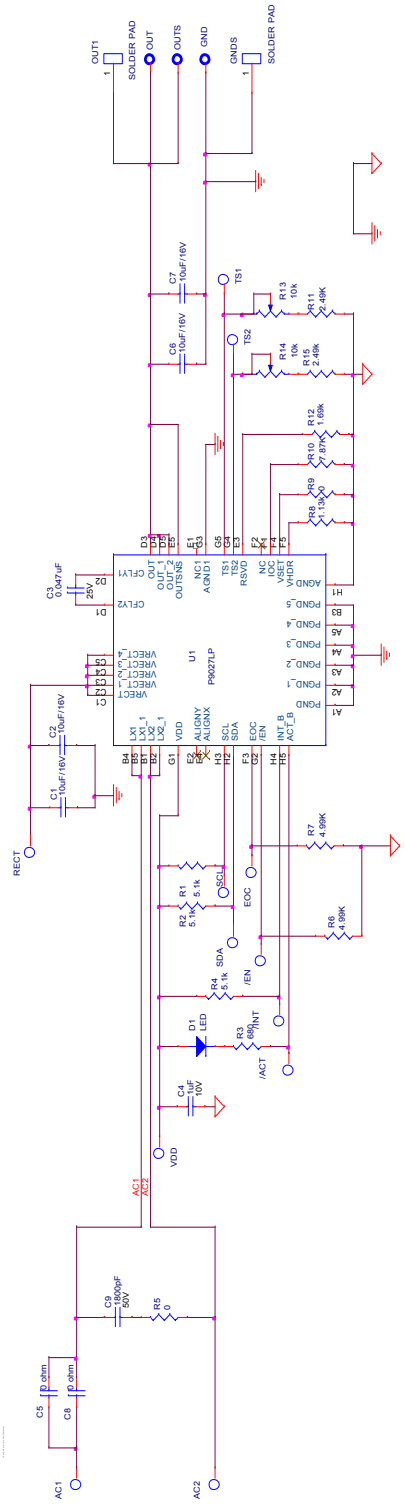
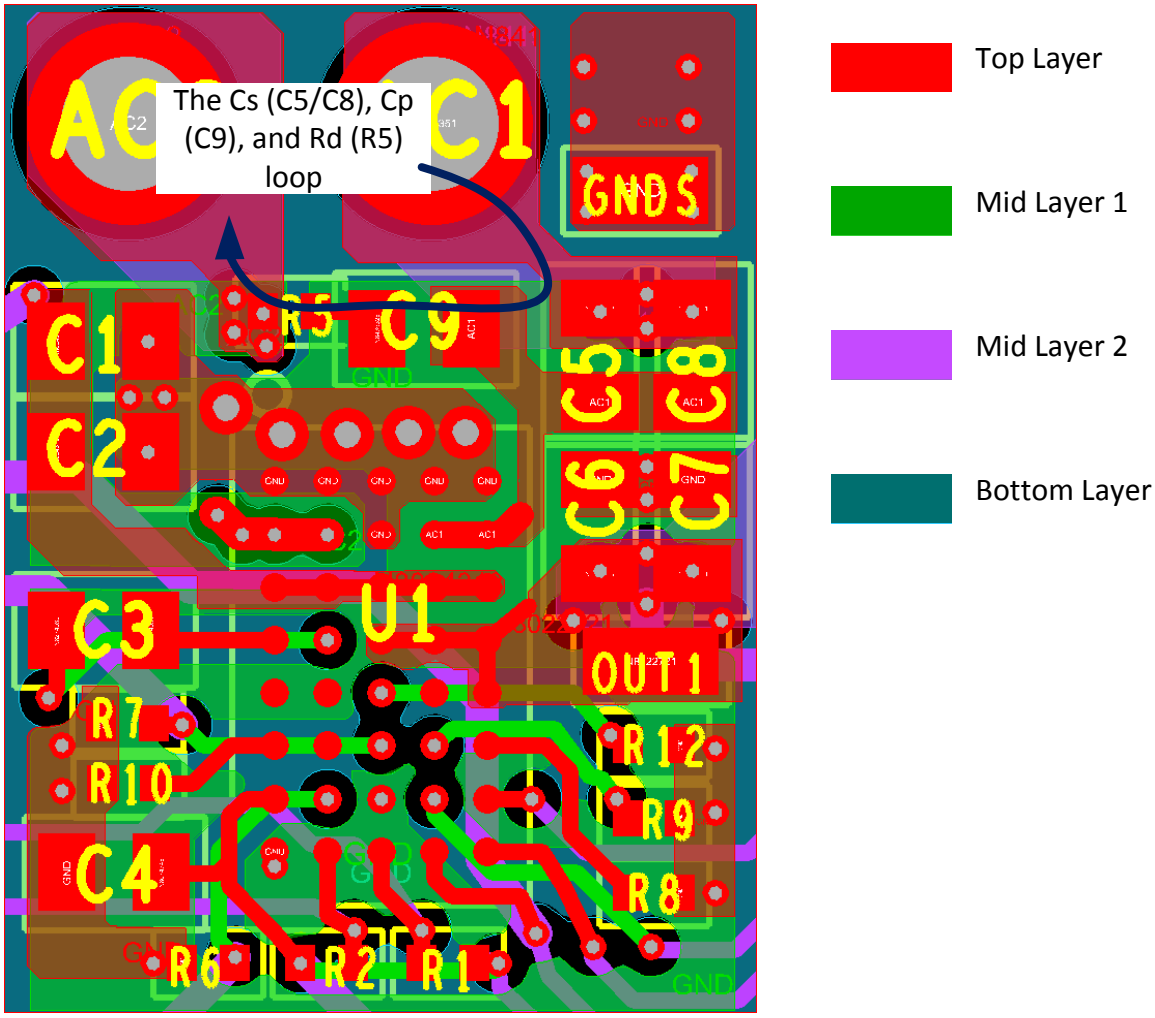


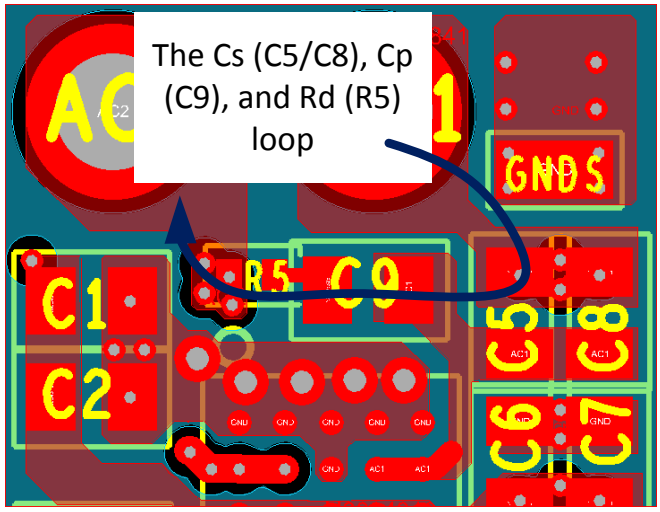
Figure 5. Recommended P9027LP-R Layout Image.



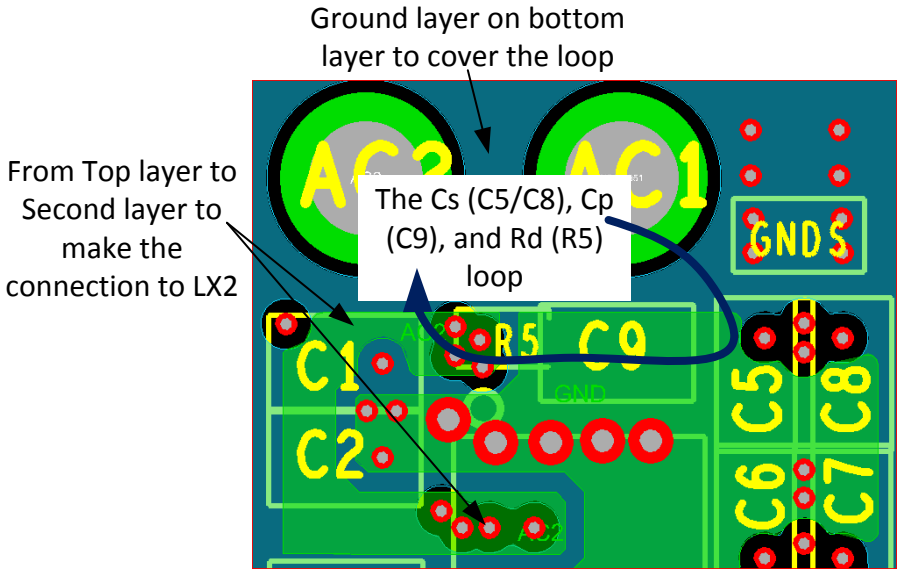
Receiver coil and LC Tank Circuit

The receiver LC tank circuit consists of the receiver coil L1and parallel resonant capacitor Cd (C9) and the damping resistor Rd (R5), as shown in Figure 4. The current running through the loop formed by these components contains high frequency harmonics. It is essential to minimize the loop area to reduce the EMI noise induced by the current. It is recommended to place the loop on the top layer with the traces close to each other to minimize the loop area. It is also recommend placing a ground layer under this loop to further shielding the unwanted EMI field. **Error! Reference source not found.** shows the recommend layout, which is captured from the P9027LP-R EV Kit layout.

Figure 6. Recommended layout for LC tank circuit.



(a) Top Layer Layout



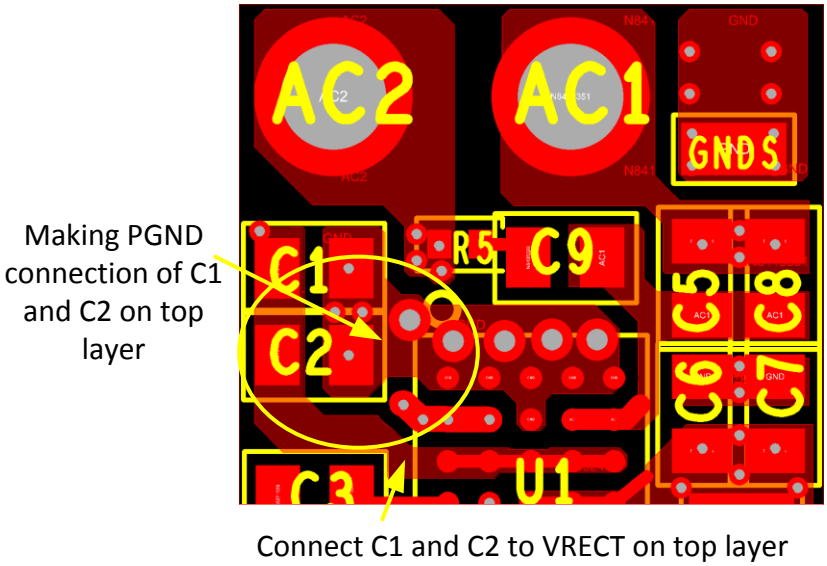
(b) Second Layer and Bottom Layer Layout

Connect LX1 and LX2 as shown in **Error! Reference source not found.**,.

VRECT Capacitors

The next important component is the rectifier capacitors: C1 and C2 shown in Figure 4. Any high frequency harmonic currents in the LC tank circuit are rectified and filtered by the VRECT capacitors. Therefore, high frequency EMI noise could be induced if the loop formed by the VRECT, PGND Bumps of the P9027LP-R and the VRECT capacitors is not minimized. It is recommended to place the rectifier capacitors as close to the P9027LP-R IC as possible. Use traces on the top layer to connect the rectifier capacitors to the RECT and PGND Bumps of the P9027LP-R. Minimize the area between the two traces on the top layer and have some GND layer on the 2nd layer to shield the loop area on top layer. This helps to minimize radiated EMI emissions as well as to reduce trace inductance. The recommended layout for rectifier capacitors is shown in **Error! Reference source not found.**.

Figure 7. Recommended layout for rectifier capacitors.

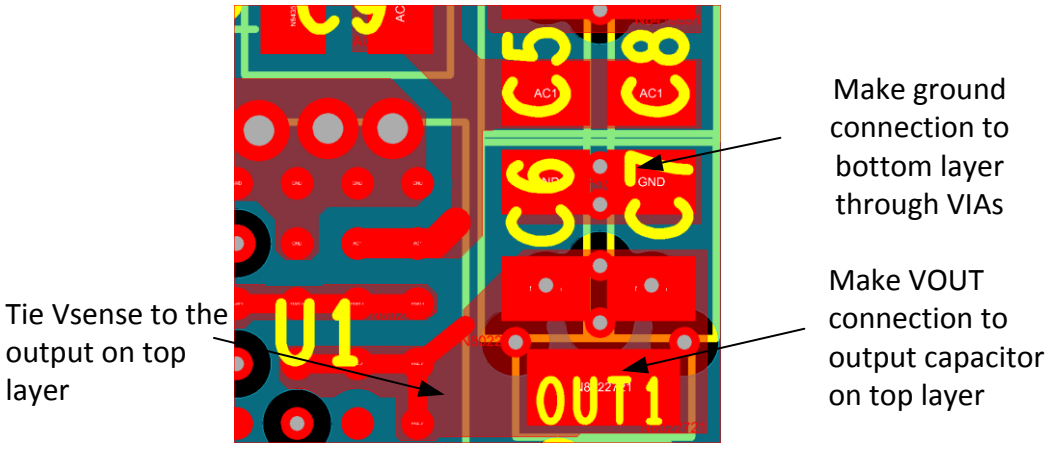


As shown in **Error! Reference source not found.**, connect all VRECT pins together on top layer with 8 mil wide traces. Change the width to a minimum 15 mil trace once outside the IC to connect the rectifier capacitors. Four 4 mil finished VIAs are needed to connect the PGND terminals of the rectifier capacitors to the PGND plane.

VOUT Capacitors

Output capacitors should be placed as close to the P9027LP IC as possible. Long traces between the P9027LP-R and the output capacitors could cause two issues: 1) the trace inductance induced by long traces between the P9027LP-R and the output capacitors could degrade the stability of the output LDO stage and 2) long traces are likely to form a large loop, which could an emission source for EMI. **Error! Reference source not found.** shows the recommended layout of the VOUT capacitors.

Figure 8. Recommended layout for VOUT capacitors.

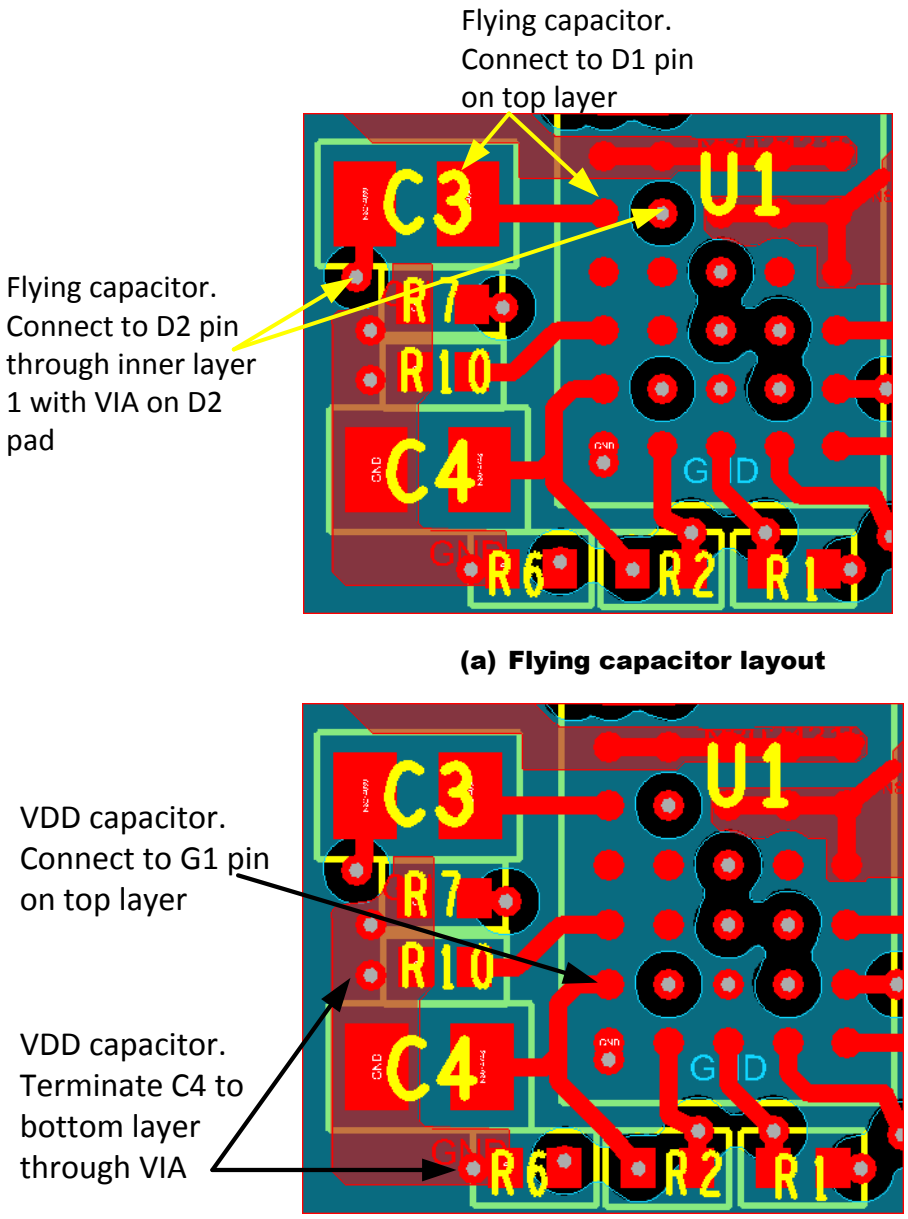


As shown in **Error! Reference source not found.**, connect all OUT and OUTSNS Bumps together on the top layer and maximize the trace width by applying the minimum allowable space between adjacent bumps. Once it is outside the IC, widen the trace to connect to the output capacitors. Please note in the reference layout the output trace is routed out through four 4mil finished VIAs to the OUT pin on the edge for test purpose. When porting to an existing system, the output trace can be routed out either on the top layer or inner layer. For reliability of the system, size the trace width accordingly (15 mil for 400 mA output current is recommended). This minimizes the voltage drop due to trace resistance, and minimizes the temperature rise.

VDD Capacitor, Flying Capacitor, Programming Resistors, and I²C

The VDD capacitor is used to stabilize a voltage supply used internally to the P9027LP-R, and must be located close to the P9027LP-R IC. The optimal placement is directly across the VDD and AGND bumps. Another critical capacitor is the flying capacitor. Use an 0402 ceramic capacitor and place it on the edge next to the FLY1 bump of the P9027LP-R IC. Use one 4 mil finished VIA to connect the flying capacitor to the FLY2 bump. For other programming resistors, place them along the edge of the P9027LP-R IC and use the top layer to connect these programming resistors to the outside pins. Use the inner layer (2nd layer) to connect these resistors to appropriate inner bumps. **Error! Reference source not found.** shows the layout for these components. Please note the programming resistors and the I²C pullup resistors are insensitive components and they can be placed away from the P9027LP-R IC if the layout runs into space issue.

Figure 9. P9027LP-R VDD capacitor, flying Capacitor, programming resistors, and I²C routing.



(a) Flying capacitor layout

(b) VDD capacitor layout

PGND and AGND Connection

It is very important to have thermal VIAs connected between the P9027LP-R IC PGND bumps and the system ground plane. Thermal VIAs must have a large enough diameter to effectively transfer heat from the IC to the PCB. It is recommended to use 8mil finished VIAs for this purpose. At least 5 thermal VIAs should be placed to achieve good thermal performance. Note that outer layers radiate heat into air much better than the inner layers. Therefore, a ground plane must be provided on the bottom layer right, directly under the location of the PGND bumps of the P9027LP-R IC. **Error! Reference source not found.** shows the recommended bottom layer layout and thermal VIAs for optimal thermal performance.

Figure 10. P9027LP-R QFN Bottom Layer layout.

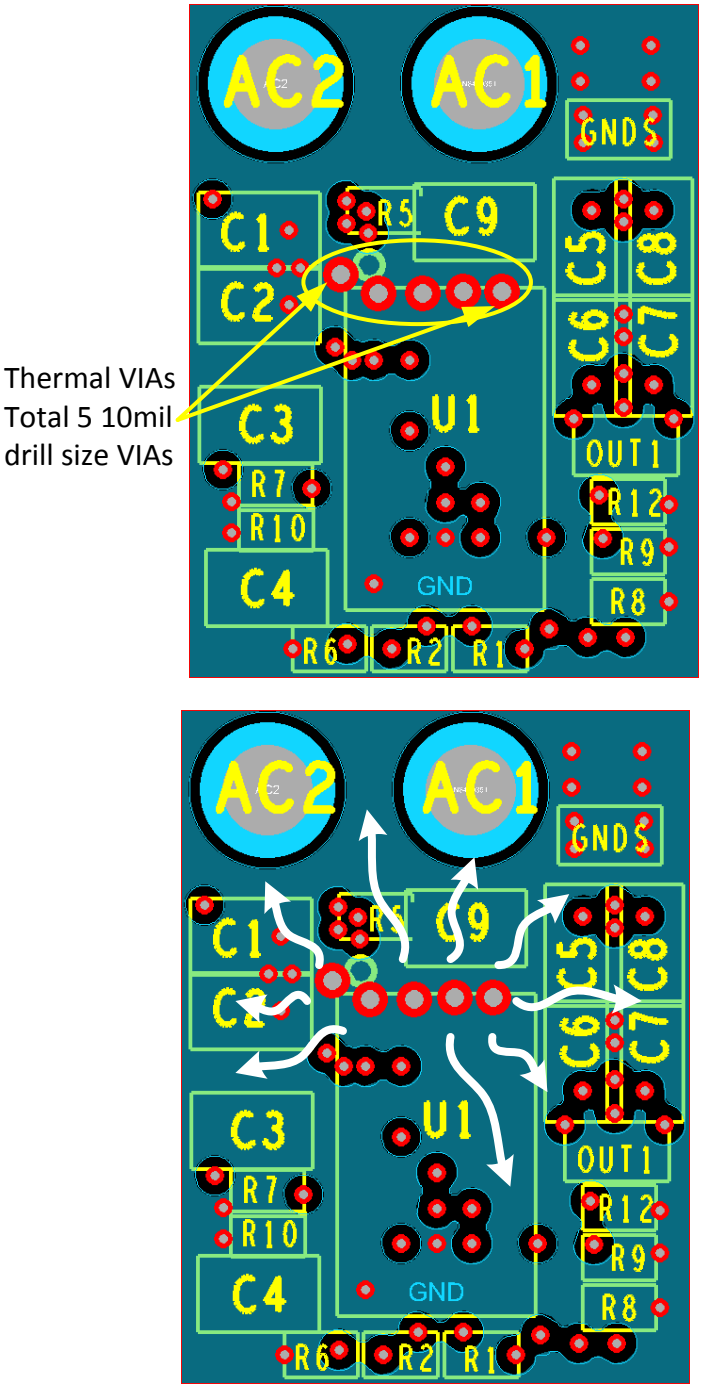
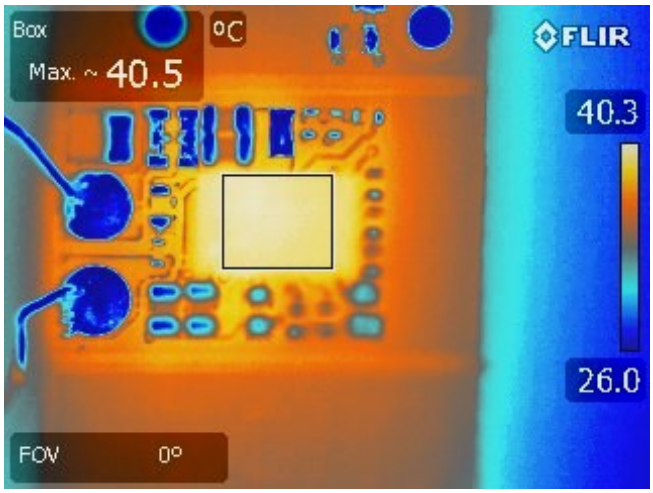


Figure 11 shows a thermal image of the P9027LP-R DEMO PCB. Notice that the top of the package is measured to be 50.3˚C (temperature rise of 25.3˚C) when delivering 2 W in an ambient temperature of 25˚C.

Figure 11. P9027LP-R Layer Heat flow paths.



Audible Noise Suppression

Wireless power receiver solutions have been observed to produce audible noise. If sound is detected there are several steps that can be taken to reduce or eliminate the noise. The first priority should be to identify the source. Typically the rectifier capacitors and/or the receiver coil are the components that generate the audible noise. Use the recommended coils to avoid audible noise from the receiving coil.

When small form factor capacitors (0402) are used for rectifier capacitors, it is more likely audible noise will be generated. The WPC communication signals are in the audible frequency range. The noise occurs due to the piezoelectric effect of these small form factor ceramic capacitors combined with the audible range frequencies of the WPC communication signals. The capacitors contract and expand while providing the communication pulses and this noise is amplified as it flexes the PCB.

The primary solution is to use low-acoustic noise capacitors. If that's not feasible, higher voltage rated components often have superior piezoelectric properties which can reduce the audible noise.

If swapping out the components is not possible, placing the capacitors on both sides of the PCB (directly above and below each other) can counter the piezoelectric forces applied to the PCB, thus eliminating the noise. Another method is to add slots through the PCB on both outer sides of the capacitors or directly under each capacitor. Lastly, some have reported success by placing additional lower-capacitance value components in parallel (such as eighteen 1µF capacitors instead of four 4.7µF capacitors) to reduce the mechanical force of the piezoelectric effect per component.

Revision History

Revision Date	Description of Change
May 16, 2016	Initial release.

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