Errata

SLG47004

CE-GP-005

Abstract

This document contains the known errata for SLG47004 and the recommended workarounds.

1 Information

Package(s)	24-pin STQFN: 3 mm x 3 mm x 0.55 mm, 0.4 mm pitch

2 Errata Summary

Table 1: Errata Summary

Issue #	Issue Title
1	Slew Rate & Inrush Current Behavior of the Analog VDD's ESD Structure

3 Errata Details

3.1 Slew Rate & Inrush Current Behavior of the Analog V_{DD}'s ESD Structure

3.1.1 Effect

Chip Current Consumption

Chip Reliability

3.1.2 Conditions

When powering ON the Analog V_{DD} with a slew rate exceeding 1 V/µs, a large inrush current exceeding 190 mA flows through the analog circuitry's ESD power clamp structure. With faster slew rates (2 V/µs), the inrush current through VDDA can reach 890 mA.

3.1.3 Technical Description

For larger slew rates and higher temperatures, this behavior can permanently damage the SLG47004 by creating a low impedance path between the power supply rails. This damage is caused by bipolar snapback within the ESD protection device. For this reason, Renesas has introduced an Abs. Max. parameter in the SLG47004's base die datasheet specifying a maximum slew rate of 2 V/µs on V_{DDA}.

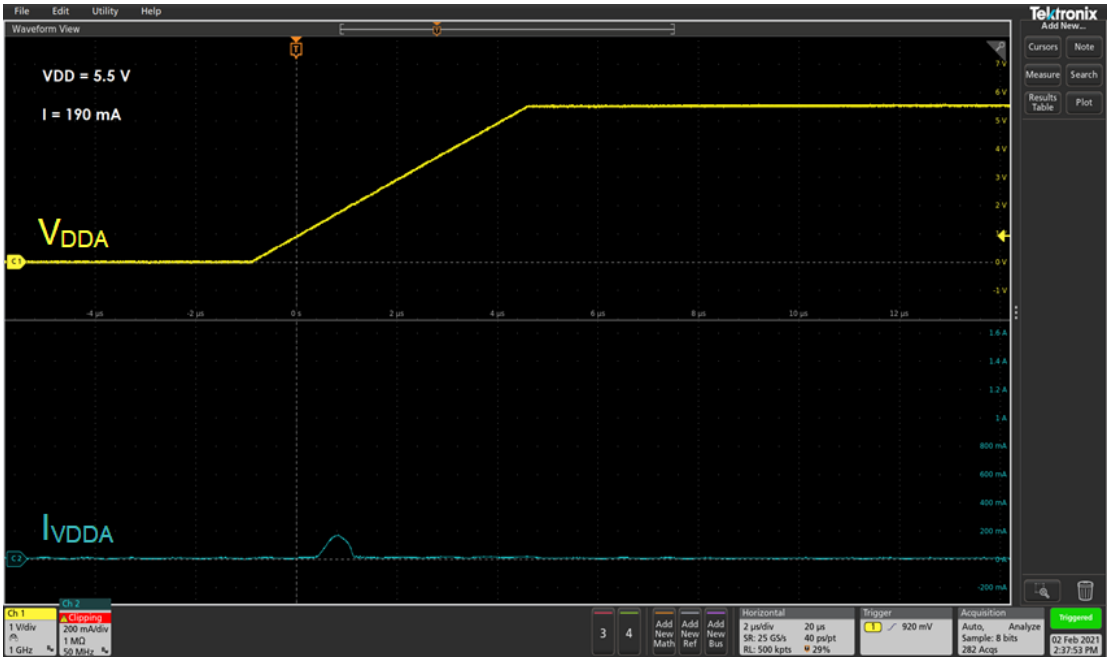

Figure 1: Inrush Current at V_{DDA} Slew Rate = 1 V/µs

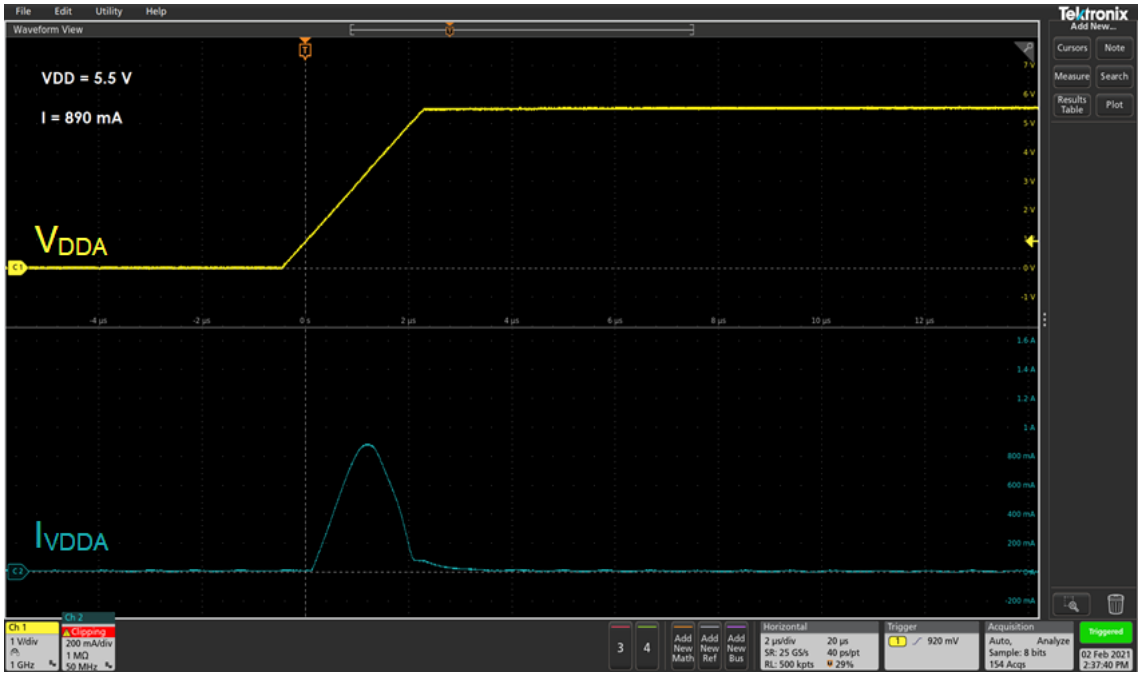

Figure 2: Inrush Current at V_{DDA} Slew Rate = 2 V/µs

In addition to damaging the SLG47004, this inrush current introduces two other concerns. When powering ON the device, the customer will see increased power consumption within their system, which can be critical for some low power applications. This behavior also introduces the risk of power supply brownout if the power source (LDO, battery, capacitor, and others) is too weak to source the inrush current drawn by the SLG47004. If ignored, these brownout issues can cause faults to occur in other ICs throughout the system.

3.1.4 Workaround

To avoid this behavior, we recommend limiting the Analog V_{DD}'s slew rate to a value lower than 2 V/µs, as this will protect the SLG47004 while limiting inrush current. This can be done by many methods including the use of slew rate limited analog switches or DC/DC converters. Alternatively, you could increase the capacitance on the SLG47004's Analog V_{DD} line and place a series resistance on the output of the power supply. Note that this resistor will introduce additional power loss to the system and will cause voltage noise on the analog power rail.

Document Revision History

Revision	Date	Description
1.2	8-Mar-2022	Renesas rebranding
1.1	12-Feb-2021	Corrected Slew Rate and Inrush Current values
1.0	9-Nov-2020	Initial version

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.