Supplemental Information

This Device Errata reflects revision 1.0 silicon and supplement information found in the documentation for this device.

Z step is revision 1.0. This is identified by material date code (top mark) of 0320 or later.

Document Revision History

Mar 19, 2007 : First version of the document.

Description and Workarounds

Item #1: Divide by 6 Output Divider

Issue: Under certain process conditions and if no master reset is applied, using the divide by six output divider may result in the outputs QAn to start up at the wrong frequency.

Workaround:

(a) Using a master reset (MR) after power up resolves the problem with the divide-by-six output divider.

(b) Applications using FSELA = high (outputs in divide-by-six) should use a master reset (MR) after power up to resolve the problem.

Fix: Device ICS87952AYI-147 is recommended as pin compatible replacement if output divider by six is required without applying master reset (MR) at start up.

Note: Only applicable to applications with FSELA = high (outputs in divide-by-six). Applications using FSELA=low (outputs in divide-by-four) are not affected.