Integrated Device Technology, Inc.
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Errata Notification

EN #: NEN-12-04 Errata Revision #: 0

Issue Date: July 4, 2012 Effective Date: July 4, 2012

Product Affected: 810252AGILF

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ERRATA DETAILS:

- ☐ Data Sheet Errata
- ■ Device Errata
- ☐ Device Manual Errata
- ☐ Application Notes Errata
- ☐ Other (Please Specify)

ATTACHMENT ■ Yes ☐ No

This notification is to advise our customers that IDT has issued a Device Errata to clarify the Output Duty Cycle (odc) on the Data Sheet.

Added notes 5 and 6 on Tables 4A & 4B (AC Characteristics) to specify that odc min and max % is with the VCXO-PLL free running or with the VCXO-PLL locked.

Refer to the attachment for the Data Sheet change details.

A test program revision has been implemented to check for this condition.

IDT Web Site Location: http://www.idt.com/node/34777

CUSTOMER NOTIFICATION:

As a result of Errata listed above, IDT has decided to notify you through this Errata Notification.
We recommend you to review this notification in details prior to the use of affected product in your application.
Please use acknowledgement below or E-Mail to request additional information.

If you have any questions, please feel free to contact your local IDT distributor or sales representative.

Customer: _____ E-Mail Address: _____

Name/Date: _____ Phone #: _____

Title: _____ Fax # : _____

CUSTOMER COMMENTS: _____

Specific Changes: Applies to the ICS810252AGILF.

1.) Tables 4A & 4B:

From:

Table 4A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Reference Frequency			25		MHz
				125		MHz
f_{VCO}	VCXO-PLL Frequency			25		MHz
f_{OUT}	Output Frequency			25		MHz
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter; NOTE 1				25	ps
*t*sk(o)	Output Skew; NOTE 2, 3				15	ps
tjit(θ)	RMS Phase Jitter (Random); NOTE 4	f_{OUT} = 25MHz, Integration Range: 12kHz – 5MHz		0.25		ps
$t_{JIT(PER)}$	Period Jitter, RMS				2.7	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	550		1100	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using a 537Hz VCXO-PLL Loop Bandwidth. Refer to VCXO_PLL Applications Section.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Refer to the Phase Noise Plot.

Table 4B. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Reference Frequency			25		MHz
				125		MHz
f_{VCO}	VCXO-PLL Frequency			25		MHz
f_{OUT}	Output Frequency			25		MHz
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter; NOTE 1				20	ps
*t*sk(o)	Output Skew; NOTE 2, 3				25	ps
tjit	RMS Phase Jitter (Random); NOTE 4	f_{OUT} = 25MHz, Integration Range: 12kHz – 5MHz		0.26		ps
$t_{JIT(PER)}$	Period Jitter, RMS				5.7	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	700		1850	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using a 537Hz VCXO-PLL Loop Bandwidth. Refer to VCXO_PLL Applications Section.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Refer to the Phase Noise Plot.

To:

Table 4A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Reference Frequency			25		MHz
				125		MHz
f_{VCO}	VCXO-PLL Frequency			25		MHz
f_{OUT}	Output Frequency			25		MHz
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter; NOTE 1				25	ps
*t*sk(o)	Output Skew; NOTE 2, 3				15	ps
tjit(θ)	RMS Phase Jitter (Random); NOTE 4	f_{OUT} = 25MHz, Integration Range: 12kHz – 5MHz		0.25		ps
$t_{JIT(PER)}$	Period Jitter, RMS				2.7	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	550		1100	ps
odc	Output Duty Cycle ; NOTE 5		48		52	%
odc	Output Duty Cycle; NOTE 6		45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using a 537Hz VCXO-PLL Loop Bandwidth. Refer to VCXO_PLL Applications Section.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Refer to the Phase Noise Plot.
NOTE 5: Specified with the VCXO-PLL free running.
NOTE 6: Specified with the VCXO-PLL locked.

Table 4B. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Reference Frequency			25		MHz
				125		MHz
f_{VCO}	VCXO-PLL Frequency			25		MHz
f_{OUT}	Output Frequency			25		MHz
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter; NOTE 1				20	ps
*t*sk(o)	Output Skew; NOTE 2, 3				25	ps
tjit	RMS Phase Jitter (Random); NOTE 4	f_{OUT} = 25MHz, Integration Range: 12kHz – 5MHz		0.26		ps
$t_{JIT(PER)}$	Period Jitter, RMS				5.7	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	700		1850	ps
odc	Output Duty Cycle ; NOTE 5		48		52	%
odc	Output Duty Cycle; NOTE 6		44		56	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using a 537Hz VCXO-PLL Loop Bandwidth. Refer to VCXO_PLL Applications Section.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Refer to the Phase Noise Plot.
NOTE 5: Specified with the VCXO-PLL free running.
NOTE 6: Specified with the VCXO-PLL locked.