Description

The ZWIR4512 enables secure low-power wireless IPv6 communication for sensors and small devices. IDT provides a user-programmable, royalty-free 6LoWPAN stack with mesh routing capability with the ZWIR4512. 6LoWPAN is an Internet Engineering Task Force (IETF) standard for building wireless, low-power IP-based sensor, and device networks. These networks can easily be integrated into existing IT infrastructure or operate autonomously.

Secure communication is provided by standard-compliant implementations of the Internet Protocol Security (IPSec) protocol suite and the Internet Key Exchange Protocol version 2 (IKEv2), which enable highly secure end-to-end communication, including over unsecure network nodes.

The module is powered by an ARM® Cortex™-M3 (ARM, Ltd. trademark) microcontroller and provides a rich set of GPIO and peripheral interfaces. Up to 192kB of flash and 32kB of RAM are available for applications. Different low power modes are provided to save energy in battery-operated devices. The modules provide superior radio properties without the need for complicated external RF design.

Firmware Features

- Serial command interface with built-in security and over-the-air update (OTAU) functionality
- Royalty-free library bundle for custom firmware: 6LoWPAN communication library with mesh routing capability; IPSec and IKEv2 security libraries; over-the-air update library; several peripheral libraries

Available Support

- Development Kit
- Programming guide and application notes
- Ethernet, USB and UART gateways
- Free packet sniffer and example programs demonstrating C-API usage
- Windows® (Microsoft Corp. trademark) and Linux® (Linus Torvalds trademark) support tools

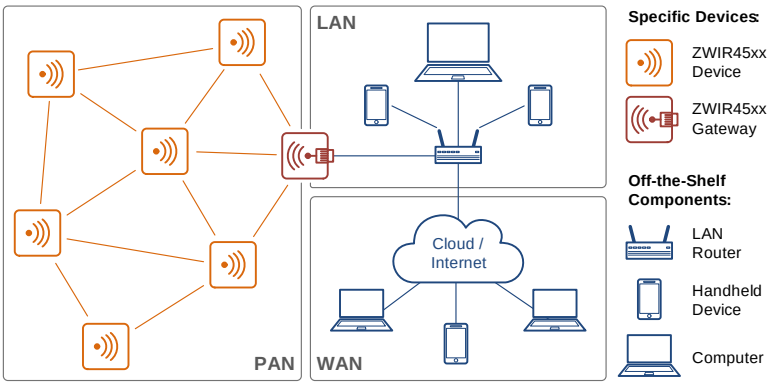
Typical Applications

- The ZWIR4512 serves as a universal secure radio communication module. Typical applications include home and industry automation, health monitoring, smart metering / smart grid applications, and keyless entry systems.
- Its very low current consumption makes the module suitable for battery-operated devices.

Hardware Features

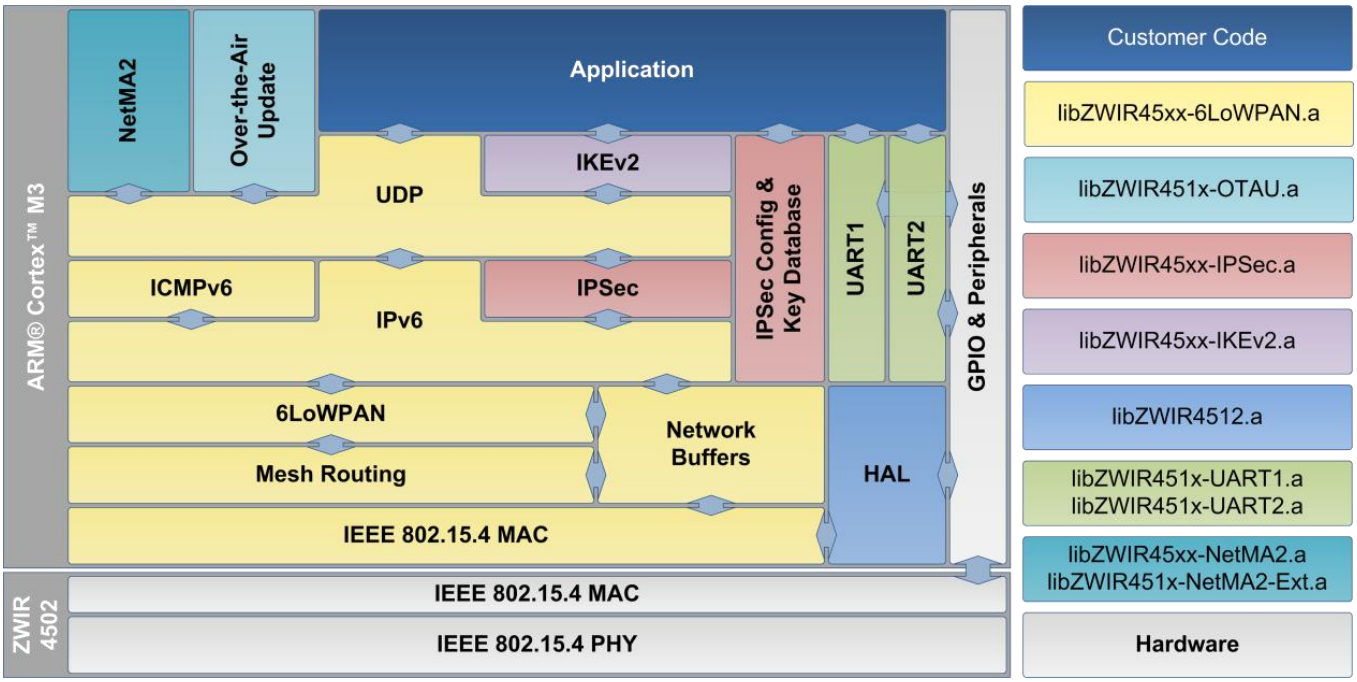
- License-free 868/915MHz frequency bands
- ARM® Cortex™-M3 32-bit microcontroller
- ≤192kB flash and 32kB RAM for user applications
- Unique EUI64 address
- 4 channels in EU mode; 10 channels in US mode
- 19 (ZWIR4512AC1) or 21 (ZWIR4512AC2) GPIOs with multiplexed peripheral functions:
  - 2 x UART, SPI, 3 x ADC, 2 x DAC, 11 x PWM, USB, CAN, I2C, 8 x timer
  - Several 5V tolerant I/Os available
- Low current consumption: 3.5µA in Standby Mode; 10.5mA in Receive Mode; 16.0mA in Transmit Mode at 0dBm
- Modulation schemes
  - BPSK (20kBps EU, 40kBps US)
  - O-QPSK (100kBps EU, 250kBps US)
- Receiver sensitivity: up to -110dBm
- TX output power: up to 10dBm (US Mode)
- Uniquely simple programmability
- Standard-compliant security solution
- No need for external microcontroller
- Plug-and-play integration into local and wide-area networks
- No RF design required
- 2D barcode label containing MAC address
- Superior radio propagation
- ETSI/FCC certified
- Supply voltage: 2.0V to 3.6V
- Operating temperature: -40°C to +85°C
- 30-pin edge-board contact package or 32-pin land grid array package

Typical ZWIR4512 Application Setup

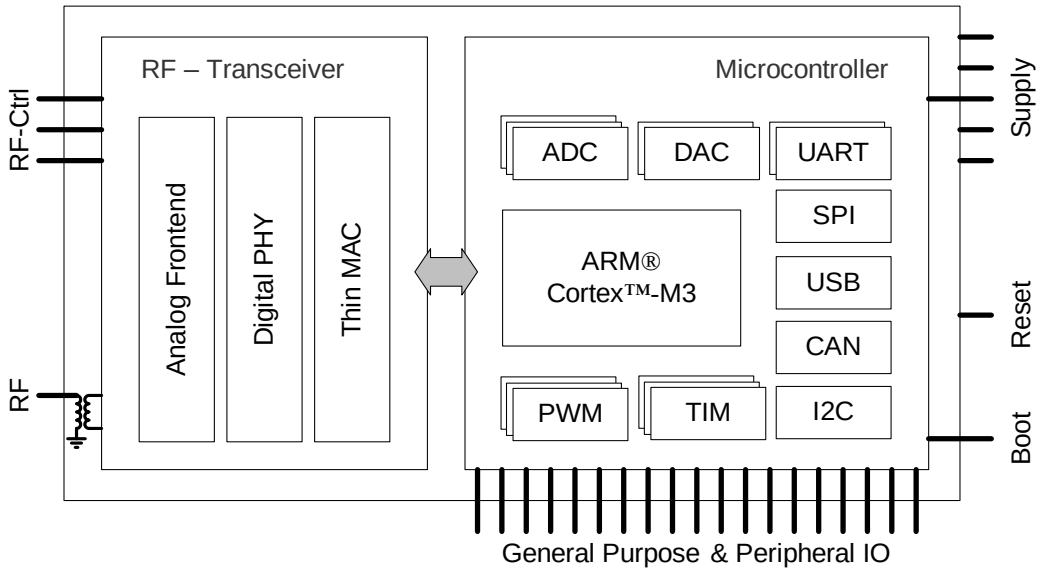


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Stack Architecture



ZWIR4512 Functional Block Diagram



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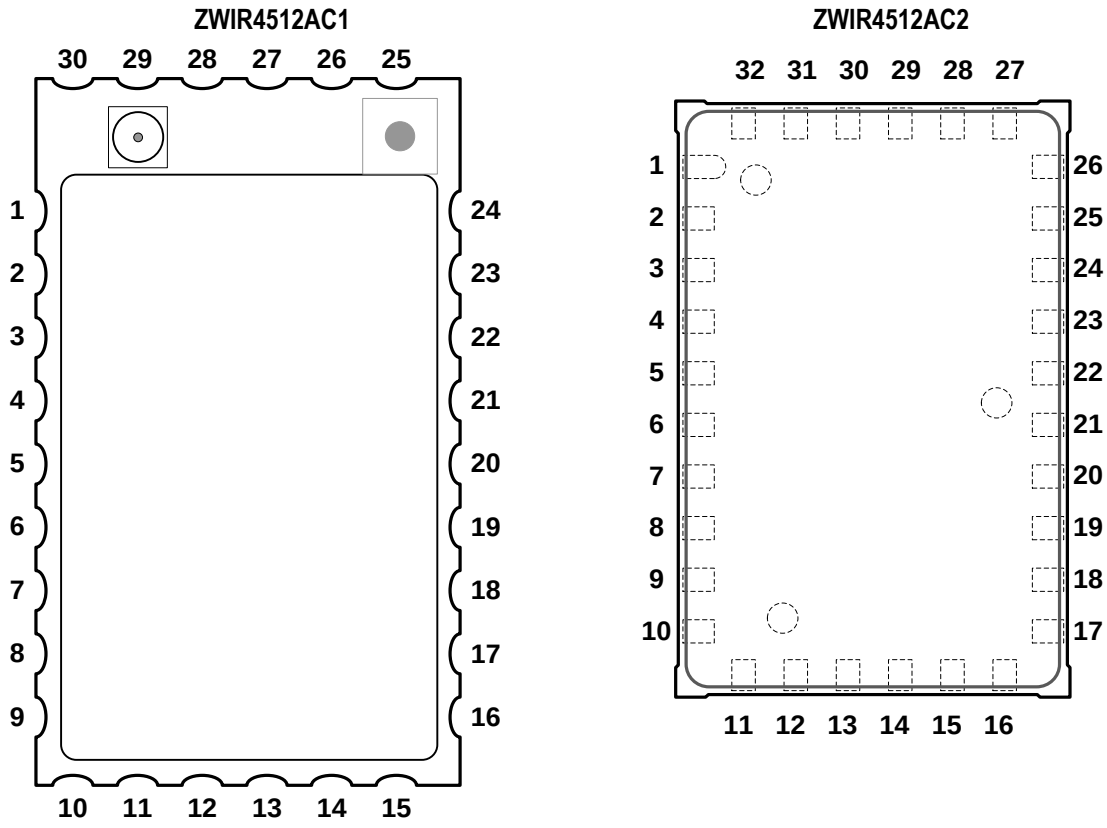
1. Pin Assignments

The ZWIR4512 GPIO pins have different functionalities, controllable by software. The most commonly used functions available on each pin are listed in Table 2.1. Furthermore, the GPIO peripheral functions are shown as an overview in Table 2.3. The full list of available functions of each pin can be obtained from the *STM32F103xC Datasheet*.

Some peripheral I/O functions are available through different pins. The default GPIO pin for each peripheral function is marked with an ♦ in Table 2.3. When it is possible to remap a peripheral function to another module pin, this is marked with a letter. The corresponding remapping function is described in Table 2.2.

There are two variations on the package: ZWIR4512AC1 (30 pins) and ZWIR4512AC2 (32 pins). See Figure 1.1 for the pin layout.

Figure 1.1 ZWIR4512ACx Pinout



2. Pin Descriptions

Table 2.1 ZWIR4512ACx Pin Description

Pins		Name	MCU Port	Type[a]	5V	API Function [b], [c]	SCI Function [c], [d]
ZWIR4512AC1	ZWIR4512AC2						
1	1	GPIO7	PA7	IO		*GPIO* SPI1 – MOSI ADC1 / ADC2 – channel 7 PWM	*SPI – MOSI*
2	2	GPIO6	PA6	IO		*GPIO* SPI1 – MISO ADC1 / ADC2 – channel 6 PWM	*SPI – MISO*
3	3	GPIO5	PA5	IO		*GPIO* SPI1 – SCK DAC – OUT2 ADC1 / ADC2 – channel 5	*SPI – SCK*
4	4	GPIO4	PA4	IO		*GPIO* SPI1 – NSS USART2 – CK DAC – OUT1 ADC1 / ADC2 – channel 4	*SPI – NSS* GPIO
5	5	GPIO3	PA3	IO		*GPIO* USART2 – RX ADC1 / ADC2 / ADC3 – channel 3 PWM	*UART2 – RX* GPIO
6	6	GPIO2	PA2	IO		*GPIO* USART2 – TX ADC1 / ADC2 / ADC3 – channel 2 PWM	*UART2 – TX*
7	7	GPIO1	PA1	IO		*GPIO* USART2 – RTS ADC1 / ADC2 / ADC3 – channel 1 PWM	*GPIO* UART2 - RTS
8	8	GPIO0	PA0-WKUP	IO		*GPIO* WKUP USART2 – CTS ADC1 / ADC2 / ADC3 – channel 0 PWM	*GPIO* UART2 CTS
9	9	GPIO12	PC13	IO		*GPIO* TAMPER-RTC	*GPIO*

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Pins		Name	MCU Port	Type[a]	5V	API Function [b], [c]	SCI Function [c], [d]
ZWIR4512AC1	ZWIR4512AC2						
18	10	VSTDBY	VBAT	S		Alternative Standby Mode power supply	
10	11	/RESET	NRST	I	✓	Reset	
11	12	GND	GND	S		Ground	
12	13	GPIO9	PA10	IO	✓	*GPIO* USART1 – RX PWM	*UART1 – RX* GPIO
13	14	GPIO8	PA9	IO	✓	*GPIO* USART1 – TX PWM	*UART1 – TX* GPIO
14	15	VCC	VCC	S		Power supply	
15	16	BSEL	BOOT0	I		Boot mode selection	
n/a	17	GPIO15	PC14	IO		*GPIO* OSC32 – IN	*GPIO*
n/a	18	GPIO16	PC15	IO		*GPIO* OSC32 – OUT	*GPIO*
16	19	GPIO10	PA11	IO	✓	*GPIO* USART1 – CTS USB – D- CAN – RX PWM	*GPIO* UART1 – CTS
17	20	GPIO11	PA12	IO	✓	*GPIO* USART1 – RTS USB – D+ CAN – TX Timer Trigger (TIM1)	*GPIO* UART1 – RTS
19	21	TDO	PB3	IO	✓	*JTAG – TDO* GPIO PWM	
20	22	TMS	PA13	IO	✓	*JTAG – TMS, SWDIO* GPIO	*GPIO*
21	23	TDI	PA15	IO	✓	*JTAG – TDI* GPIO	*GPIO*
22	24	TCK	PA14	IO	✓	*JTAG – TCK, SWCLK* GPIO	*GPIO*
23	25	GPIO14	PB7	IO	✓	*GPIO* I2C – SDA UART1 – RX PWM	*GPIO*

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Pins		Name	MCU Port	Type[a]	5V	API Function [b], [c]	SCI Function [c], [d]
ZWIR4512AC1	ZWIR4512AC2						
24	26	GPIO13	PB6	IO	✓	*GPIO* I2C-SCL UART1 – TX PWM	*GPIO*
25	27	DIG1	–	O		Unused, leave unconnected	
26	28	PACTLN	–	O		PA control (differential) complementary output, leave unconnected if unused	
27	29	PACTLP	–	O		PA control (differential), leave unconnected if unused	
28	30	GND	GND	S		Ground	
29	31	ANT	–	IO		Antenna pin	
30	32	GND	GND	S		Ground	

[a] The "Type" column indicates the type of the pin: IO = input/output, I = input only, O = output only, S = power supply.

[b] The listed functionalities include only the most important functionalities – please refer to the STM32F103xC data sheet for a full list.

[c] Functions listed in italic letters are selected by default if the device is not reprogrammed. GPIOs are analog inputs by default.

[d] Any pin marked as GPIO can be configured as indicator for incoming or outgoing packets on network or serial interfaces.

Table 2.2 ZWIR4512ACx GPIO Remapping

Name	Peripheral	Pin	Change	Required Action
A	UART1	RX	PA10 ➔ PB7	Write 1_{BIN} to AFIO_MAPR[2] (See sections 8.3 and 8.4.2 of the *STM32F103xx Reference Manual.*)
		TX	PA9 ➔ PB6	
		RTS	PA12 ➔ Ø	
		CTS	PA11 ➔ Ø	
B	Timer 1	CH1N	Ø ➔ PA7	Write 01_{BIN} to AFIO_MAPR[11:10]
C	Timer 2	Ch2	PA1 ➔ PB3	Write 01_{BIN} to AFIO_MAPR[9:8]
		Ch1	PA0 ➔ PA15	
D	JTAG	TDI	PA15 ➔ Ø	Write 010_{BIN} to AFIO_MAPR[26:24]
		TDO	PB3 ➔ Ø	
E	JTAG	TMS	PA13 ➔ Ø	Write 100_{BIN} to AFIO_MAPR[26:24]
		TCK	PA14 ➔ Ø	
		TDI	PA15 ➔ Ø	
		TDO	PB3 ➔ Ø	

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Table 2.3 ZWIR4512ACx GPIO Function Overview

Note: See important notes at the end of the table.

ZWIR4512AC2-Pin		1	2	3	4	5	6	7	8	9	13	14	17	18	19	20	21	22	23	24	25	26
ZWIR4512AC1-Pin		1	2	3	4	5	6	7	8	9	12	13	–	–	16	17	19	20	21	22	23	24
MCU – GPIO Port		A7	A6	A5	A4	A3	A2	A1	A0	C13	A10	A9	C14	C15	A11	A12	B3[a]	A13[b]	A15[a]	A14[b]	B7	B6
UART1	RX										♦										A	
	TX											♦										A
	RTS															♦,A						
	CTS														♦,A							
USART2	RX					♦																
	TX						♦															
	RTS							♦														
	CTS								♦													
	CK				♦																	
SPI1	MOSI	♦																				
	MISO		♦																			
	SCK			♦																		
	NSS				♦																	
I2C	SDA																				♦	
	SCL																					♦
USB	D-														♦							
	D+															♦						
CAN	RX														♦							
	TX															♦						
Standby Wakeup									♦													

ZWIR4512AC2-Pin		1	2	3	4	5	6	7	8	9	13	14	17	18	19	20	21	22	23	24	25	26
ZWIR4512AC1-Pin		1	2	3	4	5	6	7	8	9	12	13	–	–	16	17	19	20	21	22	23	24
MCU – GPIO Port		A7	A6	A5	A4	A3	A2	A1	A0	C13	A10	A9	C14	C15	A11	A12	B3[a]	A13[b]	A15[a]	A14[b]	B7	B6
PWM	T1 - Ch1N	B																				
	T1 - Ch2											♦,B										
	T1 - Ch3										♦,B											
	T1 - Ch4														♦,B							
	T2 - Ch1								♦										C[a]			
	T2 - Ch2							♦									C[a]					
	T2 - Ch3						♦,C															
	T2 - Ch4					♦,C																
	T3 - Ch1		♦																			
	T3 - Ch2	♦																				
	T4 - Ch1																					♦
	T4 - Ch2																				♦	
	T5 - Ch1								♦													
	T5 - Ch2							♦														
	T5 - Ch3						♦															
	T5 - Ch4					♦																
ADC	Ch0								♦													
	Ch1							♦														
	Ch2						♦															
	Ch3					♦																
	Ch4				♦																	
	Ch5			♦																		
	Ch6		♦																			
	Ch7	♦																				
DAC	DAC1				♦																	
	DAC2			♦																		
JTAG	TMS																	♦ [c]				
	TCK																			♦ [c]		
	TDI																		♦ [c]			
	TDO																♦ [c]					
SWD	SWDIO																	♦,D [d]				
	SWDCLK																			♦,D [d]		

[a] GPIO or peripheral functionality of this port is only available with remap function D or E active.

[b] GPIO functionality of this port is only available with remap function E active.

[c] JTAG functionality is only available when remap functions D and E are inactive.

[d] SWD functionality is only available when remap function E is inactive.

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3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. The device might not function or be operable above the operating conditions. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the operating conditions might affect device reliability. IDT does not recommend designing to the “Absolute Maximum Ratings.”

3.1 Absolute Maximum Voltage Characteristics

Parameter	Symbol	Min	Max	Unit
Main supply voltage	V_{CC}	-0.3	4	V
Backup supply voltage	V_{BAT}	-0.3	4	V
Input voltage at 5V-tolerant GPIO pin	V_{GPIO}	-0.3	5.5	V
Input voltage at any other GPIO pin		-0.3	V_{CC}+0.3	V

3.2 Absolute Maximum Current Characteristics

Parameter	Symbol	Max	Unit
Maximum total current consumption	I_{VCC}	175	mA
Driving strength of each GPIOx pin	I_{GPIO}	±25	mA
Driving strength of RF-control pins (PACTLN, PACTLP, DIG1)	I_{RFCTRL}	8	mA

3.3 Absolute Maximum Thermal Characteristics

Parameter	Symbol	Value	Unit
Storage temperature range	T_{STOR}	-40 to +125	°C
Ambient temperature range	T_{AMB}	-40 to +85	°C

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4. Electrical Characteristics

4.1 General Operating Conditions

Note: See important notes at the end of the table.

Parameter		Symbol	Min	Typ	Max	Unit
Electrical Characteristics						
Main supply voltage – ADC not used		V_{CC}	2.0		3.6	V
Main supply voltage – ADC used		V_{CC}	2.4		3.6	V
Backup supply voltage		V_{BKUP}	1.8		3.6	V
Digital I/O high level input voltage		V_{IH}	V_{CC} – 0.4			V
Digital I/O low level input voltage		V_{IL}			0.4	V
Digital I/O high level output voltage		V_{OH}	V_{CC} – 0.4			V
Digital I/O low level output voltage		V_{OL}			0.4	V
MCU Clock Characteristics						
MCU core clock frequency [a]		f_{AHB}	8		64	MHz
MCU core clock frequency accuracy range		Δf_{AHB}	-2		2.5	%
MCU peripheral bus 1 clock frequency [b]		f_{APB1}		4		MHz
MCU peripheral bus 2 clock frequency [b]		f_{APB2}		8		MHz
RF Parameters						
Frequency range		f_{RF}	865		928	MHz
Output power [c]			-11		10	dBm
Output power tolerance			-3		+3	dB
Receiver sensitivity	BPSK, EU Mode			-110		dBm
	BPSK, US Mode			-108		
	QPSK, EU Mode			-101		
	QPSK, US Mode			-101		
Gross data rate	BPSK, EU Mode			20		kBit/s
	BPSK, US Mode			40		
	QPSK, EU Mode			100		
	QPSK, US Mode			250		
Channel spacing	EU Mode			1		MHz
	US Mode			2		

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Parameter		Symbol	Min	Typ	Max	Unit
Number of channels	EU Mode [d]			1 (+3)		
	US Mode			10		
Input/output impedance				50		Ω
Frequency offset			-10		+10	kHz

[a] The f_{CORE} clock can be configured to be 8, 16, 32, or 64 MHz. After reset, the clock is set to 8MHz.

[b] f_{APB1} and f_{APB2} are derived from f_{AHB}. Therefore, the same tolerances apply to these clocks.

[c] 10dBm output power is only available in US Mode; EU Mode provides 5dBm maximum output power.

[d] The IEEE802.15.4 standard defines only 1 channel for EU Mode, but extension channels are available in almost all EU countries.

4.2 Current Consumption per Operating Mode

Operating Mode	Condition	Typ [a]	Unit
Run Mode	Receiver active	10.5	mA
	Transmitter active, EU frequency band, BPSK, 0dBm	16.1	
	Transmitter active, EU frequency band, QPSK, 0dBm	15.5	
	Transmitter active, EU frequency band, BPSK, 5dBm	23.4	
	Transmitter active, EU frequency band, QPSK, 5dBm	22.8	
	Transmitter active, US frequency band, BPSK, 0dBm	14.9	
	Transmitter active, US frequency band, QPSK, 0dBm	14.2	
	Transmitter active, US frequency band, BPSK, 5dBm	18.0	
	Transmitter active, US frequency band, QPSK, 5dBm	17.3	
	Transmitter active, US frequency band, BPSK, 10dBm	24.0	
	Transmitter active, US frequency band, QPSK, 10dBm	23.4	
	TRX Off	0.7	
Stop Mode	TRX Off, RTC running	26.5	µA
Standby Mode	TRX Off, RTC running	3.5	µA

[a] Current consumption values refer to devices operating at 25°C with network stack library version 1.9 and an application that does not generate a workload on the MCU.

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5. Module Description

The ZWIR4512 is a programmable wireless IPv6 communication module. Communication is based on 6LoWPAN, a free and open communication standard developed by the Internet Engineering Task Force (IETF). This standard specifies how to transmit IPv6 (Internet Protocol Version 6) packets over low-power wireless personal area networks.

ZWIR4512 modules are available with a preprogrammed command interface, allowing modem-like communication based on simple commands sent over a serial interface. Alternatively, the module is freely programmable on the basis of an application programming interface (API) that exposes abstract communication functionality to the programmer.

Both software options offer secure communication on the basis of the IP Security (IPSec) protocol suite. Additionally, an implementation of the Internet Key Exchange Protocol version 2 (IKEv2) is provided, in order to make key management as easy as possible. IPSec and IKEv2 are the mandated standards for securing IPv6 networks. Refer to *ZWIR45xx Application Note—Using IPSec and IKEv2 in 6LoWPANs* for more detailed information about IPSec and IKEv2.

The module comprises an STM32F103RC ARM® Cortex™-M3 microcontroller from ST Microelectronics and a ZWIR4502 transceiver from IDT. These components ensure leading-edge performance values at very low power consumption. The module provides a hardware-programmed 64-bit MAC address that is guaranteed to be globally unique.

5.1 Radio Transceiver

The module includes IDT's ZWIR4502 radio transceiver. This circuit performs modulation and demodulation of outgoing and incoming data, respectively. The modulation scheme is configurable according to the IEEE802.15.4 standard. The radio transceiver is never accessed directly by application code. This task is performed by the communication stack, which encapsulates such low-level functionality in abstract functions.

5.2 Microcontroller

The protocol stack and the user application are executed on an STM32F103RC microcontroller (MCU) from ST Microelectronics. It provides 256kB flash and 48kB SRAM memory. The MCU provides a rich set of peripherals and a number of general purpose input/output (GPIO) ports. The GPIO ports of the module are directly connected to the GPIOs of the MCU. Refer to Table 2.1 for an exact mapping.

5.2.1 MCU Core

The MCU core is an ARM® Cortex™-M3. This is a 32-bit RISC core with a performance of 1.25 DMIPS/MHz. Using IDT's software stack, the maximum operating frequency is 64MHz. This allows for computational intensive applications. In order to save power, the core can be shut off completely, waking up only on external activity.

5.2.2 Peripherals and Interfaces

The module was designed to make maximum use of the controller's internal peripherals. Up to 21 digital general purpose I/Os can be used by the application. Most of these I/Os have alternative functions. Some of them are 5V-tolerant. Table 2.1 shows the most commonly used functions available for each interface. Table 2.3 shows all functionalities on a single page, indicating which peripherals must not be used in parallel as their GPIOs are interfering.

In addition to communication interfaces, the module also provides signal conversion peripherals. Three analog-to-digital converters (ADCs), two digital-to-analog converters (DACs), and two pulse-width modulation (PWM) peripherals are available.

5.2.3 Programming and Debugging

Programming and debugging the module is typically done via JTAG. All required MCU ports are connected to module pins for that purpose. Alternatively, Serial Wire Debug (SWD) can be used for programming and debugging. This requires just two pins that must be reserved, providing two additional GPIO pins.

Alternatively, if debug functionality is not required, it is possible to program the module over a two-wire UART interface. For that purpose, the MCU's internal boot-loader must be started. This is done by holding the BSEL pin of the module high while a reset is performed or the module is powered on. Refer to the MCU documentation for more information about serial programming.

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5.3 Firmware

5.3.1 Serial Command Interface (SCI) Firmware

A module programmed with the Serial Command Interface firmware acts as a network processor. In this configuration, the module is controlled over a serial interface that is SPI, USB, or one of the two UARTs. The SCI firmware provides all standard communication functions for data transmission and reception, as well as all security functions and over-the-air update (OTAU) functionality. Access to internal peripherals is limited to digital control of the GPIO pins. Typically, an external microcontroller or a PC is required to control module operation. However, for simple sensing or acting applications, it is also possible to configure the module to run autonomously without the need for an external controller. Refer to the *ZWIR45xx Serial Command Interface Manual* for further information.

5.3.2 C Application Programming Interface (C-API)

A C-API is provided for applications that should run directly on the embedded microcontroller. Communication and security functionalities are encapsulated in a set of libraries that export functions for accessing and controlling them. The library architecture is modular, allowing tailoring applications to user needs. Applications running on the microcontroller can make use of the rich set of peripherals that are provided by the controller.

Depending on the library configuration, there are up to 192kB of flash and 32kB of RAM available for the user application. This is sufficient even for complex applications with high memory needs. If over-the-air update (OTAU) functionality is required, the amount of flash available for user applications is reduced to one half. For further information on C-API programming and OTAU, refer to the *ZWIR451x Programming Guide* and the *ZWIR45xx Over-the-Air Update Manual*.

5.4 Power Modes

The ZWIR4512 module provides a set of operating modes with different capabilities and power requirements. This document only highlights the main features of these operating modes. Table 5.1 gives an overview of the characteristics of the available power modes. See section 4.2 for a table of typical current consumption in the different modes.

Refer to the *ZWIR451x Programming Guide* for detailed usage instructions for the low-power modes.

Table 5.1 Power Modes Overview

Mode	Wakeup		Clock		Context [a]	I/O	Transceiver
	Source	Time	MCU Core	Peripherals			
Run			On	On [b]	Retained	As configured	On [c]
Sleep	Any IRQ	1.8µs	Off	Off [d]	Retained	As configured	Off [d]
Stop	RTC IRQ External IRQ	5.4µs	Off	Off	Retained	As configured	Off [d]
Standby	RTC IRQ Wakeup pin	50µs	Off	Off	Lost	Analog input	Off

[a] Refers to the status of the RAM and peripheral register contents after wakeup – the backup registers of the MCU are always available.

[b] Clock is enabled for all peripherals that have been enabled by application code and all peripherals that are used by the library.

[c] Can be powered off by application code.

[d] Remains if peripheral/transceiver is selected as wakeup source.

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5.4.1 Run Mode

In Run Mode, all functions of the module are available. The microcontroller and all its peripherals are powered. Typically the transceiver is also powered, but it can be disabled by software. The module enters Run Mode automatically after startup. The application software must switch to one of the other operating modes if required.

5.4.2 Sleep Mode

In Sleep Mode, the microcontroller core is not clocked. The power state of the transceiver and the microcontroller peripherals depends on the wakeup configuration. All peripherals that are selected as a wakeup source continue to operate. After wakeup, the application program continues execution at the position it was stopped. Sleep Mode allows reacting to external events such as the reception of data, external interrupts, or timer events. The power consumption in this mode strongly depends on which peripherals are enabled. The I/O configuration is not changed during Sleep Mode.

5.4.3 Stop Mode

Stop Mode is an ultra-low-power mode with RAM retention. The MCU core and the MCU peripherals are not clocked. Only the internal real-time clock or any external pin can be used for triggering wakeup from Stop Mode. After wakeup, the program continues execution at the position it was stopped. In Stop Mode, all I/Os remain in the configuration that was active when entering Stop Mode.

5.4.4 Standby Mode

Standby Mode is the lowest power mode. The transceiver and all microcontroller peripherals are consequently powered off. RAM contents are lost. Waking up from Standby Mode can be triggered by a real-time-timer event or by one dedicated pin. When going to Standby Mode, all I/Os are put into analog input mode, so the application circuit must ensure that external components receive defined signal levels if required. When the module exits Standby Mode, it is restarted from the reset handler in the same sequence as the restart after power-on or after the reset button has been pressed.

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6. Application Circuits

ZWIR4512 modules are designed to require minimal external circuitry. The following sections illustrate how modules must be connected in order to ensure proper power supply, reset behavior, programmability, and radio performance. Instructions for the connection of GPIO pins are not given.

6.1 Power Supply

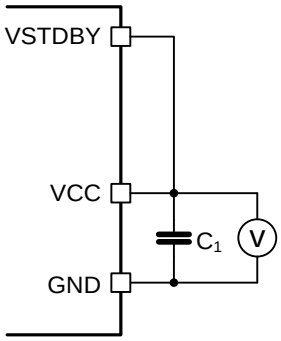
All internal components of the ZWIR4512 that require a stable power supply are internally decoupled with a number of capacitors. Nevertheless, the module requires one external decoupling capacitor between VCC and GND. This is the minimal external circuitry required for proper operation.

The module provides two different power supply pins: VCC and VSTDBY. V_{CC} is the normal supply voltage that must be applied in Run, Sleep, or Stop Mode. During Standby Mode, the module is powered by V_{STDBY} and V_{CC} can be switched off.

Figure 6.1 shows two possible power supply schemes. Scheme a) connects VSTDBY to the same voltage source as VCC. This is the commonly used configuration. However, scheme b) allows switching off V_{CC} in Standby Mode. This can help reduce power dissipation in applications with ultra-low power requirements. During the complete standby phase, VSTDBY is powered from a buffering capacitor.

Figure 6.1 Power Supply Schemes

a) Without Separate Standby Supply



b) With Capacitor Based Standby Supply

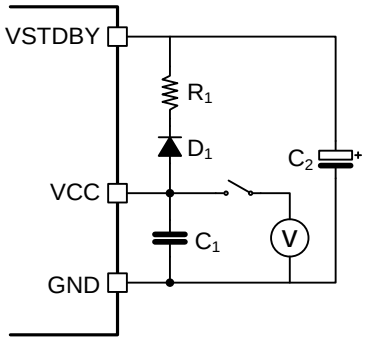


Table 6.1 External Power Supply Components

Symbol	Function	Value/Comment
C_1	Decoupling capacitor	Mandatory, 10µF
R_1	Charge current limitation	6.8kΩ
D_1	Buffering capacitor discharge protection	Schottky diode; e.g., BAT54-02V
C_2	Buffering capacitor	≥ 0.1µF

6.2 Reset and Boot Select

The /RESET pin is de-bounced and has a pull-up resistor on the PCB. Thus, a push-button can be connected directly to GND or the pin can be left unconnected if it is not required. The boot select pin (BSEL) is pulled down internally. If BSEL is not required, it can be left unconnected. Figure 6.2 shows how these pins are connected externally and illustrates the internal circuitry.

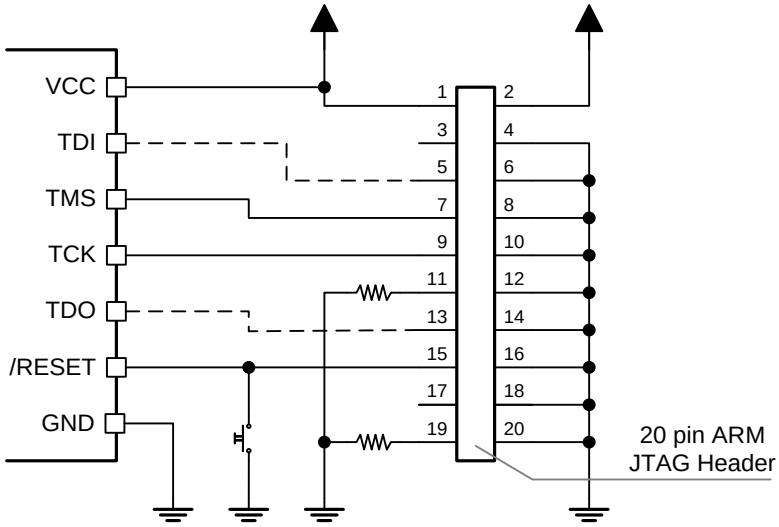
Figure 6.2 External Circuitry for /RESET and BSEL



6.3 Debug Access

The ZWIR4512 provides debug access by means of a JTAG or SWD interface. Figure 6.3 shows an example of connecting the module with a 20-pin standard ARM® JTAG header. If no JTAG connection is required, the dashed-line connections can be left out and two additional pins are available as GPIOs.

Figure 6.3 JTAG / SWD Connection for Programming and Debugging



6.4 Antenna

There are two options to connect an external antenna. The antenna can be connected to the module using a coaxial cable that is mounted on the U.FL connector, or an external antenna terminal on the host PCB can be connected to the ANT pin. If the on-board U.FL connector is used, the ANT pin must be left unconnected. An external antenna must be connected with a 50Ω microstrip wire.

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7. Customization

For larger order quantities, it is possible to deliver modules with preprogrammed customer firmware. Depending on the quantity and user requirements, hardware customization to fit customer needs might be possible. Contact IDT's support team for requests regarding module customization.

8. Certification

8.1 European R&TTE Directive Statements

The ZWIR4512 module has been tested and found to comply with Annex IV of the R&TTE Directive 1999/5/EC and is subject to a notified body opinion. The module has been approved for antennas with gains of 4dBi or less.

8.2 Federal Communication Commission Certification Statements

8.2.1 Statements

This equipment has been tested and found to comply with the limits for a **Class B Digital Device**, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from where the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Modifications not expressly approved by IDT could void the user's authority to operate the equipment.

The internal/external antennas used for this mobile transmitter must provide a separation distance of at least 20cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

8.2.2 Requirements

The ZWIR4512 complies with Part 15 of the FCC rules and regulations. In order to retain compliance with the FCC certification requirements, the following conditions must be met:

Modules must be installed by original equipment manufacturers (OEM) only.

The module must only be operated with antennas adhering to the requirements defined in section 8.3.

The OEM must place a clearly visible text label on the outside of the end-product containing the text shown in Figure 8.1.

IMPORTANT: The compliance statement as shown in Figure 8.1 must be used without modifications for both ZWIR4512 product versions as the FCC ID covers the ZWIR4512AC1 and the ZWIR4512AC2!

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Figure 8.1 FCC Compliance Statement to be Printed on Equipment Incorporating ZWIR4512 Devices

Contains FCC ID: COR-ZWIR4512AC1

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

8.3 Supported Antennas

The FCC compliance testing of the ZWIR4512 has been carried out using the MEXE902RPSM antenna from PCTEL Inc. This antenna has an omnidirectional radiation pattern at an antenna gain of 2dBi. In order to be allowed to use the module without re-certification, the product incorporating the ZWIR4512 module must either use the antenna mentioned above or must use an antenna with an omnidirectional radiation pattern and a gain less than or equal to 2dBi.

9. Related Third-Party Documents

Visit the ZWIR4512 product page www.IDT.com/ZWIR4512 for IDT's related documents.

The following related documents are available from third-parties:

Document	Related Website
STM32F103xC Data Sheet	*www.st.com*
STM32F103xx Reference Manual	*www.st.com*

10. Glossary

Term	Description
6LoWPAN	IPv6 over Low Power Wireless Personal Area Networks
ADC	Analog-to-Digital Converter
API	Application Programming Interface
CI	Command Interface
DAC	Digital-to-Analog Converter
GPIO	General Purpose Input/Output
IPv6	Internet Protocol Version 6
JTAG	Joint Test Access Group
MCU	Microcontroller (STM32F103RC)
OTAU	Over-the-Air Update
PCB	Printed Circuit Board
PWM	Pulse-Width Modulation
SWD	Serial Wire Debug
TRX	Transceiver (ZWIR4502)

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11. Package Outline Drawings

11.1 ZWIR4512AC1

The package outline drawings for the ZWIR4512AC1 parts are appended at the end of this document. The package information is the most current data available.

11.2 ZWIR4512AC2

The package outline drawings for the ZWIR4512AC2 parts are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

https://www.idt.com/document/psc/zwir4512-package-outline-drawing-149-x-229-x-365-mm-body-20mm-pitch-mod0

12. Soldering Information

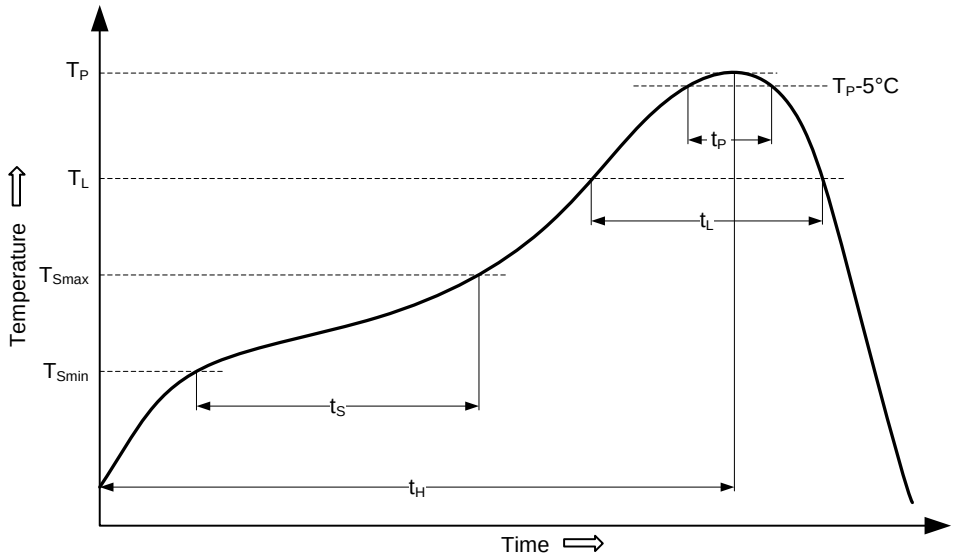
To ensure that soldered connections do not break during the reflow soldering process of the application PCB, the soldering profile described in Table 12.1 and Figure 12.1 must be maintained. This profile is aligned with the profile defined in the IPC/JEDEC standard J-STD-020D.

Table 12.1 Soldering Profile Parameters (according to J-STD-020D)

Profile Feature	Symbol	Min	Max	Unit
Time 25°C to T_P	t_H		8	min
Peak package body temperature	T_P		260	°C
Preheat / Soak				
Soak temperature	T_S	100	150	°C
Soak time	t_S	60	120	s
Ramp-up				
Ramp-up rate	T_L to T_P		3	°C/s
Time maintained above T_L	t_L		150	s
Time within 5°C of T_P	t_P		30	s
Ramp-down				
Ramp-down rate	T_P to T_L		6	°C/s

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Figure 12.1 Recommended Temperature Profile for Reflow Soldering (according to J-STD-020D)



13. Marking Diagram

13.1 ZWIR4512AC1 Package Marking Diagram



Line 1 is the part number

Line 2 is the device MAC address

Line 3 is the device MAC address

13.2 ZWIR4512AC2 Package Marking Diagram



Line 1 is the part number

Line 2 is the device MAC address

Line 3 is the device MAC address

14. Ordering Information

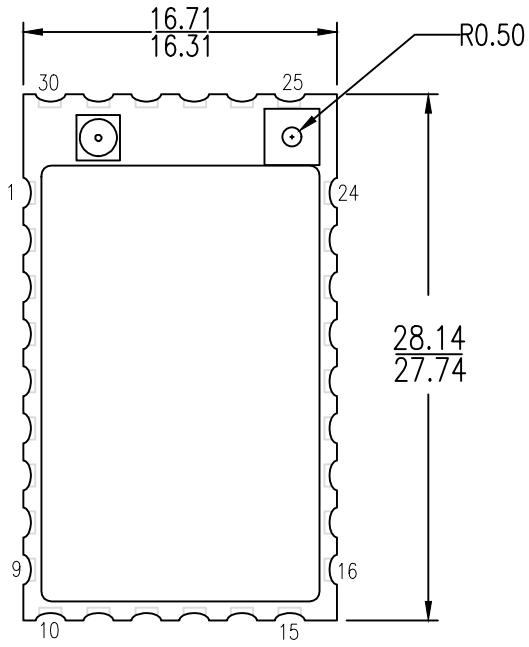
Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
ZWIR4512AC1RA	30 pin SMT, 27.9 mm x 16.5 mm, unprogrammed module for user application programs	MSL 3	Reel of 500	-40°C to +85°C
ZWIR4512AC1WA	30 pin SMT, 27.9 mm x 16.5 mm, unprogrammed module for user application programs	MSL 3	Reel of 100	-40°C to +85°C
ZWIR4512AC1RI	30 pin SMT, 27.9 mm x 16.5 mm, preprogrammed module with serial command interface	MSL 3	Reel of 500	-40°C to +85°C
ZWIR4512AC1WI	30 pin SMT, 27.9 mm x 16.5 mm, preprogrammed module with serial command interface	MSL 3	Reel of 100	-40°C to +85°C
ZWIR4512AC1RC	30 pin SMT, 27.9 mm x 16.5 mm, custom program module	MSL 3	Reel of 500	-40°C to +85°C
ZWIR4512AC1WC	30 pin SMT, 27.9 mm x 16.5 mm, custom program module	MSL 3	Reel of 100	-40°C to +85°C
ZWIR4512AC2RA	32 pin LGA, 23.1 mm x 15.1 mm, unprogrammed module for user application programs	MSL 3	Reel of 500	-40°C to +85°C
ZWIR4512AC2WA	32 pin LGA, 23.1 mm x 15.1 mm, unprogrammed module for user application programs	MSL 3	Reel of 100	-40°C to +85°C
ZWIR4512AC2RI	32 pin LGA, 23.1 mm x 15.1 mm, preprogrammed module with serial command interface	MSL 3	Reel of 500	-40°C to +85°C
ZWIR4512AC2WI	32 pin LGA, 23.1 mm x 15.1 mm, preprogrammed module with serial command interface	MSL 3	Reel of 100	-40°C to +85°C
ZWIR4512DEVKITV2	ZWIR4512 Development Kit , includes 3 development boards, 3 antennas, 3 USB cables, 3 battery cables, 2 batteries			

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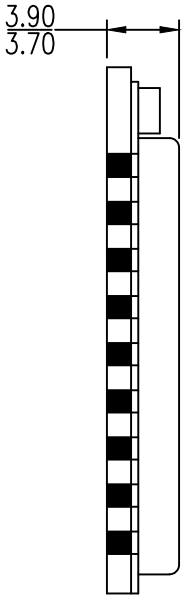
15. Revision History

Revision	Date	Description
	November 29, 2018	▪ Update for IDT template. ▪ Update for package drawings. ▪ Minor edits. ▪ Update for ordering codes.
	January 25, 2016	Changed to IDT branding. Revision reference is now the revision date.
1.30	September 7, 2015	▪ Updated module dimensions. ▪ Fixed interchanged timer channels in remap function C. ▪ Update for contact information and “Related Documents” section.
1.20	July 28, 2014	▪ Updated power consumption figures with values for low-power enabled network stack. ▪ New images, reflecting network stack changes. ▪ Update for cover images and contacts. Conversion to US letter format.
1.10	January 24, 2014	▪ Correction for interchanged USB and CAN pins in GPIO functional overview table. ▪ Correction for interchanged pins in GPIO remapping table (Table 2.2).
1.00	April 15, 2013	First release of document.

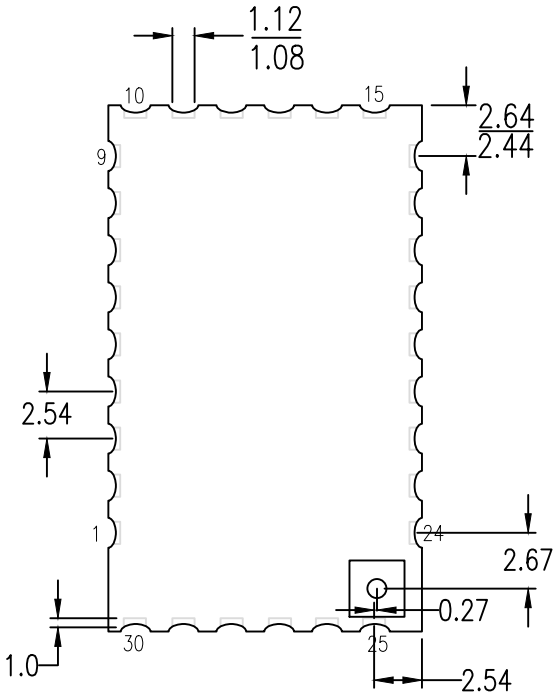
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TOP VIEW

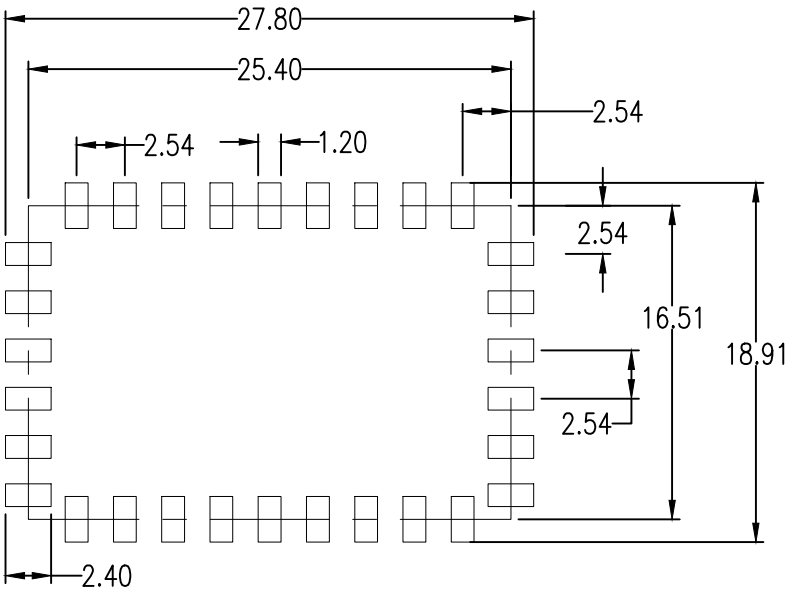


SIDE VIEW



BOTTOM VIEW

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RECOMMENDED LAND PATTERN

NOTES:
1. ALL DIMENSIONS ARE IN MM
2. TOP DOWN VIEW AS VIEWED ON PCB

Package Revision History		
Date Created	Rev No.	Description
Oct 31, 2018	Rev 00	Initial Release