ZSSC3154

Automotive Sensor Signal Conditioner with Dual Analog Output

The ZSSC3154 is an integrated circuit for highly accurate amplification and sensor-specific correction of a bridge sensor signal. Up to two temperature sensors can also be read in parallel.

The circuitry provides different configurations of the analog outputs to show two measurement results simultaneously. This also allows generating a complementary bridge sensor signal, which is often a requirement in safety-relevant applications.

The ZSSC3154 can measure and process two external temperature sensors to compensate the temperature drift of the bridge sensor signal and to output a separate temperature signal.

An integrated calibration microcontroller with an on-chip EEPROM performs the digital compensation of the sensor offset, the sensitivity, the temperature drift, and the nonlinearity of a sensor signal.

The single-pass, digital end-of-line calibration combined with the integrated broken-chip detection supports automatic and highly efficient mass production.

Features

- Differential bridge sensor input
- Half-bridge sensor or temperature sensor input
- Digital compensation of offset, gain, nonlinearity, and temperature dependency
- Two analog outputs; behavior programmable by EEPROM configuration
- Sequential analog output mode provides two measurement values at one output pin
- On-chip diagnostic and safety features including sensor connection diagnostic and broken-chip detection
- 2 EEPROM words for arbitrary user data
- Multiple configurable output options

Benefits

- Bridge sensor signal validation for safety applications via two antivalent analog outputs or via half-bridge sensor measurement output
- Simultaneous measurement of sensor signals, including temperature signal for compensation and for temperature output
- Efficient use of non-calibrated elements for bridge sensors and temperature sensors without external trimming components
- Single-pass end-of-line calibration algorithm minimizes production costs
- Excellent EMC/ESD robustness and AEC-Q100 qualification

Available Support

- Evaluation Kit
- Application Notes
- Calculation Tools

Physical Characteristics

- Supply voltage: 4.5 to 5.5V
- Maximum supply voltage: 7.7V
- Input span: 1.8 to 267mV/V
- ADC resolution: 14 bit
- Output resolution: > 12 bit from 10% to 90%
- Operating temperature range: -40°C to 150°C
- Package: QFN32 (5x5mm; wettable flank) or die

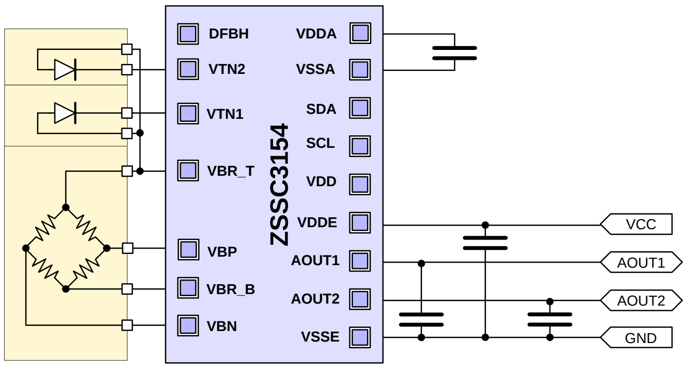

Figure 1. Basic Circuit

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1. Overview

1.1 Block Diagram

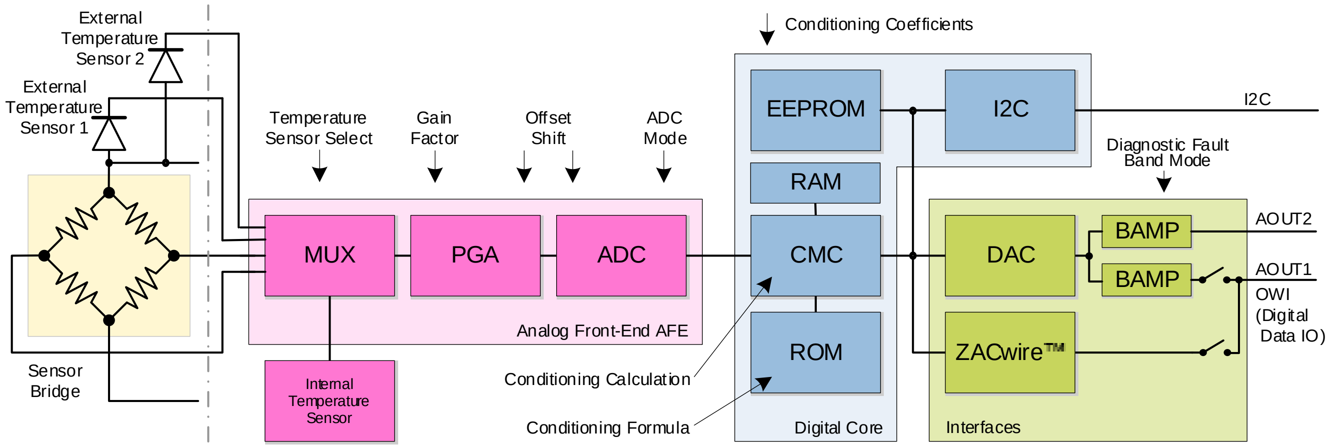


Figure 2. ZSSC3154 Block Diagram

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. The ZSSC3154 might not function or be operable above the recommended operating conditions. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. Renesas does not recommend designing to the “Absolute Maximum Ratings.”

Parameters apply in operating temperature range and without time limitations.

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min	Max	Unit
Supply voltage [1]	VDDE	To VSSE	-0.3	7.7	V
Voltage at pins AOUT1 and AOUT2 [1]	V_{AOUT1}, V_{AOUT2}	To VSSE	-0.3	7.7	V
Analog supply voltage [1]	VDDA	To VSSA	-0.3	6.5	V
Digital supply voltage [1]	VDD	To VSSA	-0.3	6.5	V
Voltage at all analog and digital pins [1]	V_{AIO}, V_{DIO}	To VSSA	-0.3	VDDA +0.3	V
Storage temperature	T_{STG}		-55	150	°C

1. Refer to ZSSC3154 Application Note – Power Management for a description of the protection features.

2.2 Operating Conditions

Table 2. Operating Conditions

Parameter	Symbol	Conditions	Min	Nominal	Max	Unit
Supply voltage [1]	VDDE	To VSSE	4.5	5	5.5	V
Power-On-Reset threshold	POR_off	VDDA to VSSA	3.3		4.1	V
Ambient temperature	T_{AMB}	EEPROM programming cycles specification depends on temperature (refer to section Table 4)	-40		125	°C
Extended ambient temperature – part number ZSSC3154BE3R only	T_{AMB_E}		-40		150	°C

Parameter	Symbol	Conditions	Min	Nominal	Max	Unit
Bridge resistance [2, 3]	RBR		1		10	kΩ

1. Refer to ZSSC3154 Application Note – Power Management for detailed specifications.
2. Symmetric behavior and identical electrical properties (especially the low pass characteristic) of both sensor inputs are required. Unsymmetrical conditions of the sensor and/or external components connected to the sensor input pins can generate a failure in signal operation.
3. No measurement in mass production; parameter is guaranteed by design and/or quality observation.

2.3 Electrical Parameters

All parameter values are valid under the operating conditions specified in section 2.2 (except as noted) and with the oscillator frequency within the specified range (fOSC). All voltages are referenced to VSSA.

Note: See important notes at the end of Table 3..

Table 3. Electrical Parameters

Parameter	Symbol	Conditions	Min	Nominal	Max	Unit
Supply Current and System Operation Conditions						
Supply current	I_S	Excluding bridge supply current and excluding output current at pins AOUT1 and AOUT2; oscillator adjusted (typical f_{OSC} = 2.6MHz)			10	mA
Supply voltage sensor bridge (internally at VDDA and VSSA)	V_{VBR}	$V_{VBR} = V_{VBR\_T} - V_{VBR\_B}$ $R_{BR} \geq 1k\Omega$ (see Table 2) V_{VBR_T} is the voltage at the VBR_T pin and V_{VBR_B} is the voltage at VBR_B pin	VDDA – 0.3V		VDDA	
Oscillator Frequency [1]	f_{OSC}	Guaranteed adjustment range (see the ZSSC3154 Application Note–Oscillator Frequency Adjustment)	2.6	2.9	3.2	MHz
Analog Front-End Characteristics						
Input span	V_{IN_SPAN}	Analog gain: 2.8 to 420; EMC robust for $V_{IN\_SPAN} \geq$ 6mV/V	1		267	mV/V
Analog offset compensation range	OC	Depends on gain adjustment (refer to section 3.8.2)			3.88	VIN_SPAN
Parasitic differential input offset current [1]	$I_{IN\_OFF\_85°C}$	-25°C to 85°C ambient	-4		4	nA
	$I_{IN\_OFF\_125°C}$	-40°C to 125°C ambient	-10		+10	nA
	$I_{IN\_OFF\_150°C}$	-40°C to 150°C ambient Part number ZSSC3154BE3R only	-20		+20	nA
Common mode input range	V_{IN_CM}	Depends on gain adjustment; XZC off (refer to section 3.8.1); V_{VBR} according to "Supply Current and System Operation Conditions" settings	0.29		0.65	VVBR
Input capacitance	C_{IN}	Capacitance at pins VBP and VBN to VSSA		10	12	nF

Parameter	Symbol	Conditions	Min	Nominal	Max	Unit
Temperature Measurement (Refer to section 3.4.3)						
Internal temperature diode sensitivity	ST_{TSI}	Raw values, without conditioning calculation	26		38	LSB14 /K
External temperature diode channel gain	A_{TSED}	Sensor at pins VTN1 or VTN2	-18		-12	LSB14 /mV
External temperature diode bias current	I_{TSED}	Sensor at pins VTN1 or VTN2	10	20	40	µA
External temperature diode input range [1]	V_{TSED}	Related to V_{VBR_T} which is the voltage at the VBR_T pin; sensor at pins VTN1 or VTN2	0.2		1.0	V
External temperature resistor channel gain	A_{TSER}	At VDDE = 5V; sensor at pins VTN1 or VTN2	-13		-9	LSB14 /mV
External temperature resistor input range [1]	V_{TSER}	Related to V_{VBR_T} which is the voltage at the VBR_T pin; sensor at pins VTN1 or VTN2	0.3		1.4	V
Sensor Diagnostic Tasks						
Sensor connection loss detection threshold	R_{SCC_TH}		20		100	kΩ
Maximum input capacitance for sensor connection check with sensor aging check enabled	$C_{IN\_SCC/SAC}$			1	1.2	nF
Maximum input capacitance for sensor connection check with sensor short check enabled	$C_{IN\_SCC/SSC}$	If input capacitance is greater than 1nF the sensor connection check high-capacitor mode must be enabled.		10	12	nF
Sensor input short detection threshold	R_{SSC_TH}		50		800	Ω
A/D Conversion (Refer to section 3.8.3)						
ADC resolution [1]	r_{ADC}				14	Bit
DNL [1]	DNL_{ADC}	f_{OSC} = 2.6MHz; best fit; complete AFE; V_{ADC_IN} according to “A/D Conversion” settings			0.95	LSB
INL	INL_{ADC}	f_{OSC} = 2.6MHz; best fit; complete AFE; V_{ADC_IN} according to “A/D Conversion” settings		3	8	LSB
ADC input range	V_{ADC_IN}	V_{VBR} according to “Supply Current and System Operation Conditions” settings.	0.1		0.9	VVBR
D/A Conversion and Analog Outputs (Pins AOUT1 and AOUT2)						
DAC resolution	r_{DAC}	Analog output; V_{OUT} = 10% to 90% of V_{DAC}; $V_{DAC} = V_{VDDE}-V_{VSSE}$		12		Bit
Output current sink and source	$I_{OUT\_SRC/SINK}$	Analog output; V_{OUT} = 10% to 90% of V_{DAC}; $V_{DAC} = V_{VDDE}-V_{VSSE}$			1.3	mA
Short circuit current	I_{OUT_SHORT}	AOUT1 or AOUT2 to VDDE/VSSE	-25		25	mA

Parameter	Symbol	Conditions	Min	Nominal	Max	Unit
Output signal range	V_{OUT_RANGE}	Ratiometric to $V_{DAC} = V_{VDDE}-V_{VSSE}$	0.046		0.954	VDAC
Output slew rate [1]	SR_{OUT}	$C_{LOAD} \leq 60nF$	0.1			V/µs
Output resistance in diagnostic mode	R_{OUT_DIAG}	Diagnostic fault band: V_{DFBL} < 4% of V_{DAC} if the DFBH pin is unconnected; V_{DFBH} > 96% of V_{DAC} if the DFBH pin is connected to VSSA; V_{DFBL} is the low diagnostic level and V_{DFBH} is the high diagnostic level for indicating faults			150	Ω
Load capacitance [1]	C_{LOAD}	C3 + C_{LOAD_AOUT1} and C4 + C_{LOAD_AOUT2} (refer to section 4)			60	nF
DNL	DNL_{OUT}		-0.95		0.95	LSB
INL	INL_{OUT}	Best fit, r_{DAC} = 12-Bit -40°C ≤ T_{AMB} ≤ 125°C	-8		8	LSB
INL (Part number ZSSC3154BExxx only)	$INL_{OUT\_150°C}$	Best fit, r_{DAC} = 12-Bit 125°C < T_{AMB} ≤ 150°C	-12		12	LSB
Output leakage current at 125°C	I_{OUT_LEAK}	In case of power or ground loss	-25		25	µA
Output leakage current at 150°C	$I_{OUT\_LEAK\_150°C}$	In case of power or ground loss	-40		40	µA
Internal pull-up current at pin DFBH to VDDA [1]	I_{DFBH_PULLUP}	For diagnostic output LOW at AOUT1 and AOUT2, do not connect the DFBH pin. For diagnostic output HIGH at AOUT1 and AOUT2, connect the DFBH pin to VSSA.		50		µA
System Response						
Startup time [1]	$t_{STARTUP}$	Time to first valid output after power-on; f_{OSC} = 2.6MHz; ROM check disabled			20	ms
Output Update Rate [1, 4]	OUR	HB Measurement disabled			0.4	ms
	OUR_{HB}	HB Measurement enabled			0.6	
Response time [1, 4]	$t_{RESPONSE}$	100% input step, HB disabled			0.8	ms
	t_{RESP_HB}	100% input step, HB enabled			1.2	
Bandwidth [1, 4]		In comparison to analog sensor signal conditioners		1		kHz
Failure Messaging Time [4]	FMT	HB disabled			10.4	ms
	FMT_{HB}	HB enabled			8.6	
Ratiometricity error	RE	Maximum error for VDDE = 5V to 4.5V or to 5.5V			1000	ppm
Overall failure [2] AFE + ADC	$F_{ALL\_85°C}$	-20°C to 85°C		0.5		% FSO [3]
	$F_{ALL\_125°C}$	T_{AMB} = -40°C to 125°C		1.0		% FSO

Parameter	Symbol	Conditions	Min	Nominal	Max	Unit
Deviation from ideal line including INL, gain, offset, and temperature impacts; no sensor caused effects. f_{OSC} = 2.6MHz, XZC off, related to digital value	$F_{ALL\_150°C}$	-40°C to 150°C Part number ZSSC3154BE3R only.		1.25		% FSO

1. No measurement in mass production, parameter is guaranteed by design and/or quality observation.
2. If XZC is active, an additional overall failure of maximum 25ppm/K for XZC = 31. Failure decreases linearly for XZC < 31.
3. FSO = Full Scale Output.
4. f_{OSC} = 2.6MHz, ADC MSB resolution=7bit, ADCSLOW=disabled, refer ZSSC3154_Timing_Calculation Sheet [TC] for timing calculation

2.4 Interface Characteristics and EEPROM

Table 4. Interface Characteristics and EEPROM

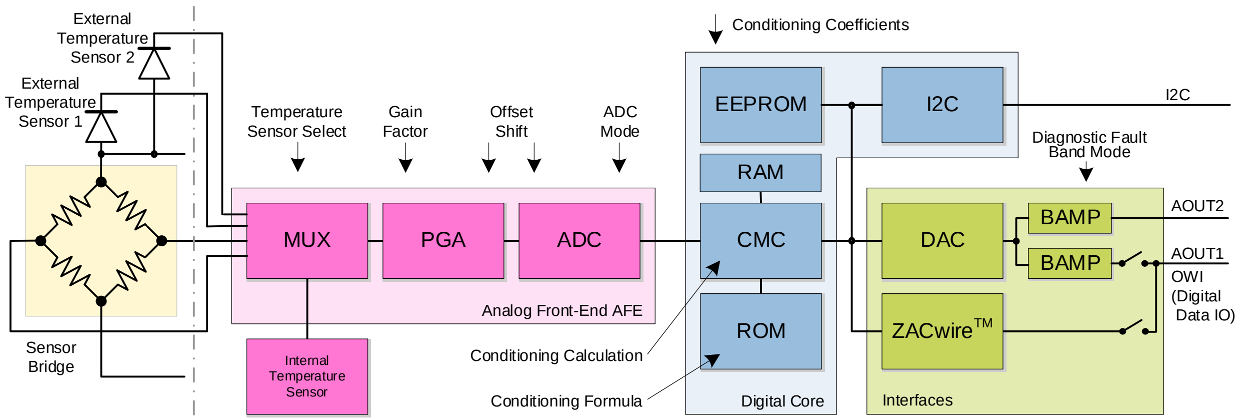
Parameter	Symbol	Conditions	Min	Nominal	Max	Unit
I2C Interface (Refer to ZSSC3154 Functional Description for timing details.)						
I2C™ voltage level HIGH [11]	V_{I2C_HIGH}		0.8			VDDA
I2C™ voltage level LOW 1	V_{I2C_LOW}				0.2	VDDA
Slave output level LOW [1]	$V_{I2C\_LOW\_OUT}$	Open drain, I_{OL} < 2mA			0.15	VDDA
SDA load capacitance [1]	C_{I2C_SDA}				400	pF
SCL clock frequency [1]	f_{I2C}	f_{OSC} ≥ 2MHz			400	kHz
Internal pull-up resistor [1]	R_{I2C_PULLUP}		25		100	kΩ
ZACwire™ One Wire Interface (OWI at pin AOUT1)						
OWI voltage level HIGH [1]	$V_{OWI\_IN\_H}$		0.8			VDDA
OWI voltage level LOW [11]	$V_{OWI\_IN\_L}$				0.2	VDDA
Slave output level LOW [11]	$V_{OWI\_OUT\_L}$	Open drain, I_{OL} < 4mA			0.15	VDDA
Start window [11]	$t_{OWI\_STARTWIN}$	f_{OSC} = Nominal			30	ms
EEPROM						
Ambient temperature for EEPROM programming	T_{AMB_EEP}		-40		125	°C
Write cycles [11]	$n_{EEP\_WRI\_85°C}$	T_{AMB_EEP} ≤ 85°C			1000	
	$n_{EEP\_WRI\_125°C}$	T_{AMB_EEP} ≤ 125°C			100	
Read cycles [1, 2, 3]	n_{EEP_READ}	T_{AMB} ≤ 150°C			8×10^8	
Data retention [1]	$t_{EEP\_RETENTION}$	Temperature Profile: [4] 100000h at 55°C 30000h at 125°C 3000h at 150°C			15	a
Programming time [1]	t_{EEP_WRI}	Per written word		12		ms

1. No measurement in mass production; parameter is guaranteed by design and/or quality observation.
2. Valid for the dice. Note: additional package and temperature range causes restrictions.
3. Specification is valid for conditions when EEPROM reading only occurs during the start-up phase in Normal Operation Mode.
4. Over lifetime and valid for the dice. Use the Renesas Temperature Profile Calculation Sheet for temperature stress calculation. Note that the package causes additional restrictions.

3. Circuit Description

3.1 Signal Flow

The ZSSC3154 signal path consists of the analog front-end (AFE), the digital signal processing unit, two analog output stages, the one-wire interface (OWI) and an overvoltage protection circuitry. Based on a differential structure, the bridge inputs VBP and VBN are handled by two signal lines, each with a dynamic range symmetrical to the common mode potential (analog ground equal to VDDA/2). Therefore, it is possible to amplify positive and negative input signals within the common mode range of the signal input. The input signals are selected by the input multiplexer.



PGA	Programmable Gain Amplifier
MUX	Multiplexer
ADC	Analog-to-Digital Converter
CMC	Calibration Microcontroller
ROM	Read-Only Memory for Correction Formula and Algorithm
RAM	Volatile Memory for Configuration and Conditioning Coefficients
EEPROM	Non-volatile Memory for Configuration and Conditioning Coefficients
DAC	Digital-to-Analog Converter
BAMP	Output Buffer Amplifier
I2C	I2C Digital Interface
ZACwire™	Digital One-Wire Interface

Figure 3. Block Diagram of the ZSSC3154

The multiplexer (MUX) transmits the signals from either the bridge sensor or from the selected temperature sensor to the analog-to-digital converter (ADC) in a defined sequence. The temperature sensors can either be external diodes, external thermistors (RTD), or an internal diode selected by EEPROM configuration. The differential signal from the bridge sensors is pre-amplified by the programmable gain amplifier (PGA). The ADC converts these signals into digital values.

The digital signal correction is processed in the calibration microcontroller (CMC) using a ROM-resident correction formula and sensor-specific coefficients stored in the EEPROM during calibration. The configuration data and the correction parameters can be programmed into the EEPROM by digital one-wire communication at the main output pin or by digital communication via the I2C™ interface. During the calibration procedure the digital interface can provide measurement values as well.

The conditioned bridge sensor signal is always output as a continuous analog signal at the main output pin. Depending on the programmed configuration, there are several output modes for the second analog output pin; e.g., output the inverse bridge sensor signal, output the conditioned temperature signal, or output the half-bridge sensor signal.

3.2 Application Modes

For each application, a configuration set must be established by programming the on-chip EEPROM for the following modes:

- Sensor channel
  - Input range: Select the gain adjustment of the analog front-end (AFE) with respect to the maximum sensor signal span and the zero point of the A/D conversion.
  - Analog sensor offset compensation (XZC): If required, this compensates large sensor offsets; e.g., if the sensor offset voltage is near to or larger than the sensor span.
  - Resolution/response time: Configure the A/D converter resolution. These settings influence the sampling rate and the signal integration time, and therefore the noise immunity.
- Temperature
  - Temperature measurement for the calibration: Select the internal or external temperature sensor for the compensation of temperature-related bridge sensor signal deviations.
  - Temperature measurement for the temperature output: Select the internal or external temperature sensor for the temperature measurement.
- Output
  - Output signals: Assign the measured and conditioned signals to the second analog output; e.g., inverse bridge sensor signal, temperature signal, or half-bridge sensor signal.
  - Output mode: Select the output mode for the second analog output; e.g., continuous signal or sequential analog output.

3.3 System Control

3.3.1 Main System Tasks

The calibration microcontroller (CMC) is the central system control unit and supports the following tasks and features:

- Manage the startup sequence
- Control the measurement cycle regarding to the EEPROM-stored configuration data
- Process the signal conditioning calculation (16-bit calculation for the measured signals using the ROM-resident signal conditioning formulas and the EEPROM-stored conditioning coefficients)
- Assign the conditioned output values to the analog outputs and control the output behavior
- Process the communication requests received via the digital interfaces
- Perform failsafe tasks and indicate detected errors by setting analog outputs to the diagnostic fault band

3.3.2 General Working Modes

The ZSSC3154 supports three different working modes:

- Normal Operation Mode (NOM) – for continuous processing of the signal conditioning
- Command Mode (CM) – for configuration and calibration and for access to all internal registers
- Diagnostic Mode (DM) – for failure messages

3.4 Normal Operation Mode

A configured and calibrated ZSSC3154 starts the Normal Operation Mode (NOM) immediately after power-on if there is no communication request within a startup window (refer to the ZSSC3154 Functional Description for details). It consists of a startup phase, the measurement cycle, the conditioning calculation, and the analog output for the sensor signals.

3.4.1 Startup Phase

After power-on, the startup phase is processed, which includes

- Settling of the internal supply voltages including the reset of the circuitry
- System start and configuration, EEPROM readout, and signature check
- ROM check, if enabled
- Processing the measurement cycle start routine including all measurements to provide the configured output signals
- One-wire communication window

If an error is detected during the startup phase, the Diagnostic Mode (DM) is activated and the analog output at the AOUT1 and AOUT2 pins remains in the diagnostic fault band range.

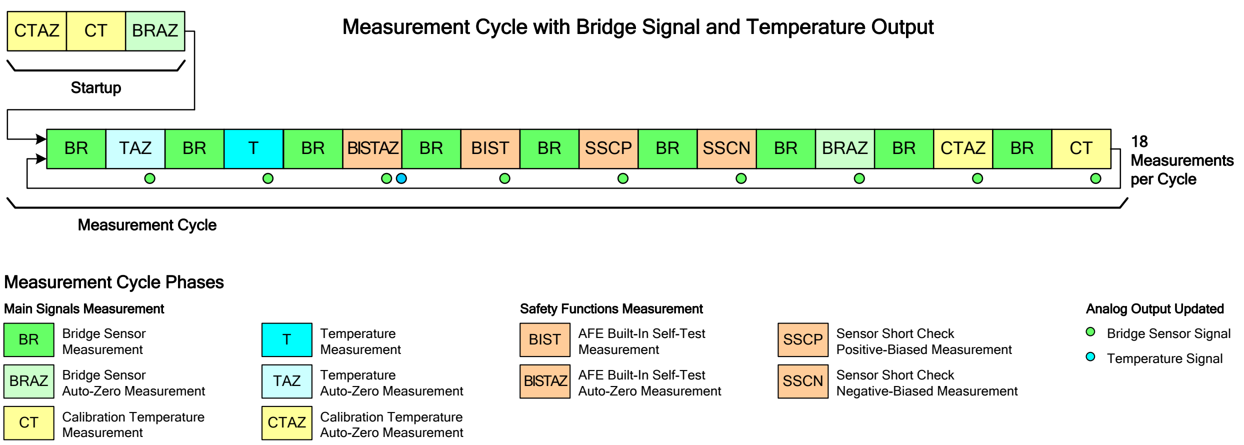
After the startup phase, the continuously running measurement and sensor signal conditioning cycle is started, and the analog or digital output of the conditioned sensor signals is activated.

3.4.2 Measurement Cycle

The measurement cycle is controlled by the CMC. Depending on EEPROM settings, the multiplexer (MUX) selects the following input signals in a defined sequence:

- Differential bridge sensor signal
- Conditioning temperature for bridge sensor signal conditioning calculation
- Temperature sensor signal
- Single-ended half-bridge sensor signal measured against an internal reference voltage
- Internal offset of the analog front end (auto-zero compensation)
- Diagnostic signals

The cycle diagram in Figure 4 shows the basic structure of the measurement cycle. After power-on, the startup routine is processed, which performs all required measurements to expedite acquiring an initial valid conditioned sensor output. After the startup routine, the normal measurement cycle runs.



(For detailed descriptions of various cycle configurations, refer to the ZSSC3154 Functional Description.)

Figure 4. Example of Measurement Cycle with Bridge Sensor Signal and Temperature Measurement

3.4.3 Conditioning Calculation

The digitalized value for the bridge signal and, if selected, for the temperature or the half-bridge signal are processed with the conditioning formulas to remove offset and temperature dependency and to compensate nonlinearity. The result is a non-negative 15-bit value in the range [0; 1).

3.5 Bridge Sensor Measurement

The ZSSC3154's main task is measuring a differential bridge sensor signal. The signal path is ratiometric and fully differential. The ratiometric reference voltage V_{REF} is equal ($V_{BR\_T} – V_{BR\_B}$). The internal offset of the analog front-end is eliminated by an auto-zero compensation.

The bridge sensor signal value is processed by a conditioning calculation to correct the temperature-dependent gain and to compensate the temperature-dependent offset and the nonlinearity up to 3rd order. The conditioning coefficients are stored in the EEPROM. For a detailed description of the bridge signal conditioning formula refer to the ZSSC3154 Functional Description.

3.6 Temperature Measurement

The ZSSC3154 supports different methods for acquiring temperature data needed for the conditioning of the sensor signal as well as for a separate temperature measurement:

- an internal pn-junction temperature sensor,
- an external pn-junction temperature sensor connected to the sensor top potential (pin VBR_T), or
- an external resistive half-bridge temperature sensor connected at the top with 1:10 resistance ratio.

Recommend resistive sensors are Pt1000, Pt10000, and Cu or Ni based positive-temperature-coefficient resistive temperature devices (PTC RTDs); e.g., KTY series.

The internal offset of the analog-front end is eliminated by an auto-zero compensation.

The temperature value is processed by a conditioning calculation to correct the gain and to compensate the offset and the 2nd order nonlinearity. The conditioning coefficients are stored in the EEPROM. For a detailed description of the temperature conditioning formula, refer to the ZSSC3154 Functional Description.

3.7 Half-Bridge Sensor Measurement

The ZSSC3154 supports measuring a half-bridge sensor signal referenced to an internal reference potential. The signal path is ratiometric and fully differential. The ratiometric reference voltage V_{REF} is equal (V_{VBR_T} - V_{VBR_B}).

The half-bridge sensor signal value is processed by a conditioning calculation to correct the temperature-dependent gain and to compensate the temperature-dependent offset and the 2nd order nonlinearity. The conditioning coefficients are stored in the EEPROM. For a detailed description of the half-bridge signal conditioning formula, refer to the ZSSC3154 Functional Description.

3.8 Analog Front End

The analog front-end (AFE) consists of the multiplexer (MUX), the programmable gain amplifier (PGA), and the analog-to-digital converter (ADC).

3.8.1 Programmable Gain Amplifier

Table 5 shows the adjustable gains, the corresponding sensor signal input spans, and the common mode range limits.

Table 5. Adjustable Gains and Resulting Sensor Signal Spans and Common Mode Ranges

PGA Gain a_{IN}	Maximum Input Span V_{IN_SPAN} [mV/V] [1]	Input Common Mode Range V_{IN_CM} [% VDDA] [2]	
		XZC = Off	XZC = On
420	1.8	29 to 65	45 to 55
280	2.7	29 to 65	45 to 55

PGA Gain a_{IN}	Maximum Input Span V_{IN_SPAN} [mV/V] [1]	Input Common Mode Range V_{IN_CM} [% VDDA] [2]	
		XZC = Off	XZC = On
210	3.6	29 to 65	45 to 55
140	5.4	29 to 65	45 to 55
105	7.1	29 to 65	45 to 55
70	10.7	29 to 65	45 to 55
52.5	14.3	29 to 65	45 to 55
35	21.4	29 to 65	45 to 55
26.3	28.5	29 to 65	45 to 55
14	53.75	29 to 65	45 to 55
9.3	80	29 to 65	45 to 55
7	107	29 to 65	45 to 55
2.8	267	32 to 57	Not applicable

1. Recommended maximum internal signal range is 80% of supply voltage.
   Span is calculated by the following formula: $V_{IN\_SPAN} = 0.8\ (V_{VBR\_T} - V_{VBR\_B}) / a_{IN}$.
2. Refer to section 3.8.2 for an explanation of the analog offset compensation.

Recommendation: To achieve the best stability and linearity performance of the AFE, operate the PGA in a voltage range within 10% to 90% of the ratiometric reference voltage $V_{REF} = (V_{VBR\_T} - V_{VBR\_B})$. The gain must be selected to guarantee this constraint for the entire operating temperature range of the application and for the specified sensor bridge tolerances.

3.8.2 Offset Compensation

The ZSSC3154 supports two methods for sensor offset compensation:

- Digital offset correction is processed during the signal conditioning calculation by the calibration micro-controller (CMC).
- Extended analog offset compensation (XZC) is achieved by adding a compensation voltage into the analog signal path. This removes large offsets up to 300% of signal span and prevents overdriving the analog signal path.

Table 6. Extended Analog Offset Compensation Ranges (XZC)

PGA Gain a_{IN}	Maximum Input Span V_{IN_SPAN} [mV/V]	Offset Shift / XZC Step [% V_{IN_SPAN}]	Maximum Offset Shift [mV/V]	Maximum Offset Shift (XZC = ±31) [% V_{IN_SP}]
420	1.8	12.5	7.8	388
280	2.7	7.6	7.1	237
210	3.6	12.5	15.5	388
140	5.4	7.6	14.2	237
105	7.1	12.5	31	388
70	10.7	7.6	28	237
52.5	14.3	12.5	62	388
35	21.4	7.6	57	237
26.3	28.5	5.2	52	161
14	53.6	12.5	233	388
10	80	7.6	207	237
7	107	5.2	194	161
2.8	267	0.83	78	26

3.8.3 Analog-to-Digital Converter

The analog-to-digital converter is implemented using the full differential switched-capacitor technique. The A/D resolution is 14-bit. The ADC operates in the second order configuration. The conversion is largely insensitive to short-term and long-term instabilities of the clock frequency. The ADC must be configured for the following features:

- Adjustable A/D conversion time and integration phase length
- Adjustable A/D conversion input voltage range

Table 7. ADC Resolution versus Output Resolution and Sample Rate

ADC Resolution r_{ADC}	ADC Resolution Integration Phase	Bridge Sensor Signal Sample Rate f_{OSC} = Nominal	Averaged Bandwidth f_{OSC} = Nominal
14-bit	10-bit	0.60kHz	225Hz
	9-bit	1.13kHz	425Hz
	8-bit	2.03kHz	765Hz
	7-bit	2.54kHz	955Hz

3.9 Signal Outputs

3.9.1 Analog Output

ZSSC3154 provides two analog outputs at the AOUT1 and AOUT2 pins. The analog output behavior and the assignment of the several conditioned sensor signals to the analog outputs are configurable:

- Conditioned bridge sensor signal is always assigned to and continuously output at the AOUT1 pin.
- Conditioned temperature signal can be assigned to the analog output at the AOUT2 pin.
- Conditioned half-bridge signal can be assigned to the analog output at the AOUT2 pin.
- A function of the conditioned bridge sensor signal can be assigned to the analog output at the AOUT2 pin.
- A sequential analog output mode can be assigned to the analog output at the AOUT2 pin. The sequence of output signals includes the diagnostic fault band HIGH and LOW level, the conditioned temperature or the half-bridge signal, and a function of the conditioned bridge sensor signal (refer to section 3.9.2).
- Both analog outputs support low-pass filtering of the assigned conditioned sensor signals.
- Both analog outputs can support diagnostic procedures of the application by providing a power-on diagnostic output waveform.

For a detailed description of analog output modes and their configuration, refer to the ZSSC3154 Functional Description.

3.9.2 Sequential Analog Output

The sequential analog output mode allows the analog output of two conditioned sensor signals at the AOUT2 pin. The sequence of output signals includes both the low and high diagnostic fault band levels (DFB Low and DFB High, respectively) for synchronization and for a repeated verification of diagnostic levels. This is followed by output of the conditioned temperature or half-bridge signal to provide the second signal. The last transmission in the sequence is a function of the conditioned bridge sensor signal for verification of the analog output at the AOUT1 pin.

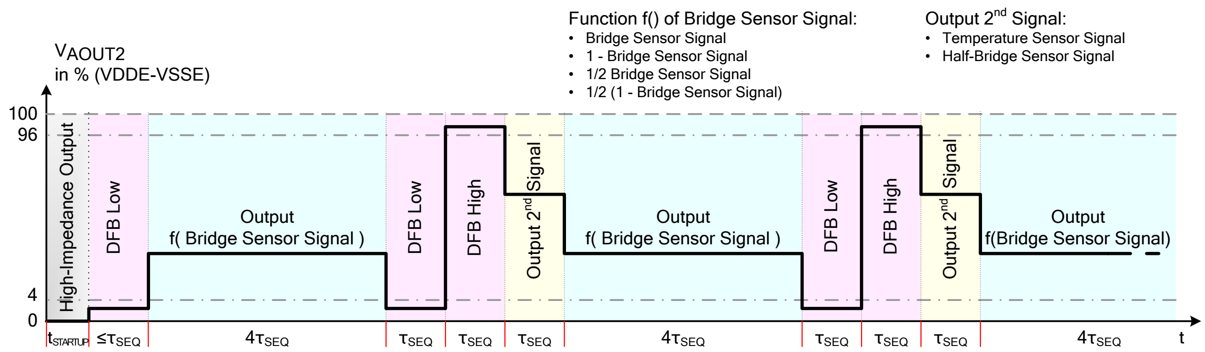


Figure 5. Sequential Analog Output—Example Sequence if the DFBH Pin is Unconnected

3.9.3 Digital Output

The ZSSC3154 contains a serial digital I2C interface that supports digital readout of the conditioned sensor signals with a resolution of 13 bits as described in section 3.10.

3.10 Serial Digital Interfaces

The ZSSC3154 contains both a serial digital I2C interface and a ZACwire™ interface for one-wire communication (OWI). The digital interfaces allow configuration and calibration of the sensor module. OWI communication can be used to perform an end-of-line calibration via the analog output pin AOUT1 of a completely assembled sensor module. The I2C interface provides the readout of the conditioned sensor signal data during normal operation mode.

For a detailed description of the digital serial interfaces and the communication protocols, refer to the ZSSC3154 Functional Description.

3.11 Failsafe Features

ZSSC3154 provides various failsafe tasks to control the proper function of the device and the connected sensors:

- Observation of sensors: bridge sensor aging, connection, and short check; temperature sensor check
- Observation of analog front-end (AFE): AFE built-in self-test; AFE overdrive control
- Observation of digital control unit: oscillator-fail detection; watchdog; arithmetic check
- Observation of memory content: EEPROM and ROM signatures, RAM and registers parity checks
- Observation of chip: supply power and ground loss, broken-chip check

For a detailed description of failsafe tasks and their configuration, refer to ZSSC3154 Functional Description.

When a failure is detected, the Diagnostic Mode (DM) is activated. The AOUT1 and AOUT2 analog outputs are set to the diagnostic fault band (DFB). The DFB output level must be selected by the wiring of the DFBH pin. If the DFBH pin is open, the outputs are switched to the diagnostic fault band level LOW. If the DFBH pin is connected to VSSA, the outputs are switched to the diagnostic fault band level HIGH. The selected DFB mode should match the connected load resistances at the analog outputs to reduce power loss if the diagnostic mode is activated.

3.12 Overvoltage and Short Circuit Protection

The ZSSC3154 is designed for a 5V (±10%) supply provided by an electronic control unit (ECU). Internal sub-assemblies are supplied and protected by integrated voltage regulators and limiters up to a supply voltage of 7.7V. The two analog output stages are protected by current limiters against short circuits to an external supply or ground. These functions are described in detail in ZSSC3154 Application Note – Power Management.

ZSSC3154 protection features are guaranteed without time limit when the device is operated in the application circuits shown in section 4.

4. Application Circuits and External Components

4.1 Application Circuit Examples

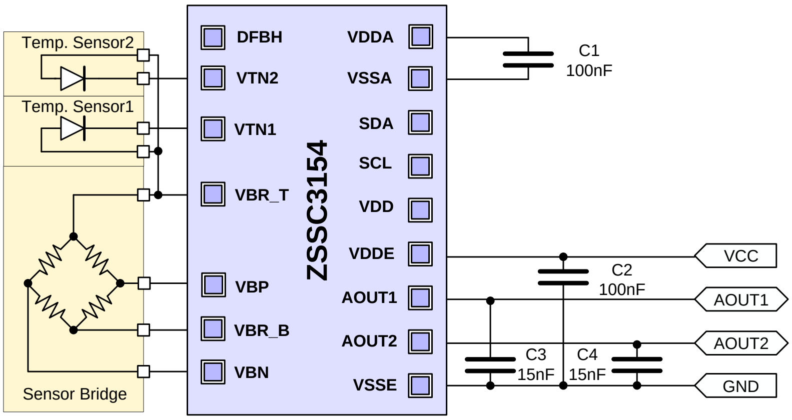


Figure 6. Application Circuit with Two Analog Outputs and Diagnostic Fault Band Level Low

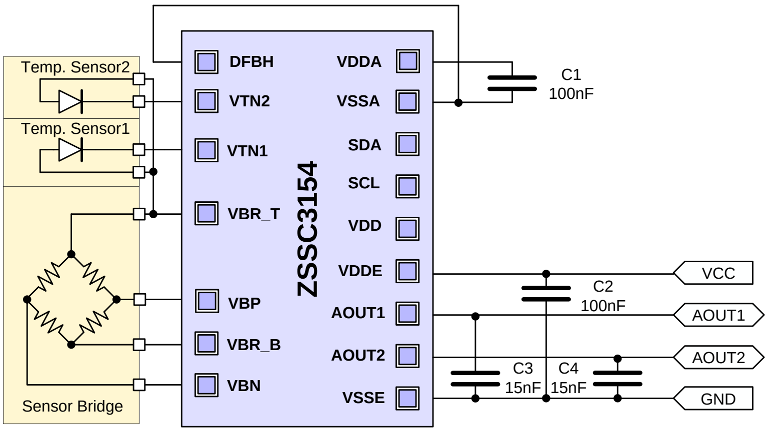


Figure 7. Application Circuit with Two Analog Outputs and Diagnostic Fault Band Level High

4.2 External Components

For the application circuit examples, refer to section 4.1.

Table 8. Dimensioning of External Components for the Application Examples

Component	Symbol	Condition	Min	Typical	Max	Unit
Capacitor	C1	$V_{max} \geq 10V$		100		nF
Capacitor	C2	$V_{max} \geq 16V$		100		nF
Capacitor	C3	$V_{max} \geq 16V$		15		nF
Capacitor	C4	$V_{max} \geq 16V$		15		nF

The capacitor values are examples and must be adapted to the requirements of the application, in particular to the EMC requirements.

5. ESD Protection and EMC Specification

All pins have an ESD protection of >2000V according to the Human Body Model (HBM). The VDDE, VSSE, AOUT1 and AOUT2 pins have an additional ESD protection of >4000V (HBM).

The level of ESD protection has been tested with devices in QFN32 5x5 packages during the product qualification. The ESD test follows the Human Body Model with 1.5kOhm/100pF based on MIL883, Method 3015.7.

The EMC performance regarding external disturbances as well as EMC emission is documented in the ZSSC3154 Application Note – Power Management.

6. Pin Configuration and Package

The ZSSC3154 is available in a QFN32 (5mm x 5mm) green package.

Table 9. Pin Configuration

Pin No Die	Pin No QFN32 5x5	Pin Name	Description	Notes
1	1	VDDA	Positive Analog Supply Voltage	Internal analog power supply
2	2	VSSA	Negative Analog Supply Voltage	Internal analog ground
3	3	SDA	I²C™ Clock	Analog input, internal pull-up
4	4	SCL	I²C™ Data I/O	Analog I/O, internal pull-up
6	5	VDD	Positive Digital Supply Voltage	Internal digital power supply
7	10	VDDE	Positive External Supply Voltage	Power supply, protected up to 7.7V
8	12	AOUT2	Analog Output 2	Analog I/O, protected up to 7.7V
9	14	VSSE	External Ground	Ground
10	16	AOUT1	Analog Output 1	Analog I/O, protected up to 7.7V
11	21	DFBH	Diagnostic Fault Band Mode Select	Analog Input, internal pull-up
12	22	VTN2	External Temperature Sensor 2	Analog I/O
13	23	VBN	Negative Bridge Sensor Input	Analog input
14	24	VBR_B	Negative Bridge Supply Voltage (Bottom)	Analog I/O
15	25	VBP	Positive Bridge Sensor Input	Analog input
16	26	VBR_T	Positive Bridge Supply Voltage (Top)	Analog I/O
17	27	VTN1	External Temperature Sensor 1	Analog I/O

Package QFN32 (5mm x 5mm) (with wettable flank)

The backside of the package (the “exposed pad”) is electrically connected to the potential VSSA.

Delivery as Die (3.10mm x 2.98mm)

The backside of the chip is electrically connected to the potential VSSA.

Drawing is not true to scale.

For exact bond pad positions, refer to ZSSC3154 Technical Note – Die Dimensions and Pads.

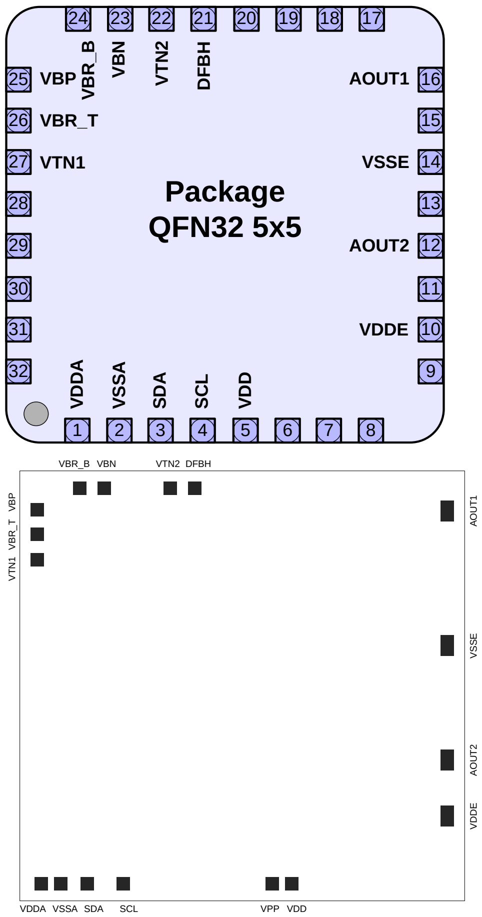


Figure 8. Pin Map and Pad Position of the ZSSC3154

7. Reliability and RoHS Conformity

The ZSSC3154 is qualified according to the AEC-Q100 standard, operating temperature grade 0.

The IC complies with the RoHS directive and does not contain hazardous substances.
The complete RoHS declaration update can be downloaded at Renesas Electronics Corporation website.

8. Ordering Information

Product Sales Code	Description	Package
ZSSC3154BA1B	ZSSC3154 Die – Temperature Range -40 to 125°C	Wafer
ZSSC3154BA1C	ZSSC3154 Die – Temperature Range -40 to 125°C	Sawn on frame
ZSSC3154BA3R	ZSSC3154 QFN32 (5x5 mm; wettable flank) – Temperature Range -40 to 125 °C	Reel
ZSSC3154BE3R	ZSSC3154 QFN32 (5x5 mm; wettable flank) – Temperature Range -40 to 150 °C	Reel
ZSSC3154KIT	ZSSC3154 SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, 5 QFN32 samples (software can be downloaded from the ZSSC3154 - Automotive Sensor Signal Conditioner with Dual Analog Output | Renesas product page.)	Kit

9. Related Documents

Note: Documents marked with an asterisk (*) require a login account for access on the web.

Documents:

- ZSSC3154 Functional Description
- ZSSC3154 Application Note – Power Management
- ZSSC3154 Application Note – Oscillator Frequency Adjustment
- Renesas Temperature Profile Calculation Spreadsheet *

Visit the ZSSC3154 product page at ZSSC3154 - Automotive Sensor Signal Conditioner with Dual Analog Output | Renesas or contact your nearest sales office for the latest version of these documents.

10. Glossary

Term	Description
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AFE	Analog Front-End
AOUT	Analog Output
BAMP	Buffer Amplifier
BR	Bridge Sensor
CM	Command Mode
CMC	Calibration Microcontroller
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DFB	Diagnostic Fault Band Mode
DM	Diagnostic Mode
DNL	Differential Nonlinearity
EEPROM	Electrically Erasable Programmable Read Only Memory
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FSO	Full Scale Output
I/O	Input/Output
I2C	Inter-Integrated Circuit, serial two-wire data bus, trademark of NXP
INL	Integral Nonlinearity

Term	Description
LSB	Least Significant Bit
MSB	Most Significant Bit
MUX	Multiplexer
NOM	Normal Operation Mode
PGA	Programmable Gain Amplifier
PTC	Positive-Temperature Coefficient
RAM	Random-Access Memory
RISC	Reduced Instruction Set Computer
ROM	Read Only Memory
RTD	Resistance Temperature Device
SAC	Sensor Aging Check
SCC	Sensor Connection Check
SSC	Sensor Short Check
XZC	Extended Zero Compensation, analog offset compensation

11. Revision History

Revision	Date	Description
1.5	April 19, 2024	Added parameter Output Update Rate and timing clarification to chapter 2.3, section system response, Changed to Renesas branding.
1.42	January 22, 2016	Changed to IDT branding.
1.41	August 27, 2014	Minor edits for die information.
1.40	April 28, 2014	Updates for specifications at 150°C for parasitic differential input offset current, INL, output leakage current, and overall failure %FSO. Update for conditions for read cycles specification. Addition of die dimensions and notes that QFN32 package has wettable flanks. Correction for specification in Table 3. Update for contact information.
1.32	March 24, 2014	Updates for maximum operational range added to 150°C product capability
1.31	March 6, 2014	Addition of extended temperature range. Maximum temperature range is now -40°C to 140°C for new part code ZSSC3154BE3R. Related updates for temperature range specifications and parasitic differential input offset current specification in Table 2 and Table 3.. Updates for overall failure at +140°C in Table 3.. Updates for EEPROM read cycles at ≤ +140°C and EEPROM data retention at +150°C in Table 4. Update for addition of power-on reset (POR) specifications in Table 2. Update for delivery form availability. PQFN32 is now available for delivery only on reels; it is not available in trays. Reel part number and size have changed. Update for kit description in part ordering table: DVD is no longer included in kit because software is now downloaded from the product page at ZSSC3154 - Automotive Sensor Signal Conditioner with Dual Analog Output | Renesas to ensure user has the latest version. Updates for cover imagery.
1.30	August 29, 2013	Corrected AFE input signal range given in footnote 1 for Table 2. Added oscillator frequency specification f_{OSC} in section 0, and added note before Table 3. stating the specifications are valid if f_{OSC} is within the specified range.
1.20	June 18, 2013	Update for description of external resistive half-bridge temperature sensor and addition of recommended resistive sensors for temperature measurement in section 3.6. Update for contact information and images for cover and headers.
1.10	June 14, 2012	Specification of input capacitance added (see Table 3). Minor edits.
1.00	June 8, 2012	First release.

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