Description
The XT devices are ultra-low phase noise quartz-based PLL oscillators supporting a large range of frequencies and output interface types.

The XT devices can be programmed to generate an output frequency from 15MHz to 2100MHz with a resolution as low as 1Hz accuracy. The configurability of this family of devices provides fast delivery times for both sample and large production orders.

Parts may be factory programmed for fixed frequency applications, or may be field configured using the I2C interface.

Features
- Output types: LVDS, LVPECL, CML
  - Frequency range: 15MHz to 2100MHz
- Output type: HCSL
  - Frequency range: 15MHz to 725MHz
- Supply voltage options: 1.8V, 2.5V, 3.3V
- Phase jitter (12kHz to 20MHz): 135 fs typical
- Package options:
  - 3.2 × 2.5 × 0.85 mm
- Operating temperature and stability:
  - -40°C to +85°C, ±3ppm
- Frequency stability for life:
  - -40°C to +85°C, ±13ppm

Pin Assignments

Figure 1. 3.2 × 2.5 mm Package – Top View

Table 1. Pin Descriptions

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OE</td>
<td>Output Enable (0 = output disabled, pulled high internally)</td>
</tr>
<tr>
<td>2</td>
<td>NC</td>
<td>No connect</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Connect to ground</td>
</tr>
<tr>
<td>4</td>
<td>OUT0</td>
<td>Output</td>
</tr>
<tr>
<td>5</td>
<td>OUT0b</td>
<td>Complementary output</td>
</tr>
<tr>
<td>6</td>
<td>VDD</td>
<td>Supply voltage</td>
</tr>
<tr>
<td>7</td>
<td>SDA</td>
<td>Serial data</td>
</tr>
<tr>
<td>8</td>
<td>SCL</td>
<td>Serial clock</td>
</tr>
</tbody>
</table>

1 Pins 7 and 8 are no connect for non-I2C applications.

See Ordering Information for more details.
## Ordering Information

<table>
<thead>
<tr>
<th>XT</th>
<th>L</th>
<th>3</th>
<th>1</th>
<th>2</th>
<th>125.000000</th>
<th>I</th>
</tr>
</thead>
<tbody>
<tr>
<td>Family and ASIC</td>
<td>Output Type</td>
<td>Package</td>
<td>Voltage</td>
<td>Precision</td>
<td>Frequency</td>
<td>Temperature Range</td>
</tr>
</tbody>
</table>

1: 1.8 VDC ±5%
2: 2.5 VDC ±5%
3: 3.3 VDC ±5%

- **XT:** 150fs jitter
- **C:** CML Enable/Disable Pin 1
- **L:** LVDS Enable/Disable Pin 1
- **P:** LVPECL Enable/Disable Pin 1
- **N:** HCSL Enable/Disable Pin 1
- **3:** 3.2 x 2.5 mm

**125.000000 Listed in MHz as example**
3 digits before decimal and 6 digits past decimal

- 015.000000 to 099.999999
- 100.000000 to 999.999999
- A00.000000 to A99.999999
- B00.000000 to B99.999999
- C00.000000 to C99.999999
- D00.000000 to D99.999999
- E00.000000 to E99.999999
- F00.000000 to F99.999999
- G00.000000 to G99.999999
- H00.000000 to H99.999999
- I00.000000 to I99.999999
- J00.000000 to J99.999999
- K00.000000 to K99.999999
- L00.000000 to L99.999999

1: Extended industrial range: -40 to +85°C

2: ±13ppm for life (±3ppm for temperature stability)

- ±13ppm for life (±3ppm for temperature stability)
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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the device. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range. Thermal characteristics, in actual applications, should be assessed case by case to guarantee junction temperature does not exceed 125°C.

Table 2. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>-0.5V to +3.8V</td>
</tr>
<tr>
<td>OE</td>
<td>-0.5V to +3.8V</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-55°C to 125°C</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>125°C</td>
</tr>
<tr>
<td>Theta $J_A$</td>
<td>LNG8</td>
</tr>
<tr>
<td>Theta $J_B$</td>
<td></td>
</tr>
</tbody>
</table>

$^1$ Thermal characteristics are based on simulation in standard condition.

ESD Compliance

Table 3. ESD Compliance

<table>
<thead>
<tr>
<th></th>
<th>2000V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human Body Model (HBM)</td>
<td></td>
</tr>
</tbody>
</table>

Mechanical Testing

Table 4. Mechanical Testing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mechanical Shock</td>
<td>Half-sine wave with 0.3ms 3000G. X, Y, Z each direction 1 time.</td>
</tr>
<tr>
<td>Mechanical Vibration</td>
<td>Frequency: 10 to 55MHz amplitude: 1.5mm.</td>
</tr>
<tr>
<td></td>
<td>Frequency: 55–2000Hz peak value: 20G.</td>
</tr>
<tr>
<td></td>
<td>Duration time: 4H for each X, Y, Z axis; total 12hours.</td>
</tr>
<tr>
<td>High Temp Operating Life (HTOL)</td>
<td>1000 hours at 125°C (under power).</td>
</tr>
</tbody>
</table>

Solder Reflow Profile

![Solder Reflow Profile Diagram](image)
## DC Electrical Characteristics

### Table 5. 3.3V IDD DC Electrical Characteristics

$V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, typical at 156.25MHz.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Output Type</th>
<th>Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDD</td>
<td>Current Consumption</td>
<td>LVDS</td>
<td>15MHz to 400MHz.</td>
<td>—</td>
<td>59</td>
<td>67</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400MHz to 2.1GHz.</td>
<td>—</td>
<td>—</td>
<td>85</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVPECL</td>
<td>15MHz to 212.5MHz.</td>
<td>—</td>
<td>84</td>
<td>94</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>212.5MHz to 400MHz.</td>
<td>—</td>
<td>—</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>212.5MHz to 2.1GHz.</td>
<td>—</td>
<td>—</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL</td>
<td>15MHz to 400MHz.</td>
<td>—</td>
<td>—</td>
<td>95</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400MHz to 725MHz.</td>
<td>—</td>
<td>74</td>
<td>83</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CML</td>
<td>15MHz to 2.1GHz.</td>
<td>—</td>
<td>54</td>
<td>61</td>
<td></td>
</tr>
</tbody>
</table>

### Table 6. 2.5V IDD DC Electrical Characteristics

$V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, typical at 156.25MHz.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Output Type</th>
<th>Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDD</td>
<td>Current Consumption</td>
<td>LVDS</td>
<td>15MHz to 400MHz.</td>
<td>—</td>
<td>59</td>
<td>66</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400MHz to 2.1GHz.</td>
<td>—</td>
<td>—</td>
<td>85</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVPECL</td>
<td>15MHz to 156.25MHz.</td>
<td>—</td>
<td>84</td>
<td>94</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>156.25MHz to 400MHz.</td>
<td>—</td>
<td>—</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400MHz to 2.1GHz.</td>
<td>—</td>
<td>—</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL</td>
<td>15MHz to 400MHz.</td>
<td>—</td>
<td>—</td>
<td>95</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400MHz to 725MHz.</td>
<td>—</td>
<td>74</td>
<td>82</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CML</td>
<td>15MHz to 2.1GHz.</td>
<td>—</td>
<td>54</td>
<td>61</td>
<td></td>
</tr>
</tbody>
</table>

### Table 7. 1.8V DD DC Electrical Characteristics

$V_{DD} = 1.8V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, typical at 156.25MHz.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Output Type</th>
<th>Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDD</td>
<td>Current Consumption</td>
<td>LVDS</td>
<td>15MHz to 400MHz.</td>
<td>—</td>
<td>59</td>
<td>66</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400MHz to 2.1GHz.</td>
<td>—</td>
<td>—</td>
<td>85</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVPECL</td>
<td>15MHz to 250MHz.</td>
<td>—</td>
<td>84</td>
<td>93</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>250MHz to 2.1GHz.</td>
<td>—</td>
<td>—</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL</td>
<td>15MHz to 400MHz.</td>
<td>—</td>
<td>—</td>
<td>95</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400MHz to 725MHz.</td>
<td>—</td>
<td>74</td>
<td>81</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CML</td>
<td>15MHz to 2.1GHz.</td>
<td>—</td>
<td>54</td>
<td>61</td>
<td></td>
</tr>
</tbody>
</table>
Table 8. LVCMOS DC Electrical Characteristics

$V_{DD} = 1.8V, 2.5V, 3.3V \pm 5\%, T_A = -40^\circ C \text{ to } +85^\circ C$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage (OE pin only)</td>
<td>$V_{DD} = 1.8V, 2.5V, 3.3V \pm 5%.$</td>
<td>$0.7 \times V_{DD}$</td>
<td>—</td>
<td>$V_{DD} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage (OE pin only)</td>
<td>$V_{DD} = 1.8V, 2.5V, 3.3V \pm 5%.$</td>
<td>GND - 0.3</td>
<td>—</td>
<td>$0.3 \times V_{DD}$</td>
<td>V</td>
</tr>
</tbody>
</table>

Table 9. LVDS DC Electrical Characteristics

$V_{DD} = 1.8V, 2.5V, 3.3V \pm 5\%, T_A = -40^\circ C \text{ to } +85^\circ C$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OD}$</td>
<td>Differential Output Voltage</td>
<td>$V_{DD} = 1.8V, 2.5V, 3.3V \pm 5%.$</td>
<td>0.30</td>
<td>0.44</td>
<td>0.60</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>Output Offset Voltage</td>
<td>$V_{DD} = 1.8V \pm 5%$</td>
<td>0.75</td>
<td>0.88</td>
<td>1.01</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 2.5V \pm 5%$</td>
<td>1.08</td>
<td>1.25</td>
<td>1.41</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3.3V \pm 5%$</td>
<td>1.11</td>
<td>1.26</td>
<td>1.41</td>
<td></td>
</tr>
</tbody>
</table>

Table 10. LVPECL DC Electrical Characteristics

$V_{DD} = 1.8V, 2.5V, 3.3V \pm 5\%, T_A = -40^\circ C \text{ to } +85^\circ C$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage</td>
<td>$V_{DD} = 1.8V \pm 5%.$</td>
<td>0.83</td>
<td>0.96</td>
<td>1.11</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 2.5V \pm 5%.$</td>
<td>1.52</td>
<td>1.69</td>
<td>1.87</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3.3V \pm 5%.$</td>
<td>2.28</td>
<td>2.49</td>
<td>2.72</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td>$V_{DD} = 1.8V \pm 5%.$</td>
<td>0.19</td>
<td>0.30</td>
<td>0.42</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 2.5V \pm 5%.$</td>
<td>0.92</td>
<td>1.04</td>
<td>1.17</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3.3V \pm 5%.$</td>
<td>1.68</td>
<td>1.84</td>
<td>2.01</td>
<td></td>
</tr>
</tbody>
</table>

Table 11. HCSL DC Electrical Characteristics

$V_{DD} = 1.8V, 2.5V, 3.3V \pm 5\%, T_A = -40^\circ C \text{ to } +85^\circ C$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage</td>
<td>$V_{DD} = 1.8V \pm 5%.$</td>
<td>0.67</td>
<td>0.81</td>
<td>0.95</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 2.5V \pm 5%.$</td>
<td>0.74</td>
<td>0.88</td>
<td>1.03</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3.3V \pm 5%.$</td>
<td>0.78</td>
<td>0.92</td>
<td>1.07</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td>—</td>
<td>-0.06</td>
<td>0.07</td>
<td>0.20</td>
<td>V</td>
</tr>
</tbody>
</table>
### Table 12. CML DC Electrical Characteristics

$V_{DD} = 1.8V, 2.5V, 3.3V \pm 5\%, T_{A} = -40^\circ C$ to $+85^\circ C$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage</td>
<td>$V_{DD} = 1.8V \pm 5%$.</td>
<td>1.61</td>
<td>1.76</td>
<td>1.91</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 2.5V \pm 5%$.</td>
<td>2.33</td>
<td>2.46</td>
<td>2.59</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3.3V \pm 5%$.</td>
<td>3.09</td>
<td>3.26</td>
<td>3.43</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td>$V_{DD} = 1.8V \pm 5%$.</td>
<td>1.24</td>
<td>1.37</td>
<td>1.52</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 2.5V \pm 5%$.</td>
<td>1.95</td>
<td>2.06</td>
<td>2.17</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3.3V \pm 5%$.</td>
<td>2.70</td>
<td>2.85</td>
<td>3.00</td>
<td></td>
</tr>
</tbody>
</table>

### Table 13. DC Electrical Characteristics – Leakage Current

$V_{DD} = 1.8V, 2.5V, 3.3V \pm 5\%, T_{A} = -40^\circ C$ to $+85^\circ C$, typical at 156.25MHz.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Input</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IH}$</td>
<td>Input Leakage High</td>
<td>$V_{DD} = 3.3V \pm 5%$.</td>
<td>OE</td>
<td>-5</td>
<td>0.8</td>
<td>5</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SCLK</td>
<td>-5</td>
<td>1.4</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SDATA</td>
<td>-5</td>
<td>1.4</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Leakage Low</td>
<td>$V_{DD} = 3.3V \pm 5%$.</td>
<td>OE</td>
<td>-20</td>
<td>-17.4</td>
<td>-14</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SCLK</td>
<td>-37</td>
<td>-33.5</td>
<td>-30</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SDATA</td>
<td>-20</td>
<td>-17</td>
<td>-14</td>
<td></td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input Leakage High</td>
<td>$V_{DD} = 1.8V \pm 5%$.</td>
<td>OE</td>
<td>-5</td>
<td>0.8</td>
<td>5</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SCLK</td>
<td>-5</td>
<td>1.4</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SDATA</td>
<td>-5</td>
<td>1.4</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Leakage Low</td>
<td>$V_{DD} = 1.8V \pm 5%$.</td>
<td>OE</td>
<td>-11.5</td>
<td>-9.5</td>
<td>-7.5</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SCLK</td>
<td>-20.8</td>
<td>-18.3</td>
<td>-15.7</td>
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</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SDATA</td>
<td>-11.5</td>
<td>-9.3</td>
<td>-7.5</td>
<td></td>
</tr>
</tbody>
</table>
AC Electrical Characteristics

Note for all AC Electrical Characteristics tables:
1. Installation should include a 0.01 μF bypass capacitor placed between V_{DD} and GND to minimize power supply line noise.

Table 14. 3.3V AC Electrical Characteristics

V_{DD} = 3.3V ± 5%, T_{A} = -40°C to +85°C.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>Output Frequency Range</td>
<td>LVDS, LVPECL, CML.</td>
<td>15</td>
<td>—</td>
<td>2100</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL.</td>
<td>15</td>
<td>—</td>
<td>725</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>Frequency Stability</td>
<td>Temperature = -40°C to +85°C.</td>
<td>—</td>
<td>—</td>
<td>±3</td>
<td>PPM</td>
</tr>
<tr>
<td></td>
<td>Frequency Tolerance (25°C)</td>
<td>T_{A} = 25°C.</td>
<td>—</td>
<td>—</td>
<td>±2</td>
<td>PPM</td>
</tr>
<tr>
<td></td>
<td>Aging (1 year)</td>
<td>T_{A} = 25°C.</td>
<td>—</td>
<td>—</td>
<td>±1</td>
<td>PPM</td>
</tr>
<tr>
<td></td>
<td>Aging (10 years)</td>
<td>T_{A} = 25°C.</td>
<td>—</td>
<td>—</td>
<td>±7</td>
<td>PPM</td>
</tr>
<tr>
<td></td>
<td>Output Load</td>
<td>LVDS. Differential.</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVPECL. Thevenin equivalent.</td>
<td>—</td>
<td>50</td>
<td>—</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL. To GND.</td>
<td>—</td>
<td>50</td>
<td>—</td>
<td>Ω</td>
</tr>
<tr>
<td>T_{ST}</td>
<td>Start-up Time</td>
<td>Output valid time after V_{DD} meets minimum specified level.</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>ms</td>
</tr>
<tr>
<td>t_{R}</td>
<td>Output Rise Time</td>
<td>LVDS.</td>
<td>—</td>
<td>299</td>
<td>400</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVPECL. 20% – 80%, 156.25MHz</td>
<td>—</td>
<td>287</td>
<td>400</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CML</td>
<td>—</td>
<td>306</td>
<td>400</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CML</td>
<td>—</td>
<td>301</td>
<td>400</td>
<td>ps</td>
</tr>
<tr>
<td>t_{F}</td>
<td>Output Fall Time</td>
<td>LVDS. 80% – 20%, 156.25MHz</td>
<td>—</td>
<td>279</td>
<td>400</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVPECL.</td>
<td>—</td>
<td>274</td>
<td>400</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL.</td>
<td>—</td>
<td>284</td>
<td>400</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CML</td>
<td>—</td>
<td>279</td>
<td>400</td>
<td>ps</td>
</tr>
<tr>
<td>O_{DC}</td>
<td>Output Clock Duty Cycle</td>
<td>LVDS. 156.25MHz</td>
<td>45</td>
<td>—</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVPECL. 156.25MHz</td>
<td>45</td>
<td>—</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL. 156.25MHz</td>
<td>45</td>
<td>—</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CML 156.25MHz</td>
<td>45</td>
<td>—</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td>T_{OE}</td>
<td>Output Enable/Disable Time</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>ms</td>
</tr>
</tbody>
</table>
Table 15.  2.5V AC Electrical Characteristics

\[ V_{DD} = 2.5V \pm 5\%, \ T_A = -40°C \text{ to } +85°C. \]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>Output Frequency Range</td>
<td>LVDS, LVPECL, CML.</td>
<td>15</td>
<td>—</td>
<td>2100</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL.</td>
<td>15</td>
<td>—</td>
<td>725</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Frequency Stability</td>
<td>Temperature = -40°C to +85°C.</td>
<td>—</td>
<td>—</td>
<td>±3</td>
<td>ppm</td>
</tr>
<tr>
<td></td>
<td>Frequency Tolerance (25°C)</td>
<td>( T_A = 25°C. )</td>
<td>—</td>
<td>—</td>
<td>±2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Aging (1 year)</td>
<td>( T_A = 25°C. )</td>
<td>—</td>
<td>—</td>
<td>±1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Aging (10 years)</td>
<td>( T_A = 25°C. )</td>
<td>—</td>
<td>—</td>
<td>±7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Load</td>
<td>LVDS. Differential.</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVPECL. Thevenin equivalent.</td>
<td>—</td>
<td>50</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL. To GND.</td>
<td>—</td>
<td>50</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>ST</td>
<td>Start-up Time</td>
<td>Output valid time after ( V_{DD} ) meets minimum specified level.</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>ms</td>
</tr>
<tr>
<td>( t_R )</td>
<td>Output Rise Time</td>
<td>LVDS.</td>
<td>—</td>
<td>303</td>
<td>400</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVPECL. 20% – 80%, 156.25MHz</td>
<td>—</td>
<td>292</td>
<td>400</td>
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<tr>
<td></td>
<td></td>
<td>HCSL.</td>
<td>—</td>
<td>310</td>
<td>400</td>
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<tr>
<td></td>
<td></td>
<td>CML</td>
<td>—</td>
<td>304</td>
<td>400</td>
<td></td>
</tr>
<tr>
<td>( t_F )</td>
<td>Output Fall Time</td>
<td>LVDS. 80% – 20%, 156.25MHz</td>
<td>—</td>
<td>282</td>
<td>400</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVPECL.</td>
<td>—</td>
<td>278</td>
<td>400</td>
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<td>288</td>
<td>400</td>
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<td></td>
<td></td>
<td>CML</td>
<td>—</td>
<td>281</td>
<td>400</td>
<td></td>
</tr>
<tr>
<td>ODC</td>
<td>Output Clock Duty Cycle</td>
<td>LVDS. 156.25MHz</td>
<td>45</td>
<td>—</td>
<td>55</td>
<td>%</td>
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<td></td>
<td></td>
<td>LVPECL. 156.25MHz</td>
<td>45</td>
<td>—</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL. 156.25MHz</td>
<td>45</td>
<td>—</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CML 156.25MHz</td>
<td>45</td>
<td>—</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td>TOE</td>
<td>Output Enable/Disable Time</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>ms</td>
</tr>
</tbody>
</table>
Table 16. 1.8V AC Electrical Characteristics

\(V_{DD} = 1.8V \pm 5\%, \ T_A = -40^\circ C \ to \ +85^\circ C.\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>Output Frequency Range</td>
<td>LVDS, LVPECL, CML.</td>
<td>15</td>
<td>—</td>
<td>2100</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL.</td>
<td>15</td>
<td>—</td>
<td>725</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Frequency Stability</td>
<td>Temperature = -40°C to +85°C.</td>
<td>—</td>
<td>—</td>
<td>±3</td>
<td>PPM</td>
</tr>
<tr>
<td></td>
<td>Frequency Tolerance (25°C)</td>
<td>(T_A = 25^\circ C.)</td>
<td>—</td>
<td>—</td>
<td>±2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Aging (1 year)</td>
<td>(T_A = 25^\circ C.)</td>
<td>—</td>
<td>—</td>
<td>±1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Aging (10 years)</td>
<td>(T_A = 25^\circ C.)</td>
<td>—</td>
<td>—</td>
<td>±7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Load</td>
<td>LVDS. Differential.</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVPECL. Thevenin equivalent.</td>
<td>—</td>
<td>50</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL. To GND.</td>
<td>—</td>
<td>50</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Start-up Time</td>
<td>Output valid time after (V_{DD}) meets minimum specified level.</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>ms</td>
</tr>
<tr>
<td>T_{ST}</td>
<td>Output Rise Time</td>
<td>LVDS.</td>
<td>—</td>
<td>300</td>
<td>450</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVPECL. 20% – 80%, 312.5MHz</td>
<td>—</td>
<td>260</td>
<td>450</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL.</td>
<td>—</td>
<td>260</td>
<td>450</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CML</td>
<td>—</td>
<td>270</td>
<td>450</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Fall Time</td>
<td>LVDS. 80% – 20%, 312.5MHz</td>
<td>—</td>
<td>280</td>
<td>450</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVPECL.</td>
<td>—</td>
<td>250</td>
<td>450</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>HCSL.</td>
<td>—</td>
<td>250</td>
<td>450</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CML</td>
<td>—</td>
<td>270</td>
<td>450</td>
<td></td>
</tr>
<tr>
<td>O_{DC}</td>
<td>Output Clock Duty Cycle</td>
<td>LVDS. 312.5MHz</td>
<td>45</td>
<td>—</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVPECL. 312.5MHz</td>
<td>45</td>
<td>—</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL. 312.5MHz</td>
<td>45</td>
<td>—</td>
<td>55</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>CML 312.5MHz</td>
<td>45</td>
<td>—</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td>T_{OE}</td>
<td>Output Enable/Disable Time</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>ms</td>
</tr>
</tbody>
</table>
### Table 17. Phase Jitter Characteristics

$V_{DD} = 1.8V, 2.5V, 3.3V \pm 5\%, T_A = -40^\circ C$ to $+85^\circ C$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typical (LVPECL)</th>
<th>Typical (LVDS)</th>
<th>Typical (CML)</th>
<th>Typical (HSCL)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{JITTER}$</td>
<td>Phase Jitter (12kHz – 20MHz)</td>
<td>312.50MHz</td>
<td>124</td>
<td>159</td>
<td>131</td>
<td>126</td>
<td>fsec</td>
</tr>
<tr>
<td></td>
<td></td>
<td>625.00MHz</td>
<td>130</td>
<td>132</td>
<td>133</td>
<td>131</td>
<td>fsec</td>
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<td></td>
<td></td>
<td>644.53MHz</td>
<td>134</td>
<td>137</td>
<td>133</td>
<td>130</td>
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<td>779.215MHz</td>
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<td>818.991MHz</td>
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<td>144</td>
<td>140</td>
<td>—</td>
<td>fsec</td>
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<tr>
<td></td>
<td></td>
<td>822.128MHz</td>
<td>164</td>
<td>167</td>
<td>164</td>
<td>—</td>
<td>fsec</td>
</tr>
<tr>
<td></td>
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<td>840.759MHz</td>
<td>146</td>
<td>152</td>
<td>151</td>
<td>—</td>
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<td></td>
<td>1588.430MHz</td>
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<td>144</td>
<td>143</td>
<td>—</td>
<td>fsec</td>
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<td>1681.518MHz</td>
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<td>—</td>
<td>fsec</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1644.256MHz</td>
<td>157</td>
<td>154</td>
<td>155</td>
<td>—</td>
<td>fsec</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1637.982MHz</td>
<td>147</td>
<td>148</td>
<td>148</td>
<td>—</td>
<td>fsec</td>
</tr>
</tbody>
</table>

### Output Phase Noise

**Figure 2. 625MHz LVDS Output**

![Output Phase Noise Graph](image)
Output Waveforms

Figure 3. LVDS/LVPECL/HCSL/CML Output Waveforms

Output Levels / Rise Time / Fall Time Measurements

Oscillator Symmetry
3.3V LVPECL Output Termination

Figure 4 shows an example of termination for 3.3V LVPECL driver.

Figure 4. 3.3V LVPECL Driver Termination Example

2.5V LVPECL Output Termination

Figure 5 shows an example of termination for 2.5V LVPECL driver.

Figure 5. 2.5V LVPECL Driver Termination Example

1.8V LVPECL Output Termination

Figure 6 shows an example of termination for 1.8V LVPECL driver.

Figure 6. 1.8V LVPECL Driver Termination Example
LVDS Output Termination

For a general LVDS interface, the recommended value for the termination impedance ($Z_T$) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance ($Z_0$) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. Renesas offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source.

The standard termination schematic as shown in Figure 7 can be used with either type of output structure. Figure 8, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact Renesas and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

**Figure 7. Standard LVDS Termination**

**Figure 8. Optional LVDS Termination**
HCSL Output Termination

Figure 9 is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential. Figure 10 is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

**Figure 9. Recommended Source Termination (where the driver and receiver will be on separate PCBs)**

**Figure 10. Recommended Termination (where a point-to-point connection can be used)**

CML Output Termination

Figure 11 shows an example of the termination for a CML driver. In this example, the transmission line characteristic impedance is 50Ω. The R1 and R2 50Ω matched load terminations are pulled up to VDDO. The matched loads are located close to the receiver.

**Figure 11. CML Driver Termination Example**
Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

Marking Diagram

Figure 12. Marking Configuration for the 3.2 × 2.5 mm (LNG8) Package (example based on XTL312625.000000I)

- Line 1 denotes the truncated part number as follows:
  - “D” = a combination of the 3rd digit (output type, e.g. “L”) and the 5th digit (voltage supply, e.g. “3”), in accordance with the mapping key as follows:
  - “xxxxxx” = the first three digits to the left of the decimal point and the last three digits to the left of the decimal point as shown in the above example. This number will vary depending upon the frequency value selected in the orderable part number. (e.g. 625000).
- Line 2 indicates the following:
  - “YWW” denotes the last digit of the year and week when the part was assembled.
  - “***” denotes the sequential lot number.
  - “$” denotes the mark location.

Revision History

<table>
<thead>
<tr>
<th>Revision Date</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>April 8, 2021</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009
2. ALL DIMENSIONS ARE IN MILLIMETERS
8-LGA, Package Outline Drawing
2.50 x 3.20 x 0.85 mm Body, 1.25mm Pitch
LNG8D1, PSC-4837-01, Rev 01, Page 2

Package Revision History

<table>
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<tr>
<th>Date Created</th>
<th>Rev No.</th>
<th>Description</th>
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<tbody>
<tr>
<td>Nov. 12, 2019</td>
<td>00</td>
<td>Initial Release</td>
</tr>
<tr>
<td>Jun. 21, 2021</td>
<td>01</td>
<td>Update to Renesas Logo</td>
</tr>
</tbody>
</table>

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NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES
2. TOP DOWN VIEW, AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN
4. NSMD PATTERN ASSUMED

RECOMMENDED LAND PATTERN DIMENSION
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