XK

Ultra-low Phase Noise Quartz-based PLL Oscillator

Description

The XK devices are a second-generation follow-on to the XF ProXO high-performance oscillators. The devices are often referred to as ProXO II.

The XK family of devices uses internal regulators to provide excellent PSNR characteristics.

The devices are offered in a range of industry-standard package footprints. Each device can be factory programmed with up to three frequencies and/or output types that are selected by the 3-level FS pin.

A list of standard frequencies is provided in Table 26.

Applications

- 10G to 800G Ethernet
- 100G to 400G OTN
- 3G to 24G SDI broadcast video
- Servers, switches, storage, accelerators, NICs, HBAs

Features

- 55fs RMS typical phase jitter (12kHz to 20MHz) at 156.25MHz
- 50MHz to 1250MHz output frequency
- Package options:
  - 1.80 × 1.40 × 0.85 mm (1.60 × 1.20 mm footprint compatible) – 6-LGA (LTV6D1)
  - 2.00 × 1.60 × 0.85 mm – 6-LGA (LLV6D1)
  - 2.50 × 2.00 × 0.70 mm – 6-LGA (LTT6D1)
  - 3.20 × 2.50 × 0.70 mm – 6-LGA (LLT6D1)
- Supply voltage options: 1.8V, 2.5V, 3.3V
- Output types:
  - LVDS, CML, and HCSL (1.8V, 2.5V, 3.3V)
  - LVPECL (3.3V only)
  - LVCMOS differential (1.8V only)
- Total stability ±50ppm (including temperature, power supply, and aging)
- Operating temperature:
  -40°C to +85°C (all operating voltages)
  -40°C to +105°C (1.8V – Preliminary. Contact Renesas for more information)

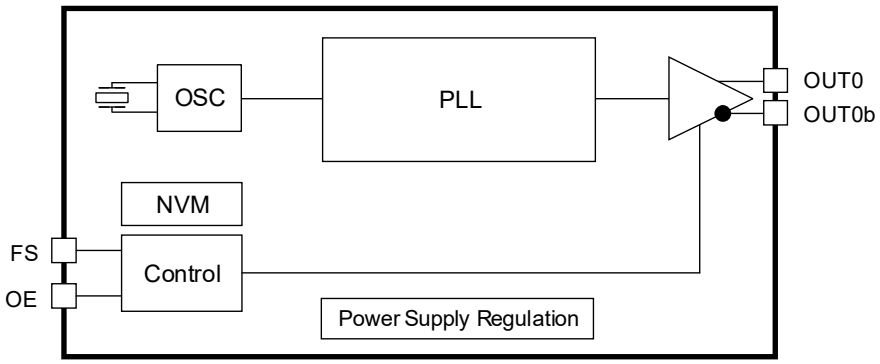

Figure 1. Block Diagram

Contents

1. Pin Information

1.1 Pin Assignments

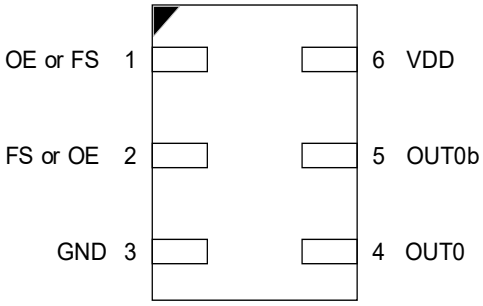

Figure 2. Pin Assignments – Top View

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1	OE or FS	Output Enable (OE) or Frequency Select (FS) pin. The function of this pin is determined by the Ordering Information. When OE is selected, the polarity of the OE is also selectable via ordering option. When FS is selected, the pin is a 3-state (High, Mid (Float), Low) pin that selects on of the three factory-programmed frequencies. *Note*: The OE function stops the outputs in a differential state, it does not tri-state the outputs or power down the internal circuitry.
2	FS or OE	Frequency Select (FS) or Output Enable (OE) pin. The function of this pin is determined by the ordering options. When FS is ordered, the pin is a 3-state (High, Mid (Float), Low) pin that selects on of the three factory-programmed frequencies. When OE is selected, the polarity of the OE is also selectable via ordering option. This pin is always the function not chosen for pin 1. *Note*: The OE function stops the outputs in a differential state, it does not tri-state the outputs or power down the internal circuitry.
3	GND	Connect to ground.
4	OUT0	True clock output.
5	OUT0b	Complementary clock output.
6	VDD	Power supply voltage.

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
V_{DD}	GND - 0.5	GND + 3.8	V
All Other Pins	GND - 0.3	V_{DD} + 0.3[1]	V
Maximum Junction Temperature	-	+125	°C
Storage Temperature Range	-55	+125	°C
Human Body Model (Tested per JS-001-2017)	-	2	kV
Charged Device Model (Tested per JS-002-2018)	-	1	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

1. Not to exceed 3.6V.

2.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
1.8V Nominal Supply Voltage, V_{DD}	1.71	1.89	V
2.5V Nominal Supply Voltage, V_{DD}	2.375	2.625	V
3.3V Nominal Supply Voltage, V_{DD}	3.135	3.465	V
Ambient Temperature	-40	+85	°C

2.3 Thermal and Mechanical Specifications

Table 1. Thermal Characteristics - JEDEC Standard PCB

Package	θ_{JA} (°C/W) [1]	θ_{JB} (°C/W) [2]
1814 Package (1612 footprint compatible)	113.2	56.7
2016 Package	114.1	61.1
2520 Package	93.1	39.4
3225 Package	92.0	42.6

1. Still air.
2. Device soldered to JEDEC standard PCB (4 × 4.5 inch 4-layer PCB, one thermal via, one PCB ground plane).

Table 2. Thermal Characteristics—Customer PCB

Package	θ_{JA} (°C/W) [1]	θ_{JB} (°C/W) [2]
1814 Package (1612 footprint compatible)	94.4	56.7
2016 Package	97.6	61.1
2520 Package	76.7	40.4
3225 Package	76.8	42.6

1. Still air.
2. Device soldered to 200 × 250 mm 10-layer PCB with one thermal via, and four PCB ground planes.

Thermal vias in the PCB pads can also be used to maximize performance. The vias act as “heat pipes” conducting heat from the device to the PCB ground plane(s). For specific recommendations, contact Renesas.

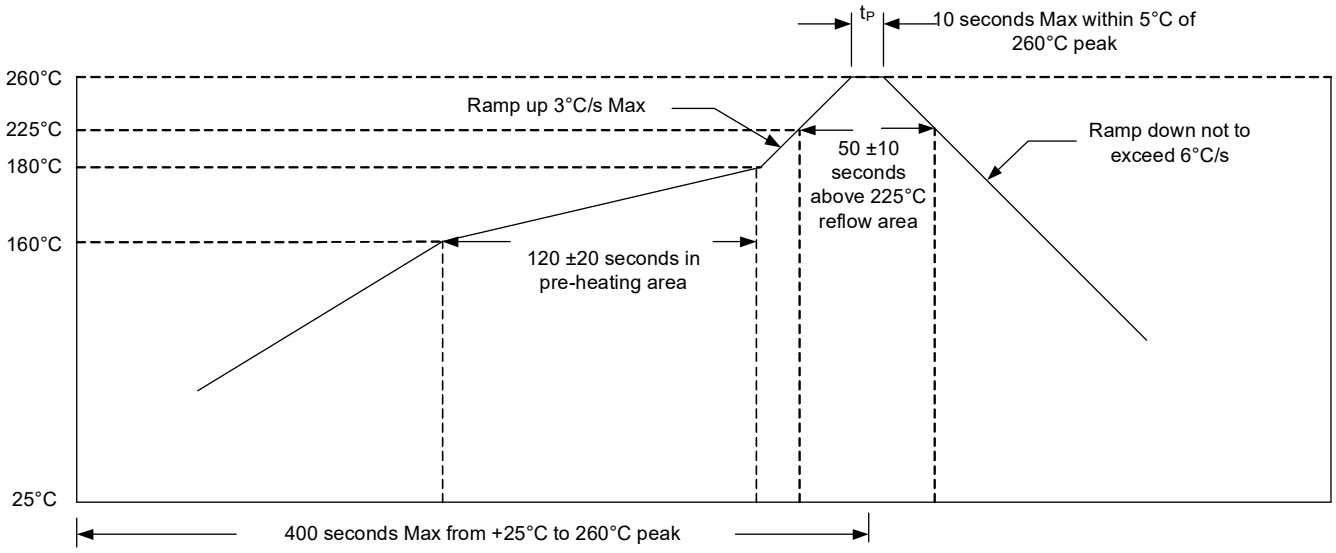

Figure 3. Solder Re-flow Profile

Table 3. Package Mechanical Characteristics

Parameter	Test Method	Value
Mechanical Shock	Half-sine wave with 0.3ms 3000G. X, Y, Z each direction 1 time.	-
Mechanical Vibration	Frequency: 10 to 55MHz amplitude: 1.5mm. Frequency: 55 to 2000Hz peak value: 20G. Duration time: 4H for each X, Y, Z axis; total 12hours.	-
High Temp Operating Life (HTOL)	1000 hours at 125°C (under power).	-
MSL Level	JEDEC-STD-020E, Moisture/Reflow Sensitivity Classification for Non-hermetic Surface Mount Devices, December 2014.	3
Pb-Free Reflow Profile	See Figure 3	-

2.4 Electrical Specifications

T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise specified. A 0.01µF bypass capacitor between V_{DD} and GND is used to minimize power supply noise.

2.4.1 Common Specifications

V_{DD} = 1.8V ± 5%, 2.5V ± 5%,3.3V ± 5%, T_A = -40°C to +85°C.

Table 4. Common Specifications

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output Frequency	F_{OUT}	-	50	-	1250	MHz
Frequency Stability[1]	-		-	-	±50	ppm
Start-up Time	T_{SU}	-	-	15	-	ms
Output Enable/Disable Time	T_{OE}	-	-	0.1	-	
Input High Voltage	V_{IH}	FS pin (tri-level)	0.8 x V_{DD}	-	V_{DD} + 0.3	V
Input Mid-Level Voltage	V_{IM}		0.4 x V_{DD}	V_{DD}/2	0.6 x V_{DD}	
Input Low Voltage	V_{IL}		GND - 0.3	-	0.2 x V_{DD}	
Input High Voltage	V_{IH}	OE pin	0.7 x V_{DD}	-	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		GND - 0.3	-	0.3 x V_{DD}	
Input Leakage High	I_{IH}	OE pin	0.5	-	2	µA
		FS pin	30	-	70	
Input Leakage Low	I_{IL}	OE pin	-70	-	-30	µA
		FS pin	-70	-	-30	

1. Includes initial accuracy, aging, and thermal effects.

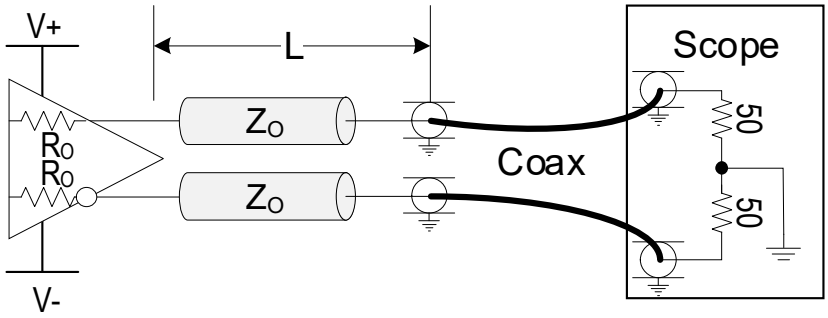

Figure 4. AC/DC Test Circuit

The AC and DC parameters are tested with Thevenin-equivalent circuits that make the most use of the 50ohm terminations built into the scope. See Table 5 for details.

Table 5. Configurations for AC/DC Tests

Output Type	V+ (V)	V- (V)	Ro (ohms)	Rs (ohms)	Zo (ohms)	L (cm)
CML	0	-1.8 ± 5%	NA	NA	50	2.5
	0	-2.5 ± 5%				
	0	-3.3 ± 5%				
HCSL	1.8 ± 5%	0	NA	NA	50	2.5
	2.5 ± 5%	0				
	3.3 ± 5%	0				
LVCMOS	0.9 ± 5% (VDD/2 ± 5%)	-0.9 ± 5% (-VDD/2 ± 5%)	28	NA	50	2.5
LVDS	1.8 ± 5%	0	NA	NA	50	2.5
	2.5 ± 5%	0				
	3.3 ± 5%	0				
LVPECL	2	-1.3 ± 5%	NA	NA	50	2.5

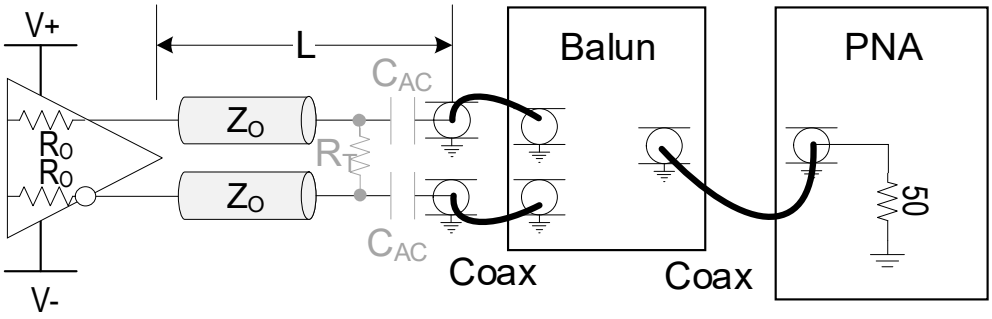

Figure 5. Phase Jitter Test Circuit

Table 6. Configurations for Phase Jitter Measurements

Output Type	V+ (V)	V- (V)	R_T (ohms)	C_{AC}	Zo (ohms)	L (cm)
CML	0	-1.8 ± 5%	Not Used	Not Used	50	2.5
	0	-2.5 ± 5%				
	0	-3.3 ± 5%				
HCSL	1.8 ± 5%	0	Not Used	Not Used	50	2.5
	2.5 ± 5%	0				
	3.3 ± 5%	0				
LVCMOS	0.9 ± 5% (VDD/2 ± 5%)	-0.9 ± 5% (-VDD/2 ± 5%)	Not Used	Not Used	50	2.5

Table 6. Configurations for Phase Jitter Measurements (Cont.)

Output Type	V+ (V)	V- (V)	R_T (ohms)	C_{AC}	Zo (ohms)	L (cm)
LVDS	1.8 ± 5%	0	100	Used	50	2.5
	2.5 ± 5%	0				
	3.3 ± 5%	0				
LVPECL	2	-1.3 ± 5%	Not Used	Not Used	50	2.5

2.4.2 1.8V Specifications

V_{DD} = 1.8V ± 5%, 12kHz to 20MHz integration range.

Table 7. Phase Jitter at 1.8V

Parameter	Symbol	Test Frequency (MHz)	Output Type	Typical	Maximum	Unit
Phase Jitter	Φjit	100	CML	76	90	fs RMS
			HCSL	78	90	
			LVCMOS	77	90	
			LVDS	85	105	
Phase Jitter	Φjit	125	CML	70	84	fs RMS
			HCSL	73	85	
			LVCMOS	70	84	
			LVDS	69	91	
Phase Jitter	Φjit	156.25	CML	55	66	fs RMS
			HCSL	53	62	
			LVCMOS	54	64	
			LVDS	55	64	
Phase Jitter	Φjit	161.132813	CML	52	61	fs RMS
			HCSL	52	61	
			LVCMOS	53	64	
			LVDS	55	66	
Phase Jitter	Φjit	250	CML	62	79	fs RMS
			HCSL	63	73	
			LVCMOS	65	79	
			LVDS	67	79	
Phase Jitter	Φjit	312.5	CML	52	63	fs RMS
			HCSL	50	59	
			LVCMOS	51	59	
			LVDS	52	61	

Table 7. (Cont.)Phase Jitter at 1.8V (Cont.)

Parameter	Symbol	Test Frequency (MHz)	Output Type	Typical	Maximum	Unit
Phase Jitter	Φjit	322.265625	CML	51	61	fs RMS
			HCSL	50	62	
			LVCMOS	53	64	
			LVDS	53	64	
Phase Jitter	Φjit	500	CML	65	75	fs RMS
			HCSL	64	74	
			LVDS	65	75	
Phase Jitter	Φjit	625	CML	62	79	fs RMS
			HCSL	63	73	
			LVDS	65	79	
Phase Jitter	Φjit	644.53125	CML	49	58	fs RMS
			HCSL	48	59	
			LVDS	49	59	
Phase Jitter	Φjit	1250	CML	51	59	fs RMS
			LVDS	52	60	

Table 8. AC Characteristics at 1.8V

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output Rise Time [1]	t_R	CML	168	195	229	ps
		HCSL	148	185	232	
		LVCMOS	152	177	207	
		LVDS	113	156	177	
Output Fall Time [1]	t_F	CML	155	182	229	ps
		HCSL	176	220	280	
		LVCMOS	147	174	207	
		LVDS	176	230	315	
Output Duty Cycle [2]	O_{DC}	$F_{OUT} \leq 1000MHz$	49	50.5	53	%
		$F_{OUT} > 1000MHz$	50	53.2	56	

1. All measurements taken with 20% to 80% thresholds at 156.25MHz
2. All measurements taken at the crossing points for differential signals and at $V_{DD}/2$ for LVCMOS outputs if applicable. Applies to all output configurations.

Table 9. 1.8V DC Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output High Voltage [1]	V_{OH}	CML	1.79	1.8	1.81	V
		HCSL	725	774	825	mV
		LVCMOS, I_{OH} = -2mA	1.6	1.66	1.7	V

Table 9. 1.8V DC Characteristics (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output Low Voltage [1]	V_{OL}	CML	1.0	1.28	1.6	V
		HCSL	0	8	15	mV
		LVCMOS, I_{OL} = 2mA	0	0.1	0.2	V
Output common mode voltage	V_{CMR}	HCSL [2]	0.29	0.36	0.45	V
		LVDS	1.1	1.2	1.31	
TRUE Binary state	V_{OT} (+)	LVDS	218	366	503	mV
FALSE binary state	V_{OT} (-)		-226	-370	-492	
Change in VOT between complementary output states	ΔV_{OT}		-	4.1	79	
Change in VCMR between complementary output states	ΔV_{CMR}		-	22	53	

1. All measurements taken at 156.25MHz.
2. For HCSL V_{CMR} is equivalent to V_{CROSS}.

Table 10. 1.8V Current Consumption

Parameter	Symbol	Output Type	Conditions	Typical	Maximum	Unit
Current Consumption	I_{DD}	CML	F_{OUT} = 156.25MHz	94	101	mA
			F_{OUT} = 1250MHz	104	111	
		HCSL	F_{OUT} = 156.25MHz	109	116	mA
			F_{OUT} = 1250MHz	121	127	
		LVCMOS	F_{OUT} = 156.25MHz	92	101	mA
			F_{OUT} = 322.265625MHz	113	120	
		LVDS	F_{OUT} = 156.25MHz	96	103	mA
			F_{OUT} = 1250MHz	111	118	

2.4.3 2.5V Specifications

V_{DD} = 2.5V ±5%, 12kHz to 20MHz integration range.

Table 11. Phase Jitter at 2.5V

Parameter	Symbol	Test Frequency (MHz)	Output Type	Typical	Maximum	Unit
Phase Jitter	Φjit	100	CML	77	86	fs RMS
			HCSL	76	87	
			LVDS	85	103	
Phase Jitter	Φjit	125	CML	70	86	fs RMS
			HCSL	66	87	
			LVDS	70	103	

Table 11. Phase Jitter at 2.5V (Cont.)

Parameter	Symbol	Test Frequency (MHz)	Output Type	Typical	Maximum	Unit
Phase Jitter	Φjit	156.25	CML	54	66	fs RMS
			HCSL	53	66	
			LVDS	54	66	
Phase Jitter	Φjit	161.132813	CML	53	65	fs RMS
			HCSL	52	64	
			LVDS	54	64	
Phase Jitter	Φjit	250	CML	63	75	fs RMS
			HCSL	63	72	
			LVDS	67	76	
Phase Jitter	Φjit	312.5	CML	51	62	fs RMS
			HCSL	50	62	
			LVDS	51	62	
Phase Jitter	Φjit	322.265625	CML	52	64	fs RMS
			HCSL	50	64	
			LVDS	53	66	
Phase Jitter	Φjit	500	CML	65	74	fs RMS
			HCSL	64	73	
			LVDS	64	77	
Phase Jitter	Φjit	625	CML	50	61	fs RMS
			HCSL	49	61	
			LVDS	49	61	
Phase Jitter	Φjit	644.53125	CML	49	62	fs RMS
			HCSL	48	62	
			LVDS	49	63	
Phase Jitter	Φjit	1250	CML	49	62	fs RMS
			LVDS	49	61	

Table 12. AC Characteristics at 2.5V

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output Rise Time [1]	t_R	CML	153	182	216	ps
		HCSL	162	191	231	
		LVDS	135	152	176	
Output Fall Time [1]	t_F	CML	146	197	232	ps
		HCSL	177	208	257	
		LVDS	183	243	313	

Table 12. (Cont.)AC Characteristics at 2.5V (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output Duty Cycle [2]	O_{DC}	$F_{OUT} \leq 1000MHz$	48	50.5	53.5	%
		CML $F_{OUT} > 1000MHz$	49	52.5	56	

1. All measurements taken with 20% to 80% thresholds at 156.25MHz
2. All measurements taken at the crossing points for differential signals and at $V_{DD}/2$ for LVCMOS outputs.

Table 13. DC Characteristics at 2.5V

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output High Voltage **[1]**	V_{OH}	CML	2.4	2.48	2.5	V
		HCSL	730	794	840	
Output Low Voltage [1]	V_{OL}	CML	1.6	1.89	2.1	V
		HCSL	0	8	20	
Output common mode voltage	V_{CMR}	HCSL[2]	0.3	0.4	0.55	V
		LVDS	1.08	1.2	1.32	
TRUE Binary state	V_{OT} (+)	LVDS	311	382	464	mV
FALSE binary state	V_{OT} (-)	LVDS	307	385	463	
Change in VOT between complementary output states	ΔV_{OT}	LVDS	-	3	21	
Change in VCMR between complementary output states	ΔV_{CMR}	LVDS		27	62	

1. All measurements taken at 156.25MHz
2. For HCSL V_{CMR} is equivalent to V_{CROSS}

Table 14. Current Consumption at 2.5V

Parameter	Symbol	Output Type	Conditions	Typical	Maximum	Unit
Current Consumption	I_{DD}	CML	F_{OUT} = 156.25MHz	94	102	mA
			F_{OUT} = 1250MHz	105	113	
		HCSL	F_{OUT} = 156.25MHz	113	120	mA
			F_{OUT} = 1250MHz	122	129	
		LVDS	F_{OUT} = 156.25MHz	97	105	mA
			F_{OUT} = 1250MHz	109	117	

2.4.4 3.3V Specifications

V_{DD} = 3.3V ± 5%, 12kHz to 20MHz integration range.

Table 15. Phase Jitter at 3.3V

Parameter	Symbol	Test Frequency (MHz)	Output Type	Typical	Maximum	Unit
Phase Jitter	Φjit	100	CML	78	96	fs RMS
			HCSL	75	89	
			LVPECL	87	105	
			LVDS	76	90	
Phase Jitter	Φjit	125	CML	72	85	fs RMS
			HCSL	68	87	
			LVPECL	71	90	
			LVDS	69	86	
Phase Jitter	Φjit	156.25	CML	55	66	fs RMS
			HCSL	54	65	
			LVDS	57	67	
			LVPECL	54	64	
Phase Jitter	Φjit	161.132813	CML	54	68	fs RMS
			HCSL	52	66	
			LVDS	54	68	
			LVPECL	52	64	
Phase Jitter	Φjit	250	CML	63	74	fs RMS
			HCSL	63	71	
			LVPECL	66	78	
			LVDS	62	75	
Phase Jitter	Φjit	312.5	CML	52	62	fs RMS
			HCSL	51	61	
			LVDS	52	62	
			LVPECL	51	61	
Phase Jitter	Φjit	322.265625	CML	52	69	fs RMS
			HCSL	51	66	
			LVDS	54	67	
			LVPECL	51	64	
Phase Jitter	Φjit	500	CML	66	78	fs RMS
			HCSL	64	74	
			LVPECL	65	78	
			LVDS	64	72	

Table 15. Phase Jitter at 3.3V (Cont.)

Parameter	Symbol	Test Frequency (MHz)	Output Type	Typical	Maximum	Unit
Phase Jitter	Φjit	625	CML	50	61	fs RMS
			HCSL	50	61	
			LVDS	50	61	
			LVPECL	49	60	
Phase Jitter	Φjit	644.53125	CML	49	67	fs RMS
			HCSL	49	65	
			LVDS	50	66	
			LVPECL	49	63	
Phase Jitter	Φjit	1250	CML	50	62	fs RMS
			LVDS	49	61	
			LVPECL	49	61	

Table 16. AC Characteristics at 3.3V

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output Rise Time [1]	t_R	CML	144	180	216	ps
		HCSL	162	190	228	
		LVDS	136	152	169	
		LVPECL	147	170	221	
Output Fall Time [1]	t_F	CML	138	190	233	ps
		HCSL	175	204	238	
		LVDS	175	216	259	
		LVPECL	164	200	251	
Output Duty Cycle [2]	O_{DC}	$F_{OUT} \leq 1000MHz$	49	51	53	%
		$F_{OUT} > 1000MHz$	51	53	56	

1. All measurements taken with 20% to 80% thresholds at 156.25MHz.
2. All measurements taken at the crossing points for differential signals and at $V_{DD}/2$ for LVCMOS outputs, if applicable. Applies to all output configurations.

Table 17. DC Characteristics at 3.3V

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output High Voltage [1]	V_{OH}	CML	3.2	3.28	3.3	V
		HCSL	760	820	875	mV
		LVPECL	2.3	2.36	2.41	V
Output Low Voltage [1]	V_{OL}	CML	2.4	2.6	2.9	V
		HCSL	0	8	20	mV
		LVPECL	1.44	1.64	1.84	V

Table 17. DC Characteristics at 3.3V (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output common mode voltage	V_{CMR}	HCSL [2]	0.33	0.40	0.47	V
		LVDS	1.1	1.2	1.3	
		LVPECL	2.22	2.26	2.3	
TRUE Binary state	V_{OT} (+)	LVDS	231	360	490	mV
FALSE binary state	V_{OT} (-)		-233	-362	-492	
Change in VOT between complementary output states	ΔV_{OT}		-	1.7	22	
Change in VCMR between complementary output states	ΔV_{CMR}		-	20.2	35	

1. All measurements taken at 156.25MHz.
2. For HCSL V_{CMR} is equivalent to V_{CROSS}.

Table 18. Current Consumption at 3.3V

Parameter	Symbol	Output Type	Conditions	Typical	Maximum	Unit
Current Consumption	I_{DD}	CML	F_{OUT} = 156.25MHz	97	104	mA
			F_{OUT} = 1250MHz	110	117	
		HCSL	F_{OUT} = 156.25MHz	113	120	mA
			F_{OUT} = 1250MHz	123	130	
		LVPECL	F_{OUT} = 156.25MHz	113	120	mA
			F_{OUT} = 1250MHz	124	132	
		LVDS	F_{OUT} = 156.25MHz	97	104	mA
			F_{OUT} = 1250MHz	110	117	

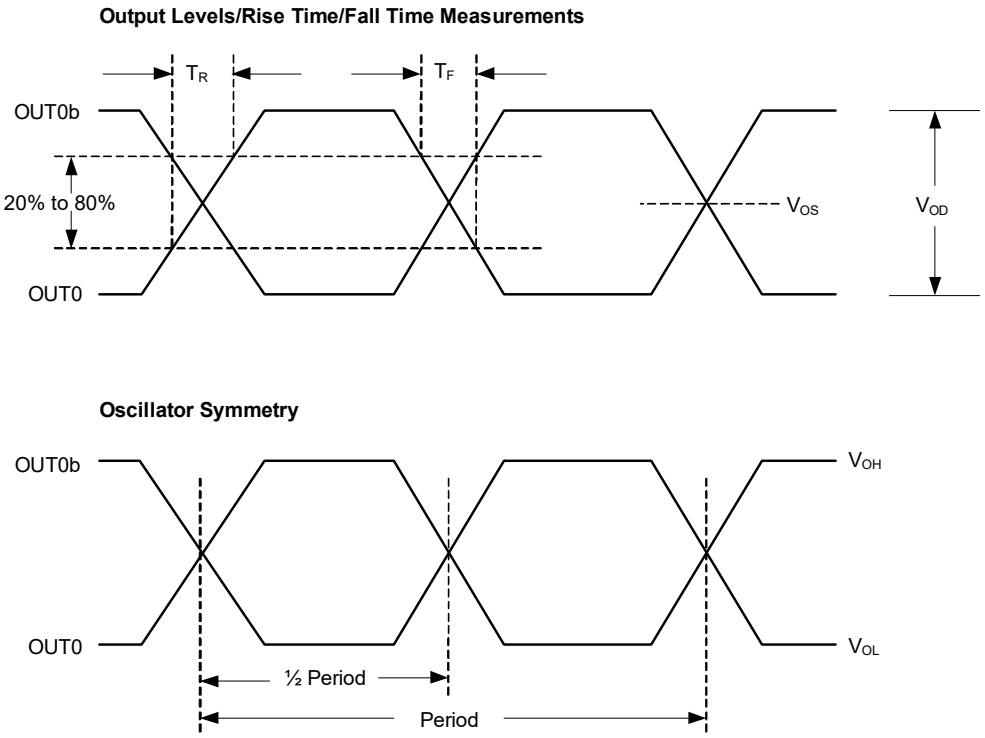

Figure 6. Differential Waveform Measurement Points

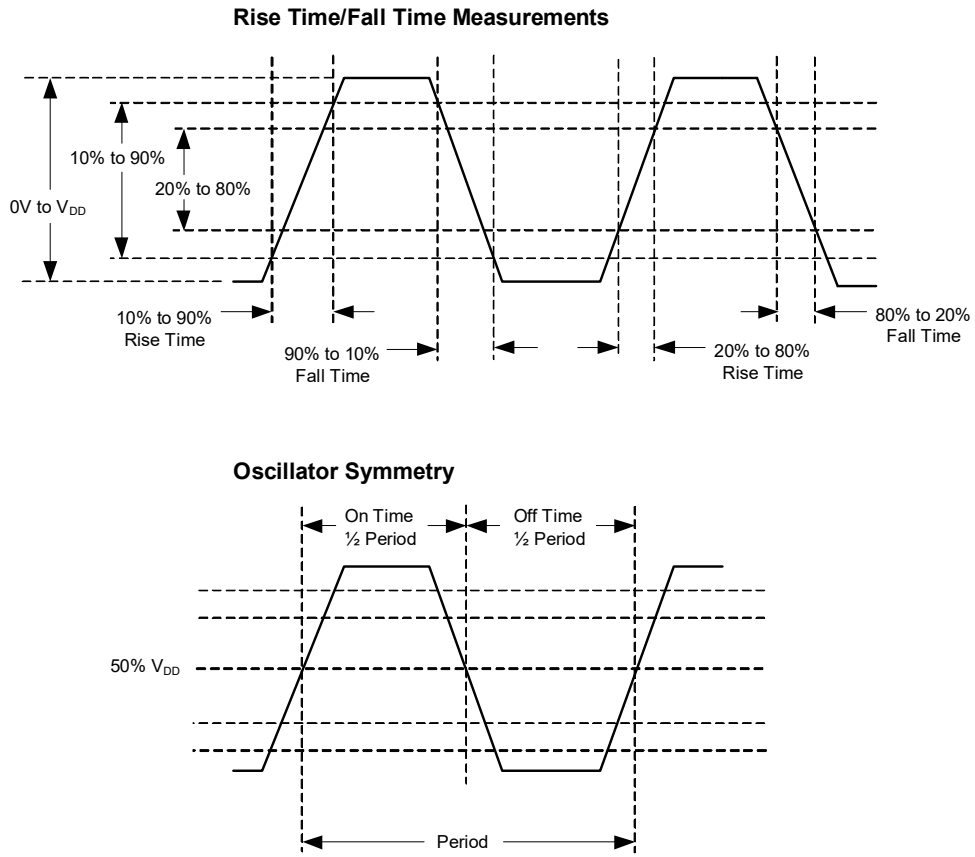

Figure 7. LVCMOS Waveform Measurement Points

3. Typical Performance Graphs

T_A = +25°C, unless otherwise stated.

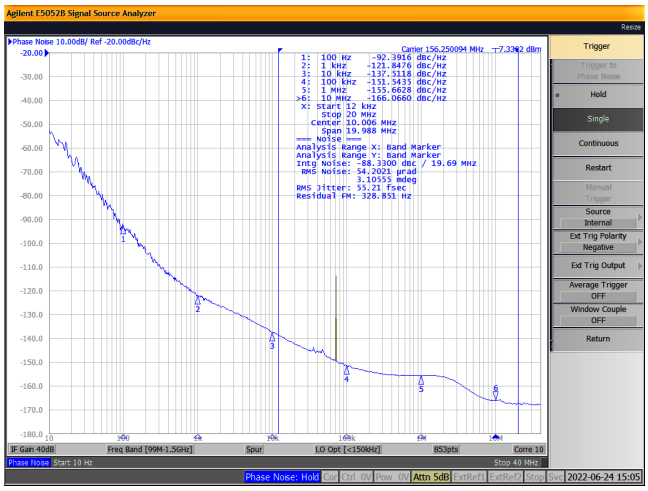

Figure 8. 1.8V LVCMOS, 156.25MHz

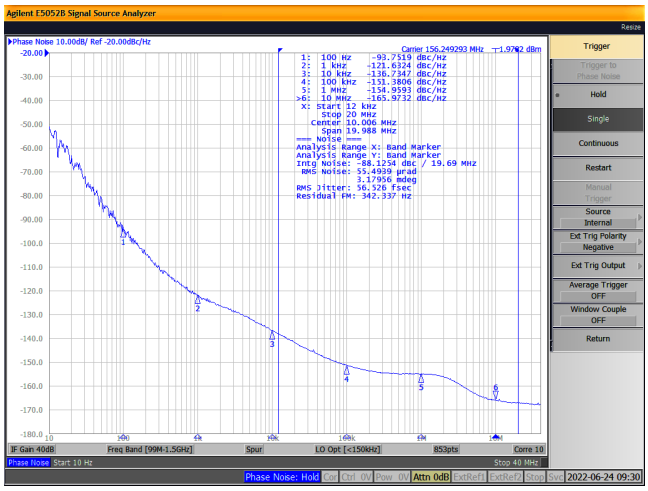

Figure 9. 3.3V HCSL, 156.25MHz

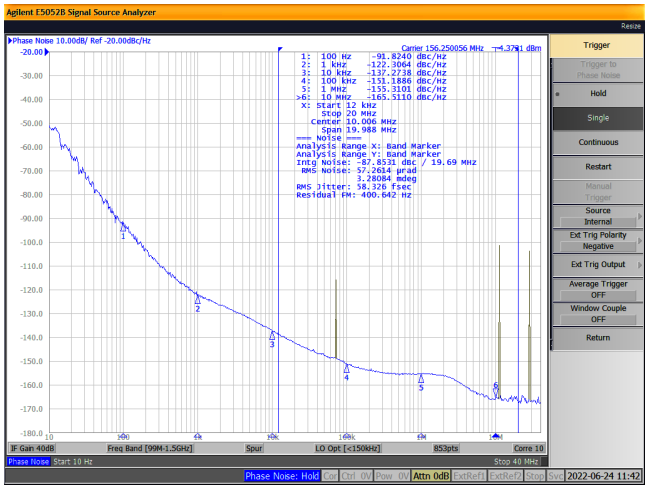

Figure 10. 1.8V LVDS, 156.25MHz

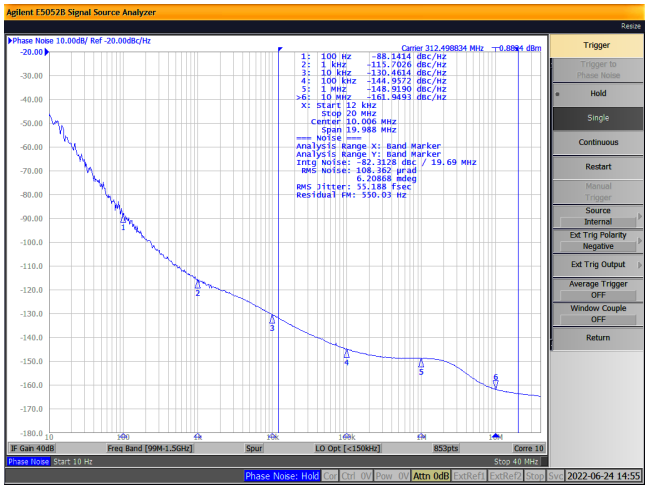

Figure 11. 3.3V LVPECL, 312.5MHz

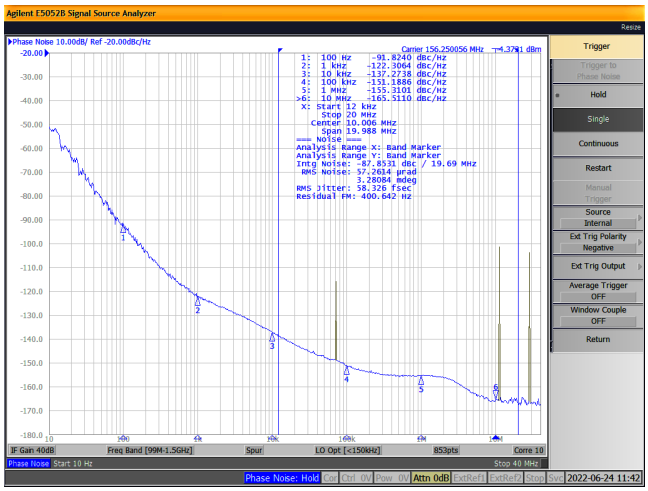

Figure 12. 1.8V HCSL, 156.25MHz

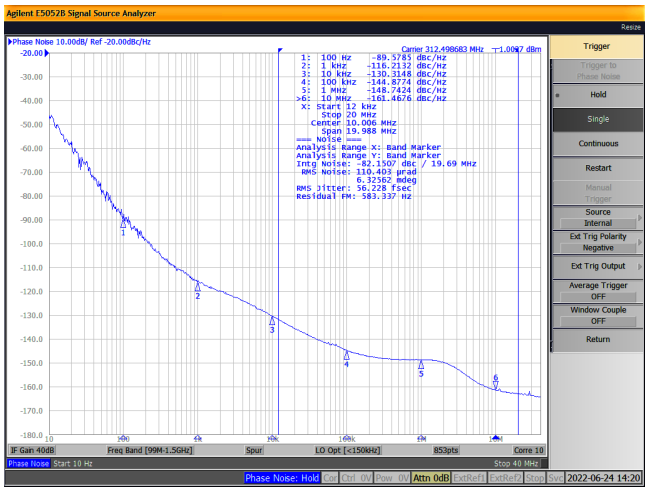

Figure 13. 3.3V CML, 312.5MHz

4. Applications Information

The following figures illustrate recommended termination schemes for each output type. Other terminations are possible, depending on the application requirements. Contact Renesas if other schemes are required.

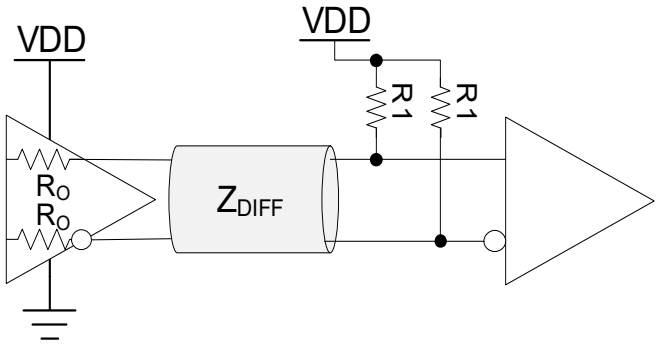

Figure 14. CML Output Termination

Table 19. CML Output Component Values

Output Type	VDD	R_O (ohms)	Z_{DIFF}(ohms)	R1 (ohms)
CML	1.8 ± 5%	NA	100	50
	2.5 ± 5%			
	3.3 ± 5%			

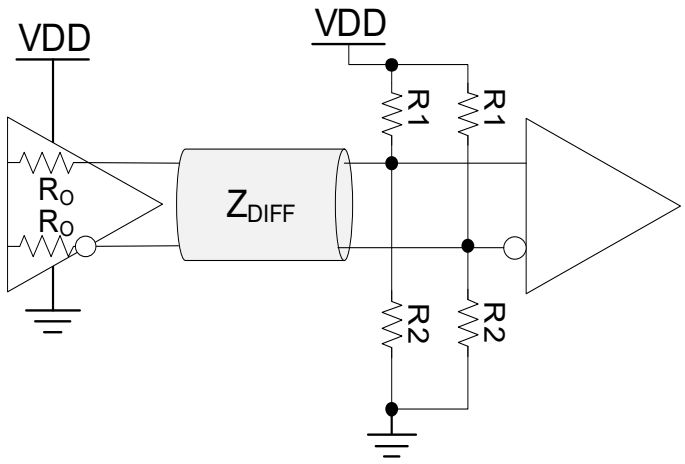

Figure 15. LVPECL Output Termination

Table 20. LVPECL Output Component Values

Output Type	VDD	R_O (ohms)	Z_{DIFF}(ohms)	R1 (ohms)	R2 (ohms)
LVPECL	3.3 ± 5%	NA	100	125	84

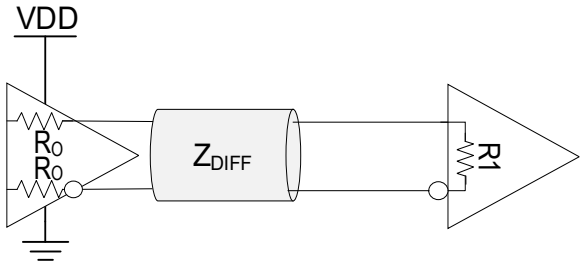

Figure 16. LVDS Output Termination

Table 21. LVDS Output Component Values

Output Type	VDD	R_O (ohms)	Z_{DIFF}(ohms)	R1 (ohms)
LVDS	1.8 ± 5%	NA	100	100
	2.5 ± 5%			
	3.3 ± 5%			

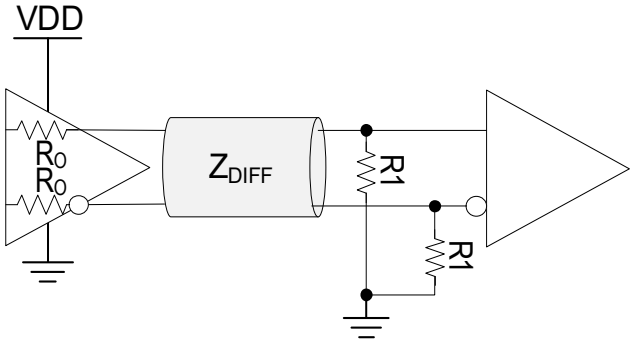

Figure 17. HCSL Output Termination

The ProXO II does not use external series resistors to drive HCSL loads. Only the R1 pull down resistors to ground are required.

Table 22. HCSL Output Component Values

Output Type	VDD	R_O (ohms)	Z_{DIFF}(ohms)	R1 (ohms)
HCSL	1.8 ± 5%	33	100	50
	2.5 ± 5%			
	3.3 ± 5%			

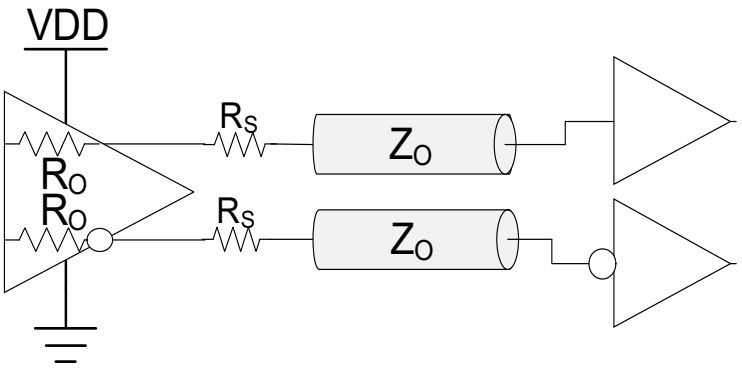

Figure 18. LVCMOS Output Termination

Table 23. LVCMOS Output Component Values

Output Type	VDD	R_O (ohms)	Rs (ohms)	Z_O(ohms)
LVCMOS	1.8 ± 5%	28	22 = Z_O - R_O	50

5. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

6. Marking Diagram

The XK devices provide operating voltage, frequency group and date code information in the crystal top mark, which is mounted on the top of the XK oscillator. Customer-specific configuration information is contained in a factory-readable field stored in the part. The XK device may be configured with up to three frequencies from *a single group*. Frequencies from different groups are not allowed in a single device.

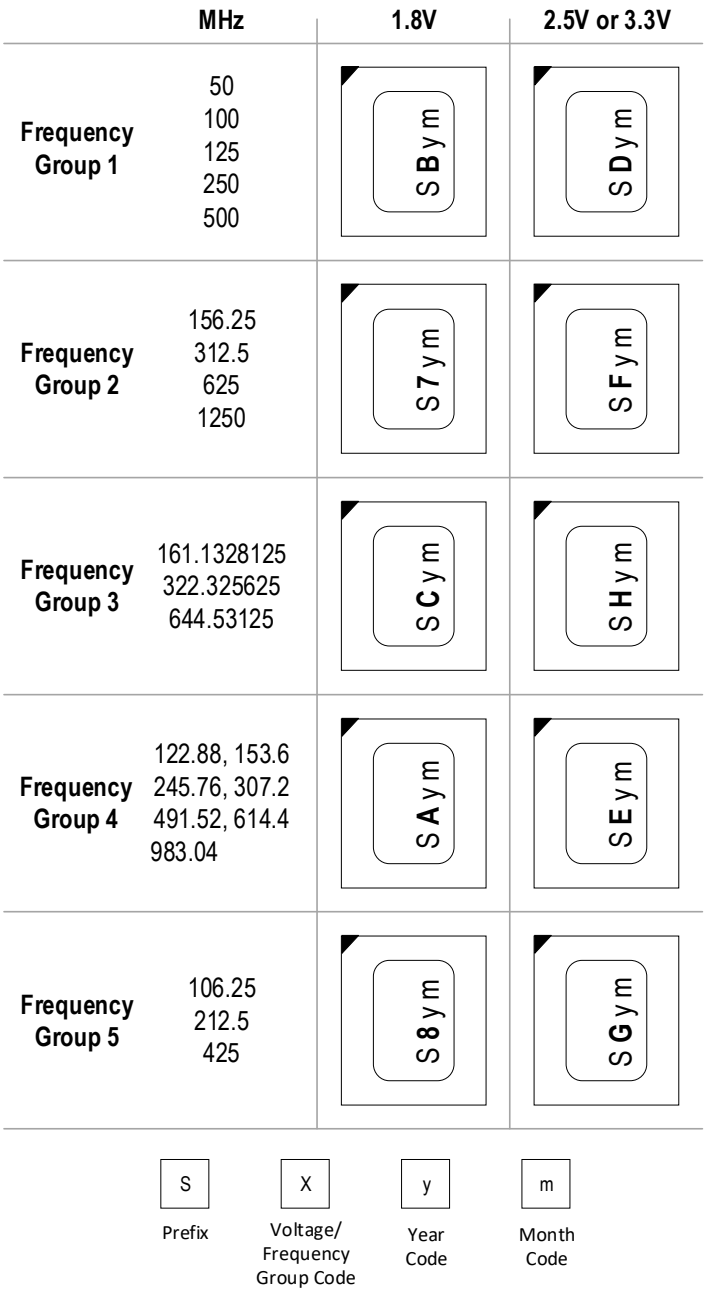

Figure 19. Voltage and Frequency Group Codes and Marking Diagrams

The topside markings consist of four characters as shown in Figure 19. The first character is always the prefix “S.” The second character indicates the operating voltage and the frequency group of the oscillator. The third and fourth character codes year and month) are described in Table 24.

Table 24. Date Codes

Last Digit of Year	Year Code (y)	Month	Month Code (m)
1	A	1	A
2	B	2	B
3	C	3	C
4	D	4	D
5	E	5	E
6	F	6	F
7	G	7	G
8	H	8	H
9	J	9	J
0	K	10	K
-	-	11	L
-	-	12	M

For example, a top mark of “S7DK” would be 1.8V, Frequency Group 2, with a crystal data code of October, 2023. Note that this is the crystal date code and not the silicon date code. The silicon information and customer configuration are stored in the device at the factory.

7. Ordering Information

	Family	Package [1]	Voltage	Config. 1 (FS = low)	Config. 2 (FS = floating)	Config. 3 (FS = high)	Temp. Range
Ordering Code	XK	0 = 1.80 x 1.40 mm [2] 1 = 2.00 x 1.60 mm 2 = 2.50 × 2.00 mm 3 = 3.20 × 2.50 mm	1 = 1.8V ±5% 2 = 2.5V ±5% 3 = 3.3V ±5%	Xfff	Xfff	Xfff	I: -40 to +85°C
		0 = 1.80 x 1.40 mm [3] 1 = 2.00 x 1.60 mm 2 = 2.50 × 2.00 mm 3 = 3.20 × 2.50 mm	1 = 1.8V ±5% only	Xfff	Xfff	Xfff	K: -40 to +105°C
Example	XK	3	3	N156	L312	R625	I

1. The Minimum Order Quantity (MOQ) for tape and reel packing is 2500 pieces. Orders less than 2500 pieces, or the portion of orders that are not multiples of 2500 pieces will be packed on cut tape. For example, a 3500 piece order will be packed as 2500 pieces on tape and reel and 1000 pieces on cut tape.
2. Footprint compatible to 1612 package.
3. Footprint compatible to 1612 package.

The example above gives us the following part number: XK33N156L312R625I. Let us dissect this part number.

We have an XK series XO in a 3225 package running from 3.3V. Three configurations are specified:

- Configuration 1 is a 156.25MHz LVPECL output, with an Active High OE on pin 1.
- Configuration 2 is a 312.5MHz LVDS output with an Active High OE on pin 1.
- Configuration 3 is a 625MHz HCSL output with an Active High OE on pin 1.

The configuration codes are described in Table 25. Note that all configurations in a device must be of the same VDD, OE Pin Polarity, and OE Pin Number assignment. The configurations can consist of different output types and frequencies.

Table 25. Output Configuration Code (X)

Output Type	OE Pin Polarity	OE Pin Number	Code (X)
CML	Active Low	1	D
		2	K
	Active High	1	P
		2	Q
HCSL	Active Low	1	E
		2	T
	Active High	1	R
		2	S
LVCMOS[1]	Active Low	1	A
		2	F
	Active High	1	H
		2	J
LVDS	Active Low	1	B
		2	G
	Active High	1	L
		2	M
LVPECL[2]	Active Low	1	C
		2	I
	Active High	1	N
		2	O

1. VDD must be 1.8 Volts (voltage code 1).
2. VDD must be 3.3 Volts (voltage code 3).

The set of available output frequencies are abbreviated into 3 digit codes to create the order-able part number. These abbreviations are defined in Table 26. If only one configuration is specified, the second and third configurations will be configured identically. If two configurations are specified, the third configuration will be configured identically to the configuration with the lowest frequency. Note that available output frequencies are grouped into frequency groups. Refer to Figure 19 for the definition of the frequency groups.

Table 26. Frequency Codes [1]

Code (fff)	Frequency (MHz)
050	50
100	100
106	106.25
122	122.88
125	125
153	153.6
156	156.25
161	161.1328125
212	212.5
245	245.76
250	250
307	307.2
312	312.5
322	322.265625
425	425
491	491.25
500	500
614	614.4
625	625
644	644.53125
983	983.04
C50	1250

1. Contact Renesas for availability of specific frequencies not listed.

8. Revision History

Revision	Date	Description
1.11	Feb 14, 2024	Updated the “Last Digit of the Year” column in Table 24.
1.10	Dec 4, 2023	▪ Added AC/DC Test Circuit to Common Specifications. ▪ Added Phase Jitter Test Circuit to Common Specifications ▪ Updated Table 7, Table 11, and Table 15 by removing entries that were missing data. ▪ Updated Applications Information with correct termination schemes. ▪ Corrected data sheet title from “Ultra-low Phase Noise Quartz-based PLL Oscillators” to “Ultra-low Phase Noise Quartz-based PLL Oscillator” ▪ Fixed connection error in Figure 17.
1.09	Oct 6, 2023	▪ Updated the 1.80 x 1.40 mm, 2.50 × 2.00 mm, and 3.20 × 2.50 mm PODs. ▪ Updated “Operating Temperature” specifications under Features on first page.
1.08	Sep 6, 2023	Added package outline drawings (POD) links to Ordering Information and “Package options” under Features on front page.
1.07	July 18, 2023	▪ Updated front page text to add reference to 1.8V -40°C to +105°C temperature range. ▪ Added 1.8V K-temperature range (-40°C to +105°C) to Ordering Information. ▪ Completed other minor changes.
1.06	Jun 23, 2023	Updated Frequency Stability in Table 4 to single ±50ppm value.
1.05	Jun 15, 2023	▪ Corrected LVPECL VOH and VOL parameters in Table 17. ▪ Updated 1.8V Frequency Group 4 marking specification in Figure 19. ▪ Added ‘-’ to blank fields in Phase Jitter tables.
1.04	Jun 9, 2023	▪ Corrected marking diagram (Figure 19) with correct Voltage/Frequency Group Codes. ▪ Minor updates to text surrounding Table 24 to be consistent with Figure 19.
1.03	May 9, 2023	▪ Updated marking diagram (Figure 19) to include frequency groups. ▪ Deleted Frequency Groups table as a result.
1.02	Mar 2, 2023	▪ Added 245.76 MHz to Table 26. ▪ Added footnote about shipping quantities and methods to Ordering Information.
1.01	Feb 15, 2023	Added Frequency Group 1 (50/100/125/250/500MHz) data.
1.00	Feb 9, 2023	Initial release.