X9015

Low Noise, Low Power, Volatile Single Digitally Controlled (XDCP™) Potentiometer

FN8157
Rev 6.00
August 14, 2015

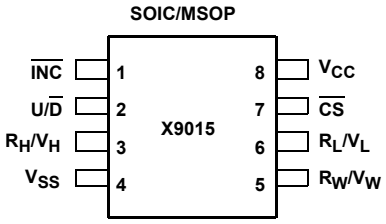
The Intersil X9015 is a 32 tap potentiometer that is volatile. The device consists of a string of 31 resistors that can be programmed to connect the R_W/V_W wiper output with any of the nodes between the connecting resistors. The connection point of the wiper is determined by information communicated to the device on the 3-wire port. The 3-wire port changes the tap position by a falling edge on the increment pin. The direction the wiper moves is determined by the state of the up/down pin. The wiper position at power up is Tap #15.

The X9015 can be used in a wide variety of applications that require a digitally controlled variable resistor to set analog values.

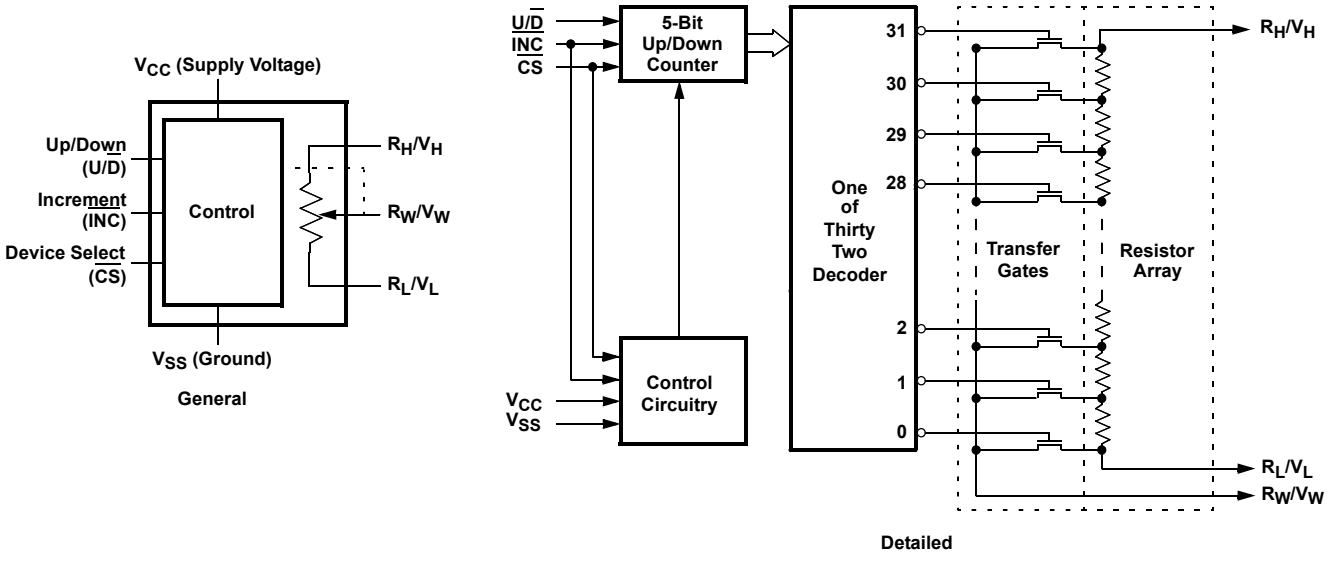
Features

- 32 taps
- Three-wire up/down serial interface
- V_{CC} = 2.7V–5V
- Operating I_{CC} = 50µA max.
- Standby current = 1µA max.
- R_{TOTAL} = 10kΩ, 50kΩ
- Packages 8 Ld SOIC, 8 Ld MSOP
- Pb-free plus anneal available (RoHS compliant)

Pinout



Block Diagram



Ordering Information

PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	R_{TOTAL} (kΩ)	TEMPERATURE RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
X9015WS8ZT1 (Note) **(No longer available, recommended replacement: X9015US8ZT1)**	X9015W Z	5 ±10%	10	0 to +70	8 Ld SOIC Tape and Reel	M8.15
X9015UM8Z (Note)	DCF			0 to +70	8 Ld MSOP	M8.118
X9015UM8IZ* (Note)	DCD			-40 to +85	8 Ld MSOP	M8.118
X9015US8Z* (Note)	X9015U Z			0 to +70	8 Ld SOIC	M8.15
X9015US8IZ* (Note)	X9015U Z I			-40 to +85	8 Ld SOIC	M8.15
X9015WS8Z-2.7* (Note) **(No longer available, recommended replacement: X9015US8Z-2.7)**	X9015W ZF	2.7-5.5	10	0 to +70	8 Ld SOIC	M8.15
X9015UM8Z-2.7* (Note)	DCF		50	0 to +70	8 Ld MSOP	M8.118
X9015UM8IZ-2.7* (Note)	DCE			-40 to +85	8 Ld MSOP	M8.118
X9015US8Z-2.7* (Note)	X9015U ZF			0 to +70	8 Ld SOIC	M8.15
X9015US8IZ-2.7* (Note)	X9015U ZG			-40 to +85	8 Ld SOIC	M8.15

* Add “T1” suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Descriptions

R_H/V_H and R_L/V_L

The high (R_H/V_H) and low (R_L/V_L) terminals of the X9015 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is V_{SS} and the maximum is V_{CC}. The terminology of R_L/V_L and R_H/V_H references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input, and not the voltage potential on the terminal.

R_W/V_W

R_W/V_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 200Ω at V_{CC}=5V. At power up the wiper position is at Tap #15. (V_L/R_L=Tap #0).

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the tap position is incremented or decremented.

Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. When $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH the X9015 will be placed in the low power standby mode until the device is selected once again.

Pin Names

SYMBOL	DESCRIPTION
R_H/V_H	High terminal
R_W/V_W	Wiper terminal
R_L/V_L	Low terminal
V_{SS}	Ground
V_{CC}	Supply voltage
U/$\overline{D}$	Up/Down control input
$\overline{INC}$	Increment control input
$\overline{CS}$	Chip select control input

Principles Of Operation

There are two sections of the X9015: the input control, counter and decode section; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. The resistor array is comprised of 31 individual resistors connected in series.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} (INC to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the wiper position is lost. When power is restored, the wiper is set to Tap #15.

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a five bit counter. The output of this counter is decoded to select one of thirty two wiper positions along the resistive array.

The system may select the X9015, move the wiper and deselect the device. The new wiper position will be maintained until changed by the system or until a power-up/down cycle.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

Mode Selection

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↘	H	Wiper up
L	↘	L	Wiper down
↗	H	X	Standby mode
H	X	X	Standby mode
L	L	X	Normal mode
↘	L	H	Wiper Up (not recommended)
↘	L	L	Wiper Down (not recommended)

Absolute Maximum Ratings

Temperature under bias . . . . . -65°C to +135°C
Storage temperature . . . . . -65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, V_H, V_L and
V_{CC} with respect to V_{SS} . . . . . -1V to +7V
$\Delta V = |V_H - V_L|$ 5V
Lead temperature (soldering 10s) . . . . . +300°C
I_W (10s) . . . . . ±7.5mA

Operating Conditions

Temperature Range
Commercial . . . . . 0°C to +70°C
Industrial . . . . . -40°C to +85°C
Supply Voltage (V_{CC})
X9015 . . . . . 5V ±10%
X9015-2.7 . . . . . 2.7V to 5.5V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Potentiometer Specifications Over recommended operating conditions unless otherwise stated

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	MIN.	TYP.	MAX.	UNIT
R_{TOTAL}	End to End Resistance Variation		–20		+20	%
V_{VH}	V_H/R_H Terminal Voltage		0		V_{CC}	V
V_{VL}	V_L/R_L Terminal Voltage		0		V_{CC}	V
	Power Rating	$R_{TOTAL} \leq 1k\Omega$			10	mW
R_W	Wiper Resistance	I_W = 1mA, V_{CC} = 5V		200	400	Ω
R_W	Wiper Resistance	I_W = 1mA, V_{CC} = 2.7V		400	1000	Ω
I_W	Wiper Current		-3.75		3.75	mA
	Noise	Ref: 1kHz		-120		dBV
	Resolution			3		%
	Absolute Linearity (Note 1)	$V_{w(n)(actual)} - V_{w(n)(expected)}$	-1		+1	MI (Note 3)
	Relative Linearity (Note 2)	$V_{w(n+1)} - [V_{w(n)} + MI]$	-0.2		+0.2	MI (Note 3)
	R_{TOTAL} Temperature Coefficient			±300		ppm/°C
	Ratiometric Temperature Coefficient				±20	ppm/°C
$C_H/C_L/C_W$	Potentiometer Capacitances	See circuit #3		10/10/25		pF

Power Up and Down Requirements

The are no restrictions on the power-up or power-down conditions of V_{CC} and the voltages applied to the potentiometer pins provided that V_{CC} is always more positive than or equal to V_H, V_L, and V_W, i.e., $V_{CC} \geq V_H, V_L, V_W$. The V_{CC} ramp rate spec is always in effect.

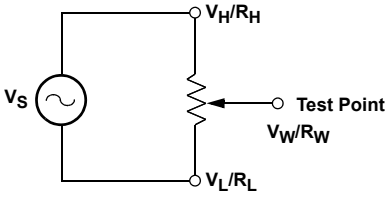
NOTES:

1. Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage = ($V_{w(n)}$(actual)–$V_{w(n)}$(expected)) = ±1 MI Maximum.
2. Relative Linearity is a measure of the error in step size between taps
= $V_{W(n+1)} - [V_{w(n)} + MI]$ = ±0.2 MI.
3. 1 MI = Minimum Increment = $R_{TOT}/31$.
4. Typical values are for T_A = +25°C and nominal supply voltage.
5. This parameter is periodically sampled and not 100% tested.

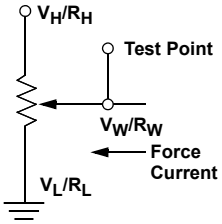
D.C. Operating Specifications *Over recommended operating conditions unless otherwise specified*

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. (Note 4)	MAX.	UNITS
I_{CC1}	V_{CC} active current (increment)	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = 0.4V @ max. t_{CYC}			50	µA
I_{CC2}	V_{CC} active current (Store) (EEPROM Store)	$\overline{CS}$ = V_{IH}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = V_{IH} @ max. t_{WR}			400	µA
I_{SB}	Standby supply current	$\overline{CS}$ = V_{CC} – 0.3V, U/$\overline{D}$ and $\overline{INC}$ = V_{SS} or V_{CC} – 0.3V			1	µA
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input leakage current	V_{IN} = V_{SS} to V_{CC}			±10	µA
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input HIGH voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input LOW voltage		-0.5		V_{CC} x 0.1	V
C_{IN} (Note 5)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input capacitance	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = 25°C, f = 1MHz			10	pF

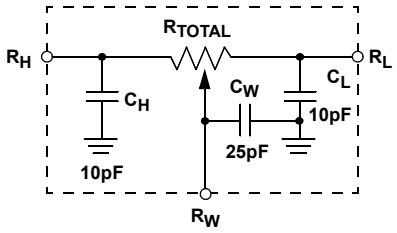
TEST CIRCUIT #1



TEST CIRCUIT #2



CIRCUIT #3 SPICE MACRO MODEL



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

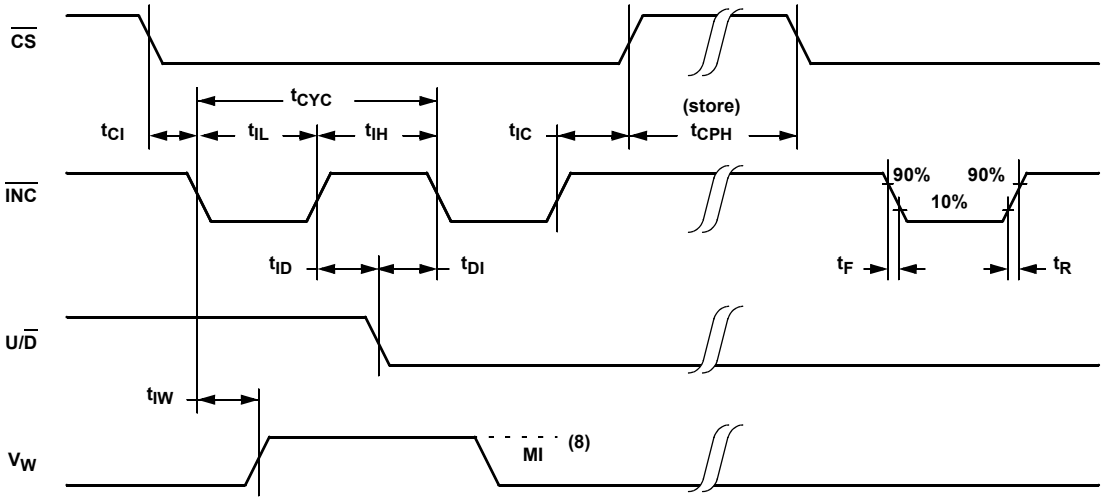
A.C. Conditions of Test

Input pulse levels	0V to 3V
Input rise and fall times	10ns
Input reference levels	1.5V

A.C. Operating Specifications *Over recommended operating conditions unless otherwise specified*

SYMBOL	PARAMETER	MIN.	TYP. (Note 6)	MAX.	UNIT
t_{CI}	$\overline{CS}$ to $\overline{INC}$ setup	100			ns
t_{ID}	$\overline{INC}$ HIGH to U/$\overline{D}$ change	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ setup	2.9			µs
t_{IL}	$\overline{INC}$ LOW period	1			µs
t_{IH}	$\overline{INC}$ HIGH period	1			µs
t_{IC}	$\overline{INC}$ inactive to $\overline{CS}$ inactive	1			µs
t_{CPH}	$\overline{CS}$ deselect time (NO STORE)	100			ns
t_{CPH}	$\overline{CS}$ deselect time (STORE)	10			ms
t_{IW}	$\overline{INC}$ to Vw change		1	5	µs
t_{CYC}	$\overline{INC}$ cycle time	4			µs
t_R, t_F (Note 7)	$\overline{INC}$ input rise and fall time			500	µs
t_{PU}(Note 7)	Power up to wiper stable			5	µs
t_R V_{CC}(Note 7)	V_{CC} power-up rate	0.2		50	V/ms
t_{WR}	Store cycle		5	10	ms

A.C. Timing



NOTES:

6. Typical values are for T_A = +25°C and nominal supply voltage.
7. This parameter is periodically sampled and not 100% tested.
8. MI in the A.C. timing diagram refers to the minimum incremental change in the V_W output due to a change in the wiper position.

Performance Characteristics (Typical)

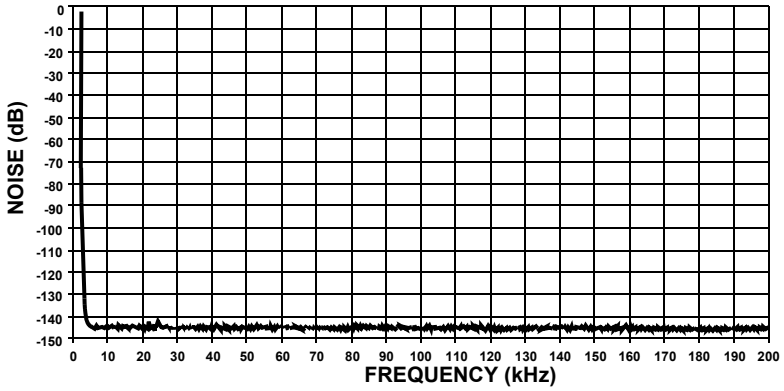


FIGURE 1. TYPICAL NOISE

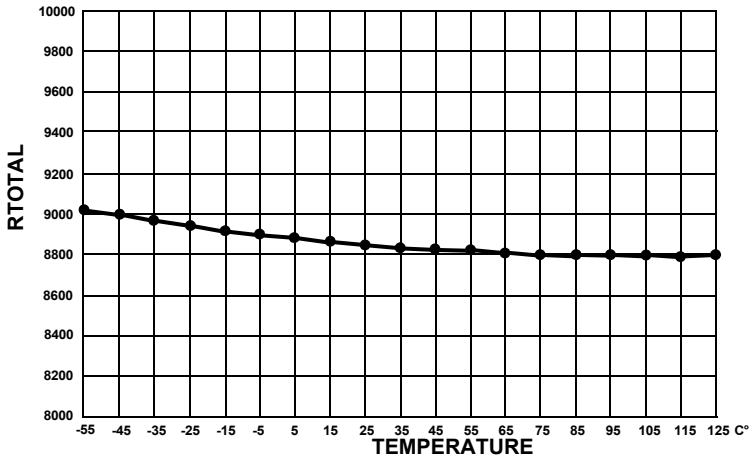


FIGURE 2. TYPICAL RTOTAL VS. TEMPERATURE

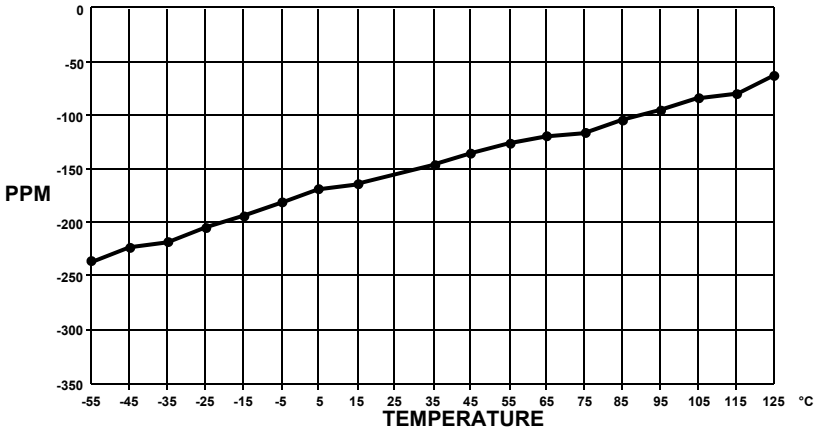


FIGURE 3. TYPICAL TOTAL RESISTANCE TEMPERATURE COEFFICIENT

Performance Characteristics (Typical) (Continued)

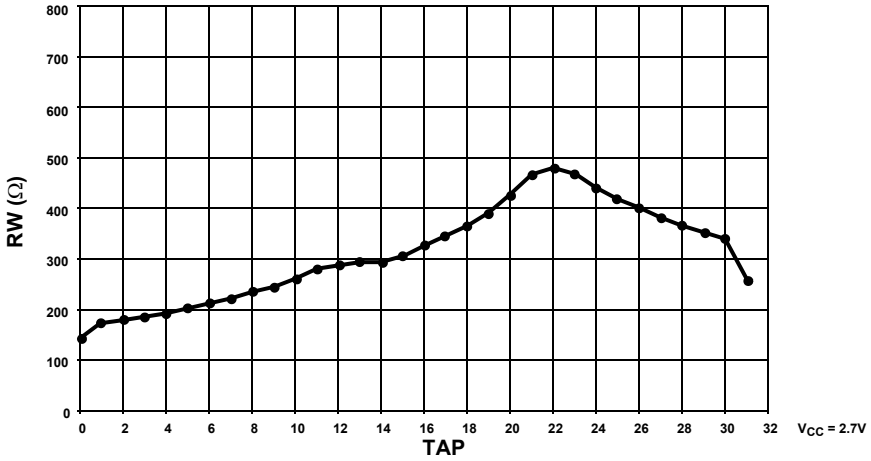


FIGURE 4. TYPICAL WIPER RESISTANCE

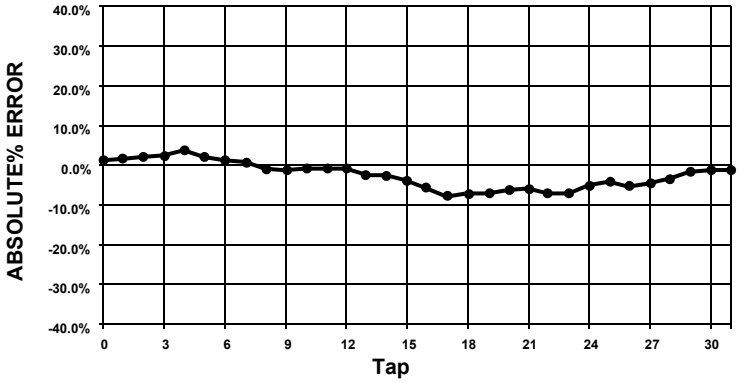


FIGURE 5. TYPICAL ABSOLUTE% ERROR PER TAP POSITION

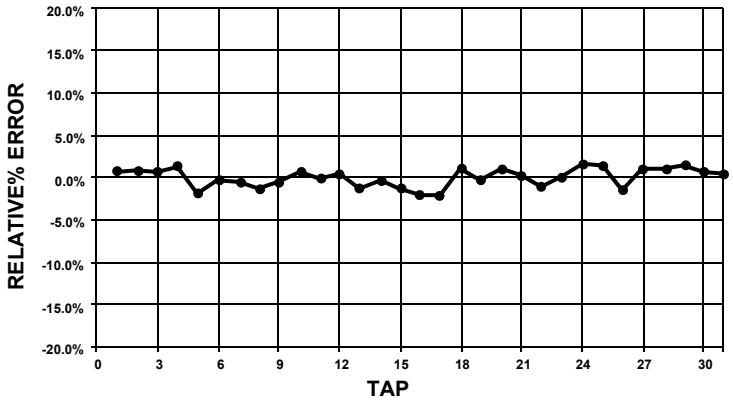
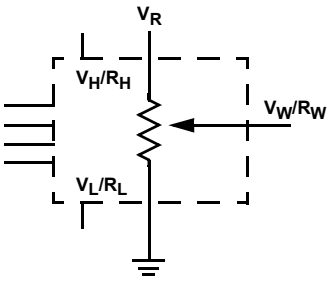


FIGURE 6. TYPICAL RELATIVE% ERROR PER TAP POSITION

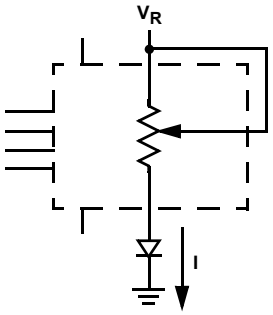
Applications Information

Electronic digitally controlled potentiometers provide two powerful application advantages: (1) the variability and reliability of a solid-state potentiometer, and (2) the flexibility of computer-based digital controls.

Basic Configurations of Electronic Potentiometers



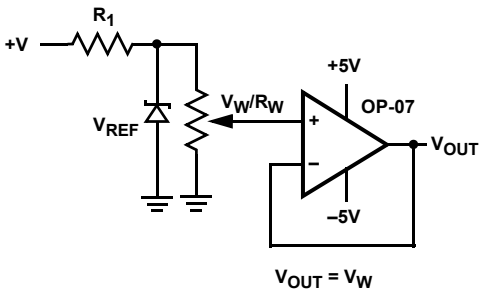
THREE-TERMINAL POTENTIOMETER;
VARIABLE VOLTAGE DIVIDER



TWO-TERMINAL VARIABLE RESISTOR;
VARIABLE CURRENT

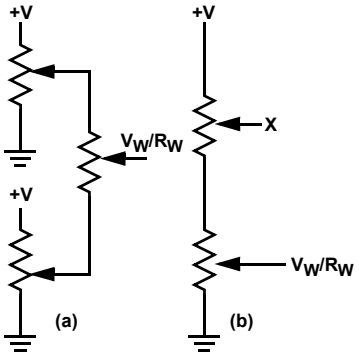
Basic Circuits

Buffered Reference Voltage

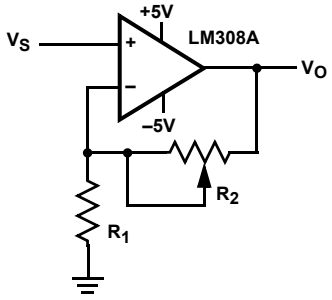


$V_{OUT} = V_W$

Cascading Techniques

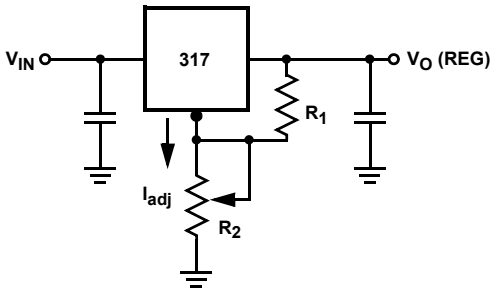


Noninverting Amplifier



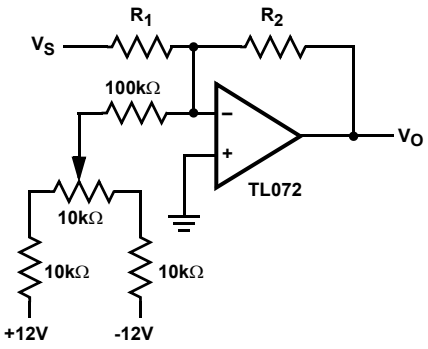
$V_O = (1+R_2/R_1)V_S$

VOLTAGE REGULATOR

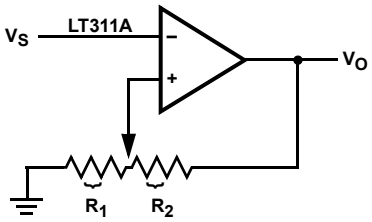


V_O (REG) = 1.25V (1+R_2/R_1)+I_{adj} R_2

OFFSET VOLTAGE ADJUSTMENT



COMPARATOR WITH HYSTERESIS



$V_{UL} = \{R_1/(R_1+R_2)\}\ V_O(max)$
$V_{LL} = \{R_1/(R_1+R_2)\}\ V_O(min)$

(FOR ADDITIONAL CIRCUITS, SEE AN115.)

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 14, 2015	FN8157.6	Updated Ordering Information on page 2. Added Revision History and About Intersil sections. Updated POD M8.118 to most current revision with changes as follows: Corrected lead width dimension in side view 1 from "0.25 - 0.036" to "0.25 - 0.36" Updated to new intersil format by adding land pattern and moving dimensions from table onto drawing. Updated POD M8.15 to most current revision with changes as follows: Changed Note 1 "1982" to "1994" Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205)

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

© Copyright Intersil Americas LLC 2005-2015. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

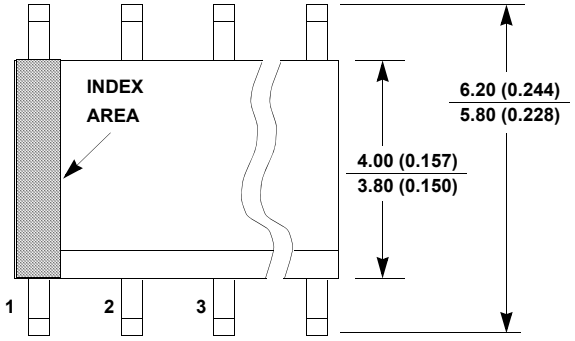
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

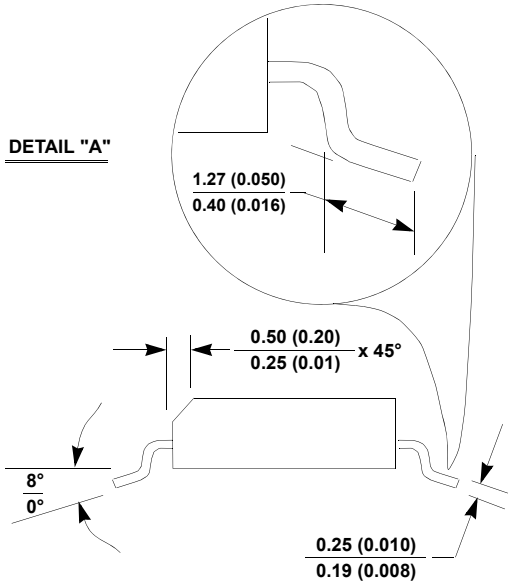
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

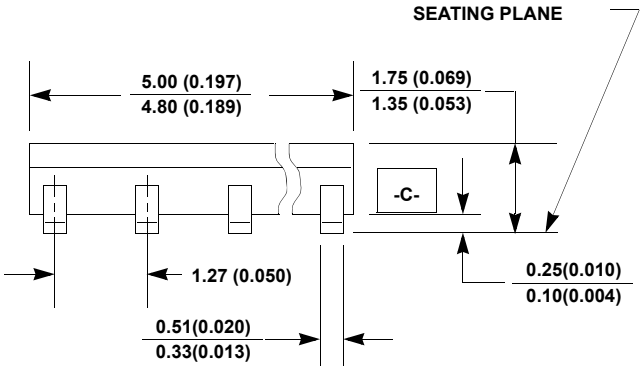
Rev 4, 1/12



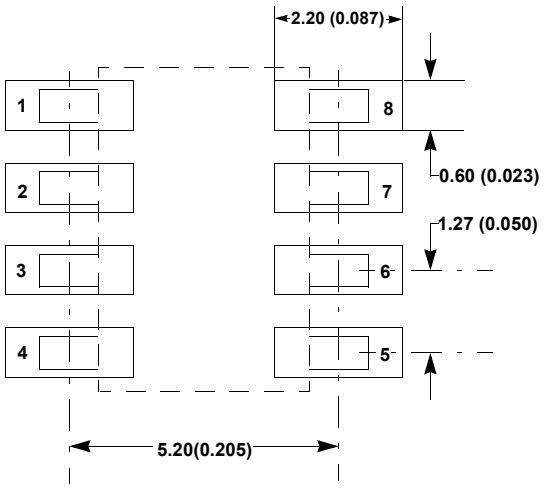
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

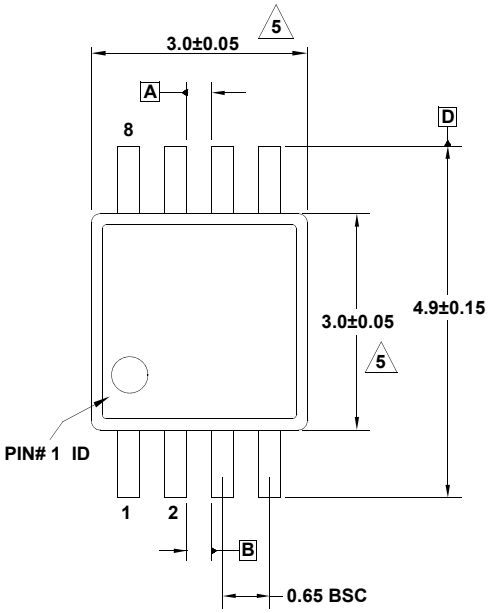
1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Package Outline Drawing

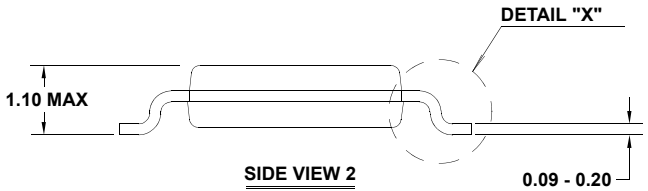
M8.118

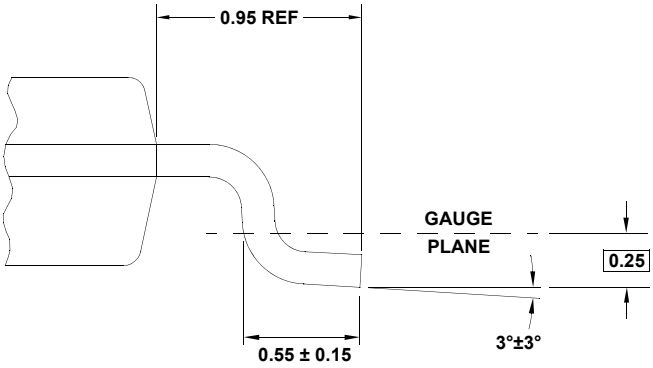
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 4, 7/11

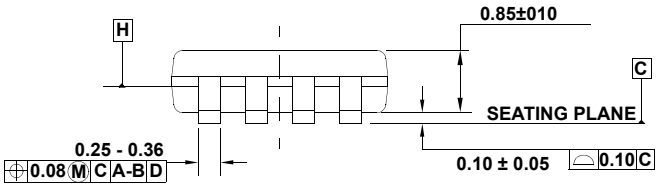


TOP VIEW

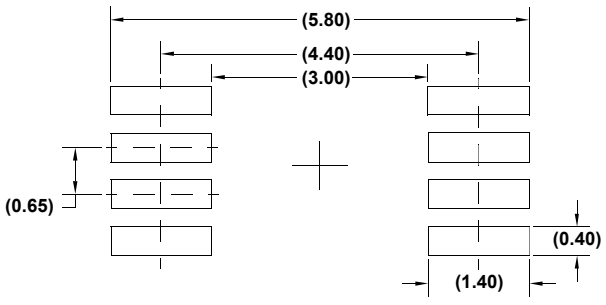




DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.