

X3102

3 Cell Li-Ion Battery Protection and Monitor IC

FN8246
Rev 0.00
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The X3102 is a protection and monitor IC for use in battery packs consisting of 3 series Lithium-Ion battery cells. The device provides internal over-charge, over-discharge, and overcurrent protection circuitry, internal EEPROM memory, an internal voltage regulator, and internal drive circuitry for external FET devices that control cell charge, discharge, and cell voltage balancing.

Over-charge, over-discharge, and overcurrent thresholds reside in an internal EEPROM memory register and are selected independently via software using a 3MHz SPI serial interface. Detection and time-out delays can also be individually varied using external capacitors.

Using an internal analog multiplexer, the X3102 allows battery parameters such as cell voltage and current (using a sense resistor) to be monitored externally by a separate microcontroller with A/D converter. Software on this microcontroller implements gas gauge and cell balancing functionality in software.

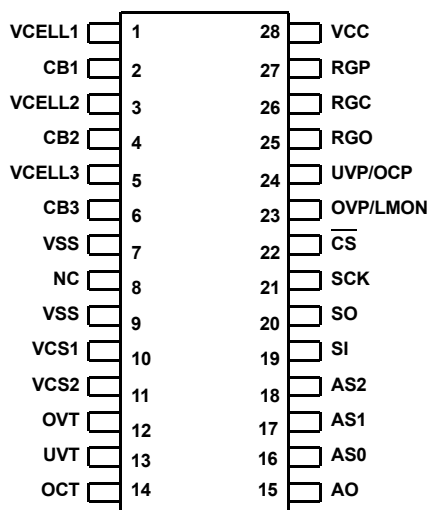
The X3102 contains a current sense amplifier. Selectable gains of 10, 25, 80 and 160 allow an external 10 bit A/D converter to achieve better resolution than a more expensive 14 bit converter.

An internal 4kbit EEPROM memory featuring IDLock™, allows the designer to partition and “lock in” written battery cell/pack data.

The X3102 is housed in a 28 Pin TSSOP package.

Pinout

X3102 (TSSOP)
TOP VIEW



Features

- Software Selectable Protection Levels and Variable Protect Detection/Release Times
- Integrated FET Drive Circuitry
- Cell Voltage and Current Monitoring
- 0.5% Accurate Voltage Regulator
- Integrated 4kbit EEPROM
- Flexible Power Management with 1µA Sleep Mode
- Cell Balancing Control

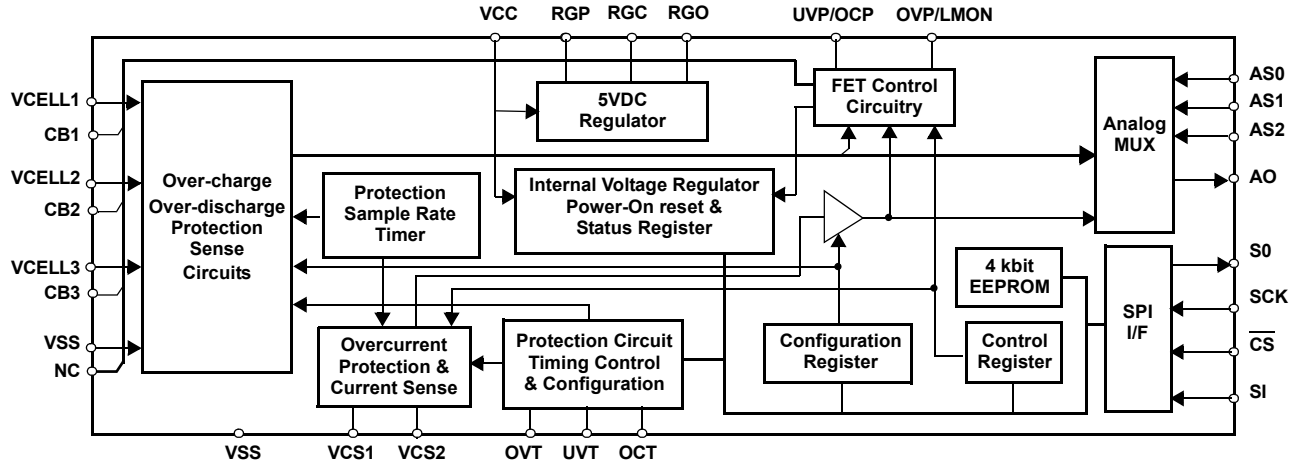
Benefit

- Optimize protection for chosen cells to allow maximum use of pack capacity.
- Reduce component count and cost
- Simplify implementation of gas gauge
- Accurate voltage and current measurements
- Record battery history to optimize gas gauge, track pack failures and monitor system use
- Reduce power to extend battery life
- Increase battery capacity and improve cycle life battery life

Ordering Information

PART NUMBER	V _{CC} LIMITS	TEMP. RANGE (°C)	PACKAGE
X3102V28	6V to 24V	-20 to +70	28 Ld TSSOP

Functional Diagram



Pin Names

PIN	SYMBOL	DESCRIPTION
1	VCELL1	Battery cell 1 voltage input. This pin is used to monitor the voltage of this battery cell internally. The voltage of an individual cell can also be monitored externally at pin AO. The X3102 monitors 3 battery cells.
2	CB1	Cell balancing FET control output 1. This output is used to switch an external FET in order to perform cell voltage balancing control. This function can be used to adjust an individual cell voltage (e.g., during cell charging). CB1 can be driven high (Vcc) or low (Vss) to switch the external FET ON/OFF.
3	VCELL2	Battery cell 2 voltage. This pin is used to monitor the voltage of this battery cell internally. The voltage of an individual cell can also be monitored externally at pin AO. The X3102 monitors 3 battery cells.
4	CB2	Cell balancing FET control output 2. This output is used to switch an external FET in order to perform cell voltage balancing control. This function can be used to adjust individual cell voltages (e.g., during cell charging). CB2 can be driven high (Vcc) or low (Vss) to switch the external FET ON/OFF.
5	VCELL3	Battery cell 3 voltage. This pin is used to monitor the voltage of each battery cell internally. The voltage of an individual cell can also be monitored externally at pin AO. The X3102 monitors 3 battery cells.
6	CB3	Cell balancing FET control output 3. This output is used to switch an external FET in order to perform cell voltage balancing control. This function can be used to adjust an individual cell voltage (e.g., during cell charging). CB3 can be driven high (Vcc) or low (Vss) to switch the external FET ON/OFF.
7	VSS	Ground.
8	NC	No Connect.
9	VSS	Ground.
10	VCS1	Current sense voltage pin 1. A sense resistor (R_{SENSE}) is connected between VCS1 and VCS2 (Figure 1). R_{SENSE} has a resistance in the order of 20m Ω to 100m Ω , and is used to monitor current flowing through the battery terminals, and protect against overcurrent conditions. The voltage at each end of R_{SENSE} can also be monitored at pin AO.
11	VCS2	Current sense voltage pin 2. A sense resistor (R_{SENSE}) is connected between VCS1 and VCS2 (Figure 1). R_{SENSE} has a resistance in the order of 20m Ω to 100m Ω , and is used to monitor current flowing through the battery terminals, and protect against overcurrent conditions. The voltage at each end of R_{SENSE} can also be monitored at pin AO.
12	OVT	Over-charge detect/release time input. This pin is used to control the delay time (T_{OV}) associated with the detection of an over-charge condition (See section "Over-charge Protection" on page 19).
13	UVT	Over-discharge detect/release time input. This pin is used to control the delay times associated with the detection (T_{UV}) and release (T_{UVR}) of an over-discharge (undervoltage) condition (See section "Over-discharge Protection" on page 20).
14	OCT	Overcurrent detect/release time input. This pin is used to control the delay times associated with the detection (T_{OC}) and release (T_{OCR}) of an overcurrent condition (See section "Overcurrent Protection" on page 23).

Pin Names (Continued)

PIN	SYMBOL	DESCRIPTION
15	AO	Analog multiplexer output. The analog output pin is used to externally monitor various battery parameter voltages. The voltages which can be monitored at AO (See section "Analog Multiplexer Selection" on page 25) are: – Individual cell voltages – Voltage across the current sense resistor (R_{SENSE}): This voltage is amplified with a gain set by the user in the control register (See section "Current Monitor Function" on page 25.) The analog select pins AS0–AS2 select the desired voltage to be monitored on the AO pin.
16	AS0	Analog output select pin 0. These pins select which voltage is to be multiplexed to the output AO (See section "Sleep Control (SLP)" on page 17 and section "Current Monitor Function" on page 25)
17	AS1	Analog output select pin 1. These pins select which voltage is to be multiplexed to the output AO (See section "Sleep Control (SLP)" on page 17 and section "Current Monitor Function" on page 25)
18	AS2	Analog output select pin 2. These pins select which voltage is to be multiplexed to the output AO (See section "Sleep Control (SLP)" on page 17 and section "Current Monitor Function" on page 25)
19	SI	Serial data input. SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the device are input on this pin.
20	SO	Serial data output. SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock. While \overline{CS} is HIGH, SO will be in a High Impedance state. Note: SI and SO may be tied together to form one line (SI/SO). In this case, all serial data communication with the X3102 is undertaken over one I/O line. This is permitted ONLY if no simultaneous read/write operations occur.
21	SCK	Serial data clock input. The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.
22	\overline{CS}	Chip select input pin. When \overline{CS} is HIGH, the device is deselected and the SO output pin is at high impedance. \overline{CS} LOW enables the SPI serial bus.
23	OVP/LMON	Over-charge Voltage Protection output/Load Monitor output. This one pin performs two functions depending upon the present mode of operation of the X3102. Over-charge Voltage Protection (OVP) This pin controls the switching of the battery pack charge FET. This power FET is a P-channel device. As such, cell charge is possible when OVP/LMON= V_{SS} , and cell charge is prohibited when OVP/LMON= V_{CC} . In this configuration the X3102 turns off the charge voltage when the cells reach the over-charge limit. This prevents damage to the battery cells due to the application of charging voltage for an extended period of time (See section "Over-charge Protection" on page 19). Load Monitor (LMON) In Overcurrent Protection mode, a small test current (7.5 μ A typ.) is passed out of this pin to sense the load resistance. The measured load resistance determines whether or not the X3102 returns from an overcurrent protection mode (See section "Overcurrent Protection" on page 23).
24	UVP/OCP	Over-discharge protection output/Overcurrent protection output. Pin UVP/OCP controls the battery cell discharge via an external power FET. This P-channel FET allows cell discharge when UVP/OCP= V_{SS} , and prevents cell discharge when UVP/OCP= V_{CC} . The X3102 turns the external power FET off when the X3102 detects either: Over-discharge Protection (UVP) In this case, pin 24 is referred to as "Over-discharge (Undervoltage) protection (UVP)" (See section "Over-discharge Protection" on page 20). UVP/OCP turns off the FET to prevent damage to the battery cells by being discharged to excessively low voltages. Overcurrent protection (OCP) In this case, pin 24 is referred to as "Overcurrent protection (OCP)" (See section "Overcurrent Protection" on page 23). UVP/OCP turns off the FET to prevent damage to the battery pack caused by excessive current drain (e.g. as in the case of a surge current resulting from a stalled disk drive).
25	RGO	Voltage regulator output pin. This pin is an input that connects to the collector of an external PNP transistor. The voltage at this pin is the regulated output voltage, but it also provides the feedback voltage for the regulator and the operating voltage for the device.
26	RGC	Voltage regulator control pin. This pin connects to the base of an external PNP transistor and controls the transistor turn on.
27	RGP	Voltage regulator protection pin. This pin is an input that connects to the emitter of an external PNP transistor and an external current limit resistor and provides a current limit voltage.
28	VCC	Power supply. This pin is provides the voltage for FET control, regulator operation, and wake-up circuits.

Absolute Maximum Ratings

Storage temperature	-55 to 125°C
Operating temperature	-40 to 85°C
DC output current	5mA
Lead temperature (soldering 10s)	300°C
Power supply voltage, V _{CC}	V _{SS} -0.5 to V _{SS} +27.0V
Cell voltage, V _{CELL}	-0.5 to 6.75V
Terminal voltage, V _{TERM1} (Pins: SCK, SI, SO, CS, AS0, AS1, AS2, VCS1, VCS2, OVT, UVT, OCT, AO)	V _{SS} -0.5 to V _{RGO} + 0.5V
Terminal voltage, V _{TERM2} (VCELL1)	V _{SS} -0.5 to V _{CC} + 1.0V
Terminal voltage V _{TERM3} , (all other pins)	V _{SS} -0.5 to V _{CC} + 0.5V

Recommended Operating Conditions

Commercial	-20°C to +70°C
Supply Voltage Range	6V to 24V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications Over the recommended operating conditions, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
I _{LI}	Input leakage current (SCK, SI, \overline{CS} , AS0, AS1, AS2)			±10	μA
I _{LO}	Output leakage current (SO)			±10	μA
V _{IL} (Note 1)	Input LOW voltage (SCK, SI, \overline{CS} , AS0, AS1, AS2)		-0.3	V _{RGO} × 0.3	V
V _{IH} (Note 1)	Input HIGH voltage (SCK, SI, \overline{CS} , AS0, AS1, AS2)		V _{RGO} × 0.7	V _{RGO} + 0.3	V
VOL1	Output LOW voltage (SO)	I _{OL} = 1.0mA		0.4	V
VOH1	Output HIGH voltage (SO)	I _{OH} = -0.4mA	V _{RGO} - 0.8		V
VOL2	Output LOW voltage (UVP/OCF, OVP/LMON, CB1-CB4)	I _{OL} = 100μA		0.4	V
VOH2	Output HIGH voltage (UVP/OCF, OVP/LMON, CB1-CB4)	I _{OH} = -20μA	V _{CC} - 0.4		V
VOL3	Output LOW voltage (RGC)	I _{OL} = 2mA, RGP = V _{CC} , RGO = 5V		0.4	V
VOH3	Output HIGH voltage (RGC)	I _{OH} = -20μA, RGP = V _{CC} - 4V, RGO = 5V	V _{CC} - 4.0		V

NOTE:

1. V_{IL} min. and V_{IH} max. are for reference only and are not 100% tested.

Operating Specifications Over the recommended operating conditions unless otherwise specified

SYMBOL	DESCRIPTION	CONDITION	MIN	TYP (Note 2)	MAX	UNIT
V _{RGO}	5V regulated voltage	On power up or at wake-up	4.5		5.5	V
		After self-tuning (@ 10mA V _{RGO} current; 25°C)	4.97	4.99	5.01	
		After self-tuning (@ 10mA V _{RGO} current; 0-50°C) (Note 5)	4.95		5.02	
		After self-tuning (@ 50mA V _{RGO} current) (Note 5)	4.90		5.00	V
I _{LMT} (Note 3)	5VDC voltage regulator current limit	R _{LMT} = 10Ω		250		mA
I _{CC1}	V _{CC} supply current (1)	Normal operation		85	250	μA
I _{CC2}	V _{CC} supply current (2)	during nonvolatile EEPROM write		1.3	2.5	mA
I _{CC3}	V _{CC} supply current (3)	During EEPROM read SCK = 3.3MHz		0.9	1.2	mA
I _{CC4}	V _{CC} supply current (4)	Sleep mode			1	μA
I _{CC5}	V _{CC} supply current (5)	Monitor mode AN2, AN1, AN0 not equal to 0		365	600	μA

Operating Specifications Over the recommended operating conditions unless otherwise specified **(Continued)**

SYMBOL	DESCRIPTION	CONDITION	MIN	TYP (Note 2)	MAX	UNIT	
V_{OV} (Note 4)	Cell over-charge protection mode voltage threshold (Default in Boldface)	$V_{OV} = 4.20V (V_{OV1}, V_{OV0} = 0,0)$		4.10		4.275	V
			0°C to 50°C	4.15		4.25	
		$V_{OV} = 4.25V (V_{OV1}, V_{OV0} = 0,1)$		4.15		4.325	V
			0°C to 50°C	4.20		4.30	V
		$V_{OV} = 4.30V (V_{OV1}, V_{OV0} = 1,0)$		4.2		4.375	V
		0°C to 50°C	4.25		4.35	V	
		$V_{OV} = 4.35V (V_{OV1}, V_{OV0} = 1,1)$		4.25		4.425	V
			0°C to 50°C	4.30		4.40	V
V_{OVR}	Cell over-charge protection mode release voltage threshold			$V_{OV} - 0.20$		V	
T_{OV}	Cell over-charge detection time	$C_{OV} = 0.1\mu F$		1		s	
V_{UV} (Note 4)	Cell over-discharge protection mode (SLEEP) threshold. (Default in Boldface)	$V_{UV} = 2.25V (V_{UV1}, V_{UV0} = 0,0)$		2.15		2.35	V
		$V_{UV} = 2.35V (V_{UV1}, V_{UV0} = 0,1)$		2.25		2.45	V
		$V_{UV} = 2.45V (V_{UV1}, V_{UV0} = 1,0)$		2.35		2.55	V
		$V_{UV} = 2.55V (V_{UV1}, V_{UV0} = 1,1)$		2.45		2.65	V
V_{UVR}	Cell over-discharge protection mode release threshold			$V_{UV} + 0.6$		V	
T_{UV}	Cell over-discharge detection time	$C_{UV} = 0.1\mu F$		1		s	
		$C_{UV} = 200pF$		2		ms	
T_{UVR}	Cell over-discharge release time	$C_{UV} = 0.1\mu F$		7		ms	
		$C_{UV} = 200pF$		100		μs	
V_{OC} (Note 4)	Overcurrent mode detection voltage (Default in Boldface)	$V_{OC} = 0.075V (V_{OC1}, V_{OC0} = 0,0)$		0.050		0.100	V
			0°C to 50°C	0.060		0.090	
		$V_{OC} = 0.100V (V_{OC1}, V_{OC0} = 0,1)$		0.075		0.125	V
			0°C to 50°C	0.085		0.115	
		$V_{OC} = 0.125V (V_{OC1}, V_{OC0} = 1,0)$		0.100		0.150	V
		0°C to 50°C	0.110		0.140		
		$V_{OC} = 0.150V (V_{OC1}, V_{OC0} = 1,1)$		0.125		0.175	V
			0°C to 50°C	0.135		0.165	
T_{OC}	Overcurrent mode detection time	$C_{OC} = 0.001\mu F$		10		ms	
		$C_{OC} = 200pF$		2		ms	
T_{OCR}	Overcurrent mode release time	$C_{OC} = 0.001\mu F$		10		ms	
		$C_{OC} = 200pF$		2		ms	
R_{OCR}	Load resistance overcurrent mode release condition	Releases when OVP/LMON pin > 2.5V		250		k Ω	

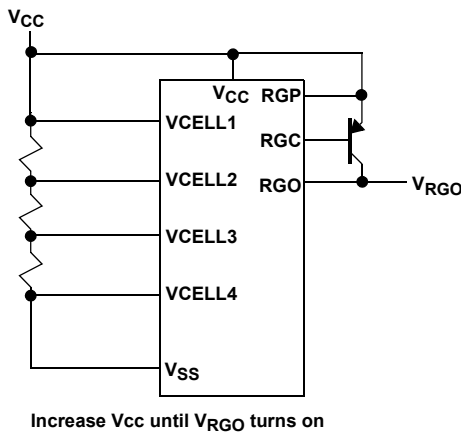
Operating Specifications Over the recommended operating conditions unless otherwise specified **(Continued)**

SYMBOL	DESCRIPTION	CONDITION	MIN	TYP (Note 2)	MAX	UNIT
V _{CE}	Cell charge threshold voltage	V _{CE} = 0.5V (V _{CE1} , V _{CE0} = 0,0)	0.4	0.5	0.6	V
		V _{CE} = 0.8V (V _{CE1} , V _{CE0} = 0,1)	0.7	0.8	0.9	V
		V _{CE} = 1.1V (V _{CE1} , V _{CE0} = 1,0)	1	1.1	1.2	V
		V_{CE} = 1.4V (V_{ce1}, V_{CE0} = 1,1)	1.3	1.4	1.5	V
V _{SLR}	X3102 wake-up voltage (For V _{cc} above this voltage, the device wakes up)	(See Wake-up test circuit) 0°C to 50°C	8.5	9.5	11.2	V
V _{SLP}	X3102 sleep voltage (For V _{cc} above this voltage, the device cannot go to sleep)	(See Sleep test circuit) 0°C to 50°C	7.5	8.8	10.5	V

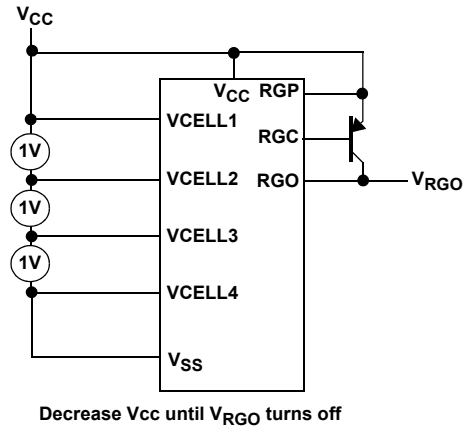
NOTES:

2. Typical at 25°C.
3. See Figure 10 on page 21.
4. The default setting is set at the time of shipping, but may be changed by the user via changes in the configuration register.
5. For reference only, this parameter is not 100% tested.

Test Circuits



WAKE-UP TEST CIRCUIT



SLEEP TEST CIRCUIT

Power-Up Timing

SYMBOL	PARAMETER	MIN	MAX	UNIT
t _{PUR} (Note 6)	Power-up to SPI read operation (RDSTAT, EEREAD STAT)		T _{OC} + 2ms	ms
t _{P_{UW1}} (Note 6)	Power-up to SPI write operation (WREN, WRDI, EEWRITE, WCFIG, SET IDL, WCNTR)		T _{OC} + 2ms	ms
t _{P_{UW2}} (Note 6)	Power-up to SPI write operation (WCNTR - bits 10 and 11)		T _{OV} + 200ms or T _{UV} + 200ms (Note 7)	ms

NOTES:

6. t_{PUR}, t_{P_{UW1}} and t_{P_{UW2}} are the delays required from the time V_{CC} is stable until a read or write can be initiated. These parameters are not 100% tested.
7. Whichever is longer.

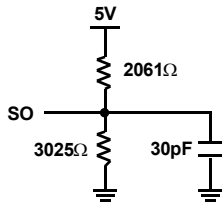
Capacitance $T_A = +25^\circ\text{C}$, $f = 1\text{MHz}$, $V_{\text{RGO}} = 5\text{V}$

SYMBOL	PARAMETER	CONDITIONS	MAX	UNITS
C _{OUT} (Note 8)	Output capacitance (SO)	$V_{\text{OUT}} = 0\text{V}$	8	pF
C _{IN} (Note 8)	Input capacitance (SCK, SI, $\overline{\text{CS}}$)	$V_{\text{IN}} = 0\text{V}$	6	pF

NOTE:

8. This parameter is not 100% tested.

Equivalent A.C. Load Circuit



A.C. Test Conditions

Input pulse levels	0.5 – 4.5V
Input rise and fall times	10ns
Input and output timing level	2.5V

A.C. Characteristics (Over the recommended operating conditions, unless otherwise specified.)

Serial Input Timing

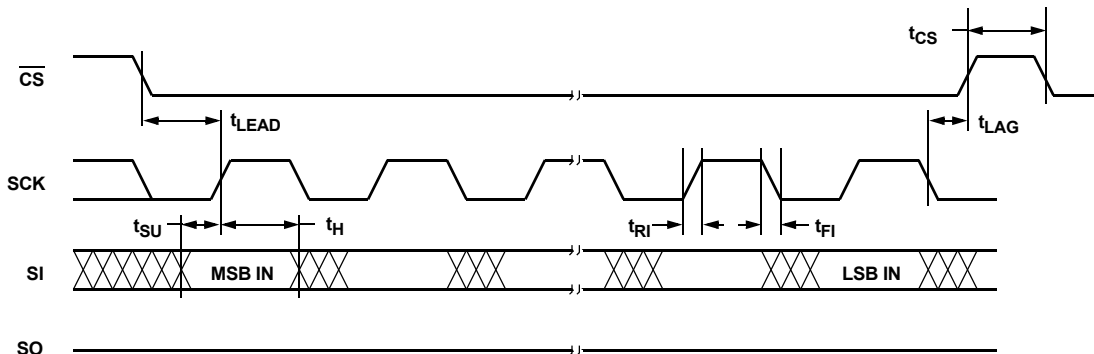
SYMBOL	PARAMETER	MIN	MAX	UNITS
f_{SCK}	Clock frequency	0	3.3	MHz
t_{CYC}	Cycle time	300		ns
t_{LEAD}	$\overline{\text{CS}}$ lead time	150		ns
t_{LAG}	$\overline{\text{CS}}$ lag time	150		ns
t_{WH}	Clock HIGH time	130		ns
t_{WL}	Clock LOW time	130		ns
t_{SU}	Data setup time	20		ns
t_{H}	Data hold time	20		ns
t_{RI} (Note 9)	Data in rise time		2	μs
t_{FI} (Note 9)	Data in fall time		2	μs
t_{CS}	$\overline{\text{CS}}$ deselect time	100		ns
t_{WC} (Note 10)	Write cycle time		5	ms

NOTES:

9. This parameter is not 100% tested.

10. t_{WC} is the time from the rising edge of $\overline{\text{CS}}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

Serial Input Timing



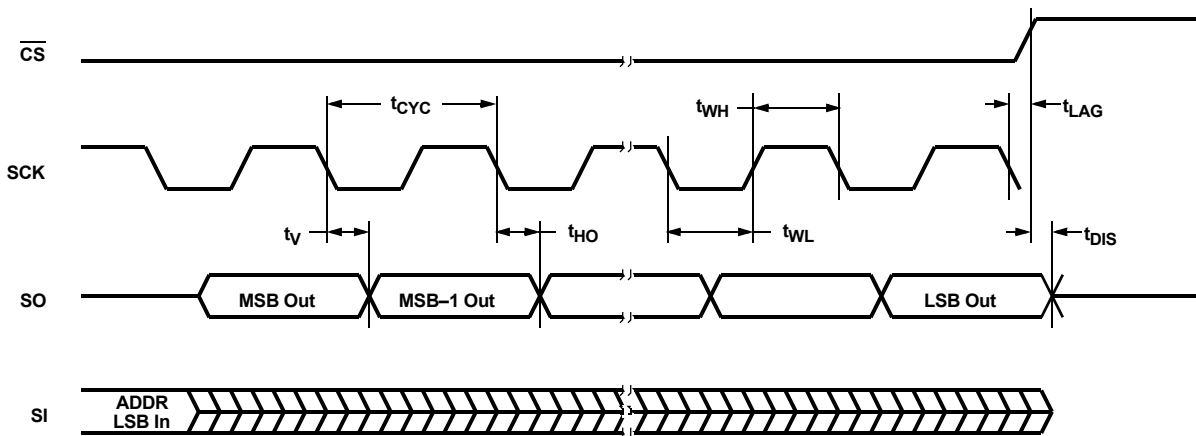
Serial Output Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS
f_{SCK}	Clock Frequency	0	3.3	MHz
t_{DIS}	Output Disable Time		150	ns
t_V	Output Valid from Clock LOW		130	ns
t_{HO}	Output Hold Time	0		ns
t_{RO} (Note 11)	Output Rise Time		50	ns
t_{FO} (Note 11)	Output Fall Time		50	ns

NOTE:

11. This parameter is not 100% tested.

Serial Output Timing



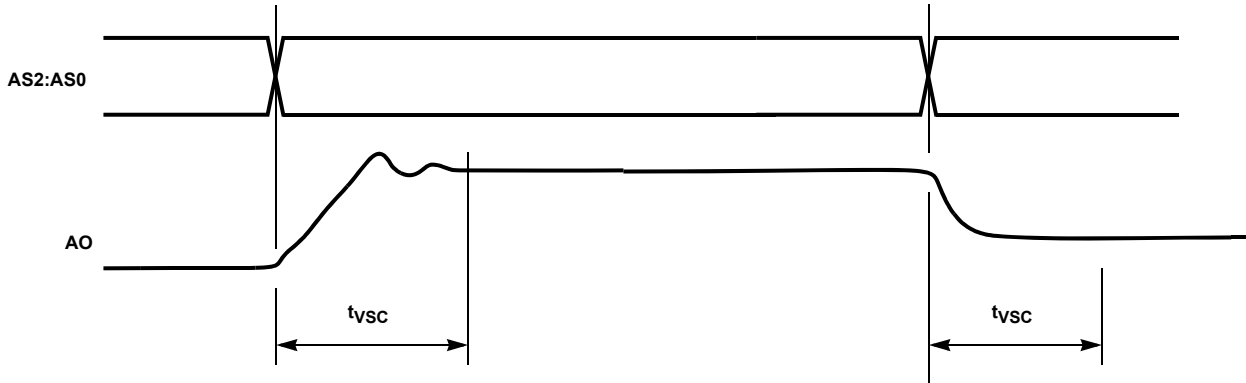
Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

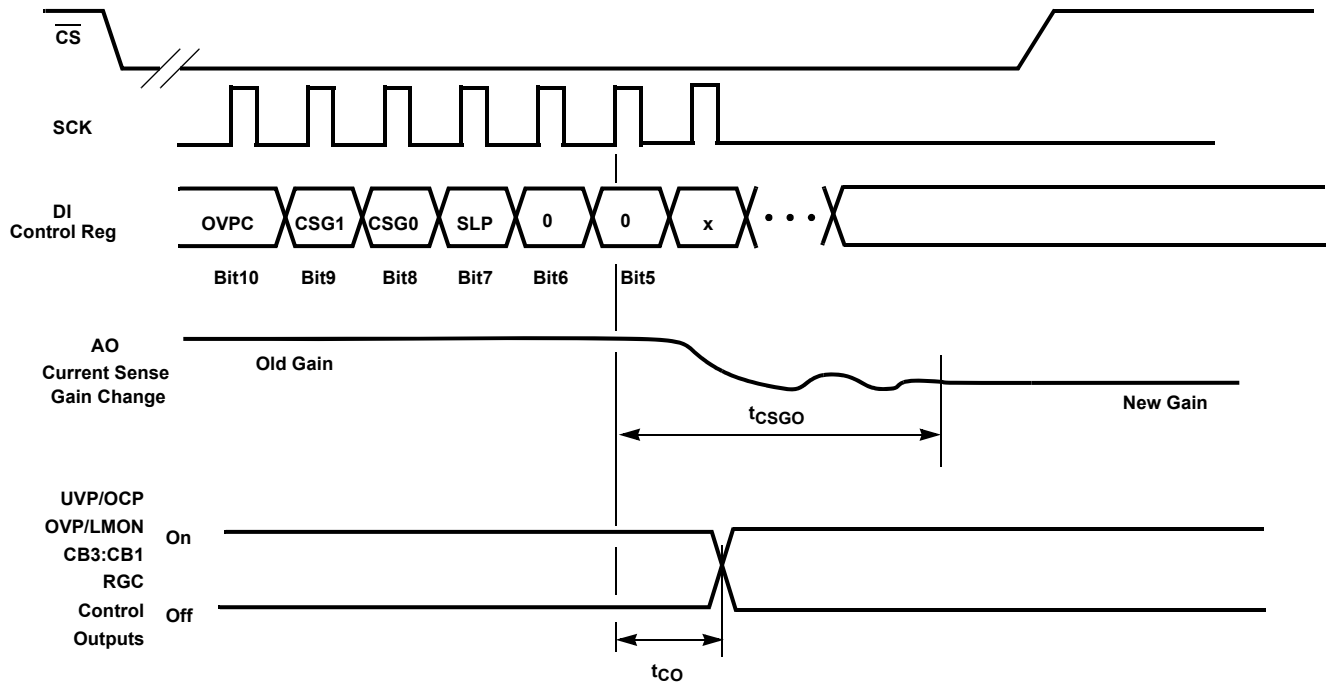
Analog Output Response Time

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{VSC}	AO Output Stabilization Time (Voltage Source Change)			1.0	ms
t_{CSGO}	AO Output Stabilization Time (Current Sense Gain Change)			1.0	ms
t_{CO}	Control Outputs Response Time (UVP/OCP, OVP/MON, CB4, CB3, CB2, CB1, RGC)			1.0	μ s

Change in Voltage Source



Change in Current Sense Gain Amplification and Control Bits



Typical Operating Characteristics

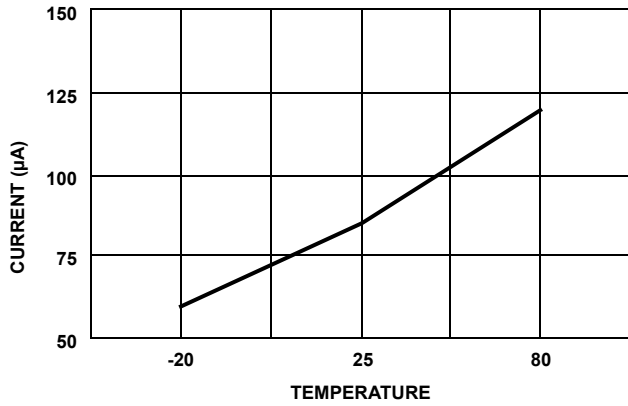


FIGURE 1. NORMAL OPERATING CURRENT

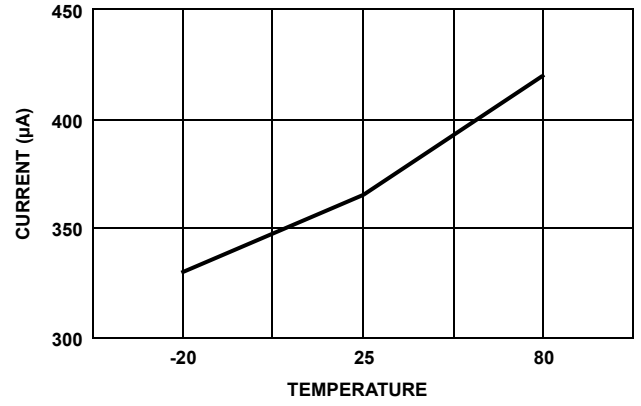


FIGURE 2. MONITOR MODE CURRENT

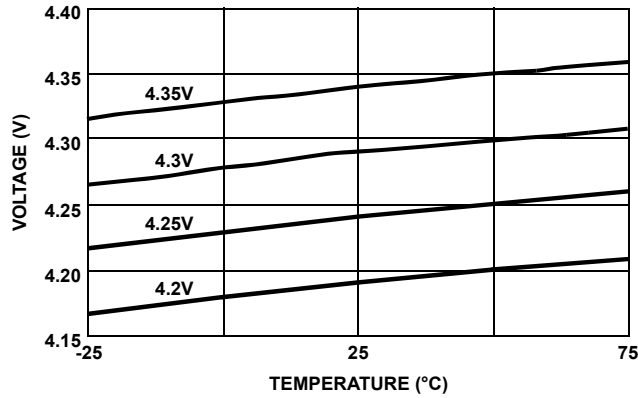


FIGURE 3. OVER CHARGE TRIP VOLTAGE (TYPICAL)

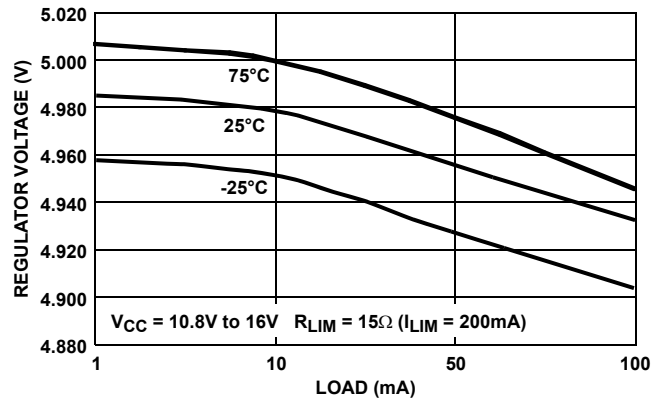


FIGURE 4. VOLTAGE REGULATOR OUTPUT (TYPICAL)

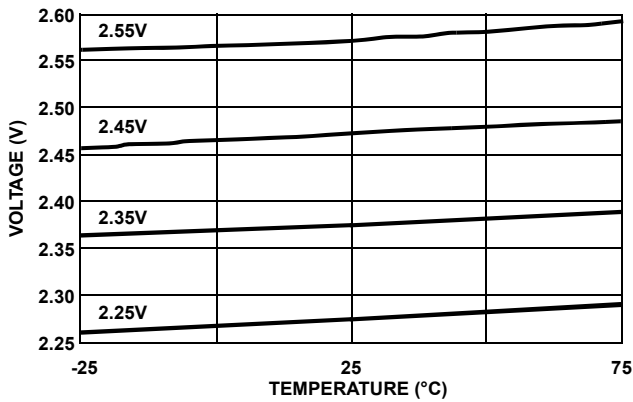


FIGURE 5. OVER DISCHARGE TRIP VOLTAGE (TYPICAL)

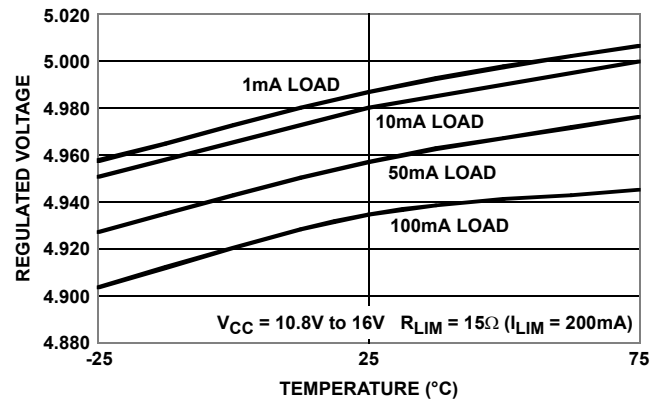


FIGURE 6. VOLTAGE REGULATOR OUTPUT (TYPICAL)

Principles of Operation

The X3102 provides two distinct levels of functionality and battery cell protection:

First, in Normal mode, the device periodically checks each cell for an over-charge and over-discharge state, while continuously watching for a pack overcurrent condition. A protection mode violation results from an over-charge, over-discharge, or overcurrent state. The thresholds for these states are selected by the user through software. When one of these conditions occur, a Discharge FET or a Charge FET or both FETs are turned off to protect the battery pack. In an over-discharge condition, the X3102 device goes into a low power sleep mode to conserve battery power. During sleep, the voltage regulator turns off, removing power from the microcontroller to further reduce pack current.

Second, in Monitor mode, a microcontroller with A/D converter measures battery cell voltage and pack current via pin AO and the X3102 on-board MUX. The user can thus implement protection, charge/discharge, cell balancing or gas gauge software algorithms to suit the specific application and characteristics of the cells used. While monitoring these voltages, all protection circuits are on continuously.

In a typical application, the microcontroller is also programmed to provide an SMBus interface along with the Smart Battery System interface protocols. These additions allow an X3102 based module to adhere to the latest industry battery pack standards.

Typical Application Circuit

The X3102 has been designed to operate correctly when used as connected in the Typical Application Circuit (See Figure 7).

The power MOSFET's Q1 and Q2 are referred to as the "Discharge FET" and "Charge FET," respectively. Since these FETs are p-channel devices, they will be ON when the gates are at V_{SS} , and OFF when the gates are at V_{CC} . As their names imply, the discharge FET is used to control cell discharge, while the charge FET is used to control cell charge. Diode D1 allows the battery cells to receive charge even if the Discharge FET is OFF, while diode D2 allows the cells to discharge even if the charge FET is OFF. D1 and D2 are integral to the Power FETs. It should be noted that the cells can neither charge nor discharge if both the charge FET and discharge FET are OFF.

Power to the X3102 is applied to pin VCC via diodes D6 and D7. These diodes allow the device to be powered by the Li-Ion battery cells in normal operating conditions, and allow the device to be powered by an external source (such as a charger) via pin P+ when the battery cells are being charged. These diodes should have sufficient current and voltage ratings to handle both cases of battery cell charge and discharge.

The operation of the voltage regulator is described in section "Voltage Regulator" on page 26. This regulator provides a $5VDC \pm 0.5\%$ output. The capacitor (C1) connected from RGO to ground provides some noise filtering on the RGO output. The recommended value is $0.1\mu F$ or less. The value chosen must allow V_{RGO} to decay to $0.1V$ in $170ms$ or less when the X3102 enters the sleep mode. If the decay is slower than this, a resistor (R1) can be placed in parallel with the capacitor.

During an initial turn-on period ($T_{PUR} + T_{OC}$), V_{RGO} has a stable, regulated output in the range of $5VDC \pm 10\%$ (See Figure 8). The selection of the microcontroller should take this into consideration. At the end of this turn on period, the X3102 "self-tunes" the output of the voltage regulator to $5V \pm 0.5\%$. As such, V_{RGO} can be used as a reference voltage for the A/D converter in the microcontroller. Repeated power up operations, consistently re-apply the same "tuned" value for V_{RGO} .

Figure 1 shows a battery pack temperature sensor implemented as a simple resistive voltage divider, utilizing a thermistor (R_T) and resistor (R_T'). The voltage V_T can be fed to the A/D input of a microcontroller and used to measure and monitor the temperature of the battery cells. R_T' should be chosen with consideration of the dynamic resistance range of R_T as well as the input voltage range of the microcontroller A/D input. An output of the microcontroller can be used to turn on the thermistor divider to allow periodic turn-on of the sensor. This reduces power consumption since the resistor string is not always drawing current.

Diode D3 is included to facilitate load monitoring in an overcurrent protection mode (See section "Overcurrent Protection" on page 23), while preventing the flow of current into pin OVP/LMON during normal operation. The N-Channel transistor turns off this function during the sleep mode.

Resistor R_{PU} is connected across the gate and drain of the charge FET (Q2). The discharge FET Q1 is turned off by the X3102, and hence the voltage at pin OVP/LMON will be (at maximum) equal to the voltage of the battery terminal, minus one forward biased diode voltage drop ($V_{P+} - V_{D7}$). Since the drain of Q2 is connected to a higher potential (V_{P+}) a pull-up resistor (R_{PU}) in the order of $1M\Omega$ should be used to ensure that the charge FET is completely turned OFF when $OVP/LMON = V_{CC}$.

The capacitors on the V_{CELL1} to V_{CELL4} inputs are used in a first order low pass filter configuration, at the battery cell voltage monitoring inputs (V_{CELL1} – V_{CELL4}) of the X3102. This filter is used to block any unwanted interference signals from being inadvertently injected into the monitor inputs. These interference signals may result from:

- Transients created at battery contacts when the battery pack is being connected/disconnected from the charger or the host.
- Electrostatic discharge (ESD) from something/someone touching the battery contacts.
- Unfiltered noise that exists in the host device.
- RF signals which are induced into the battery pack from the surrounding environment.

Such interference can cause the X3102 to operate in an unpredictable manner, or in extreme cases, damage the device. As a guide, the capacitor should be in the order of $0.01\mu\text{F}$ and the resistor, should be in the order of $10\text{K}\Omega$. The capacitors should be of the ceramic type. In order to minimize interference, PCB tracks should be made as short and as wide as possible to reduce their impedance. The battery cells should also be placed as close to the X3102 monitor inputs as possible.

Resistors R_{CB} and the associated n-channel MOSFET's (Q_6 – Q_9) are used for battery cell voltage balancing. The X3102 provides internal drive circuitry which allows the user to switch FETs Q_6 – Q_9 ON or OFF via the microcontroller and SPI port (See section "Cell Voltage Balance Control (CBC1–CBC3)" on page 17). When any of the these FETs are switched ON, a current, limited by resistor R_{CB} , flows across the particular battery cell. In doing so, the user can control the voltage across each individual battery cell. This is important when using Li-Ion battery cells since imbalances in cell voltages can, in time, greatly reduce the usable capacity of the battery pack. Cell voltage balancing may be implemented in various ways, but is usually performed towards the end of cell charging ("Top-of-charge method"). Values for R_{CB} will vary according to the specific application.

The internal 4kbit EEPROM memory can be used to store the cell characteristics for implementing such functions as gas gauging, battery pack history, charge/discharge cycles, and minimum/maximum conditions. Battery pack manufacturing data as well as serial number information can also be stored in the EEPROM array. An SPI serial bus provides the communication link to the EEPROM.

A current sense resistor (R_{SENSE}) is used to measure and monitor the current flowing into/out of the battery terminals, and is used to protect the pack from overcurrent conditions (See section "Overcurrent Protection" on page 23). R_{SENSE} is also used to externally monitor current via a microcontroller (See section "Current Monitor Function" on page 25).

FETs Q_4 and Q_5 may be required on general purpose I/Os of the microcontroller that connect outside of the package. In some cases, without FETs, pull-up resistors external to the pack force a voltage on the V_{CC} pin of the microcontroller during a pack sleep condition. This voltage can affect the proper tuned voltage of the X3102 regulator. These FETs should be turned-on by the microcontroller. (See Figure 1.)

Power On Sequence

Initial connection of the Li-Ion cells in the battery pack will not normally power up the battery pack. Instead, the X3102 enters and remains in the SLEEP mode. To exit the SLEEP mode, after the initial power up sequence, or following any other SLEEP MODE, a minimum of 8.5V is applied to the VCC pin, as would be the case during a battery charge condition. (See Figure 8.)

When V_{SLR} is applied to VCC, the analog select pins (AS_2 – AS_0) and the SPI communication pins (\overline{CS} , CLK, SI, SO) must be low, so the X3102 powers up correctly into the normal operating mode. This can be done by using a power-on reset circuit.

When entering the normal operating mode, either from initial power up or following the SLEEP MODE, all bits in the control register are zero. With UVPC and OVPC bits at zero, the charge and discharge FETs are off. The microcontroller must turn these on to activate the pack. The microcontroller would typically check the voltage and current levels prior to turning on the FETs via the SPI port. The software should prevent turning on the FETs throughout an initial measurement/calibration period. The duration of this period is $T_{OV} + 200\text{ms}$ or $T_{UV} + 200\text{ms}$, whichever is longer.

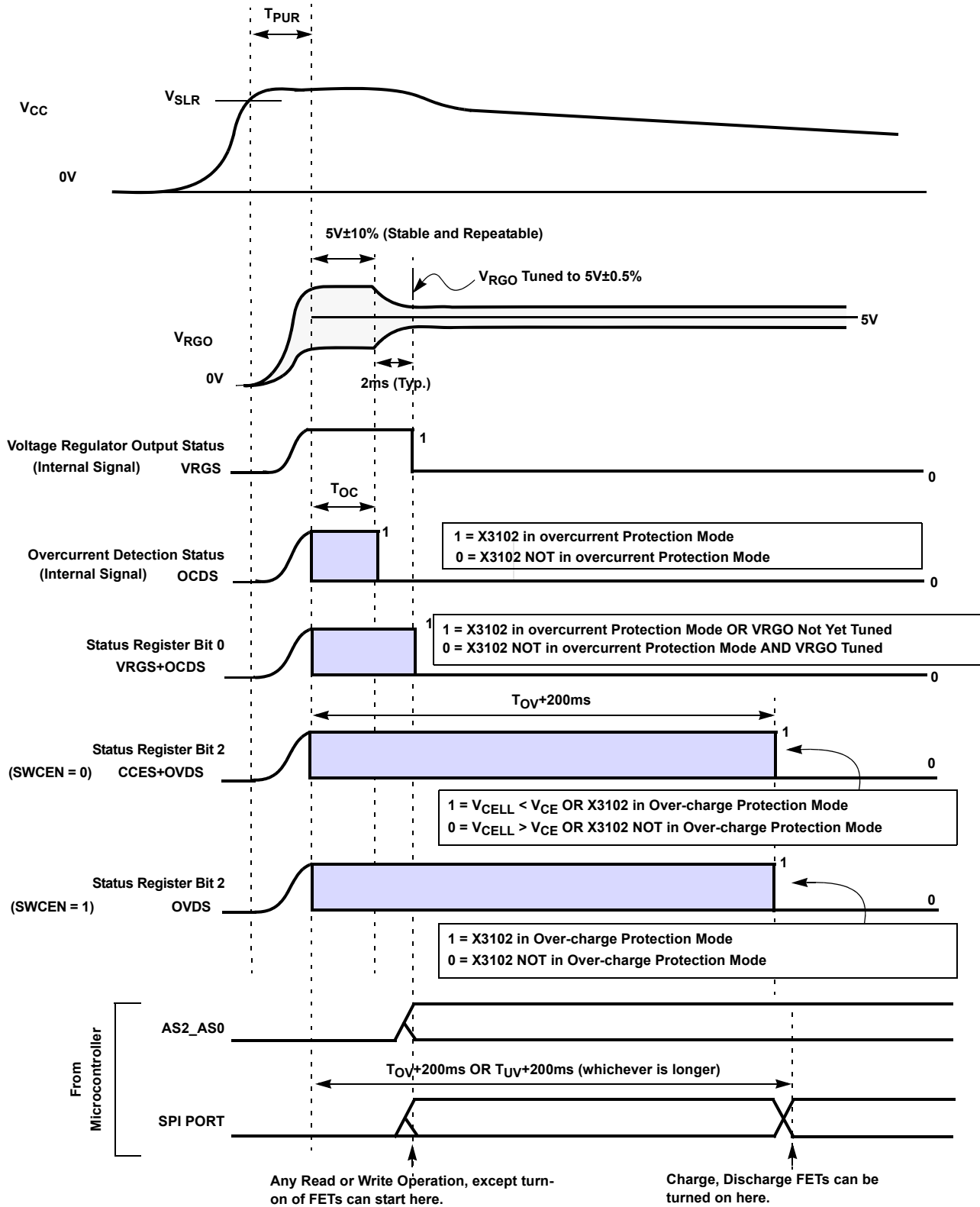


FIGURE 8. POWER UP TIMING (INITIAL POWER UP OR AFTER SLEEP MODE)

Configuration Register

The X3102 can be configured for specific user requirements using the Configuration Register.

TABLE 1. CONFIGURATION REGISTER FUNCTIONALITY

BIT(s)	NAME	FUNCTION
0-5	–	(don't care)
6	SWCEN	Switch Cell Charge Enable threshold function ON/OFF
7	CELLN	Set the number of Li-Ion battery cells used (3 or 4)
8-9	VCE1–VCE0	Select Cell Charge Enable threshold
10–11	VOC1–VOC0	Select overcurrent threshold
12–13	VUV1–VUV0	Select over-discharge (under voltage) threshold
14–15	VOV1–VOV0	Select over-charge voltage threshold

TABLE 2. CONFIGURATION REGISTER - UPPER BYTE

15	14	13	12	11	10	9	8
VOV1	VOV0	VUV1	VUV0	VOC1	VOC0	VCE1	VCE0

Default = 03H

TABLE 3. CONFIGURATION REGISTER - LOWER BYTE

7	6	5	4	3	2	1	0
CELLN	SWCEN	x	x	x	x	x	x

Default = 40H

Over-Charge Voltage Settings

VOV1 and VOV0 control the cell over-charge level. See section “Over-charge Protection” on page 19.

TABLE 4. OVER-CHARGE VOLTAGE THRESHOLD SELECTION

CONFIGURATION REGISTER BITS		OPERATION
VOV1	VOV0	
0	0	$V_{OV} = 4.20V$ (Default)
0	1	$V_{OV} = 4.25V$
1	0	$V_{OV} = 4.30V$
1	1	$V_{OV} = 4.35V$

Over-Discharge Settings

VUV1 and VUV0 control the cell over-discharge (under voltage threshold) level. See section “Over-discharge Protection” on page 20.

TABLE 5. OVER-DISCHARGE THRESHOLD SELECTION

CONFIGURATION REGISTER BITS		OPERATION
VUV1	VUV0	
0	0	$V_{UV} = 2.25V$ (default)
0	1	$V_{UV} = 2.35V$
1	0	$V_{UV} = 2.45V$
1	1	$V_{UV} = 2.55V$

Overcurrent Settings

VOC1 and VOC0 control the pack overcurrent level. See section “Overcurrent Protection” on page 23.

TABLE 6. OVERCURRENT THRESHOLD VOLTAGE SELECTION.

CONFIGURATION REGISTER BITS		OPERATION
VOC1	VOC0	
0	0	$V_{OC} = 0.075V$ (Default)
0	1	$V_{OC} = 0.100V$
1	0	$V_{OC} = 0.125V$
1	1	$V_{OC} = 0.150V$

Cell Charge Enable Settings

VCE1, VCE0 and SWCEN control the pack charge enable function. SWCEN enables or disables a circuit that prevents charging if the cells are at too low a voltage. VCE1 and VCE0 select the voltage that is recognized as too low. See section “Sleep Mode” on page 20.

TABLE 7. CELL CHARGE ENABLE FUNCTION

CONFIGURATION REGISTER BIT	OPERATION
SWCEN	
0	Charge enable function: ON
1	Charge enable function: OFF

TABLE 8. CELL CHARGING THRESHOLD VOLTAGE SELECTION.

CONFIGURATION REGISTER BITS		OPERATION
VCE1	VCE0	
0	0	$V_{CE} = 0.5V$
0	1	$V_{CE} = 0.80V$
1	0	$V_{CE} = 1.10V$
1	1	$V_{CE} = 1.40V$ (Default)

Cell Number Selection

The X3102 is designed to operate with three (3) Li-Ion battery cells. The CELLN bit of the configuration register (Table 9) sets the number of cells recognized. For the X3102, the value for CELLN should always be zero.

TABLE 9. SELECTION OF NUMBER OF BATTERY CELLS

CONFIGURATION REGISTER BIT	
CELLN	OPERATION
1	Not used
0	3 Li-Ion battery cells

The configuration register consists of 16 bits of NOVRAM memory (Table 2, Table 3). This memory features a high-speed static RAM (SRAM) overlaid bit-for-bit with non-volatile “Shadow” EEPROM. An automatic array recall operation reloads the contents of the shadow EEPROM into the SRAM configuration register upon power-up (Figure 9).

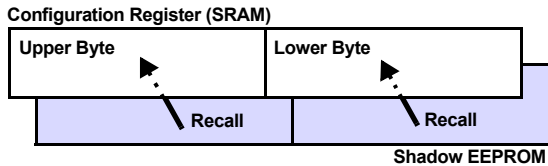


FIGURE 9. POWER UP OF CONFIGURATION REGISTER

The configuration register is designed for unlimited write operations to SRAM, and a minimum of 1,000,000 store operations to the EEPROM. Data retention is specified to be greater than 100 years.

It should be noted that the bits of the shadow EEPROM are for the dedicated use of the configuration register, and are NOT part of the general purpose 4kbit EEPROM array.

The WCFIG command writes to the configuration register, see Table 30 and section “X3102 SPI Serial Communication” on page 27.

After writing to this register using a WCFIG instruction, data will be stored only in the SRAM of the configuration register. In order to store data in shadow EEPROM, a WREN instruction, followed by a EEWRITE to any address of the 4kbit EEPROM memory array must occur. See Figure 10. This sequence initiates an internal nonvolatile write cycle which permits data to be stored in the shadow EEPROM cells. It must be noted that even though a EEWRITE is made to the general purpose 4kbit EEPROM array, the value and address to which it is written, is unimportant. If this procedure is not followed, the configuration register will power up to the last previously stored values following a power down sequence.

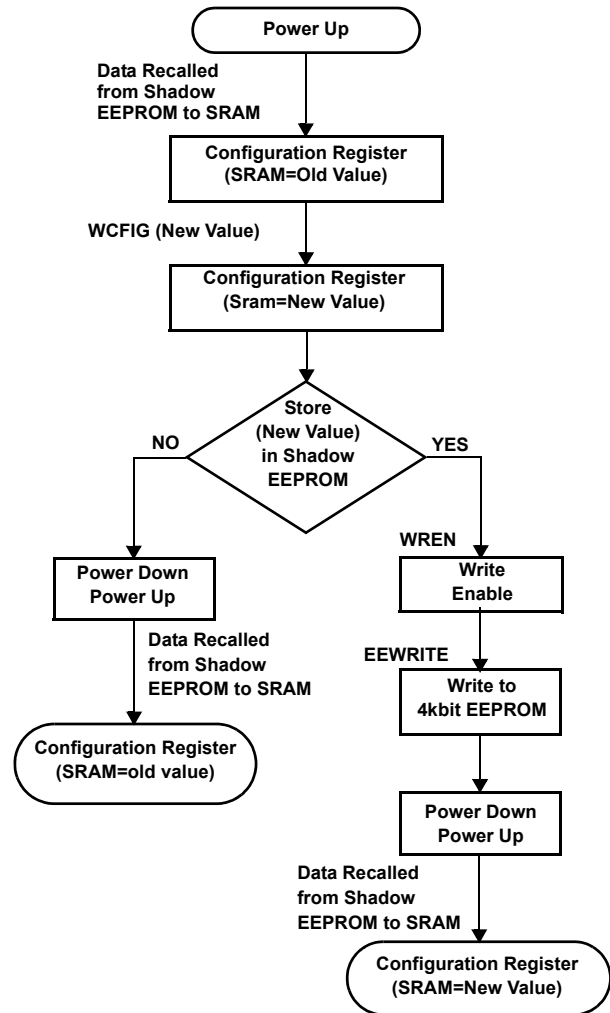


FIGURE 10. WRITING TO CONFIGURATION REGISTER

Control Register

The Control Register is realized as two bytes of volatile RAM (Table 10, Table 11). This register is written using the WCNTR instruction, see Table 30 and section “X3102 SPI Serial Communication” on page 27.

TABLE 10. CONTROL REGISTER - UPPER BYTE

14	14	13	12	11	10	9	8
x	CBC3	CBC2	CBC1	UVPC	OVPC	CSG1	CSG0

TABLE 11. CONTROL REGISTER - LOWER BYTE

7	6	5	4	3	2	1	0
SLP	0	0	x	x	x	x	x

Since the control register is volatile, data will be lost following a power down and power up sequence. The default value of the control register on initial power up or when exiting the SLEEP MODE is 00h (for both upper and lower bytes respectively).

The functions that can be manipulated by the Control Register are shown in Table 12.

TABLE 12. CONTROL REGISTER FUNCTIONALITY

BIT(S)	NAME	FUNCTION
0–4	–	(don't care)
5, 6	0, 0	Reserved—write 0 to these locations.
7	SLP	Select sleep mode.
8,9	CSG1, CSG0	Select current sense voltage gain
10	OVPC	OVP control: switch pin OVP = V_{CC}/V_{SS}
11	UVPC	UVP control: switch pin UVP = V_{CC}/V_{SS}
12	CBC1	CB1 control: switch pin CB1 = V_{CC}/V_{SS}
13	CBC2	CB2 control: switch pin CB2 = V_{CC}/V_{SS}
14	CBC3	CB3 control: switch pin CB3 = V_{CC}/V_{SS}
15	–	(don't care)

Sleep Control (SLP)

Setting the SLP bit to '1' forces the X3102 into the sleep mode, if $V_{CC} < V_{SLP}$. See section "Sleep Mode" on page 20.

TABLE 13. SLEEP MODE SELECTION

CONTROL REGISTER BITS	OPERATION
SLP	
0	Normal operation mode
1	Device enters Sleep mode

Current Sense Gain (CSG1, CSG0)

These bits set the gain of the current sense amplifier. These are x10, x25, x80 and x160. For more detail, see section "Current Monitor Function" on page 25.

TABLE 14. CURRENT SENSE GAIN CONTROL

CONTROL REGISTER BITS		OPERATION
CSG1	CSG0	
0	0	Set current sense gain=x10
0	1	Set current sense gain=x25
1	0	Set current sense gain=x80
1	1	Set current sense gain=x160

Charge/Discharge Control (OVPC, UVPC)

The OVPC and UVPC bits allow control of cell charge and discharge externally, via the SPI port. These bits control the OVP/LMON and UVP/OCF pins, which in turn control the external power FETs.

Using P-channel power FETs ensures that the FET is on when the pin voltage is low (V_{SS}), and off when the pin voltage is high (V_{CC}).

OVP/LMON and UVP/OCF can be controlled by using the WCNTR Instruction to set bits OVPC and UVPC in the Control register (See page 17).

TABLE 15. UVP/OVP CONTROL

CONTROL REGISTER BITS		OPERATION
OVPC	UVPC	
1	x	Pin OVP = V_{SS} (FET ON)
0	x	Pin OVP = V_{CC} (FET OFF)
x	1	Pin UVP = V_{SS} (FET ON)
x	0	Pin UVP = V_{CC} (FET OFF)

It is possible to set/change the values of OVPC and UVPC during a protection mode. A change in the state of the pins OVP/LMON and UVP/OCF, however, will not take place until the device has returned from the protection mode.

Cell Voltage Balance Control (CBC1–CBC3)

This function can be used to adjust individual battery cell voltage during charging. Pins CB1–CB3 are used to control external power switching devices. Cell voltage balancing is achieved via the SPI port.

TABLE 16. CB1–CB3 CONTROL

Control Register Bits			Operation
CBC3	CBC2	CBC1	
x	x	1	Set CB1 = V_{CC} (ON)
x	x	0	Set CB1 = V_{SS} (OFF)
x	1	x	Set CB2 = V_{CC} (ON)
x	0	x	Set CB2 = V_{SS} (OFF)
1	x	x	Set CB3 = V_{CC} (ON)
0	x	x	Set CB3 = V_{SS} (OFF)
x	x	x	Set CB4 = V_{CC} (ON)
x	x	x	Set CB4 = V_{SS} (OFF)

CB1–CB3 can be controlled by using the WCNTR Instruction to set bits CBC1–CBC3 in the control register (Table 16).

Status Register

The status of the X3102 can be verified by using the RDSTAT command to read the contents of the Status Register (Table 17).

TABLE 17. STATUS REGISTER

7	6	5	4	3	2	1	0
0	0	0	0	0	CCES + OVDS	UVDS	VRGS + OCDS

The function of each bit in the status register is shown in Table 18.

Bit 0 of the status register (VRGS + OCDS) actually indicates the status of two conditions of the X3102. Voltage Regulator Status (VRGS) is an internally generated signal which indicates that the output of the Voltage Regulator (VRGO) has reached an output of $5VDC \pm 0.5\%$. In this case, the voltage regulator is said to be “tuned”. Before the signal VRGS goes low (i.e. before the voltage regulator is tuned), the voltage at the output of the regulator is nominally $5VDC \pm 10\%$ (See section “Voltage Regulator” on page 26.) Overcurrent Detection Status (OCDS) is another internally generated signal which indicates whether or not the X3102 is in overcurrent protection mode.

Signals VRGS and OCDS are logically OR’ed together (VRGS+OCDS) and written to bit 0 of the status register (See Table 18, Table 17 and Figure 8).

Bit 1 of the status register simply indicates whether or not the X3102 is in over-discharge protection mode.

Bit 2 of the status register (CCES + OVDS) indicates the status of two conditions of the X3102. Cell Charge Enable Status (CCES) is an internally generated signal which indicates the status of any cell voltage (V_{CELL}) with respect to the Cell Charge Enable Voltage (V_{CE}). Over-charge Voltage Detection Status (OVDS) is an internally generated signal which indicates whether or not the X3102 is in over-charge protection mode.

When the cell charge enable function is switched ON (configuration bit SWCEN = 0), the signals CCES and OVDS are logically OR’ed (CCES + OVDS) and written to bit 2 of the status register. If the cell charge enable function is switched OFF (configuration bit SWCEN = 1), then bit 2 of the status register effectively only represents information about the over-charge status (OVDS) of the X3102 (See Table 18, Table 17 and Figure 8).

TABLE 18. STATUS REGISTER FUNCTIONALITY

BIT(S)	NAME	DESCRIPTION	CASE	STATUS	INTERPRETATION
0	VRGS + OCDS	Voltage regulator status + Overcurrent detection status	-	1	V_{RGO} not yet tuned ($V_{RGO} = 5V \pm 10\%$) OR X3102 in overcurrent protection mode.
				0	V_{RGO} tuned ($V_{RGO} = 5V \pm 0.5\%$) AND X3102 NOT in overcurrent protection mode.
1	UVDS	Over-discharge detection status	-	1	X3102 in over-discharge protection mode
				0	X3102 NOT in over-discharge protection mode
2	CCES + OVDS	Cell charge enable status + Over-charge detection status	SWCEN = 0 (Note)	1	$V_{CELL} < V_{CE}$ OR X3102 in over-charge protection mode
				0	$V_{CELL} > V_{CE}$ AND X3102 NOT in over-charge protection mode
			SWCEN = 1 (Note)	1	X3102 in over-charge protection mode
				0	X3102 NOT in over-charge protection mode
3-7	-		-	0	Not used (always return zero)

NOTE: This bit is set in the configuration register.

X3102 Internal Protection Functions

The X3102 provides periodic monitoring (See section “Periodic Protection Monitoring” on page 19) for over-charge and over-discharge states and continuous monitoring for an overcurrent state. It has automatic shutdown when a protection mode is encountered, as well as automatic return after the device is released from a protection mode. When sampling voltages through the analog port (Monitor Mode), over-charge and over-discharge protection monitoring is also performed on a continuous basis.

Voltage thresholds for each of these protection modes (V_{OV} , V_{UV} , and V_{OC} respectively) can be individually selected via software and stored in an internal non-volatile register. This feature allows the user to avoid the restrictions of mask programmed voltage thresholds, and is especially useful during prototype/evaluation design stages or when cells with slightly different characteristics are used in an existing design.

Delay times for the detection of, and release from protection modes (T_{OV} , T_{UV}/T_{UVR} , and T_{OC}/T_{OCR} respectively) can be individually varied by setting the values of external capacitors connected to pins OVT, UVT, OCT.

Periodic Protection Monitoring

In normal operation, the analog select pins are set such that $AS2 = L$, $AS1 = L$, $AS0 = L$. In this mode the X3102 conserves power by sampling the cells for over or over-discharge conditions.

In this state over-charge and over-discharge protection circuitry are usually off, but are periodically switched on by the internal Protection Sample Rate Timer (PSRT). The over-charge and over-discharge protection circuitry is on for approximately 2ms in each 125ms period. Overcurrent monitoring is continuous. In monitor mode (See page 25) over-charge and over-discharge monitoring is also continuous.

Over-charge Protection

The X3102 monitors the voltage on each battery cell (V_{CELL}). If for any cell, $V_{CELL} > V_{OV}$ for a time exceeding T_{OV} , then the Charge FET will be switched OFF ($OVP/LMON=V_{CC}$). The device has now entered Over-charge protection mode (Figure 11). The status of the discharge FET (via pin UVP) will remain unaffected.

While in over-charge protection mode, it is possible to change the state of the OVPC bit in the control register such that $OVP/LMON=V_{SS}$ (Charge FET=ON). Although the OVPC bit in the control register can be changed, the change will not be seen at pin OVP until the X3102 returns from over-charge protection mode.

The over-charge detection delay T_{OV} , is varied using a capacitor (C_{OV}) connected between pin OVT and GND. A typical delay time is shown in Table 10. The delay T_{OV} that results from a particular capacitance C_{OV} , can be approximated by the following linear equation:

$$T_{OV} (s) \approx 10 \times C_{OV} (\mu F)$$

TABLE 19. TYPICAL OVER-CHARGE DETECTION TIME

Symbol	C_{OV}	Delay
T_{OV}	0.1 μ F	1.0s (Typ)

The device further continues to monitor the battery cell voltages, and is released from over-charge protection mode when $V_{CELL} < V_{OVR}$, for all cells. When the X3102 is released from over-charge protection mode, the charge FET is automatically switched ON ($OVP/LMON=V_{SS}$). When the device returns from over-charge protection mode, the status of the discharge FET (pin UVP/OCP) remains unaffected.

The value of V_{OV} can be selected from the values shown in Table 4 by setting bits $VOV1$, $VOV0$. These bits are set by using the WCFIG instruction to write to the configuration register.

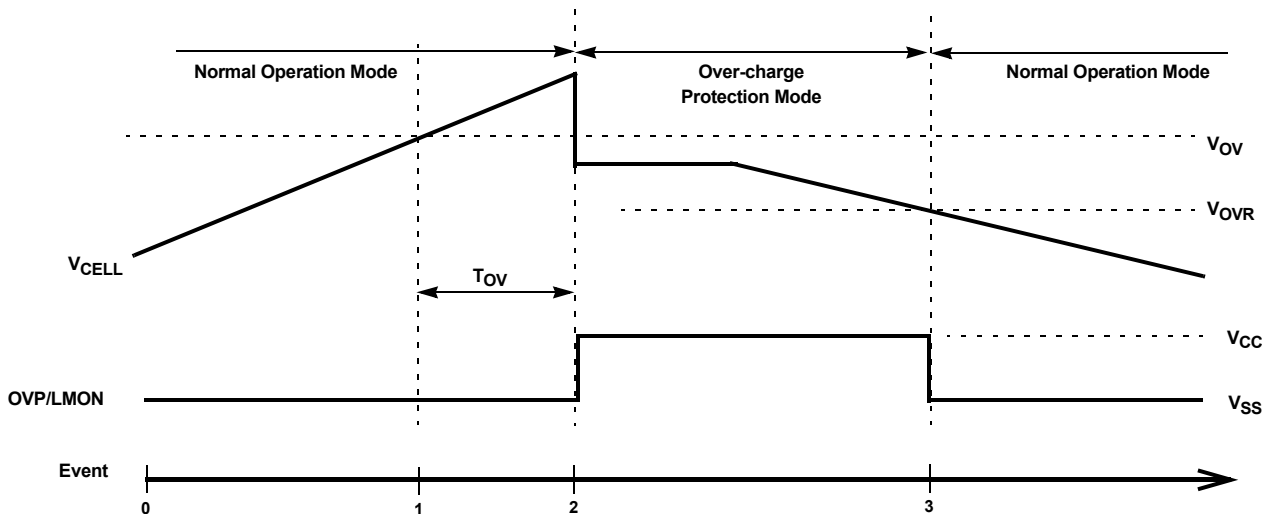


FIGURE 11. OVER-CHARGE PROTECTION MODE-EVENT DIAGRAM

TABLE 20. OVER-CHARGE PROTECTION MODE-EVENT DIAGRAM DESCRIPTION

EVENT	EVENT DESCRIPTION
[0,1)	<ul style="list-style-type: none"> Discharge FET is ON (UVP/OCP=V_{SS}). Charge FET is ON (OVP/LMON=V_{SS}), and hence battery cells are permitted to receive charge. All cell voltages (V_{CELL1} – V_{CELL4}) are below the over-charge voltage threshold (V_{OV}). The device is in normal operation mode (i.e. not in a protection mode).
[1]	<ul style="list-style-type: none"> The voltage of one or more of the battery cells (V_{CELL}), exceeds V_{OV}. The internal over-charge detection delay timer begins counting down. The device is still in normal operation mode
(1,2)	The internal over-charge detection delay timer continues counting for T _{OV} seconds.
[2]	<p>The internal over-charge detection delay timer times out AND V_{CELL} still exceeds V_{OV}.</p> <ul style="list-style-type: none"> Therefore, the internal over-charge sense circuitry switches the charge FET OFF (OVP/LMON=V_{CC}). The device has now entered over-charge protection mode.
(2,3)	<ul style="list-style-type: none"> While in over-charge protection mode: The battery cells are permitted to discharge via the discharge FET, and diode D₂ across the charge FET The X3102 monitors the voltages V_{CELL1} - V_{CELL4} to determine whether or not they have all fallen below the “Return from over-charge threshold” (V_{OV_R}). (It is possible to change the status of UVP/OCP or OVP/LMON using the control register)
[3]	<ul style="list-style-type: none"> All cell voltages fall below V_{OV_R}—The device is now in normal operation mode. The X3102 automatically switches charge FET = ON (OVP/LMON = V_{SS}) The status of the discharge FET remains unaffected. Charging of the battery cells can now resume.

Over-discharge Protection

If V_{CELL} < V_{UV}, for a time exceeding T_{UV}, the cells are said to be in a over-discharge state (Figure 12). In this instance, the X3102 automatically switches the discharge FET OFF (UVP/OCP=V_{CC}), and then enter sleep mode.

The over-discharge (undervoltage) value, V_{UV}, can be selected from the values shown in Table 5 by setting bits VUV1, VUV0 in the configuration register. These bits are set using the WCFIG command. Once in the sleep mode, the following steps must occur before the X3102 allows the battery cells to discharge:

- The X3102 must wake from sleep mode (See section “Voltage Regulator” on page 26).
- The charge FET must be switched ON by the microcontroller (OVP/LMON=V_{SS}), via the control register (See section “CONTROL REGISTER FUNCTIONALITY” on page 17).
- All battery cells must satisfy the condition: V_{CELL} > V_{UV_R} for a time exceeding T_{UV_R}.
- The discharge FET must be switched ON by the microcontroller (UVP/OCP=V_{SS}), via the control register (See section “CONTROL REGISTER FUNCTIONALITY” on page 17)

The times T_{UV}/T_{UV_R} are varied using a capacitor (C_{UV}) connected between pin UVT and GND (Table 13). The delay T_{UV} that results from a particular capacitance C_{UV}, can be approximated by the following linear equation:

$$T_{UV} \text{ (s)} \approx 10 \times C_{UV} \text{ (}\mu\text{F)}$$

$$T_{UV_R} \text{ (ms)} \approx 70 \times C_{UV} \text{ (}\mu\text{F)}$$

TABLE 21. TYPICAL OVER-DISCHARGE DELAY TIMES

SYMBOL	DESCRIPTION	C _{UV}	DELAY
T _{UV}	Over-discharge detection delay	0.1μF	1.0s (Typ)
T _{UV_R}	Over-discharge release time	0.1μF	7ms (Typ)

Sleep Mode

The X3102 can enter sleep mode in two ways:

- The device enters the over-discharge protection mode.
- The user sends the device into sleep mode using the control register.

A sleep mode can be induced by the user, by setting the SLP bit in the control register (Table 13) using the WCNTR Instruction.

In sleep mode, power to all internal circuitry is switched off, minimizing the current drawn by the device to 1μA (max). In this state, the discharge FET and the charge FET are switched OFF (OVP/LMON=V_{CC} and UVP/OCP=V_{CC}), and the 5VDC regulated output (V_{RGO}) is 0V. Control of UVP/OCP and OVP/LMON via bits UVPC and OVPC in the control register is also prohibited.

TABLE 22. OVER-DISCHARGE PROTECTION MODE—EVENT DIAGRAM DESCRIPTION

EVENT	EVENT DESCRIPTION	
[0,1]	<ul style="list-style-type: none"> • Charge FET is ON (OVP/LMON = V_{SS}) • Discharge FET is ON (UVP/OCP = V_{SS}), and hence battery cells are permitted to discharge. • All cell voltages (V_{CELL1}–V_{CELL4}) are above the Over-discharge threshold voltage (V_{UV}). • The device is in normal operation mode (i.e. not in a protection mode). 	
[1]	<ul style="list-style-type: none"> • The voltage of one or more of the battery cells (V_{CELL}), falls below V_{UV}. • The internal over-discharge detection delay timer begins counting down. • The device is still in normal operation mode 	
(1,2)	<ul style="list-style-type: none"> • The internal over-discharge detection delay timer continues counting for T_{UV} seconds. 	
[2]	<ul style="list-style-type: none"> • The internal over-discharge detection delay timer times out, AND V_{CELL} is still below V_{UV}. • The internal over-discharge sense circuitry switches the discharge FET OFF (UVP/OCP = V_{CC}). • The charge FET is switched OFF (OVP/LMON = V_{CC}). • The device has now entered over-discharge protection mode. • At the same time, the device enters sleep mode (See section “Voltage Regulator” on page 26). 	
(2,3)	<ul style="list-style-type: none"> • While device is in sleep (in over-discharge protection) mode: • The power to ALL internal circuits is switched OFF limiting power consumption to less than $1\mu A$. • The output of the 5VDC voltage regulator (RGO) is 0V. • Access to the X3102 via the SPI port is NOT possible. 	
[3]	<ul style="list-style-type: none"> • Return from sleep mode (but still in over-discharge protection mode): • V_{CC} rises above the “Return from Sleep mode threshold Voltage” (V_{SLR})—This would normally occur in the case that the battery pack was connected to a charger. The X3102 is now powered via P+/P-, and not the battery pack cells. • Power is returned to ALL internal circuitry • 5VDC output is returned to the regulator output (RGO). • Access is enabled to the X3102 via the SPI port. • The status of the discharge FET remains OFF (It is possible to change the status of UVPC in the control register, although it will have no effect at this time). 	
(3,4)	If the cell charge enable function is switched ON AND $V_{CELL} > V_{CE}$ OR Charge enable function is switched OFF	<ul style="list-style-type: none"> • The X3102 initiates a reset operation that takes the longer of $T_{OV}+200ms$ or $T_{UV}+200ms$ to complete. Do not write to the FET control bits during this time. • The charge FET is switched On (OVP/LMON = V_{SS}) by the microcontroller by writing a “1” to the OVPC bit in the control register. • The battery cells now receive charge via the charge FET and diode D1 across the discharge FET (which is OFF). • The X3102 monitors the V_{CELL} voltage to determine whether or not it has risen above V_{UVR}.
	If the cell charge enable function is switched ON AND $V_{CELL} < V_{CE}$	<ul style="list-style-type: none"> • Charge/discharge of the battery cells via P+ is no longer permitted (Charge FET and discharge FET are held OFF). • (Charging may re-commence only when the Cell Charge Enable function is switched OFF - See Sections: “Configuration Register” page 4, and “Sleep mode” page 17.)
[4]	<ul style="list-style-type: none"> • The voltage of all of the battery cells (V_{CELL}), have risen above V_{UVR}. • The internal Over-discharge release timer begins counting down. • The X3102 is still in over-discharge protection mode. 	
(4,5)	<ul style="list-style-type: none"> • The internal over-discharge release timer continues counting for t_{UVR} seconds. • The X3102 should be in monitor mode (AS2:AS0 not all low) for recovery time based on t_{UVR}. Otherwise recovery is based on two successive samples about 120ms apart. 	
[5]	<ul style="list-style-type: none"> • The internal over-discharge release timer times out, AND V_{CELL} is still above V_{UVR}. • The device returns from over-discharge protection mode, and is now in normal operation mode. • The Charger voltage can now drop below V_{SLR} and the X3102 will not go back to sleep. • The discharge FET is can now be switched ON (UVP/OCP = V_{SS}) by the microcontroller by writing a “1” to the UVPC bit of the control register. • The status of the charge FET remains unaffected (ON) • The battery cells continue to receive charge via the charge FET and discharge FET (both ON). 	

Overcurrent Protection

In addition to monitoring the battery cell voltages, the X3102 continually monitors the voltage V_{CS21} ($V_{CS2} - V_{CS1}$) across the current sense resistor (R_{SENSE}). If $V_{CS21} > V_{OC}$ for a time exceeding T_{OC} , then the device enters overcurrent protection mode (Figure 7). In this mode, the X3102 automatically switches the discharge FET OFF ($UVP/OCP = V_{CC}$) and hence prevent current from flowing through the terminals P+ and P-.

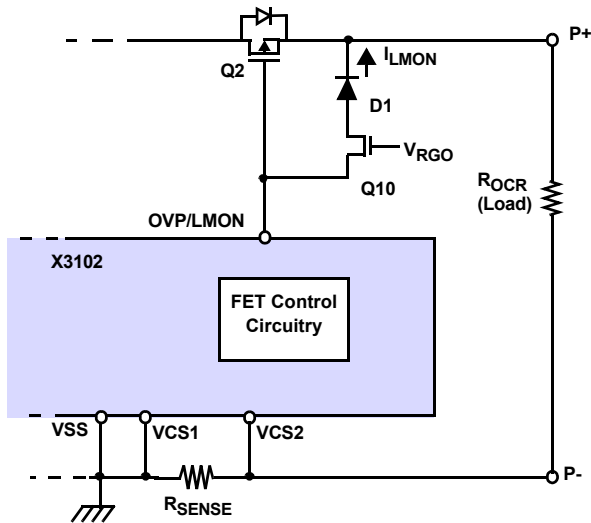


FIGURE 13. OVERCURRENT PROTECTION

The 5VDC voltage regulator output (V_{RGO}) is always active during an overcurrent protection mode.

Once the device enters overcurrent protection mode, the X3102 begin a load monitor state. In the load monitor state, a small current ($I_{LMON} = 7.5\mu A$ typ.) is passed out of pin OVP/ LMON in order to determine the load resistance. The load resistance is the impedance seen looking out of pin OVP/ LMON, between terminal P+ and pin VSS (See Figure 13.)

If the load resistance $> R_{OCR}$ ($I_{LMON} = 0\mu A$) for a time exceeding T_{OCR} , then the X3102 is released from overcurrent protection mode. The discharge FET is then automatically switched ON ($UVP/OCP = V_{SS}$) by the X3102, unless the status of UVP/OCP has been changed in control register (by manipulating bit UVPC) during the overcurrent protection mode.

T_{OC}/T_{OCR} are varied using a capacitor (C_{OC}) connected between pin OCT and VSS. A list of typical delay times is shown in Table 23. Note that the value C_{OC} should be larger than 1nF.

The delay T_{OC} and T_{OCR} that results from a particular capacitance C_{OC} can be approximated by the following equations:

$$T_{OC} \text{ (ms)} \approx 10,000 \times C_{OC} \text{ (\mu F)}$$

$$T_{OCR} \text{ (ms)} \approx 10,000 \times C_{OC} \text{ (\mu F)}$$

TABLE 23. TYPICAL OVERCURRENT DELAY TIMES

Symbol	Description	C_{OC}	Delay
T_{OC}	Overcurrent detection delay	0.001 μF	10ms (Typ)
T_{OCR}	Overcurrent release time	0.001 μF	10ms (Typ)

The value of V_{OC} can be selected from the values shown in Table 6, by setting bits VOC1, VOC0 in the configuration register using the WCFIG command.

Note: If the Charge FET is turned off, due to an overcharge condition or by direct command from the microcontroller, the cells are not in an undervoltage condition and the pack has a load, then excessive current may flow through Q10 and diode D1. To eliminate this effect, the gate of Q10 can be turned off by the microcontroller.

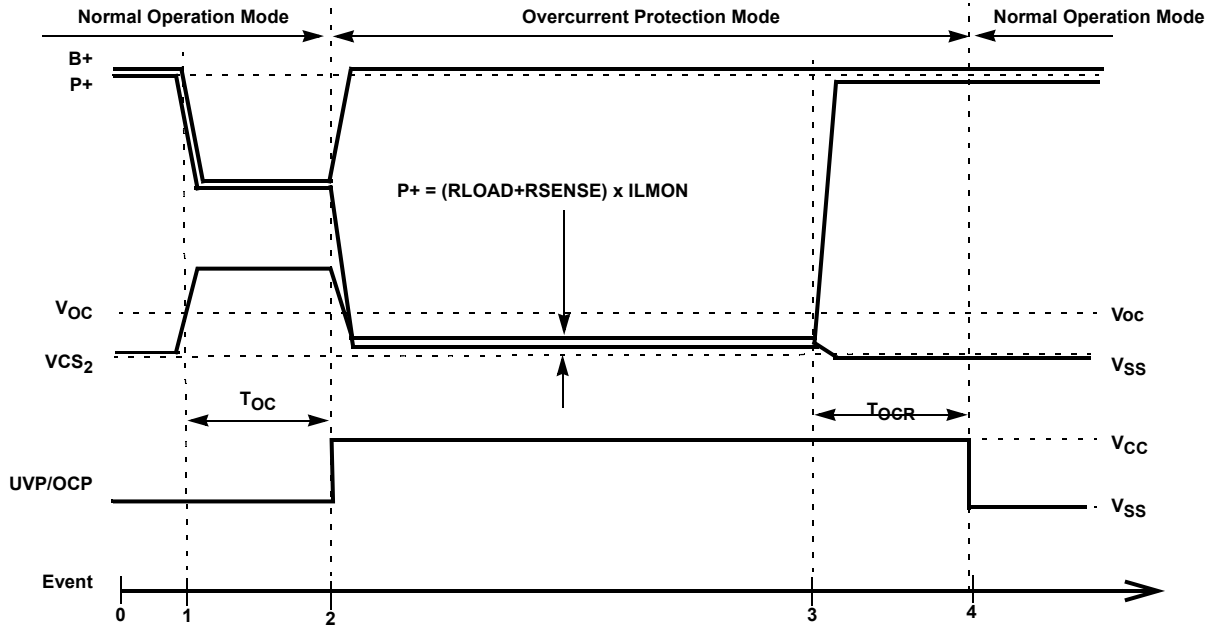


FIGURE 14. OVERCURRENT PROTECTION MODE - EVENT DIAGRAM

TABLE 24. OVERCURRENT PROTECTION MODE-EVENT DIAGRAM DESCRIPTION

EVENT	EVENT DESCRIPTION
[0,1)	<ul style="list-style-type: none"> Discharge FET is ON (OCP = V_{SS}). Battery cells are permitted to discharge. V_{CS21} (V_{CS2} - V_{CS1}) is less than the overcurrent threshold voltage (V_{OC}). The device is in normal operation mode (i.e. not in a protection mode).
[1]	<ul style="list-style-type: none"> Excessive current flows through the battery terminals P+, dropping the voltage. (See Figure 14.). The positive battery terminal voltage (P+) falls, and V_{CS21} exceeds V_{OC}. The internal overcurrent detection delay timer begins counting down. The device is still in Normal Operation Mode
(1,2)	The internal Overcurrent detection delay timer continues counting for T _{OC} seconds.
[2]	<ul style="list-style-type: none"> The internal overcurrent detection delay timer times out, AND V_{CS21} is still above V_{OC}. The internal overcurrent sense circuitry switches the discharge FET OFF (UVP/OCP = V_{CC}). The device now begins a load monitor state by passing a small test current (I_{LMON} = 7.5μA) out of pin OVP/LMON. This senses if an overcurrent condition (i.e. if the load resistance < R_{OCR}) still exists across P+/P-. The device has now entered overcurrent protection mode. It is possible to change the status of UVPC and OVPC in the control register, although the status of pins UVP/OCP and OVP/LMON will not change until the device has returned from overcurrent protection mode.
(2,3)	The X3102 now continuously monitors the load resistance to detect whether or not an overcurrent condition is still present across the battery terminals P+/P-.
[3]	<ul style="list-style-type: none"> The device detects the load resistance has risen above R_{OCR}. Voltages P+ and V_{CS21} return to their normal levels. The test current from pin OVP/LMON is stopped (I_{LMON} = 0μA) The device has now returned from the load monitor state The internal overcurrent release time timer begins counting down. Device is still in overcurrent protection mode.
(3,4)	The internal overcurrent release timer continues counting for T _{OCR} seconds.
[4]	<ul style="list-style-type: none"> The internal overcurrent release timer times out, and V_{CS21} is still below V_{OC}. The device returns from overcurrent protection mode, and is now in normal operation mode. The discharge FET is automatically switched ON (UVP/OCP = V_{SS}) - unless the status of UVPC has been changed in the control register during the overcurrent protection mode. The status of the charge FET remains unaffected. Discharge of the battery cells is once again possible.

Monitor Mode

Analog Multiplexer Selection

The X3102 can be used to externally monitor individual battery cell voltages, and battery current. Each quantity can be monitored at the analog output pin (AO), and is selected using the analog select (AS0–AS2) pins (Table 25). Also, see Figure 15.

TABLE 25. AO SELECTION MAP

AS2	AS1	AS0	AO OUTPUT
L	L	L	V _{SS} ⁽¹⁾
L	L	H	VCELL ₁ –VCELL ₂ (VCELL ₁₂)
L	H	L	VCELL ₂ –VCELL ₃ (VCELL ₂₃)
L	H	H	VCELL ₃ –VCELL ₄ (VCELL ₃₄)
H	L	L	VCELL ₄ –V _{SS} (VCELL ₄)
H	L	H	VCS ₁ –VCS ₂ (VCS ₁₂) ⁽²⁾
H	H	L	VCS ₂ –VCS ₁ (VCS ₂₁) ⁽²⁾
H	H	H	V _{SS}

NOTES:

1. This is the normal state of the X3102. While in this state Over-charge and Over-discharge Protection conditions are periodically monitored (See “Periodic Protection Monitoring” on page 19.)
2. VCS₁, VCS₂ are read at AO with respect to a DC bias voltage of 2.5V (See section “Current Monitor Function” on page 25).

Current Monitor Function

The voltages monitored at pins VCS₁ and VCS₂ can be used to calculate current flowing through the battery terminals, using an off-board microcontroller with an A/D.

Since the value of the sense resistor (R_{SENSE}) is small (typically in the order of tens of mΩ), and since the resolution of various A/D converters may vary, the voltage across R_{SENSE} (VCS₁ and VCS₂) is amplified internally with a gain of between 10 and 160, and output to pin AO (Figure 15).

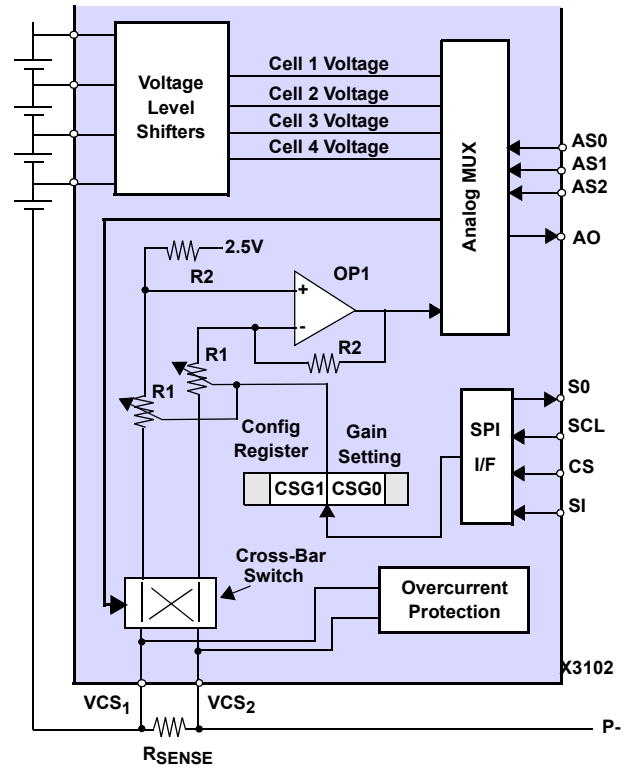


FIGURE 15. MONITOR CIRCUIT

The internal gain of the X3102 current sense voltage amplifier can be selected by using the WCNTR Instruction to set bits CSG1 and CSG0 in the control register (Table 14). The CSG1 and CSG0 bits select one of four input resistors to Op Amp OP1. The feedback resistors remain constant. This ratio of input to feedback resistors determines the gain. Putting external resistors in series with the inputs reduces the gain of the amplifier.

VCS₁ and VCS₂ are read at AO with respect to a DC bias voltage of 2.5V. Therefore, the voltage range of VCS₁₂ and VCS₂₁ changes depending upon the direction of current flow (i.e. battery cells are in Charge or Discharge - Table 21).

TABLE 26. AO VOLTAGE RANGE FOR VCS₁₂ AND VCS₂₁

AO	CELL STATE	AO VOLTAGE RANGE
VCS ₁₂	Charge	2.5V ≤ AO ≤ 5.0V
VCS ₁₂	Discharge	0V ≤ AO ≤ 2.5V
VCS ₂₁	Charge	0V ≤ AO ≤ 2.5V
VCS ₂₁	Discharge	2.5V ≤ AO ≤ 5.0V

By calculating the difference of VCS₁₂ and VCS₂₁ the offset voltage of the internal op-amp circuitry is cancelled. This allows for the accurate calculation of current flow into and out of the battery cells.

Pack current is calculated using the following formula:

$$\text{Pack Current} = \frac{(VCS_{12} - VCS_{21})}{(2)(\text{gain setting})(\text{current sense resistor})}$$

Voltage Regulator

The X3102 is able to supply peripheral devices with a regulated 5VDC±0.5% output at pin RGO. The voltage regulator should be configured externally as shown in Figure 16.

The non-inverting input of OP1 is fed with a high precision 5VDC supply. The voltage at the output of the voltage regulator (V_{RGO}) is compared to this 5V reference via the inverting input of OP1. The output of OP1 in turn drives the regulator pnp transistor (Q1). The negative feedback at the regulator output maintains the voltage at 5VDC ±0.5% (including ripple) despite changes in load, and differences in regulator transistors.

When power is applied to pin VCC of the X3102, V_{RGO} is regulated to 5VDC±10% for a nominal time of $T_{OC}+2ms$. During this time period, V_{RGO} is “tuned” to attain a final value of 5VDC ±0.5% (Figure 8).

The maximum current that can flow from the voltage regulator (I_{LMT}) is controlled by the current limiting resistor (R_{LMT}) connected between RGP and VCC. When the voltage across VCC and RGP reaches a nominal 2.5V (i.e. the threshold voltage for the FET), Q2 switches ON, shorting VCC to the base of Q1. Since the base voltage of Q1 is now higher than the emitter voltage, Q1 switches OFF, and hence the supply current goes to zero.

Typical values for R_{LMT} and I_{LMT} are shown in Table 27. In order to protect the voltage regulator circuitry from damage in case of a short-circuit, $R_{LMT} \geq 10\Omega$ should always be used.

TABLE 27. TYPICAL VALUES FOR R_{LMT} AND I_{LMT}

R_{LMT}	VOLTAGE REGULATOR CURRENT LIMIT (I_{LMT})
10 Ω	250mA ± 50% (Typical)
25 Ω	100mA ± 50% (Typical)
50 Ω	50mA ± 50% (Typical)

When choosing the value of R_{LMT} , the drive limitations of the PNP transistor used should also be taken into consideration. The transistor should have a gain of at least 100 to support an output current of 250mA.

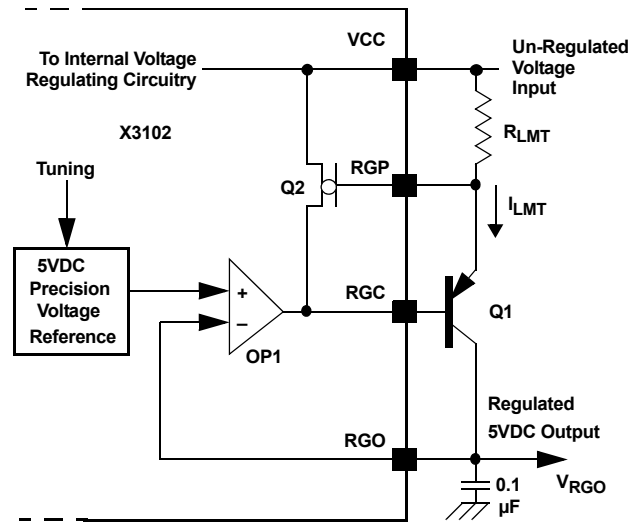


FIGURE 16. VOLTAGE REGULATOR OPERATION

4KBit EEPROM Memory

The X3102 contains a CMOS 4k-bit serial EEPROM, internally organized as 512 x 8 bits. This memory is accessible via the SPI port, and features the IDLock function.

The 4kbit EEPROM array can be accessed by the SPI port at any time, even during a protection mode, except during sleep mode. After power is applied to VCC of the X3102, EEREAD and EEWRITE Instructions can be executed only after times t_{PUR} (power up to read time) and t_{PUW} (power up to write time) respectively.

IDLock is a programmable locking mechanism which allows the user to lock data in different portions of the EEPROM memory space, ranging from as little as one page to as much as 1/2 of the total array. This is useful for storing information such as battery pack serial number, manufacturing codes, battery cell chemistry data, or cell characteristics.

EEPROM Write Enable Latch

The X3102 contains an EEPROM “Write Enable” latch. This latch must be SET before a write to EEPROM operation is initiated. The WREN instruction will set the latch and the WRDI instruction will reset the latch (Figure 17). This latch is automatically reset upon a power-up condition and after the completion of a byte or page write cycle.

IDLock Memory

Intersil’s IDLock memory provides a flexible mechanism to store and lock battery cell/pack information. There are seven distinct IDLock memory areas within the array which vary in size from one page to as much as half of the entire array.

Prior to any attempt to perform an IDLock operation, the WREN instruction must first be issued. This instruction sets the "Write Enable" latch and allows the part to respond to an IDLock sequence. The EEPROM memory may then be IDLocked by writing the SET IDL instruction (Table 30 and Figure 25), followed by the IDLock protection byte.

TABLE 28. IDLock PARTITION BYTE DEFINITION

IDLock PROTECTION BYTES	EEPROM MEMORY ADDRESS IDLocked
0000 0000	None
0000 0001	000h–07Fh
0000 0010	080h–0FFh
0000 0011	100h–17Fh
0000 0100	180h–1FFh
0000 0101	000h–0FFh
0000 0110	000h–00Fh
0000 0111	1F0h–1FFh

The IDLock protection byte contains the IDLock bits IDL2-IDL0, which defines the particular partition to be locked (Table 28). The rest of the bits [7:3] are unused and must be written as zeroes. Bringing \overline{CS} HIGH after the two byte IDLock instruction initiates a nonvolatile write to the status register. Writing more than one byte to the status register will overwrite the previously written IDLock byte.

Once an IDLock instruction has been completed, that IDLock setup is held in a nonvolatile IDLock Register (Table 29) until the next IDLock instruction is issued. The sections of the

memory array that are IDLocked can be read but not written until IDLock is removed or changed.

TABLE 29. IDLock REGISTER

7	6	5	4	3	2	1	0
0	0	0	0	0	IDL2	IDL1	IDL0

NOTE: Bits [7:3] specified to be "0's".

X3102 SPI Serial Communication

The X3102 is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of many popular microcontroller families. This interface uses four signals, \overline{CS} , SCK, SI and SO. The signal \overline{CS} when low, enables communications with the device. The SI pin carries the input signal and SO provides the output signal. SCK clocks data in or out. The X3102 operates in SPI mode 0 which requires SCK to be normally low when not transferring data. It also specifies that the rising edge of SCK clocks data into the device, while the falling edge of SCK clocks data out.

This SPI port is used to set the various internal registers, write to the EEPROM array, and select various device functions.

The X3102 contains an 8-bit instruction register. It is accessed by clocking data into the SI input. \overline{CS} must be LOW during the entire operation. Table 30 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after \overline{CS} goes LOW. SCK is static, allowing the user to stop the clock, and then start it again to resume operations where left off.

TABLE 30. INSTRUCTION SET

INSTRUCTION NAME	INSTRUCTION FORMAT*	DESCRIPTION
WREN	0000 0110	Set the write enable latch (write enable operation) (Figure 17)
WRDI	0000 0100	Reset the write enable latch (write disable operation) (Figure 17)
EEWRITE	0000 0010	Write command followed by address/data (4kbit EEPROM) (Figure 18, Figure 19)
EEREAD STAT	0000 0101	Reads IDLock settings & status of EEPROM EEWRITE instruction (Figure 20)
EEREAD	0000 0011	Read operation followed by address (for 4kbit EEPROM) (Figure 21)
WCFIG	0000 1001	Write to configuration register followed by two bytes of data (Figure 10, Figure 22). Data stored in SRAM only and will power-up to previous settings (Figure 9)
WCNTR	0000 1010	Write to control register, followed by two bytes of data (Figure 23)
RDSTAT	0000 1011	Read contents of status register (Figure 24)
SET IDL	0000 0001	Set EEPROM ID lock partition followed by partition byte (Figure 25)

*Instructions have the MSB in leftmost position and are transferred MSB first.

Write Enable/Write Disable (WREN/WRDI)

Any write to a nonvolatile array or register, requires the WREN command be sent prior to the write command. This command sets an internal latch allowing the write operation to proceed. The WRDI command resets the internal latch if the system decides to abort a write operation. See Figure 17.

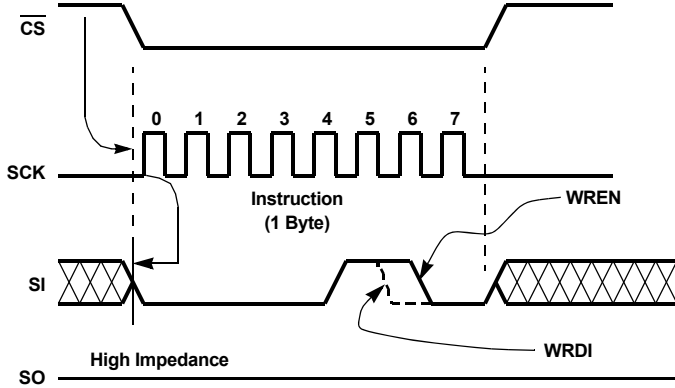


FIGURE 17. EEPROM WRITE ENABLE LATCH (WREN/WRDI) OPERATION SEQUENCE

EEPROM Write Sequence (EWRITE)

Prior to any attempt to write data into the EEPROM of the X3102, the “Write Enable” latch must first be set by issuing the WREN instruction (See Table 30 and Figure 17). CS is first taken LOW. Then the WREN instruction is clocked into the X3102. After all eight bits of the instruction are transmitted, CS must then be taken HIGH. If the user continues the write operation without taking CS HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the EEPROM memory array, the user issues the EWRITE instruction, followed by the 16 bit address and

the data to be written. Only the last 9 bits of the address are used and bits [15:9] are specified to be zeroes. This is minimally a thirty-two clock operation. CS must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 16 bytes of data to the X3102. The only restriction is the 16 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will “roll over” to the first address of the page and overwrite any data that may have been previously written.

For a byte or page write operation to be completed, CS can only be brought HIGH after bit 0 of the last data byte to be written is clocked in. If it is brought HIGH at any other time, the write operation will not be completed. Refer to Figure 18 and Figure 19 for detailed illustration of the write sequences and time frames in which CS going HIGH are valid.

EEPROM Read Status Operation (EEREAD STAT)

If there is not a nonvolatile write in progress, the EEREAD STAT instruction returns the IDLock byte from the IDLock register which contains the IDLock bits IDL2-IDL0 (Table 29). The IDLock bits define the IDLock condition (Table 28). The other bits are reserved and will return ‘0’ when read.

If a nonvolatile write to the EEPROM (i.e. EWRITE instruction) is in progress, the EEREAD STAT returns a HIGH on SO. When the nonvolatile write cycle in the EEPROM is completed, the status register data is read out.

Clocking SCK is valid during a nonvolatile write in progress, but is not necessary. If the SCK line is clocked, the pointer to the status register is also clocked, even though the SO pin shows the status of the nonvolatile write operation (See Figure 20).

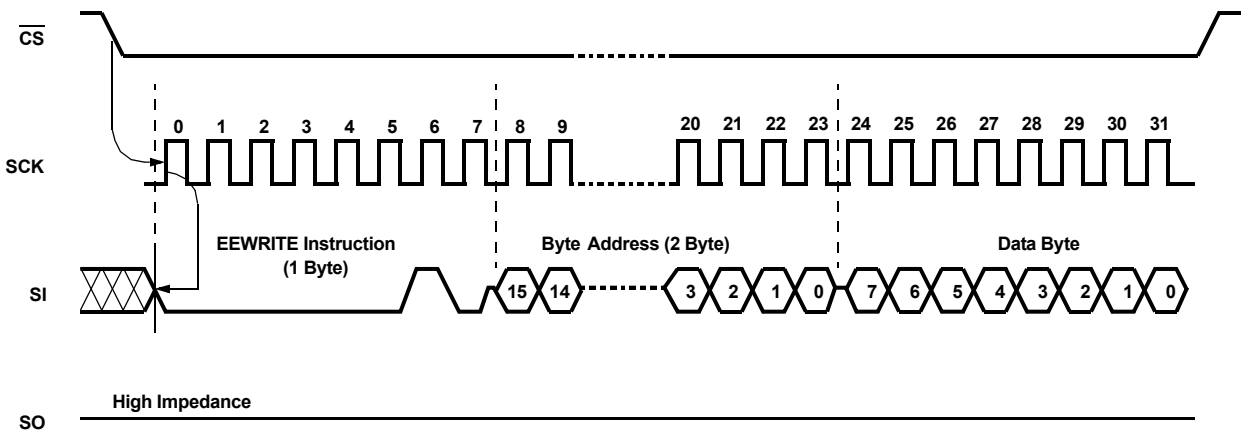


FIGURE 18. EEPROM BYTE WRITE (EWRITE) OPERATION SEQUENCE

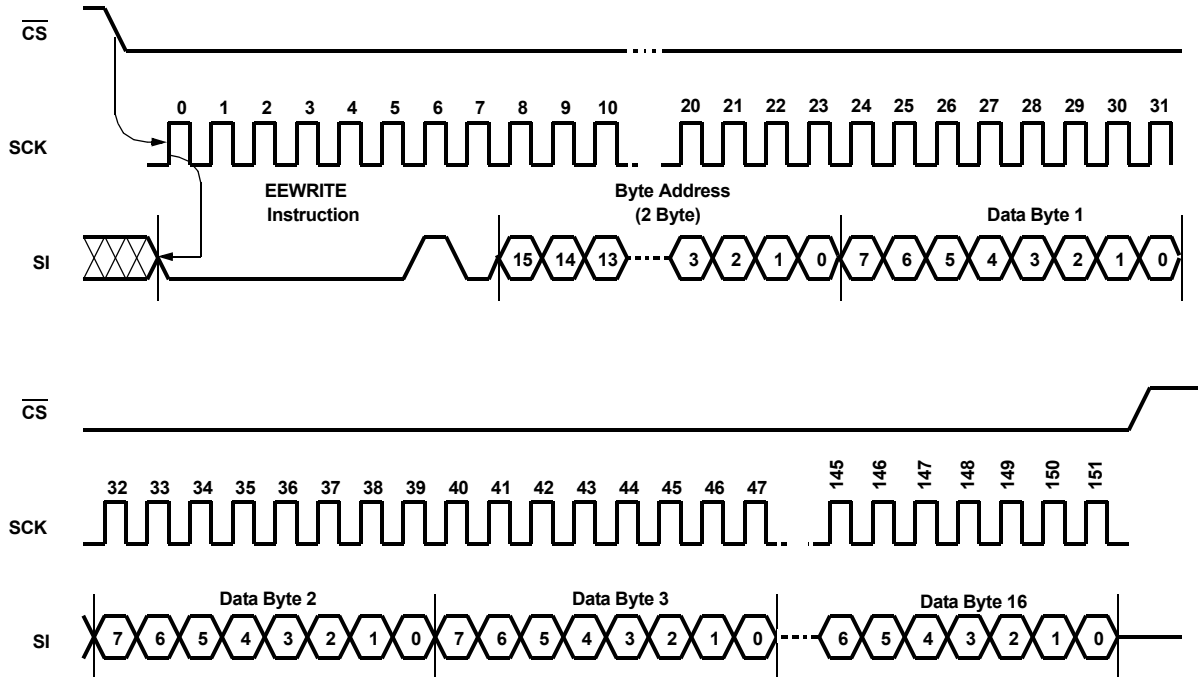


FIGURE 19. EEPROM PAGE WRITE (EERWRITE) OPERATION SEQUENCE

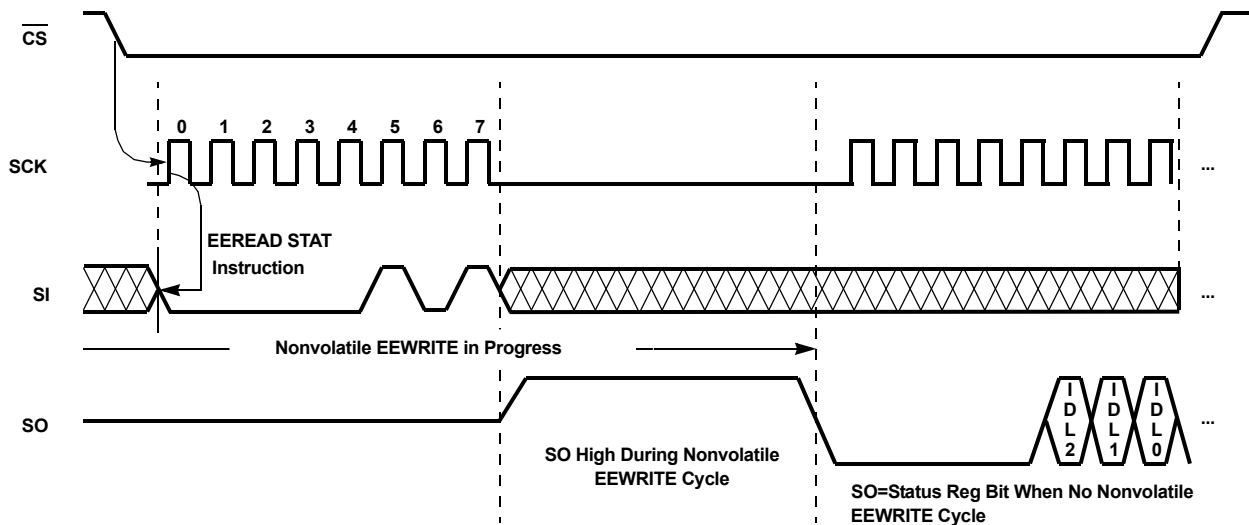


FIGURE 20. EEPROM READ STATUS (EEREAD STAT) OPERATION SEQUENCE

EEPROM Read Sequence (EEREAD)

When reading from the X3102 EEPROM memory, \overline{CS} is first pulled LOW to select the device. The 8-bit EEREAD instruction is transmitted to the X3102, followed by the 16-bit address, of which the last 9 bits are used (bits [15:9] specified to be zeroes). After the EEREAD opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (01FFh), the address counter rolls over to address 0000h, allowing the read cycle to be continued

indefinitely. The read operation is terminated by taking \overline{CS} HIGH. Refer to the EEPROM Read (EEREAD) operation sequence illustrated in Figure 21.

Write Configuration Register (WCFIG)

The Write Configuration Register (WCFIG) instruction updates the static part of the Configuration Register. These new values take effect immediately, for example writing a new Over-discharge voltage limit. However, to make these changes permanent, so they remain if the cell voltages are removed, an EERWRITE operation to the EEPROM array is required following the WCFIG command. This command is shown in Figure 22.

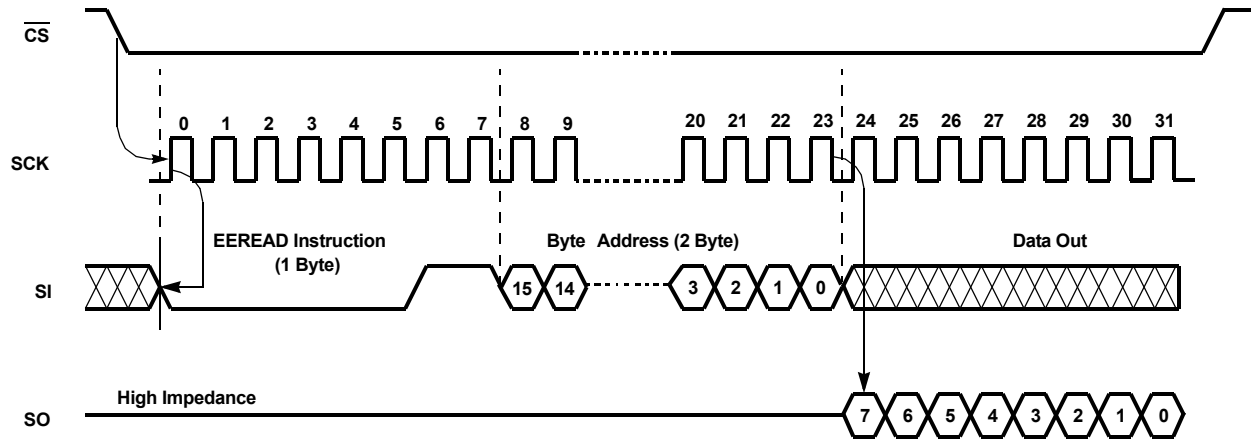


FIGURE 21. EEPROM (EEREAD) READ OPERATION SEQUENCE

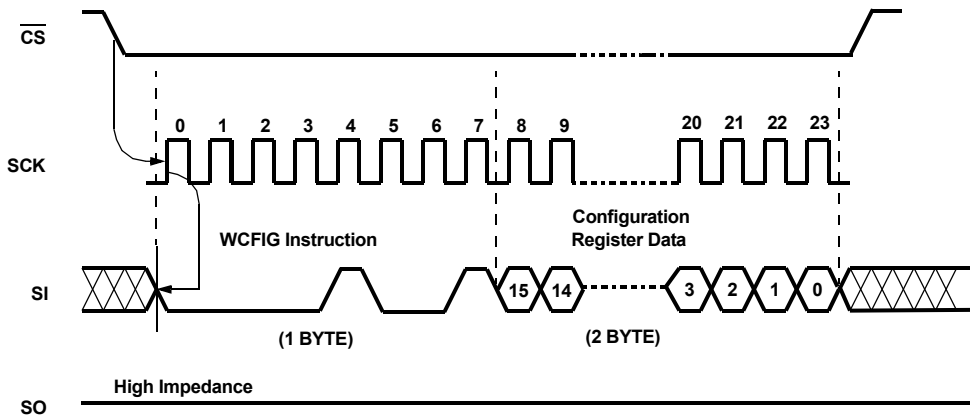


FIGURE 22. WRITE CONFIGURATION REGISTER (WCFIG) OPERATION SEQUENCE

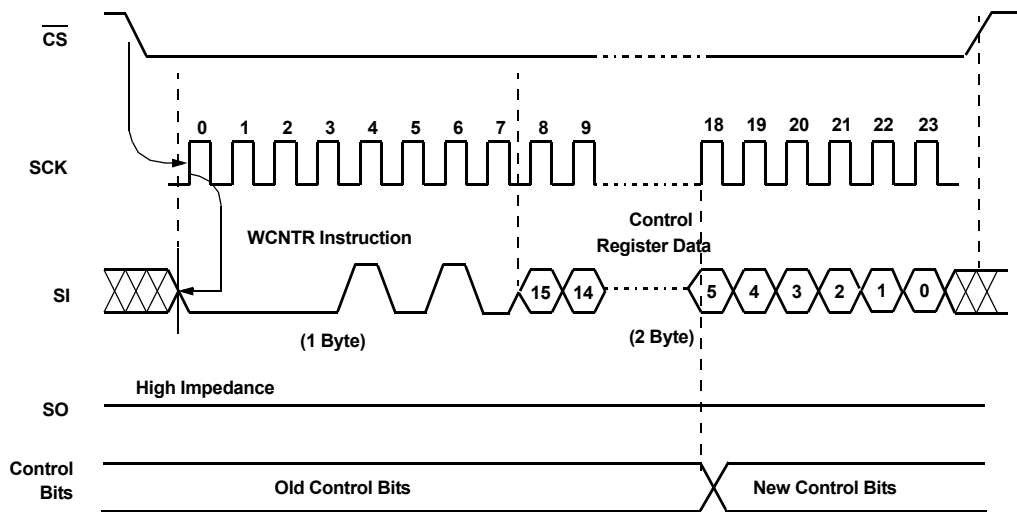


FIGURE 23. WRITE CONTROL REGISTER (WCNTR) OPERATION SEQUENCE

Write Control Register (WCNTRL)

The Write Control Register (WCNTRL) instruction updates the contents of the volatile Control Register. This command sets the status of the FET control pins, the cell balancing outputs, the current sense gain and external entry to the sleep mode. Since this instruction controls a volatile register, no other commands are required and there is no delay time needed after the instruction, before subsequent commands. The operation of the WCNTRL command is shown in Figure 23.

Read Status Register (RDSTAT)

The Read Status Register (RDSTAT) command returns the status of the X3102. The Status Register contains three bits that indicate whether the voltage regulator is stabilized, and if there are any protection failure conditions. The operation of the RDSTAT instruction is shown in Figure 24.

Set ID Lock (SET IDL)

The contents of the EEPROM memory array in the X3102 can be locked in one of eight configurations using the SET ID lock command. When a section of the EEPROM array is locked, the contents cannot be changed, even when a valid write operation attempts a write to that area. The SET IDL command operation is shown in Figure 25.

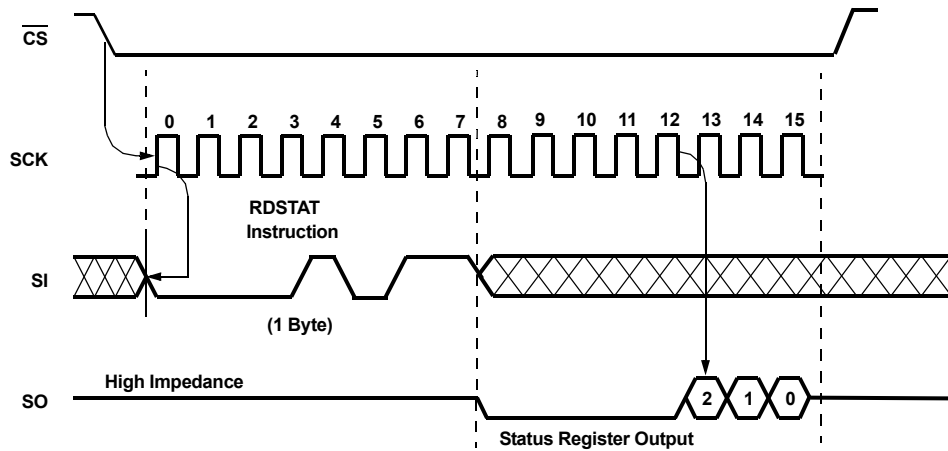


FIGURE 24. READ STATUS REGISTER (RDSTAT) OPERATION SEQUENCE

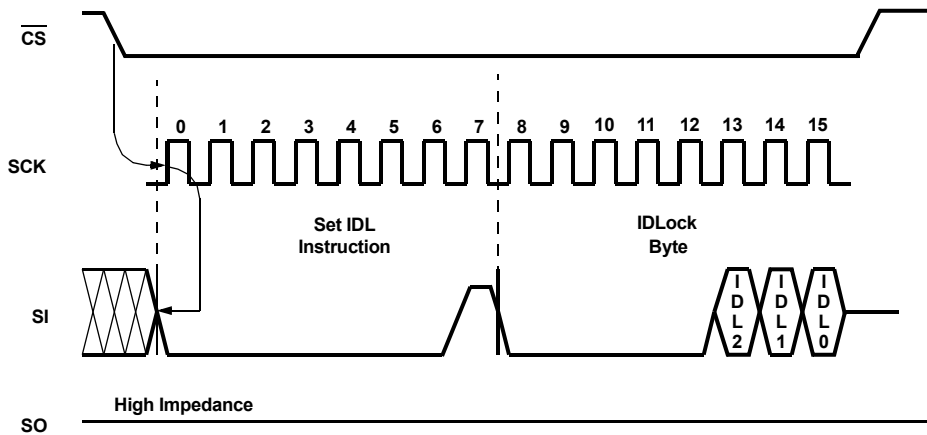
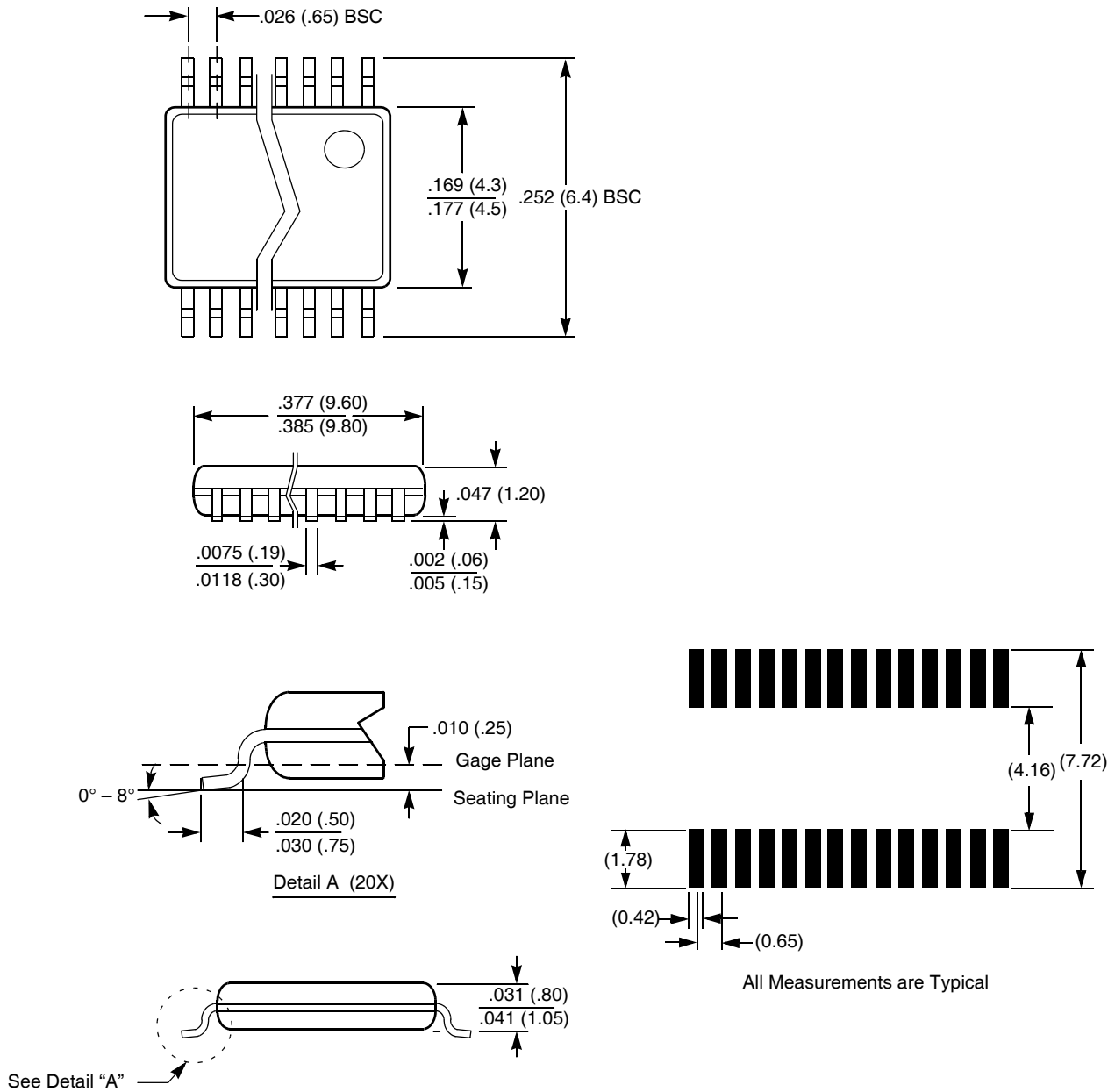


FIGURE 25. EEPROM IDLock (SET IDL) OPERATION SEQUENCE

28-Lead Plastic, TSSOP, Package Code V28



NOTE: All dimensions in inches (in parentheses in millimeters)

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