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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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## 8-BIT SINGLE-CHIP MICROCONTROLLER

### DESCRIPTION

The  $\mu$ PD78P083(A) is a member of the  $\mu$ PD78083 Subseries of the 78K/0 Series products. Comparing with the  $\mu$ PD78P083 (standard), more strict quality assurance programs are applied to this product (called Special of the quality grade in NEC). The  $\mu$ PD78P083(A) uses one-time PROM instead of internal ROMs of the  $\mu$ PD78081(A) and  $\mu$ PD78082(A).

Because this device can be programmed by users, it is ideally suited for applications involving the evaluation of systems in development stages, small-scale production of many different products, and rapid development and time-to-market of a new product.

**The details of functions are described in the user's manuals. Be sure to read the following manuals before designing.**

$\mu$ PD78083 Subseries User's Manual : U12176E  
78K/0 Series User's Manual — Instructions : IEU-1372

### FEATURES

- Pin-compatible with mask ROM version (except  $V_{PP}$  pin)
- Internal PROM: 24 Kbytes <sup>Note</sup>
  - $\mu$ PD78P083CU(A),  $\mu$ PD78P083GB(A): One-time programmable (ideally suited for small-scale production)
- Internal high-speed RAM: 512 bytes <sup>Note</sup>
- Can be operated in the same supply voltage as the mask ROM version ( $V_{DD} = 1.8$  to  $5.5$  V)
- Corresponding to QTOP™ Microcontrollers (under planning)

**Note** The internal PROM and internal high-speed RAM capacities can be changed by setting the internal memory size switching register (IMS).

- Remarks**
1. QTOP microcontroller is a general term for microcontrollers which incorporate one-time PROM and are totally supported by NEC's programming service (from programming to marking, screening and verification).
  2. For the differences between PROM and Mask ROM versions, refer to **Chapter 1. DIFFERENCES BETWEEN THE  $\mu$ PD78P083(A) AND MASK ROM VERSIONS.**

The information in this document is subject to change without notice.

**ORDERING INFORMATION**

Part Number	Package	Internal ROM
μPD78P083CU(A)	42-pin plastic shrink DIP (600 mil)	One-Time PROM
μPD78P083GB(A)-3B4	44-pin plastic QFP (10 × 10 mm)	One-Time PROM
μPD78P083GB(A)-3BS-MTX <sup>Note</sup>	44-pin plastic QFP (10 × 10 mm)	One-Time PROM

**Note** Under planning

**Caution** μPD78P083GB(A) has two types of packages. (Refer to Chapter 7. PACKAGE DRAWINGS). Consult an NEC's sales representative for suppliable packages.

**QUALITY GRADE**

Part Number	Package	Quality Grades
μPD78P083CU(A)	42-pin plastic shrink DIP (600 mil)	Special
μPD78P083GB(A)-3B4	44-pin plastic QFP (10 × 10 mm)	Special
μPD78P083GB(A)-3BS-MTX <sup>Note</sup>	44-pin plastic QFP (10 × 10 mm)	Special

**Note** Under planning

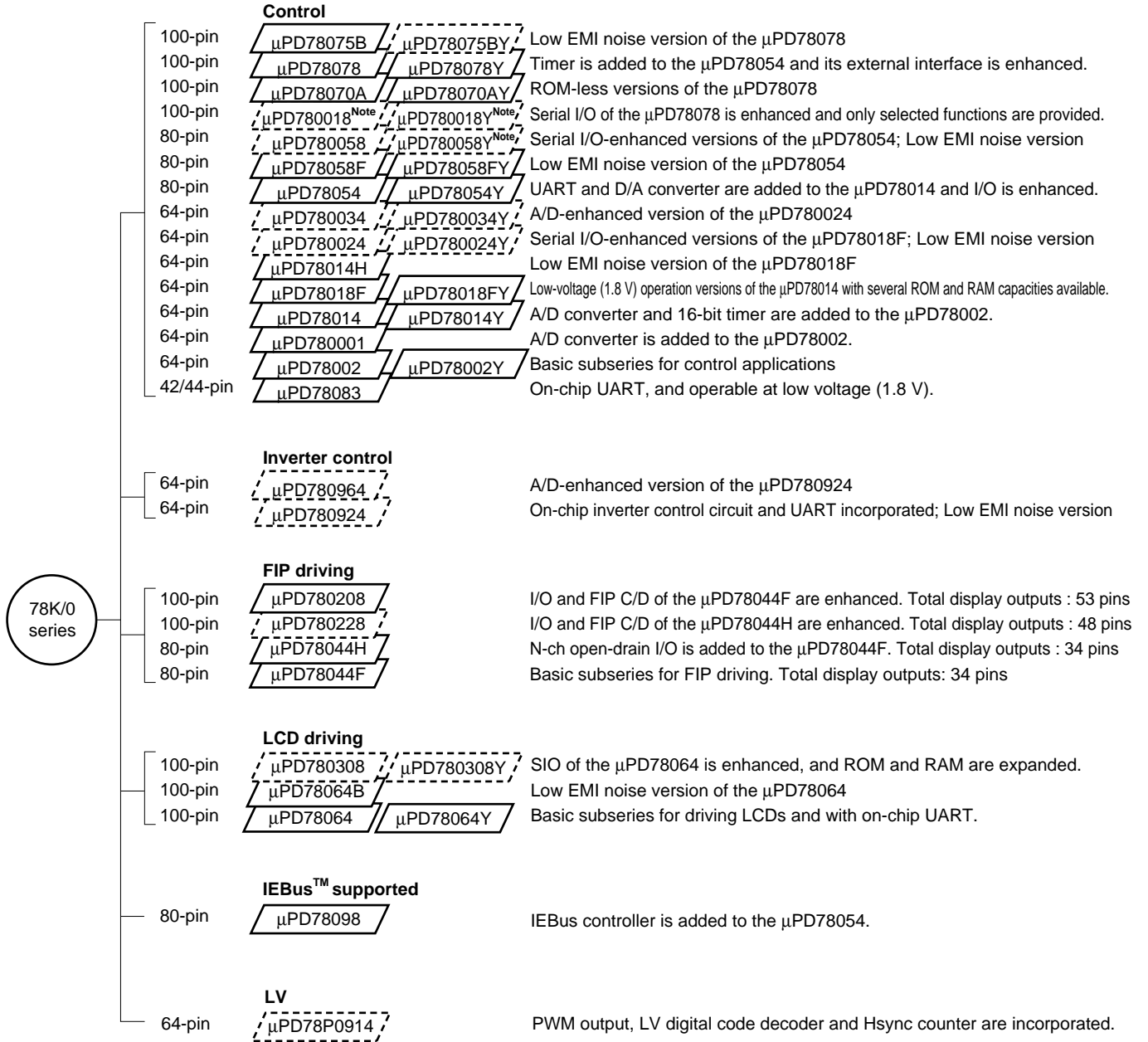
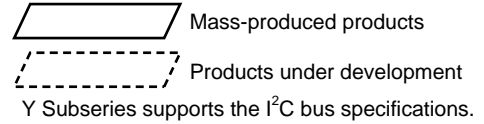
Please refer to “Quality grades on NEC Semiconductor Devices” (Document number C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

**Deferences between μPD78P083(A) and μPD78P083**

Product Item	μPD78P083(A)	μPD78P083
Quality Grade	Special	Standard
Package	42-pin plastic shrink DIP (600 mil) 44-pin plastic QFP (10 × 10 mm)	42-pin plastic shrink DIP (600 mil) 44-pin plastic QFP (10 × 10 mm) 42-pin ceramic shrink DIP (with window) (600 mil)

**78K/0 SERIES DEVELOPMENT**

The following shows the 78K/0 Series products development. Subseries names are shown inside frames.



**Note** Under planning

The following table shows the differences among subseries functions.

Function Subseries name		ROM capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial interface	I/O	V <sub>DD</sub> MIN. value	External expansion						
			8-bit	16-bit	Watch	WDT													
Control	μPD78075B	32K to 40K	4 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	88	1.8 V	Available						
	μPD78078	48K to 60K									61								
	μPD78070A	—									88								
	μPD780018	48K to 60K								2 ch	—	2 ch (Time division 3-wire: 1 ch)		88	1.8 V				
	μPD780058	24K to 60K												68					
	μPD78058F	48K to 60K												69					
	μPD78054	16K to 60K												2.0 V					
	μPD780034	8K to 32K												—		8 ch	3 ch (UART: 1 ch, Time division 3-wire: 1 ch)	51	1.8 V
	μPD780024													8 ch		—		53	
	μPD78014H	8K to 60K								2 ch	—	2 ch		53	2.7 V				
	μPD78018F															8K to 32K			
	μPD78014	8K to 32K								1 ch	—	1 ch (UART: 1 ch)		39	1.8 V				
	μPD780001	8K												53					
	μPD78002	8K to 16K	—																
μPD78083	—	8 ch	—	1 ch (UART: 1 ch)	33	1.8 V	—												
Inverter control	μPD780964	8K to 32K	3 ch	<b>Note</b>	—	1 ch	—	8 ch	—	2 ch (UART: 2 ch)	47	2.7 V	Available						
	μPD780924						8 ch												
FIP driving	μPD780208	32K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	2 ch	74	2.7 V	—						
	μPD780228	48K to 60K								3 ch	—	—		1 ch	72	4.5 V			
	μPD78044H	32K to 48K								2 ch	1 ch	1 ch		—	—	2 ch	68	2.7 V	
	μPD78044F	16K to 40K																	
LCD driving	μPD780308	48K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	3 ch (Time division UART: 1 ch)	57	2.0 V	—						
	μPD78064B	32K								2 ch (UART: 1 ch)									
	μPD78064	16K to 32K																	
IEBus supported	μPD78098	32K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	69	2.7 V	Available						
LV	μPD78P0914	32K	6 ch	—	—	1 ch	8 ch	—	—	2 ch	54	4.5 V	Available						

**Note** 10 bits timer: 1 channel

**FUNCTION DESCRIPTION**

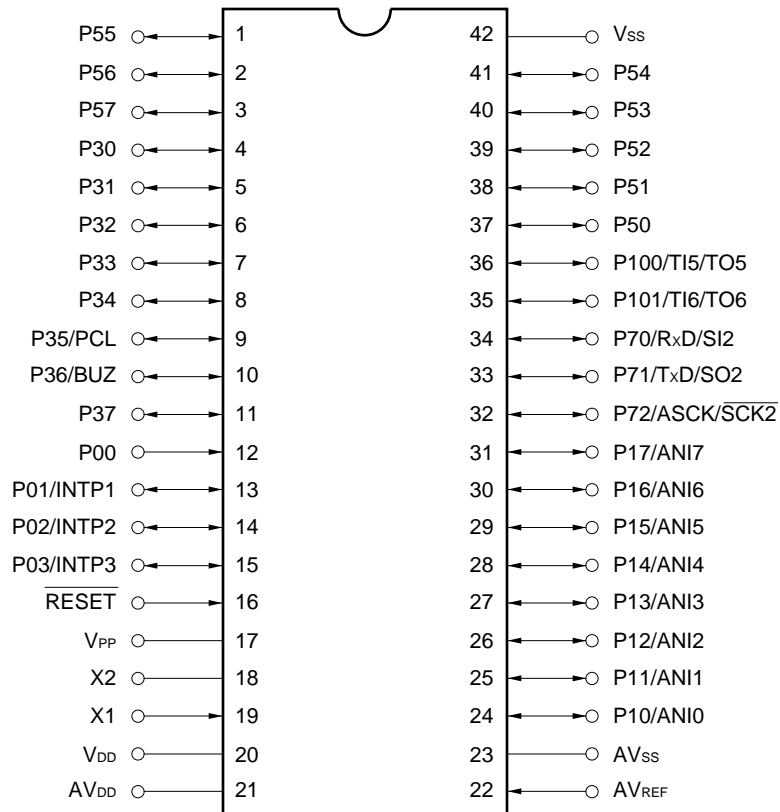
Item	Function	
Internal memory	<ul style="list-style-type: none"> <li>• PROM: 24 Kbytes <sup>Note</sup></li> <li>• RAM</li> <li>High-speed RAM: 512 bytes <sup>Note</sup></li> </ul>	
Memory space	64 Kbytes	
General register	8 bits x 32 registers (8 bits x 8 registers x 4 banks)	
Instruction cycles	Instruction execution time variable function is integrated. 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@5.0-MHz operation with main system clock)	
Instruction set	<ul style="list-style-type: none"> <li>• 16-bit operation</li> <li>• Multiply/divide (8 bits x 8 bits, 16 bits ÷ 8 bits)</li> <li>• Bit manipulation (set, reset, test, Boolean operation)</li> <li>• BCD adjust, etc.</li> </ul>	
I/O ports	Total : 33 <ul style="list-style-type: none"> <li>• CMOS input : 1</li> <li>• CMOS input/output : 32</li> </ul>	
A/D converter	<ul style="list-style-type: none"> <li>• 8-bit resolution x 8 channels</li> </ul>	
Serial interface	<ul style="list-style-type: none"> <li>• 3-wired serial I/O/UART mode selectable: 1 channel</li> </ul>	
Timer	<ul style="list-style-type: none"> <li>• 8-bit timer/event counter: 2 channels</li> <li>• Watchdog timer: 1 channel</li> </ul>	
Timer output	2 pins (8-bit PWM output enable)	
Clock output	19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, and 5.0 MHz (@ 5.0-MHz operation with main system clock)	
Buzzer output	1.2 kHz, 2.4 kHz, 4.9 kHz, and 9.8 kHz (@ 5.0-MHz operation with main system clock)	
Vectored-interrupt source	Maskable	Internal : 8 external : 3
	Non-maskable	Internal : 1
	Software	Internal : 1
Power supply voltage	V <sub>DD</sub> = 1.8 to 5.5 V	
Operating ambient temperature	T <sub>A</sub> = -40 to +85°C	
Packages	<ul style="list-style-type: none"> <li>• 42-pin plastic shrink DIP (600 mil)</li> <li>• 44-pin plastic QFP (10 × 10 mm)</li> </ul>	

**Note** Internal PROM and high-speed RAM capacities can be changed by setting the memory size switching register (IMS).

**PIN CONFIGURATIONS (Top View)**

**(1) Normal operating mode**

- 42-pin plastic shrink DIP (600 mil)  
μPD78P083CU(A)

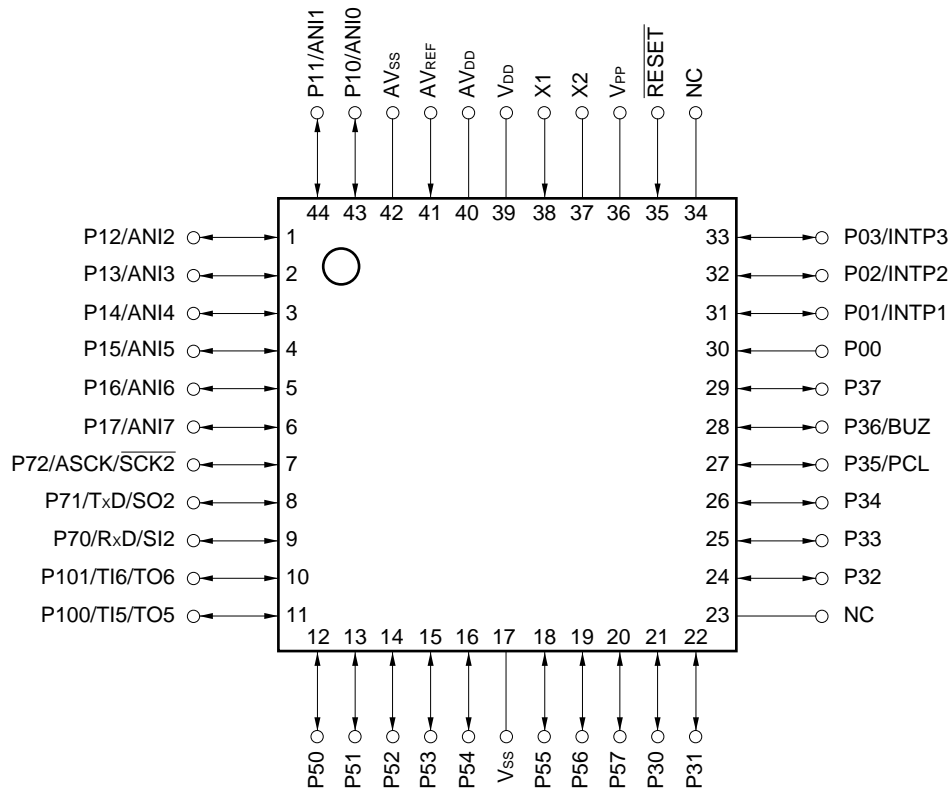


- Cautions**
1. Connect V<sub>PP</sub> pin directly to V<sub>SS</sub>.
  2. Connect AV<sub>DD</sub> pin to V<sub>DD</sub>.
  3. Connect AV<sub>SS</sub> pin to V<sub>SS</sub>.



- 44-pin plastic QFP (10 x 10 mm)  
 μPD78P083GB(A)-3B4, μPD78P083GB(A)-3BS-MTX<sup>Note</sup>

**Note** Under planning

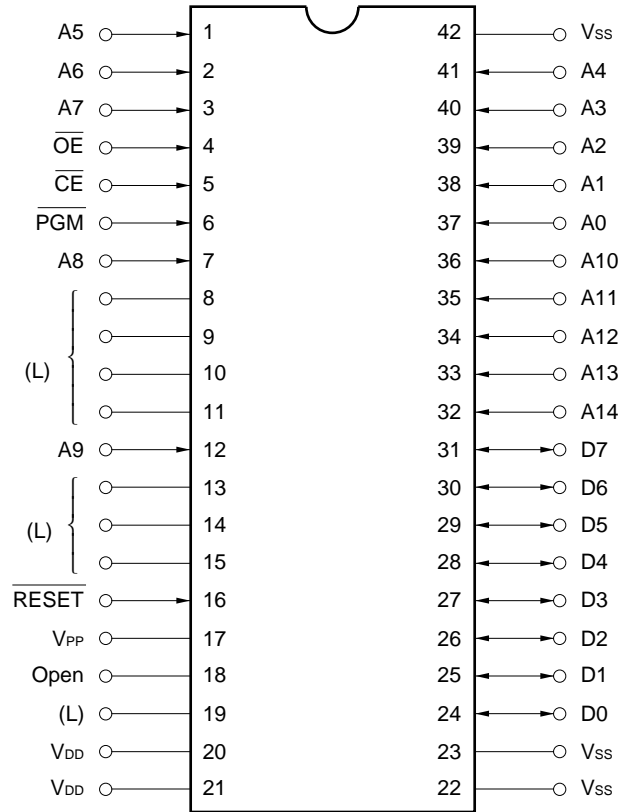


- Cautions**
1. Connect V<sub>PP</sub> pin directly to V<sub>SS</sub>.
  2. Connect AV<sub>DD</sub> pin to V<sub>DD</sub>.
  3. Connect AV<sub>SS</sub> pin to V<sub>SS</sub>.
  4. Connect NC pin to V<sub>SS</sub> for noise protection (It can be left open).

ANI0 to ANI7	: Analog Input	PCL	: Programmable Clock
ASCK	: Asynchronous Serial Clock	$\overline{\text{RESET}}$	: Reset
AV <sub>DD</sub>	: Analog Power Supply	RxD	: Receive Data
AV <sub>REF</sub>	: Analog Reference Voltage	$\overline{\text{SCK2}}$	: Serial Clock
AV <sub>SS</sub>	: Analog Ground	SI2	: Serial Input
BUZ	: Buzzer Clock	SO2	: Serial Output
INTP1 to INTP3	: Interrupt from Peripherals	TI5, TI6	: Timer Input
NC	: Non-connection	TO5, TO6	: Timer Output
P00 to P03	: Port 0	TxD	: Transmit Data
P10 to P17	: Port 1	V <sub>DD</sub>	: Power Supply
P30 to P37	: Port 3	V <sub>PP</sub>	: Programming Power Supply
P50 to P57	: Port 5	V <sub>SS</sub>	: Ground
P70 to P72	: Port 7	X1, X2	: Crystal (Main System Clock)
P100, P101	: Port 10		

(2) PROM programming mode

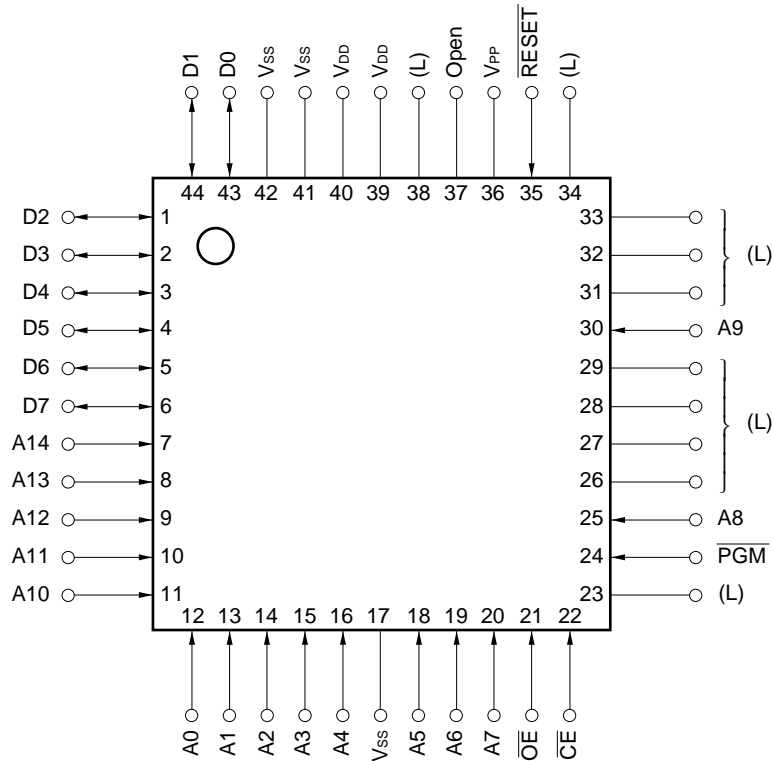
- 42-pin plastic shrink DIP (600 mil)  
μPD78P083CU(A)



- Cautions**
1. (L): Individually connect to Vss via a pull-down resistor.
  2. Vss: Connect to GND.
  3. RESET: Set to low level.
  4. Open: Leave open.

- 44-pin plastic QFP (10 x 10 mm)  
 μPD78P083GB(A)-3B4, μPD78P083GB(A)-3BS-MTX<sup>Note</sup>

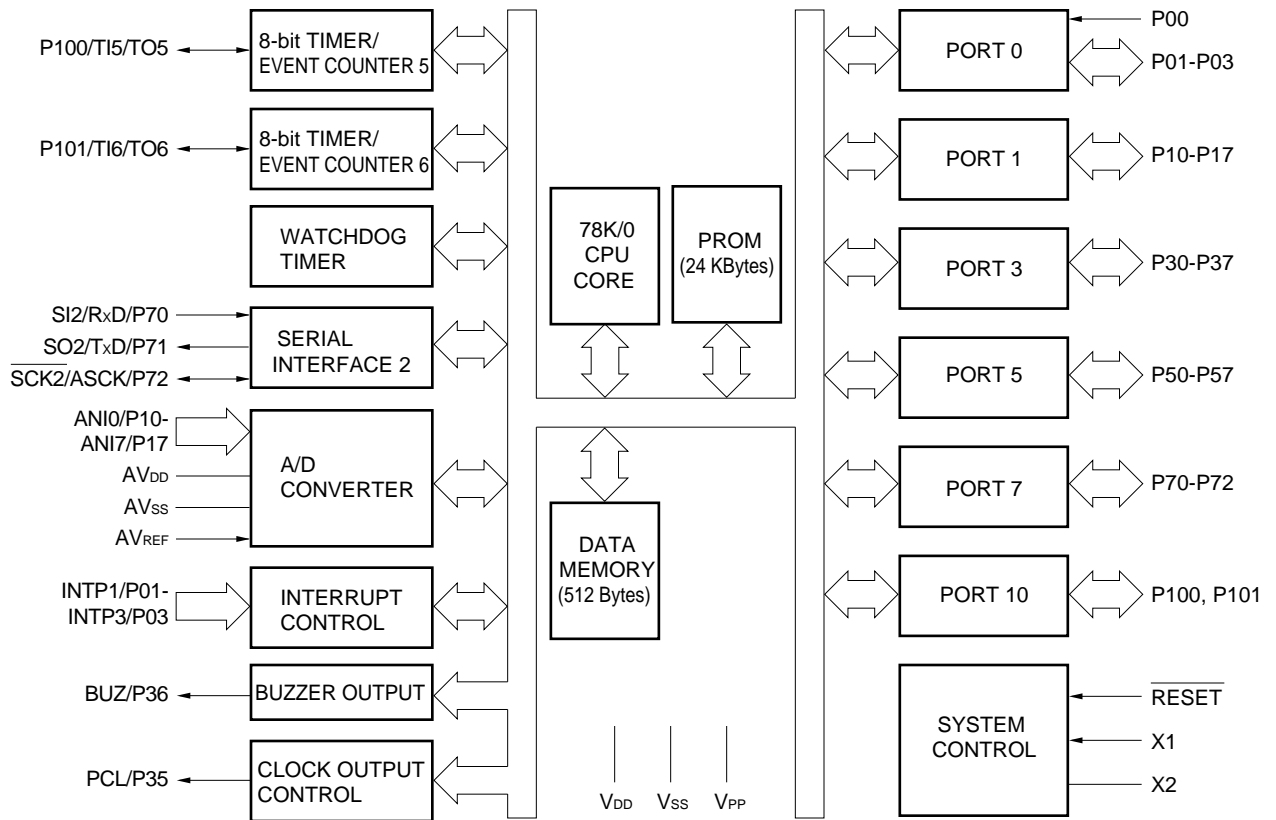
**Note** Under planning



- Cautions**
1. (L): Individually connect to Vss via a pull-down resistor.
  2. Vss: Connect to GND.
  3.  $\overline{\text{RESET}}$ : Set to low level.
  4. Open: Leave open.

A0 to A14	: Address Bus	$\overline{\text{RESET}}$	: Reset
$\overline{\text{CE}}$	: Chip Enable	VDD	: Power Supply
D0 to D7	: Data Bus	VPP	: Programming Power Supply
$\overline{\text{OE}}$	: Output Enable	Vss	: Ground
$\overline{\text{PGM}}$	: Program		

BLOCK DIAGRAM



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## 1. DIFFERENCES BETWEEN THE $\mu$ PD78P083(A) AND MASK ROM VERSIONS

The  $\mu$ PD78P083(A) is a single-chip microcontroller with an on-chip one-time PROM.

Setting the memory size switching register (IMS) makes the functions except the PROM specification identical to the mask ROM versions.

Table 1-1 shows differences between the PROM version ( $\mu$ PD78P083(A)) and mask ROM versions ( $\mu$ PD78081(A) and  $\mu$ PD78082(A)).

**Table 1-1. Differences between the  $\mu$ PD78P083(A) and Mask ROM Versions**

Parameter	$\mu$ PD78P083(A)	Mask ROM Versions
Internal ROM type	One-time PROM/EPROM	Mask ROM
Internal ROM capacity	24 Kbytes	$\mu$ PD78081(A) : 8 Kbytes $\mu$ PD78082(A) : 16 Kbytes
Internal high-speed RAM capacity	512 bytes	$\mu$ PD78081(A) : 256 bytes $\mu$ PD78082(A) : 384 bytes
Internal ROM and internal high-speed RAM capacity change by memory size switching register (IMS)	Enable <sup>Note</sup>	Disable
IC pin	No	Yes
V <sub>PP</sub> pin	Yes	No
Electrical specifications	Refer to a data sheet of each product	

**Note** The internal PROM becomes 24 Kbytes and the internal high-speed RAM becomes 512 bytes by the  $\overline{\text{RESET}}$  input.

2. PIN FUNCTIONS

2.1 Pins in Normal Operating Mode

(1) Port pins

Pin Name	Input/Output	Function		After Reset	Alternate Function
P00	Input	Port 0	Input only	Input	—
P01	Input/output	4-bit input/output port	Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.	Input	INTP1
P02					INTP2
P03					INTP3
P10 to P17	Input/output	Port 1	8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software. <sup>Note</sup>	Input	ANI0 to ANI7
P30-P34	Input/output	Port 3	8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.	Input	—
P35					PCL
P36					BUZ
P37					—
P50 to P57	Input/output	Port 5	8-bit input/output port Can drive up to seven LEDs directly. Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.	Input	—
P70	Input/output	Port 7	3-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.	Input	SI2/RxD
P71					SO2/TxD
P72					̄SCK2/ASCK
P100	Input/output	Port 10	2-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.	Input	TI5/TO5
P101					TI6/TO6

**Note** When P10/ANI0-P17/ANI7 pins are used as the analog inputs for the A/D converter, set the port 1 to the input mode. The on-chip pull-up resistor is automatically disabled.



(2) Non-port pins

Pin Name	Input/Output	Function	After Reset	Alternate Function
INTP1	Input	External interrupt input by which the active edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P01
INTP2				P02
INTP3				P03
SI2	Input	Serial interface serial data input.	Input	P70/RxD
SO2	Output	Serial interface serial data output.	Input	P71/TxD
SCK2	Input/Output	Serial interface serial clock input/output.	Input	P72/ASCK
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/ $\overline{\text{SCK2}}$
TI5	Input	External count clock input to 8-bit timer (TM5).	Input	P100/TO5
TI6		External count clock input to 8-bit timer (TM6).		P101/TO6
TO5	Output	8-bit timer output.	Input	P100/TO5
TO6				P101/TO6
PCL	Output	Clock output. (for main system clock trimming)	Input	P35
BUZ	Output	Buzzer output.	Input	P36
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AV <sub>REF</sub>	Input	A/D converter reference voltage input.	–	–
AV <sub>DD</sub>	–	A/D converter analog power supply. Connected to V <sub>DD</sub> .	–	–
AV <sub>SS</sub>	–	A/D converter ground potential. Connected to V <sub>SS</sub> .	–	–
RESET	Input	System reset input.	–	–
X1	Input	Main system clock oscillation crystal connection.	–	–
X2	–		–	–
V <sub>DD</sub>	–	Positive power supply.	–	–
V <sub>PP</sub>	–	High-voltage applied during program write/verification. Connected directly to V <sub>SS</sub> in normal operating mode.	–	–
V <sub>SS</sub>	–	Ground potential.	–	–
NC	–	Does not internally connected. Connect to V <sub>SS</sub> . (It can be left open)	–	–

**2.2 Pins in PROM Programming Mode**

Pin Name	Input/Output	Function
RESET	Input	PROM programming mode setting When +5 V or +12.5 V is applied to the V <sub>PP</sub> pin and a low-level signal is applied to the RESET pin, this chip is set in the PROM programming mode.
V <sub>PP</sub>	Input	PROM programming mode setting and high-voltage applied during program write/verification.
A0 to A14	Input	Address bus
D0-D7	Input/output	Data bus
CE	Input	PROM enable input/program pulse input
OE	Input	Read strobe input to PROM
PGM	Input	Program/program inhibit input in PROM programming mode.
V <sub>DD</sub>	—	Positive power supply
V <sub>SS</sub>	—	Ground potential

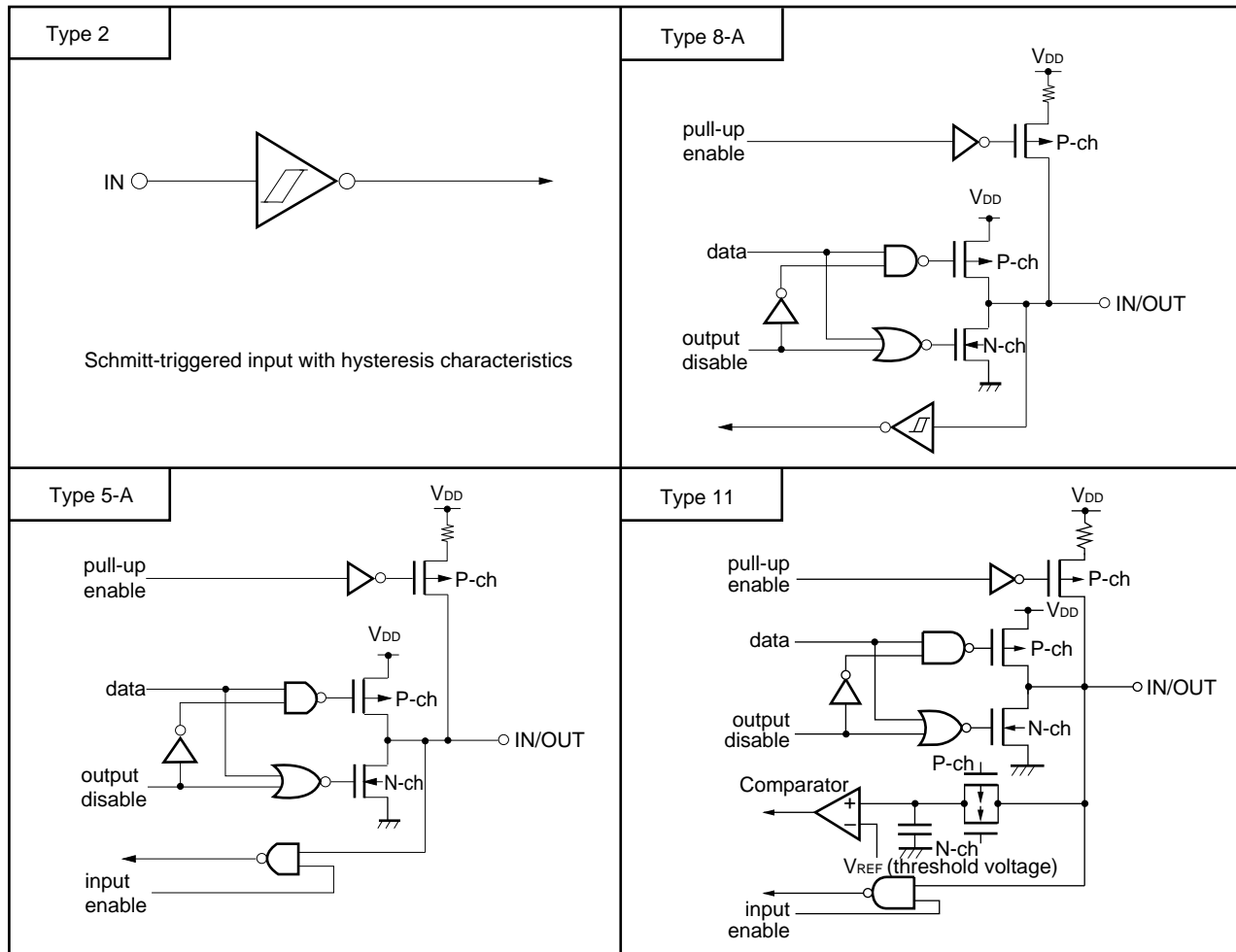
**2.3 Pin Input/Output Circuits and Recommended Connection of Unused Pins**

Types of input/output circuits of the pins and recommended connection of unused pins are shown in Table 2-1. For the configuration of each type of input/output circuit, see Figure 2-1.

**Table 2-1. Type of Input/Output Circuit of Each Pin**

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection for Unused Pins		
P00	2	Input	Connect to V <sub>SS</sub> .		
P01/INTP1	8-A	Input/Output	Independently connect to V <sub>SS</sub> via a resistor.		
P02/INTP2					
P03/INTP3					
P10/ANI0 to P17/ANI7	11	Input/Output	Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor.		
P30 to P32	5-A				
P33, P34	8-A				
P35/PCL	5-A				
P36/BUZ	5-A				
P37					
P50 to P57					
P70/SI2/RxD	8-A				
P71/SO2/TxD	5-A				
P72/SCK2/ASCK	8-A				
P100/TI5/TO5	8-A				
P101/TI6/TO6					
RESET	2			Input	—
AV <sub>REF</sub>	—			—	Connect to V <sub>SS</sub> .
AV <sub>DD</sub>		Connect to V <sub>DD</sub> .			
AV <sub>SS</sub>		Connect to V <sub>SS</sub> .			
V <sub>PP</sub>		Connect directly to V <sub>SS</sub> .			
NC		Connect to V <sub>SS</sub> (can leave open)			

Figure 2-1. Types of Pin Input/Output Circuits



### 3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

This is a register to disable use of part of internal memories by software. By setting this memory size switching register (IMS), it is possible to get the same memory mapping as that of the mask ROM versions with a different internal memory (ROM, RAM).

IMS is set with an 8-bit memory manipulation instruction.

RESET input sets IMS to 46H.

**Figure 3-1. Internal Memory Size Switching Register Format**

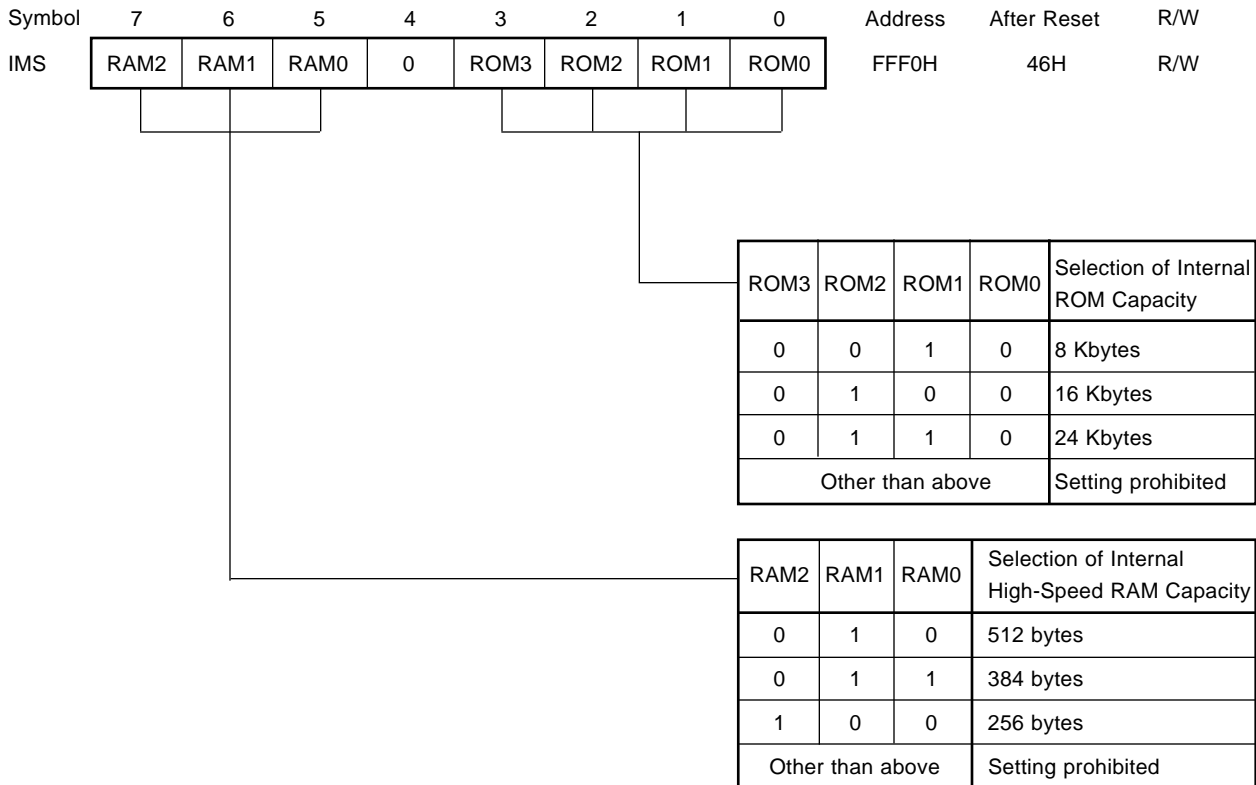


Table 3-1 shows the setting values of IMS which make the memory mapping the same as that of the mask ROM version.

**Table 3-1. Internal Memory Size Switching Register Setting Values**

Target Mask ROM Versions	IMS Setting Value
μPD78081(A)	82H
μPD78082(A)	64H

4. PROM PROGRAMMING

The μPD78P083(A) has an internal 24-Kbyte PROM as a program memory. For programming, set the PROM programming mode with the V<sub>PP</sub> and  $\overline{\text{RESET}}$  pins. For the connection of unused pins, refer to “PIN CONFIGURATIONS (TOP VIEW) (2) PROM programming mode.”

**Caution** Programs must be written in addresses 0000H to 5FFFH (The last address 5FFFH must be specified). They cannot be written by a PROM programmer which cannot specify the write address.

4.1 Operating Modes

When +5 V or +12.5 V is applied to the V<sub>PP</sub> pin and a low-level signal is applied to the  $\overline{\text{RESET}}$  pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 4-1 when the  $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$ , and  $\overline{\text{PGM}}$  pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 4-1. Operating Modes of PROM Programming

Pin	$\overline{\text{RESET}}$	V <sub>PP</sub>	V <sub>DD</sub>	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	D0 to D7
Operating Mode							
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				x	H	H	High-impedance
				x	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	x	High-impedance
Standby				H	x	x	High-impedance

x : L or H

**(1) Read mode**

Read mode is set if  $\overline{CE} = L$ ,  $\overline{OE} = L$  is set.

**(2) Output disable mode**

Data output becomes high-impedance, and is in the output disable mode, if  $\overline{OE} = H$  is set.

Therefore, it allows data to be read from any device by controlling the  $\overline{OE}$  pin, if multiple  $\mu$ PD78P083(A)s are connected to the data bus.

**(3) Standby mode**

Standby mode is set if  $\overline{CE} = H$  is set.

In this mode, data outputs become high-impedance irrespective of the  $\overline{OE}$  status.

**(4) Page data latch mode**

Page data latch mode is set if  $\overline{CE} = H$ ,  $\overline{PGM} = H$ ,  $\overline{OE} = L$  are set at the beginning of page write mode.

In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

**(5) Page write mode**

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1-ms program pulse (active low) to the  $\overline{PGM}$  pin with  $\overline{CE} = H$ ,  $\overline{OE} = H$ . Then, program verification can be performed, if  $\overline{CE} = L$ ,  $\overline{OE} = L$  are set.

If programming is not performed by a one-time program pulse, X times ( $X \leq 10$ ) write and verification operations should be executed repeatedly.

**(6) Byte write mode**

Byte write is executed when a 0.1-ms program pulse (active low) is applied to the  $\overline{PGM}$  pin with  $\overline{CE} = L$ ,  $\overline{OE} = H$ . Then, program verification can be performed if  $\overline{OE} = L$  is set.

If programming is not performed by a one-time program pulse, X times ( $X \leq 10$ ) write and verification operations should be executed repeatedly.

**(7) Program verify mode**

Program verify mode is set if  $\overline{CE} = L$ ,  $\overline{PGM} = H$ ,  $\overline{OE} = L$  are set.

In this mode, check if a write operation is performed correctly after the write.

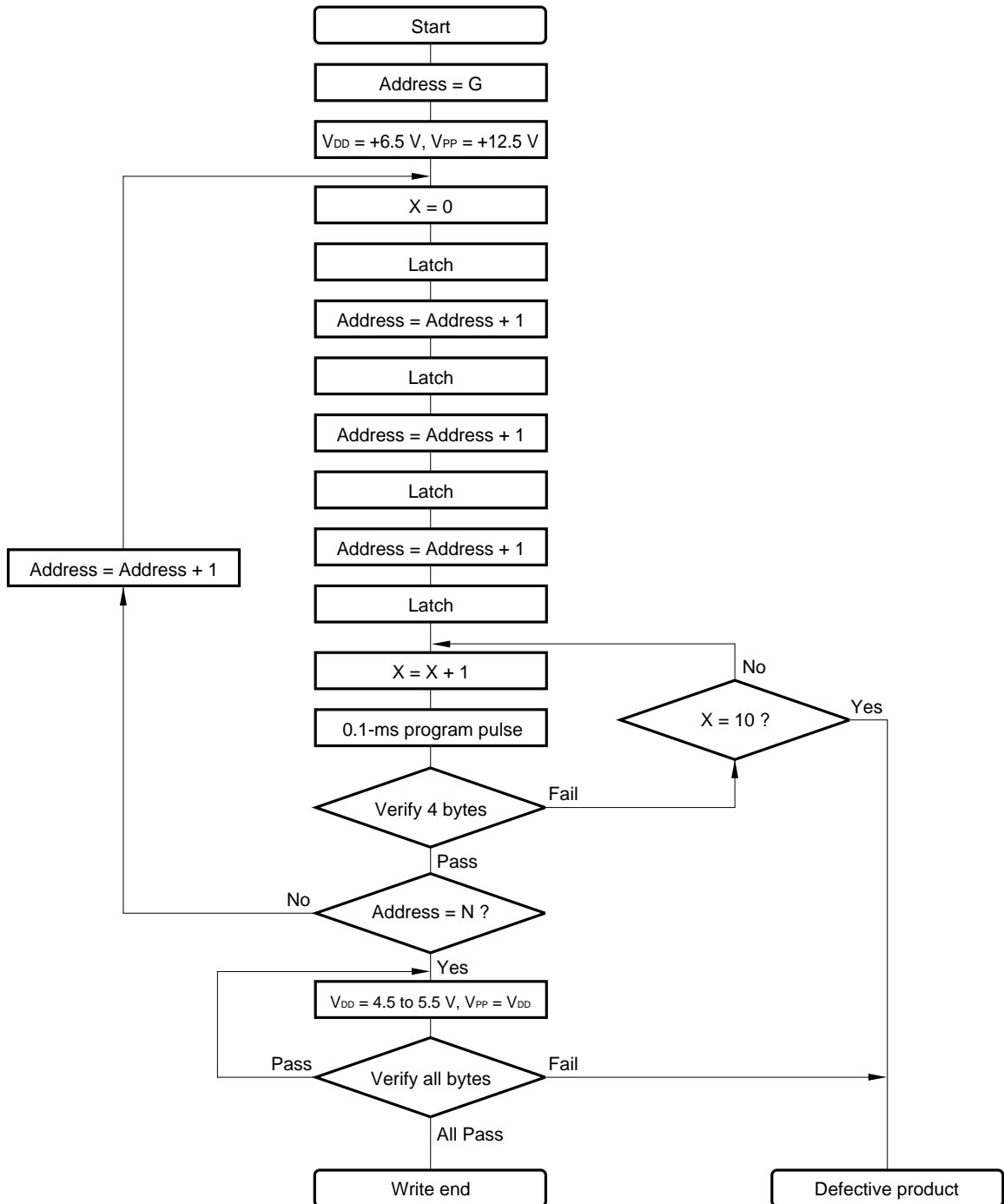
**(8) Program inhibit mode**

Program inhibit mode is used when the  $\overline{OE}$  pin,  $V_{PP}$  pin, and D0-D7 pins of multiple  $\mu$ PD78P083(A)s are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the  $\overline{PGM}$  pin driven high.

4.2 PROM Write Procedure

Figure 4-1. Page Program Mode Flow Chart



G = Start address  
 N = Program last address

Figure 4-2. Page Program Mode Timing

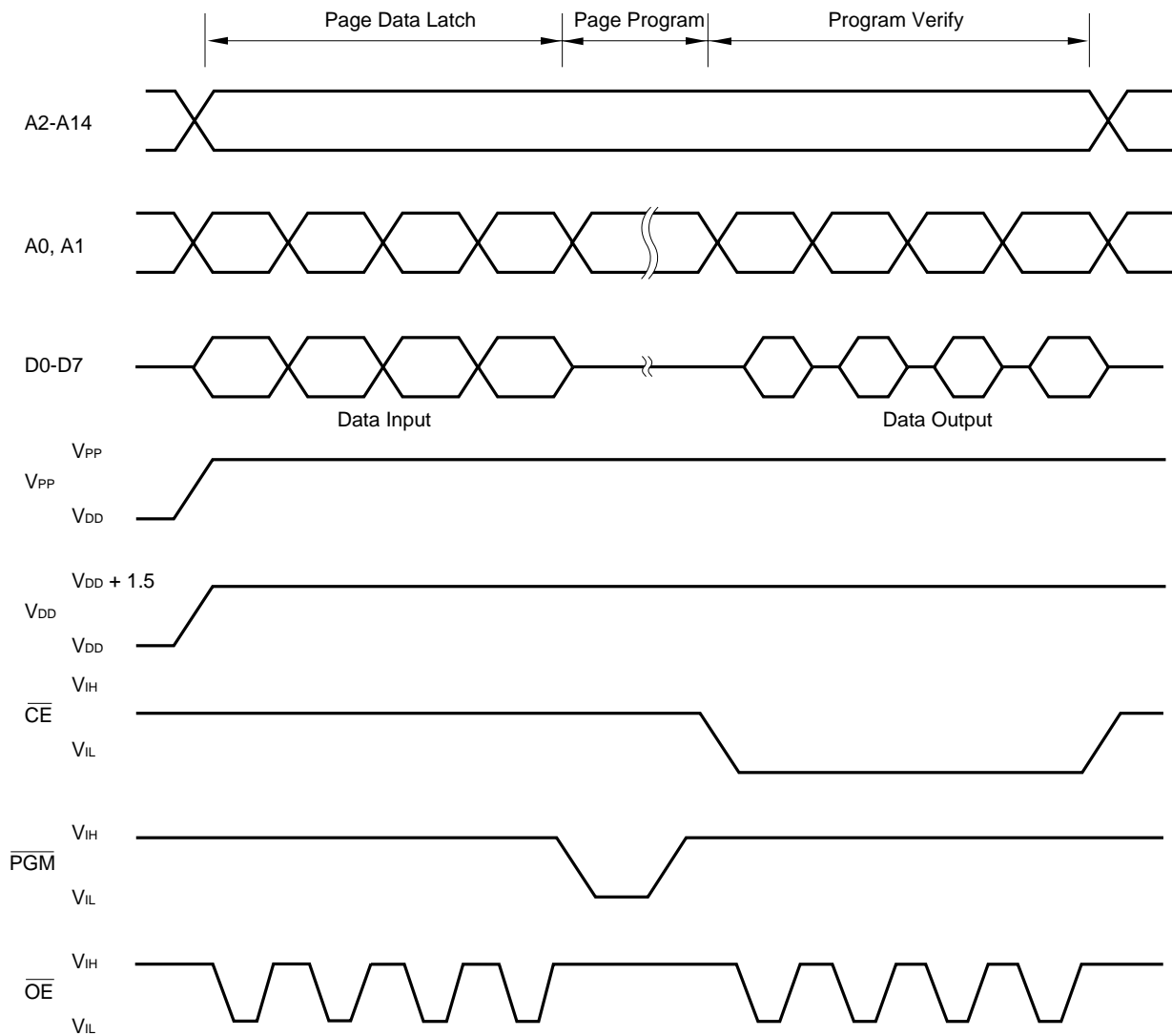
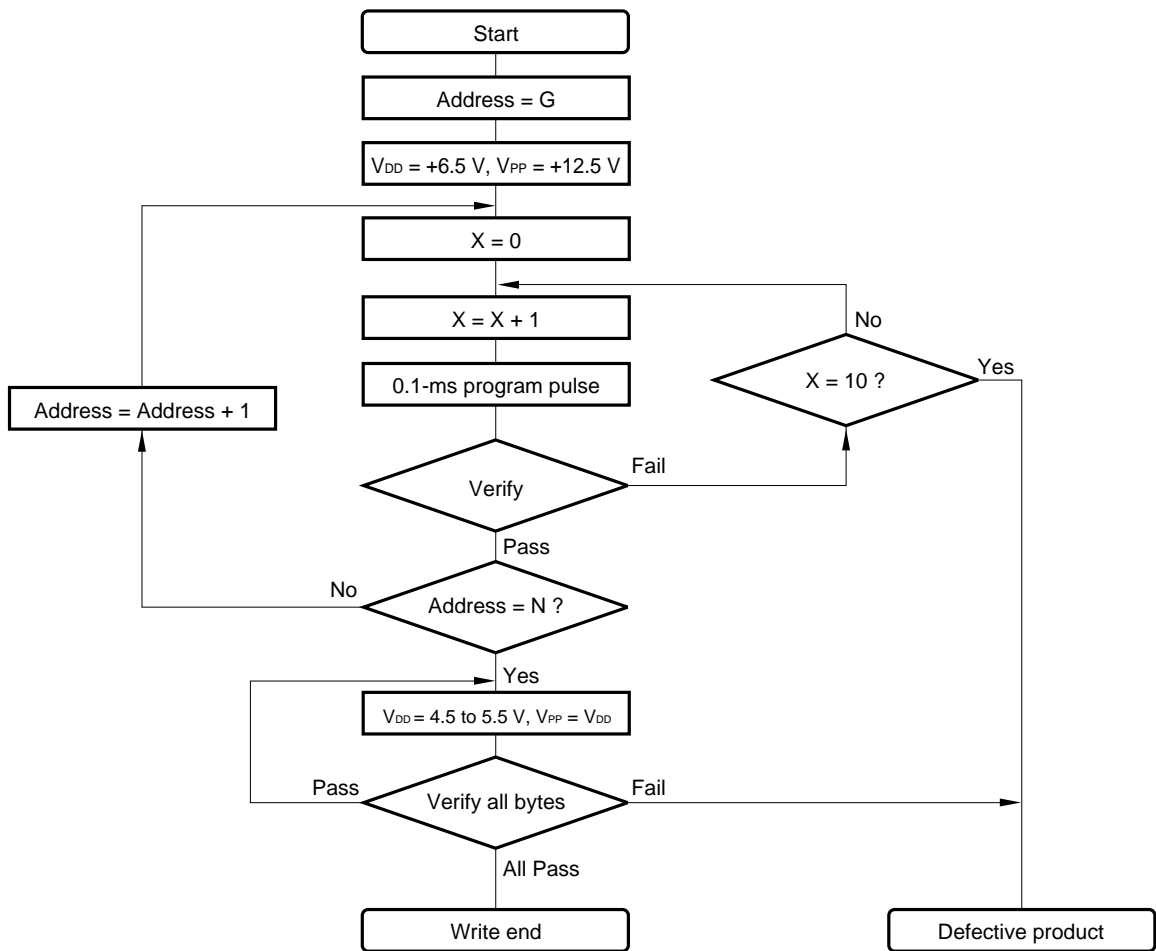




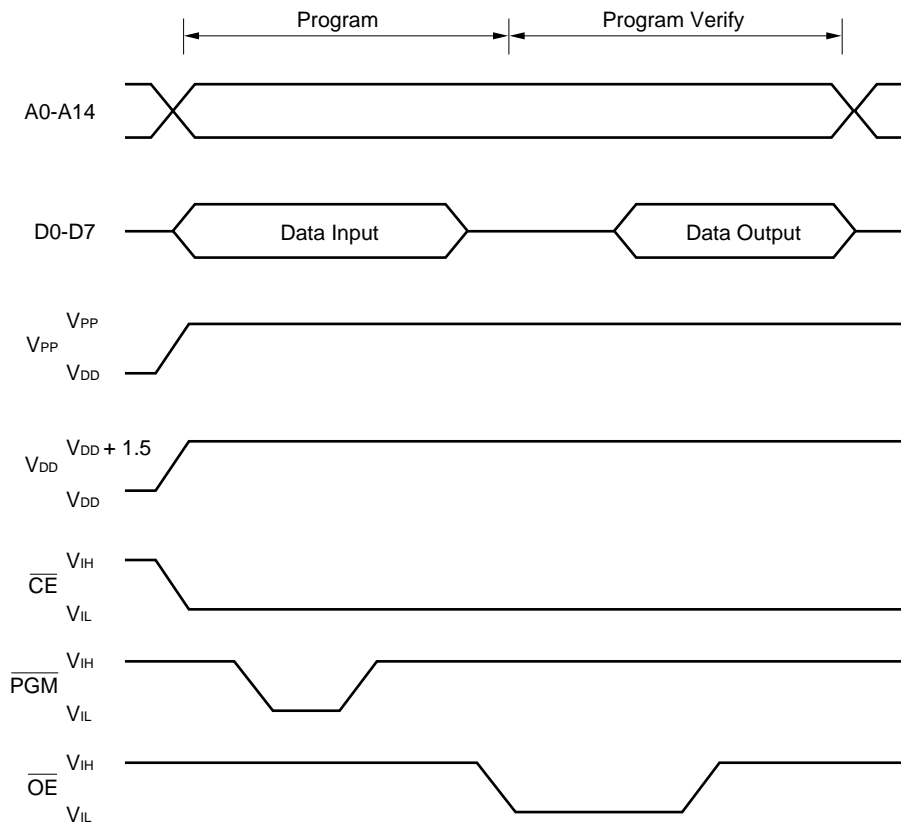
Figure 4-3. Byte Program Mode Flow Chart



G = Start address

N = Program last address

Figure 4-4. Byte Program Mode Timing



- Cautions**
1. V<sub>DD</sub> should be applied before V<sub>PP</sub> and removed after V<sub>PP</sub>.
  2. V<sub>PP</sub> must not exceed +13.5 V including overshoot.
  3. Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to V<sub>PP</sub>.

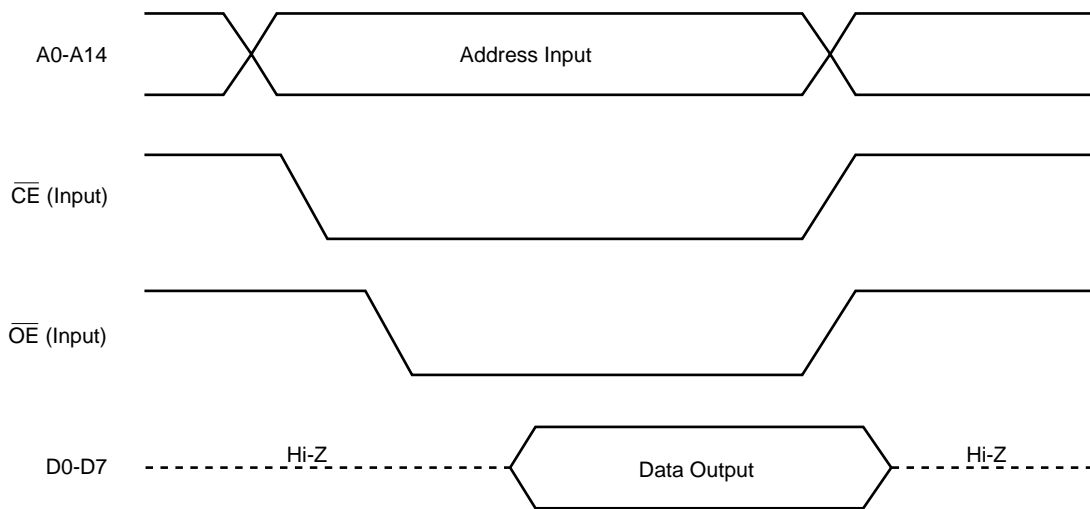
**4.3 PROM Read Procedure**

The contents of PROM are readable to the external data bus (D0-D7) according to the read procedure shown below.

- (1) Fix the  $\overline{\text{RESET}}$  pin at low level, supply +5 V to the  $V_{PP}$  pin, and connect all other unused pins as shown in “PIN CONFIGURATIONS (TOP VIEW) (2) PROM programming mode”.
- (2) Supply +5 V to the  $V_{DD}$  and  $V_{PP}$  pins.
- (3) Input address of read data into the A0 to A14 pins.
- (4) Read mode
- (5) Output data to D0 to D7 pins.

The timings of the above steps (2) to (5) are shown in Figure 4-5.

**Figure 4-5. PROM Read Timings**



**5. ONE-TIME PROM VERSION SCREENING**

The one-time PROM version (μPD78P083CU(A), 78P083GB(A)-3B4, 78P083GB(A)-3BS-MTX<sup>Note</sup>) cannot be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

**Note** Under planning

Storage Temperature	Storage Time
125°C	24 hours

NEC offers for an additional fee one-time PROM writing to marking, screening, and verify for products designated as QTOP Microcontroller. A fee-charged service for the μPD78P083(A) is under planning. Consult an NEC sales representative for details.

6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T<sub>A</sub> = 25°C)

Parameter	Symbol	Test Conditions		Ratings	Unit		
Supply voltage	V <sub>DD</sub>			-0.3 to +7.0	V		
	V <sub>PP</sub>			-0.3 to +13.5	V		
	AV <sub>DD</sub>			-0.3 to V <sub>DD</sub> + 0.3	V		
	AV <sub>REF</sub>			-0.3 to V <sub>DD</sub> + 0.3	V		
	AV <sub>SS</sub>			-0.3 to +0.3	V		
Input voltage	V <sub>I1</sub>			-0.3 to V <sub>DD</sub> + 0.3			
	V <sub>I2</sub>	A9	PROM programming mode	-0.3 to +13.5	V		
Output voltage	V <sub>O</sub>			-0.3 to V <sub>DD</sub> + 0.3	V		
Analog input voltage	V <sub>AN</sub>	P10 to P17	Analog input pins	AV <sub>SS</sub> - 0.3 to AV <sub>REF</sub> + 0.3	V		
Output current, high	I <sub>OH</sub>	Per pin		-10	mA		
		Total for P10 to P17, P50 to P54, P70 to P72, P100, P101		-15	mA		
		Total for P01 to P03, P30 to P37, P55 to P57		-15	mA		
Output current, low	I <sub>OL</sub> <sup>Note</sup>	Per pin	Peak value	30	mA		
			r.m.s. value	15	mA		
		Total for P50 to P54	Peak value	100	mA		
			r.m.s. value	70	mA		
		Total for P55 to P57	Peak value	100	mA		
			r.m.s. value	70	mA		
		Total for P10 to P17, P70 to P72, P100, P101	Peak value	50	mA		
			r.m.s. value	20	mA		
		Total for P01 to P03, P30 to P37	Peak value	50	mA		
			r.m.s. value	20	mA		
		Operating ambient temperature	T <sub>A</sub>			-40 to +85	°C
		Storage temperature	T <sub>stg</sub>			-65 to +150	°C

**Note** The r.m.s. value should be calculated as follows: [r.m.s. value] = [Peak value] × √Duty

**Caution** If the absolute maximum rating of even one of the above parameters is exceeded, the quality of the product may be degraded. The absolute maximum ratings are therefore the rated values that may, if exceeded, physically damage the product. Be sure to use the product with all the absolute maximum ratings observed.

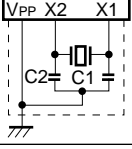
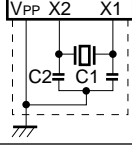
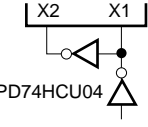
**Remark** Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

**Capacitance** (TA = 25°C, VDD = VSS = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>IN</sub>	f = 1 MHz, Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C <sub>IO</sub>	f = 1 MHz, Unmeasured pins returned to 0 V.			15	pF
		P01 to P03, P10 to P17, P30 to P37, P50 to P57, P70 to P72, P100, P101				

**Remark** Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

**Main System Clock Oscillator Characteristics** (TA = -40 to +85°C, VDD = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f <sub>X</sub> ) <sup>Note 1</sup>	V <sub>DD</sub> = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time <sup>Note 2</sup>	After V <sub>DD</sub> came to MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f <sub>X</sub> ) <sup>Note 1</sup>		1.0		5.0	MHz
		Oscillation stabilization time <sup>Note 2</sup>	V <sub>DD</sub> = 4.5 to 5.5 V			10 30	ms
External clock		X1 input frequency (f <sub>X</sub> ) <sup>Note 1</sup>		1.0		5.0	MHz
		X1 input high- and low-level widths (t <sub>xH</sub> , t <sub>xL</sub> )		85		500	ns

**Notes** 1. Only the oscillator characteristics are shown. For the instruction execution time, refer to **AC Characteristics**.

2. Time required for oscillation to stabilize after a reset or the STOP mode has been released.

**Caution** When using the oscillation circuit of the main system clock, wire the portion enclosed in broken lines in the figures as follows to avoid adverse influences on the wiring capacitance:

- Keep the wiring length as short as possible.
- Do not cross the wiring over other signal lines.
- Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.
- Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V<sub>SS</sub>.
- Do not connect the power source pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

DC Characteristics (TA = -40 to +85°C, VDD = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	VIH1	P10 to P17, P30 to P32, P35 to P37, P50 to P57, P71	VDD = 2.7 to 5.5 V	0.7VDD		VDD	V
				0.8VDD		VDD	V
	VIH2	P00 to P03, P33, P34, P70, P72, P100, P101, RESET	VDD = 2.7 to 5.5 V	0.8VDD		VDD	V
				0.85VDD		VDD	V
	VIH3	X1, X2	VDD = 2.7 to 5.5 V	VDD - 0.5		VDD	V
				VDD - 0.2		VDD	V
Input voltage, low	VIL1	P10 to P17, P30 to P32, P35 to P37, P50 to P57, P71	VDD = 2.7 to 5.5 V	0		0.3VDD	V
				0		0.2VDD	V
	VIL2	P00 to P03, P33, P34, P70, P72, P100, P101, RESET	VDD = 2.7 to 5.5 V	0		0.2VDD	V
				0		0.15VDD	V
	VIL3	X1, X2	VDD = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
Output voltage, high	VOH	VDD = 4.5 to 5.5 V, IOH = -1 mA		VDD - 1.0			V
		IOH = -100 μA		VDD - 0.5			V
Output voltage, low	VOL	P50 to P57	VDD = 2.0 to 4.5 V, IOL = 10 mA			0.8	V
			VDD = 4.5 to 5.5 V, IOL = 15 mA		0.4	2.0	V
		P01 to P03, P10 to P17, P30 to P37, P70 to P72, P100, P101	VDD = 4.5 to 5.5 V, IOL = 1.6 mA			0.4	V
			IOL = 400 μA			0.5	V
Input-leak current, high	IIH1	VIN = VDD	P00 to P03, P10 to P17, P30 to P37, P50 to P57, P70 to P72, P100, P101, RESET			3	μA
	IIH2		X1, X2			20	μA
Input-leak current, low	IIIL1	VIN = 0 V	P00 to P03, P10 to P17, P30 to P37, P50 to P57, P70 to P72, P100, P101, RESET			-3	μA
	IIIL2		X1, X2			-20	μA
Output leak current, high	ILOH	VOUT = VDD				3	μA
Output leak current, low	ILOL	VOUT = 0 V				-3	μA
Software pull-up resistor	R	VIN = 0 V	P01 to P03, P10 to P17, P30 to P37, P50 to P57, P70 to P72, P100, P101	15	40	90	kΩ

**Remark** Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

**DC Characteristics** (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Supply current <sup>Note 1</sup>	I <sub>DD1</sub>	5.0-MHz crystal oscillation operating mode (f <sub>XX</sub> = 2.5 MHz) <sup>Note 2</sup>	V <sub>DD</sub> = 5.0 V ± 10% <sup>Note 4</sup>		5.4	16.2	mA
			V <sub>DD</sub> = 3.0 V ± 10% <sup>Note 5</sup>		0.8	2.4	mA
			V <sub>DD</sub> = 2.0 V ± 10% <sup>Note 5</sup>		0.45	1.35	mA
		5.0-MHz crystal oscillation operating mode (f <sub>XX</sub> = 5.0 MHz) <sup>Note 3</sup>	V <sub>DD</sub> = 5.0 V ± 10% <sup>Note 4</sup>		9.5	28.5	mA
			V <sub>DD</sub> = 3.0 V ± 10% <sup>Note 5</sup>		1.0	3.0	mA
	I <sub>DD2</sub>	5.0-MHz crystal oscillation HALT mode (f <sub>XX</sub> = 2.5 MHz) <sup>Note 2</sup>	V <sub>DD</sub> = 5.0 V ± 10%		1.4	4.2	mA
			V <sub>DD</sub> = 3.0 V ± 10%		0.5	1.5	mA
			V <sub>DD</sub> = 2.0 V ± 10%		280	840	μA
		5.0-MHz crystal oscillation HALT mode (f <sub>XX</sub> = 5.0 MHz) <sup>Note 3</sup>	V <sub>DD</sub> = 5.0 V ± 10%		1.6	4.8	mA
			V <sub>DD</sub> = 3.0 V ± 10%		0.65	1.95	mA
	I <sub>DD3</sub>	STOP mode	V <sub>DD</sub> = 5.0 V ± 10%		0.1	30	μA
			V <sub>DD</sub> = 3.0 V ± 10%		0.05	10	μA
V <sub>DD</sub> = 2.0 V ± 10%				0.05	10	μA	

- Notes**
1. Not including AV<sub>REF</sub>, AV<sub>DD</sub> currents or port currents (including current flowing into internal pull-up resistors).
  2. f<sub>XX</sub> = f<sub>X</sub>/2 operation (when oscillation mode selection register (OSMS) is set to 00H).
  3. f<sub>XX</sub> = f<sub>X</sub> operation (when oscillation mode selection register (OSMS) is set to 01H).
  4. High-speed mode operation (when processor clock control register (PCC) is set to 00H).
  5. Low-speed mode operation (when processor clock control register (PCC) is set to 04H).

**Remark** f<sub>XX</sub>: Main system clock frequency (f<sub>X</sub> or f<sub>X</sub>/2)  
 f<sub>X</sub>: Main system clock oscillation frequency



AC Characteristics

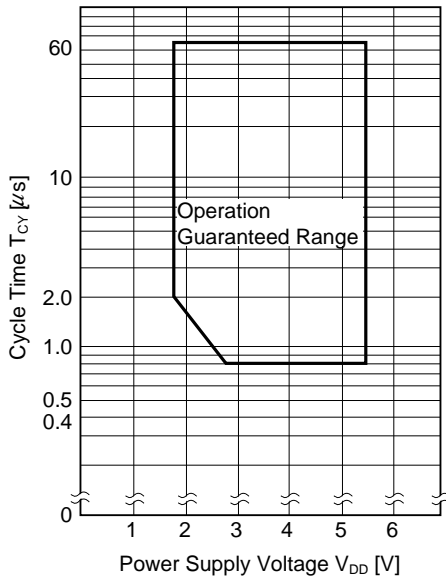
(1) Basic Operation (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Cycle time (minimum instruction execution time)	T <sub>CY</sub>	f <sub>XX</sub> = f <sub>X</sub> /2 <sup>Note1</sup>	V <sub>DD</sub> = 2.7 to 5.5 V	0.8		64	μs
				2.0		64	μs
		f <sub>XX</sub> = f <sub>X</sub> <sup>Note2</sup>	3.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	0.4		32	μs
			2.7 V ≤ V <sub>DD</sub> < 3.5 V	0.8		32	μs
T15, T16 input frequency	f <sub>I1</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	0		4	MHz	
			0		275	kHz	
T15, T16 input high-/ low-level widths	t <sub>TIH</sub> ,	V <sub>DD</sub> = 4.5 to 5.5 V	100			ns	
	t <sub>TIL</sub>		1.8			μs	
Interrupt input high-/ low-level widths	t <sub>INTH</sub> ,	V <sub>DD</sub> = 2.7 to 5.5 V	10			μs	
	t <sub>INTL</sub>		20			μs	
RESET low-level width	t <sub>RSL</sub>	V <sub>DD</sub> = 2.7 to 5.5 V	10			μs	
			20			μs	

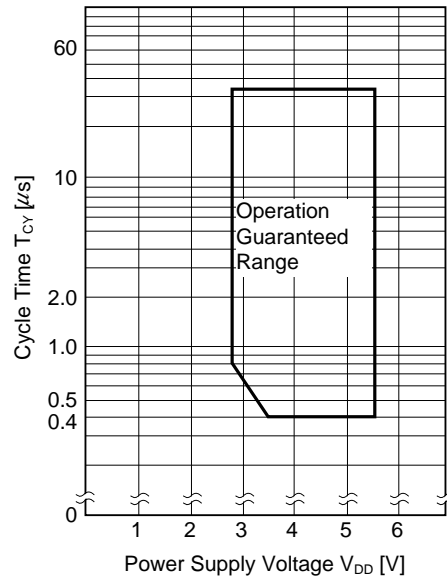
- Notes**
1. When oscillation mode selection register (OSMS) is set to 00H.
  2. When OSMS is set to 01H.

**Remark** f<sub>XX</sub>: Main system clock frequency (f<sub>X</sub> or f<sub>X</sub>/2)  
 f<sub>X</sub>: Main system clock oscillation frequency

**T<sub>CY</sub> vs V<sub>DD</sub>**  
 (Main System Clock f<sub>XX</sub> = f<sub>X</sub>/2 Operation)



**T<sub>CY</sub> vs V<sub>DD</sub>**  
 (Main System Clock f<sub>XX</sub> = f<sub>X</sub> Operation)



(2) Serial Interface (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 5.5 V)

(a) 3-wired serial I/O mode ( $\overline{\text{SCK2}}$  ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK2}}$ cycle time	t <sub>KCY1</sub>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	800			ns
		2.7 V ≤ V <sub>DD</sub> < 4.5 V	1600			ns
		2.0 V ≤ V <sub>DD</sub> < 2.7 V	3200			ns
			4800			ns
$\overline{\text{SCK2}}$ high-/low-level width	t <sub>KH1</sub> ,	V <sub>DD</sub> = 4.5 to 5.5 V	t <sub>KCY1</sub> /2-50			ns
	t <sub>KL1</sub>					t <sub>KCY1</sub> /2-100
SI2 setup time (to $\overline{\text{SCK2}}$ ↑)	t <sub>SIK1</sub>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	100			ns
		2.7 V ≤ V <sub>DD</sub> < 4.5 V	150			ns
		2.0 V ≤ V <sub>DD</sub> < 2.7 V	300			ns
			400			ns
SI2 hold time (from $\overline{\text{SCK2}}$ ↑)	t <sub>KSI1</sub>		400			ns
$\overline{\text{SCK2}}$ ↓ → SO2 output delay time	t <sub>KSO1</sub>	C = 100 pF <sup>Note</sup>			300	ns

**Note** C is the  $\overline{\text{SCK2}}$ , SO2 output line load capacitance.

(b) 3-wired serial I/O mode ( $\overline{\text{SCK2}}$  ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit			
$\overline{\text{SCK2}}$ cycle time	t <sub>KCY2</sub>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	800			ns			
		2.7 V ≤ V <sub>DD</sub> < 4.5 V	1600			ns			
		2.0 V ≤ V <sub>DD</sub> < 2.7 V	3200			ns			
			4800			ns			
$\overline{\text{SCK2}}$ high-/low-level width	t <sub>KH2</sub> ,	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	400			ns			
	t <sub>KL2</sub>					2.7 V ≤ V <sub>DD</sub> < 4.5 V	800		ns
						2.0 V ≤ V <sub>DD</sub> < 2.7 V	1600		ns
							2400		ns
SI2 setup time (to $\overline{\text{SCK2}}$ ↑)	t <sub>SIK2</sub>	V <sub>DD</sub> = 2.0 to 5.5 V	100			ns			
			150			ns			
SI2 hold time (from $\overline{\text{SCK2}}$ ↑)	t <sub>KSI2</sub>		400			ns			
$\overline{\text{SCK2}}$ ↓ → SO2 output delay time	t <sub>KSO2</sub>	C = 100 pF <sup>Note</sup>	V <sub>DD</sub> = 2.0 to 5.5 V		300	ns			
					500	ns			
$\overline{\text{SCK2}}$ rise, fall time	t <sub>R2</sub> ,				1000	ns			
	t <sub>F2</sub>								

**Note** C is the SO2 output line load capacitance.

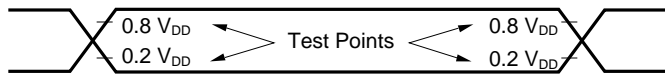
(c) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			78125	bps
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$			39063	bps
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$			19531	bps
					9766	bps

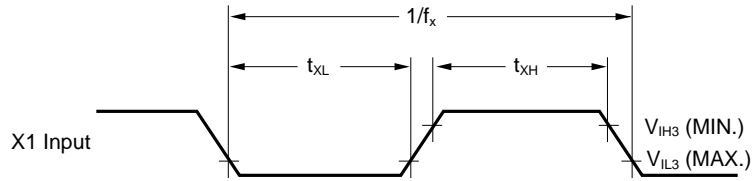
(d) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t <sub>KCY3</sub>	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	800			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	1600			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	3200			ns
			4800			ns
ASCK high-/low-level width	t <sub>KH3</sub> ,	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	400			ns
	t <sub>KL3</sub>	$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	800			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	1600			ns
			2400			ns
Transfer rate		$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			39063	bps
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$			19531	bps
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$			9766	bps
					6510	bps
ASCK rise, fall time	t <sub>R3</sub> ,				1000	ns
	t <sub>F3</sub>					

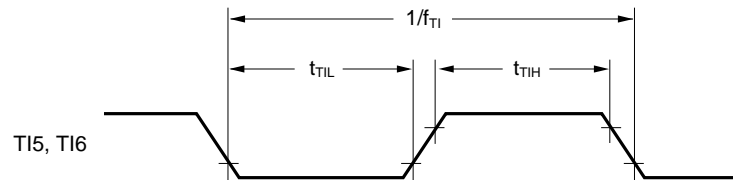
AC Timing Test Point (Excluding X1 Input)



Clock Timing

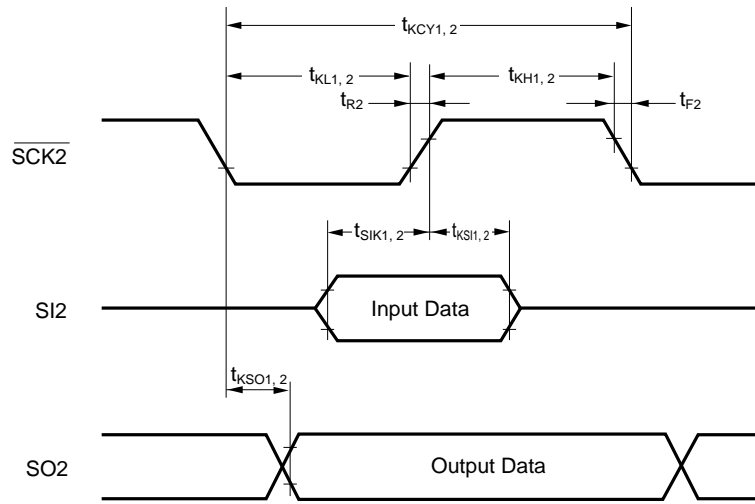


TI Timing

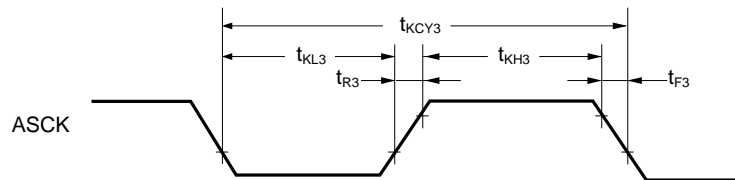


Serial Transfer Timing

3-wired serial I/O mode:



UART mode (external clock input):



**A/D Converter Characteristics** ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $AV_{DD} = V_{DD} = 2.7$  to  $5.5$  V,  $AV_{SS} = V_{SS} = 0$  V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error <sup>Note</sup>		$2.7\text{ V} \leq AV_{REF} \leq AV_{DD}$			1.4	%
Conversion time	$t_{CONV}$		19.1		200	μs
Sampling time	$t_{SAMP}$		$12/f_{XX}$			μs
Analog input voltage	$V_{IAN}$		$AV_{SS}$		$AV_{REF}$	V
Reference voltage	$AV_{REF}$		2.7		$AV_{DD}$	V
$AV_{REF}$ - $AV_{SS}$ resistance	$R_{AIREF}$		4	14		kΩ

**Note** Excluding quantization error ( $\pm 1/2$  LSB). Shown as a percentage of the full scale value.

**Remark**  $f_{XX}$ : Main system clock frequency ( $f_x$  or  $f_x/2$ )  
 $f_x$ : Main system clock oscillation frequency

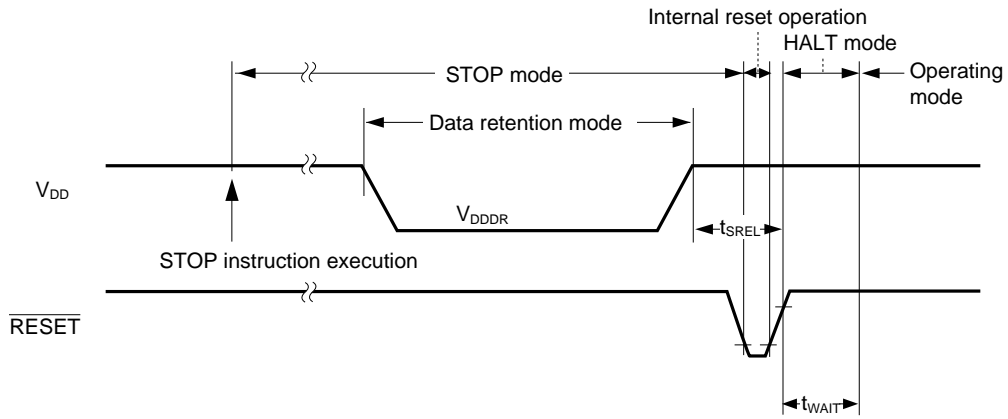
**Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics** (TA = -40 to +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V <sub>DDDR</sub>		1.8		5.5	V
Data retention supply current	I <sub>DDDR</sub>	V <sub>DDDR</sub> = 1.8 V		0.1	10	μA
Release signal set time	t <sub>SREL</sub>		0			μs
Oscillation stabilization wait time	t <sub>WAIT</sub>	Release by $\overline{\text{RESET}}$		2 <sup>17</sup> /f <sub>x</sub>		ms
		Release by interrupt		<b>Note</b>		ms

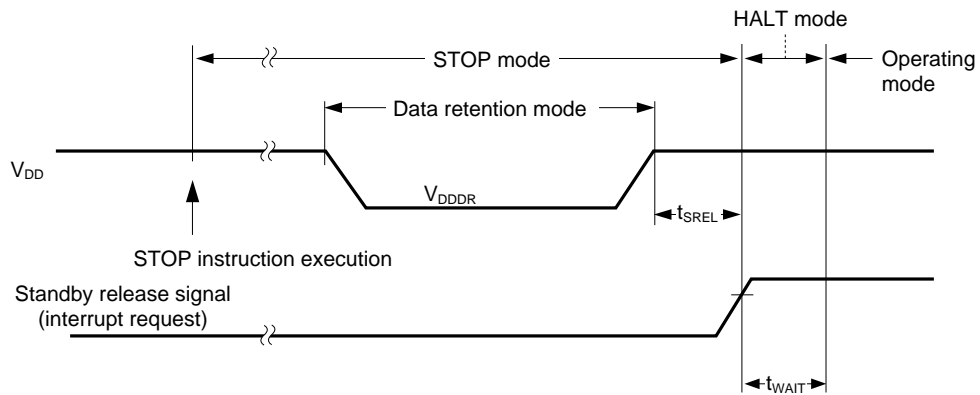
**Note** 2<sup>12</sup>/f<sub>xx</sub> or 2<sup>14</sup>/f<sub>xx</sub> to 2<sup>17</sup>/f<sub>xx</sub> can be selected by bit 0 to bit 2 (OSTS0 to OSTS2) of oscillation stabilization time selection register (OSTS).

**Remark** f<sub>xx</sub>: Main system clock frequency (f<sub>x</sub> or f<sub>x</sub>/2)  
 f<sub>x</sub>: Main system clock oscillation frequency

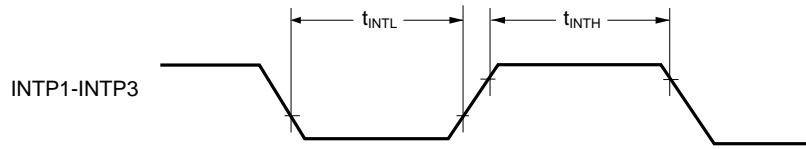
**Data Retention Timing (STOP mode released by  $\overline{\text{RESET}}$ )**



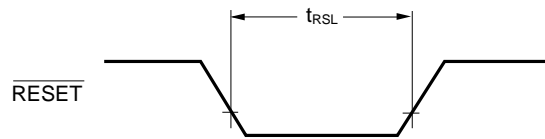
**Data Retention Timing (Standby release signal: STOP mode released by interrupt request signal)**



Interrupt Input Timing



$\overline{\text{RESET}}$  Input Timing





**PROM Programming Characteristics**

**DC Characteristics**

(1) **PROM Write Mode** ( $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{DD} = 6.5 \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5 \pm 0.3\text{ V}$ )

Parameter	Symbol	Symbol <sup>Note</sup>	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	$V_{IH}$	$V_{IH}$		$0.7V_{DD}$		$V_{DD}$	V
Input voltage, low	$V_{IL}$	$V_{IL}$		0		$0.3V_{DD}$	V
Output voltage, high	$V_{OH}$	$V_{OH}$	$I_{OH} = -1\text{ mA}$	$V_{DD} - 1.0$			V
Output voltage, low	$V_{OL}$	$V_{OL}$	$I_{OL} = 1.6\text{ mA}$			0.4	V
Input leakage current	$I_{LI}$	$I_{LI}$	$0 \leq V_{IN} \leq V_{DD}$	-10		+10	μA
$V_{PP}$ supply voltage	$V_{PP}$	$V_{PP}$		12.2	12.5	12.8	V
$V_{DD}$ supply voltage	$V_{DD}$	$V_{CC}$		6.25	6.5	6.75	V
$V_{PP}$ supply current	$I_{PP}$	$I_{PP}$	$\overline{PGM} = V_{IL}$			50	mA
$V_{DD}$ supply current	$I_{DD}$	$I_{CC}$				50	mA

(2) **PROM Read Mode** ( $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{DD} = 5.0 \pm 0.5\text{ V}$ ,  $V_{PP} = V_{DD} \pm 0.6\text{ V}$ )

Parameter	Symbol	Symbol <sup>Note</sup>	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	$V_{IH}$	$V_{IH}$		$0.7V_{DD}$		$V_{DD}$	V
Input voltage, low	$V_{IL}$	$V_{IL}$		0		$0.3V_{DD}$	V
Output voltage, high	$V_{OH1}$	$V_{OH1}$	$I_{OH} = -1\text{ mA}$	$V_{DD} - 1.0$			V
	$V_{OH2}$	$V_{OH2}$	$I_{OH} = -100\ \mu\text{A}$	$V_{DD} - 0.5$			V
Output voltage, low	$V_{OL}$	$V_{OL}$	$I_{OL} = 1.6\text{ mA}$			0.4	V
Input leakage current	$I_{LI}$	$I_{LI}$	$0 \leq V_{IN} \leq V_{DD}$	-10		+10	μA
Output leakage current	$I_{LO}$	$I_{LO}$	$0 \leq V_{OUT} \leq V_{DD}$ , $\overline{OE} = V_{IH}$	-10		+10	μA
$V_{PP}$ supply voltage	$V_{PP}$	$V_{PP}$		$V_{DD} - 0.6$	$V_{DD}$	$V_{DD} + 0.6$	V
$V_{DD}$ supply voltage	$V_{DD}$	$V_{CC}$		4.5	5.0	5.5	V
$V_{PP}$ supply current	$I_{PP}$	$I_{PP}$	$V_{PP} = V_{DD}$			100	μA
$V_{DD}$ supply current	$I_{DD}$	$I_{CCA1}$	$\overline{CE} = V_{IL}$ , $V_{IN} = V_{IH}$			50	mA

**Note** Corresponding μPD27C1001A symbol.

AC Characteristics

(1) PROM Write Mode

(a) Page program mode ( $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{DD} = 6.5 \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5 \pm 0.3\text{ V}$ )

Parameter	Symbol	Symbol <sup>Note</sup>	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{\text{OE}} \downarrow$ )	t <sub>AS</sub>	t <sub>AS</sub>		2			μs
$\overline{\text{OE}}$ setup time	t <sub>OES</sub>	t <sub>OES</sub>		2			μs
$\overline{\text{CE}}$ setup time (to $\overline{\text{OE}} \downarrow$ )	t <sub>CES</sub>	t <sub>CES</sub>		2			μs
Input data setup time (to $\overline{\text{OE}} \downarrow$ )	t <sub>DS</sub>	t <sub>DS</sub>		2			μs
Address hold time (from $\overline{\text{OE}} \uparrow$ )	t <sub>AH</sub>	t <sub>AH</sub>		2			μs
	t <sub>AHL</sub>	t <sub>AHL</sub>		2			μs
	t <sub>AHV</sub>	t <sub>AHV</sub>		0			μs
Input data hold time (from $\overline{\text{OE}} \uparrow$ )	t <sub>DH</sub>	t <sub>DH</sub>		2			μs
$\overline{\text{OE}} \uparrow \rightarrow$ Data output float delay time	t <sub>DF</sub>	t <sub>DF</sub>		0		250	ns
V <sub>PP</sub> setup time (to $\overline{\text{OE}} \downarrow$ )	t <sub>VPS</sub>	t <sub>VPS</sub>		1.0			ms
V <sub>DD</sub> setup time (to $\overline{\text{OE}} \downarrow$ )	t <sub>VDS</sub>	t <sub>VCS</sub>		1.0			ms
Program pulse width	t <sub>PW</sub>	t <sub>PW</sub>		0.095	0.1	0.105	ms
$\overline{\text{OE}} \downarrow \rightarrow$ Valid data delay time	t <sub>OE</sub>	t <sub>OE</sub>				1	μs
$\overline{\text{OE}}$ pulse width during data latching	t <sub>LW</sub>	t <sub>LW</sub>		1			μs
PGM setup time	t <sub>PGMS</sub>	t <sub>PGMS</sub>		2			μs
$\overline{\text{CE}}$ hold time	t <sub>CEH</sub>	t <sub>CEH</sub>		2			μs
$\overline{\text{OE}}$ hold time	t <sub>OEH</sub>	t <sub>OEH</sub>		2			μs

(b) Byte program mode ( $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{DD} = 6.5 \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5 \pm 0.3\text{ V}$ )

Parameter	Symbol	Symbol <sup>Note</sup>	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{\text{PGM}} \downarrow$ )	t <sub>AS</sub>	t <sub>AS</sub>		2			μs
$\overline{\text{OE}}$ setup time	t <sub>OES</sub>	t <sub>OES</sub>		2			μs
$\overline{\text{CE}}$ setup time (to $\overline{\text{PGM}} \downarrow$ )	t <sub>CES</sub>	t <sub>CES</sub>		2			μs
Input data setup time (to $\overline{\text{PGM}} \downarrow$ )	t <sub>DS</sub>	t <sub>DS</sub>		2			μs
Address hold time (from $\overline{\text{OE}} \uparrow$ )	t <sub>AH</sub>	t <sub>AH</sub>		2			μs
Input data hold time (from $\overline{\text{PGM}} \uparrow$ )	t <sub>DH</sub>	t <sub>DH</sub>		2			μs
$\overline{\text{OE}} \uparrow \rightarrow$ Data output float delay time	t <sub>DF</sub>	t <sub>DF</sub>		0		250	ns
V <sub>PP</sub> setup time (to $\overline{\text{PGM}} \downarrow$ )	t <sub>VPS</sub>	t <sub>VPS</sub>		1.0			ms
V <sub>DD</sub> setup time (to $\overline{\text{PGM}} \downarrow$ )	t <sub>VDS</sub>	t <sub>VCS</sub>		1.0			ms
Program pulse width	t <sub>PW</sub>	t <sub>PW</sub>		0.095	0.1	0.105	ms
$\overline{\text{OE}} \downarrow \rightarrow$ Valid data delay time	t <sub>OE</sub>	t <sub>OE</sub>				1	μs
$\overline{\text{OE}}$ hold time	t <sub>OEH</sub>	—		2			μs

**Note** Corresponding μPD27C1001A symbol.

**(2) PROM Read Mode** ( $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{DD} = 5.0 \pm 0.5\text{ V}$ ,  $V_{PP} = V_{DD} \pm 0.6\text{ V}$ )

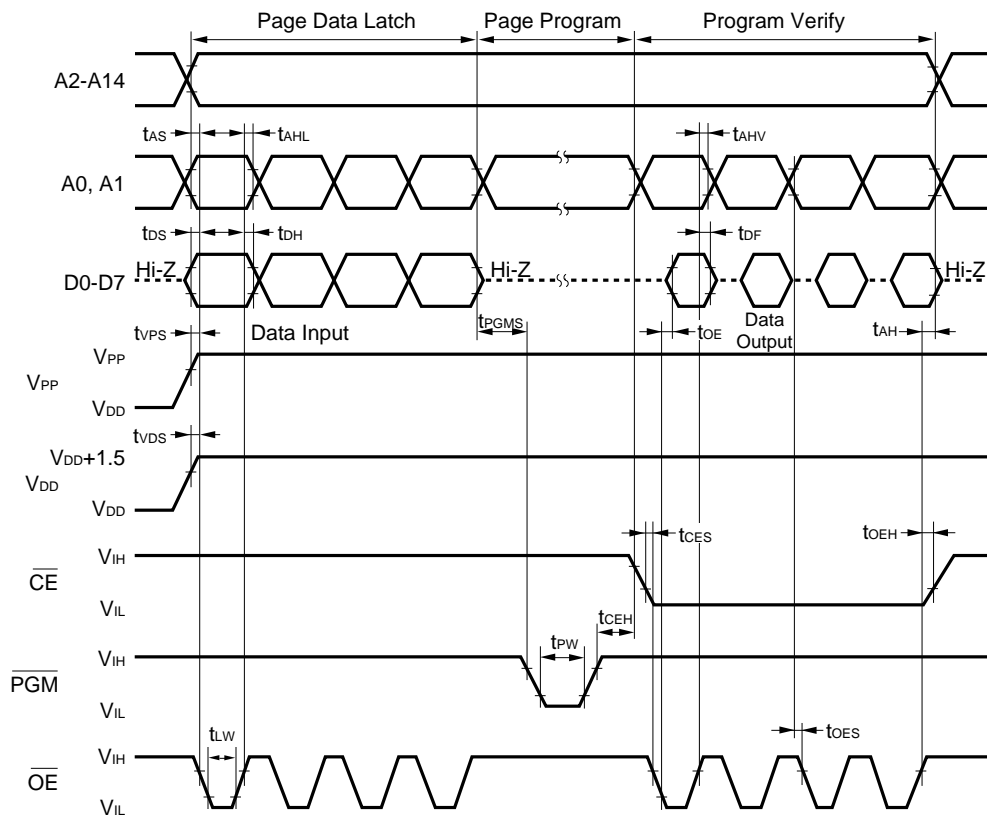
Parameter	Symbol	Symbol <sup>Note</sup>	Test Conditions	MIN.	TYP.	MAX.	Unit
Address $\uparrow$ → Data output float delay time	t <sub>ACC</sub>	t <sub>ACC</sub>	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$			800	ns
$\overline{\text{CE}} \downarrow$ → Valid output delay time	t <sub>CE</sub>	t <sub>CE</sub>	$\overline{\text{OE}} = V_{IL}$			800	ns
$\overline{\text{OE}} \downarrow$ → Valid output delay time	t <sub>OE</sub>	t <sub>OE</sub>	$\overline{\text{CE}} = V_{IL}$			200	ns
$\overline{\text{OE}} \downarrow$ → Data output float delay time	t <sub>DF</sub>	t <sub>DF</sub>	$\overline{\text{CE}} = V_{IL}$	0		60	ns
Address → Data hold time	t <sub>OH</sub>	t <sub>OH</sub>	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	0			ns

**Note** Corresponding μPD27C1001A symbol.

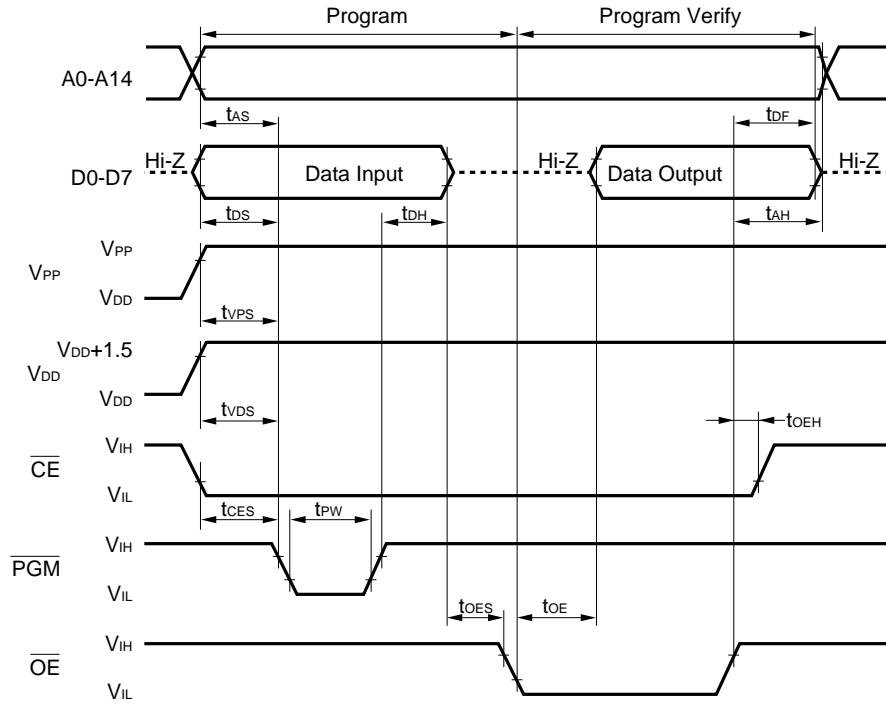
**(3) PROM Programming Mode** ( $T_A = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PROM programming mode setup time	t <sub>SMA</sub>		10			μs

PROM Write Mode Timing (page program mode)

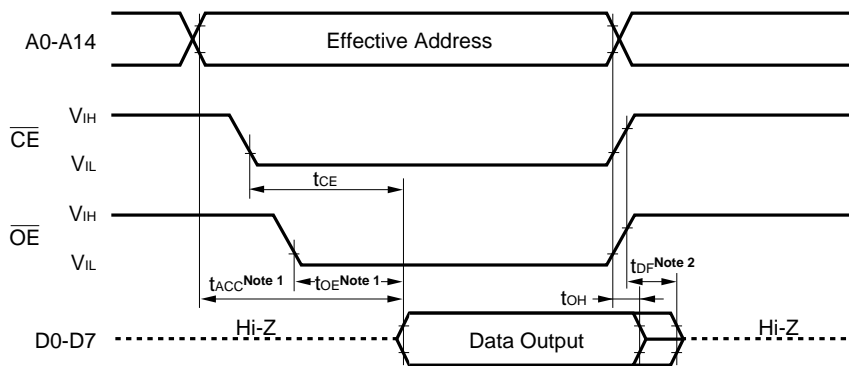


**PROM Write Mode Timing (byte program mode)**



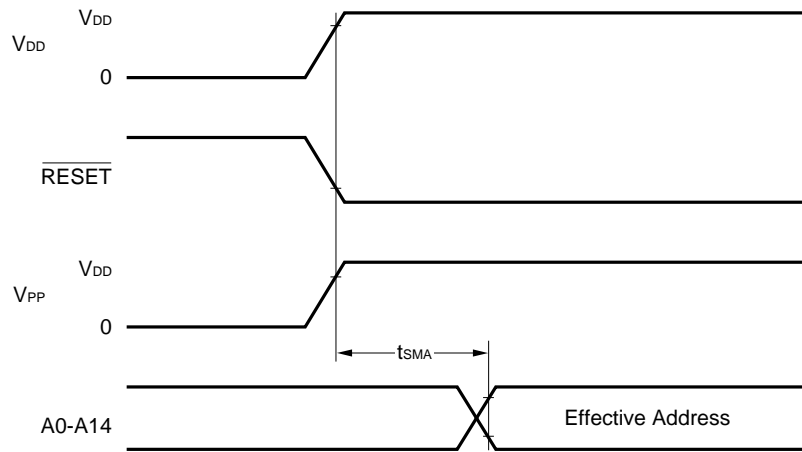
- Cautions**
1.  $V_{DD}$  should be applied before  $V_{PP}$ , and removed after  $V_{PP}$ .
  2.  $V_{PP}$  must not exceed +13.5 V including overshoot.
  3. Reliability may be adversely affected if removal/reinsertion is performed while + 12.5 V is being applied to  $V_{PP}$ .

**PROM Read Mode Timing**



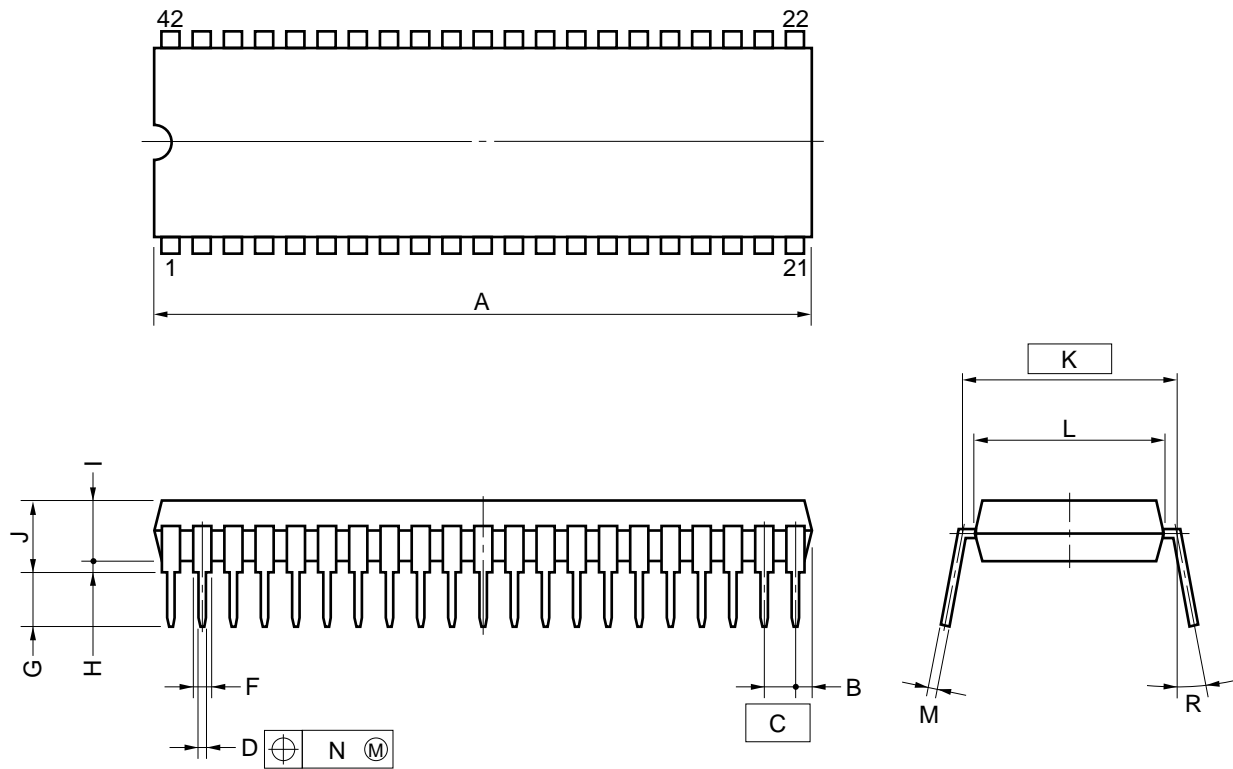
- Notes**
1. If you want to read within the range of  $t_{ACC}$ , make the  $\overline{OE}$  input delay time from the fall of  $\overline{CE}$  a maximum of  $t_{ACC} - t_{OE}$ .
  2.  $t_{DF}$  is the time from when either  $\overline{OE}$  or  $\overline{CE}$  first reaches  $V_{IH}$ .

PROM Programming Mode Setting Timing



7. PACKAGE DRAWINGS

42PIN PLASTIC SHRINK DIP (600 mil)



NOTES

- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

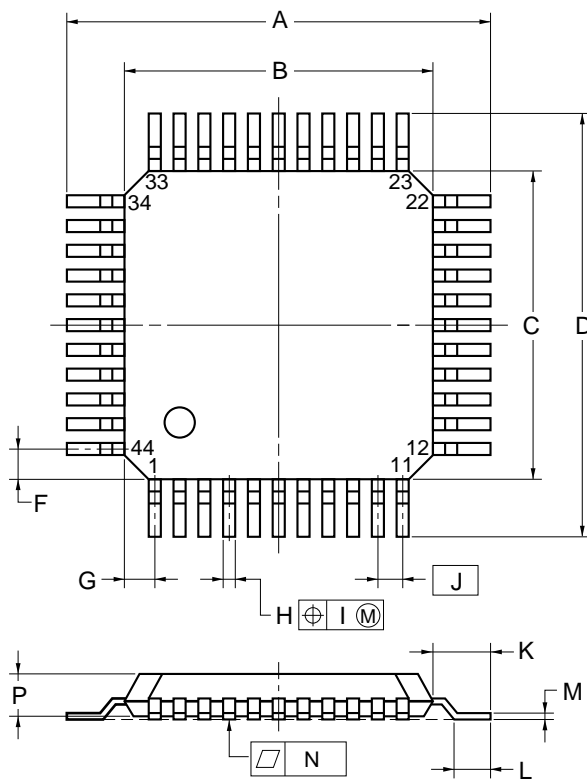
ITEM	MILLIMETERS	INCHES
A	39.13 MAX.	1.541 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 <sup>+0.004</sup> <sub>-0.005</sub>
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	0.25 <sup>+0.10</sup> <sub>-0.05</sub>	0.010 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.17	0.007
R	0~15°	0~15°

P42C-70-600A-1

**Remark** The shape and material of ES versions are the same as those of mass-produced versions.

μPD78P083GB(A)-3B4

44 PIN PLASTIC QFP (□10)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.6±0.4	0.535 <sup>+0.017</sup> <sub>-0.016</sub>
B	10.0±0.2	0.394 <sup>+0.008</sup> <sub>-0.009</sub>
C	10.0±0.2	0.394 <sup>+0.008</sup> <sub>-0.009</sub>
D	13.6±0.4	0.535 <sup>+0.017</sup> <sub>-0.016</sub>
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	0.014 <sup>+0.004</sup> <sub>-0.005</sub>
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071 <sup>+0.008</sup> <sub>-0.009</sub>
L	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

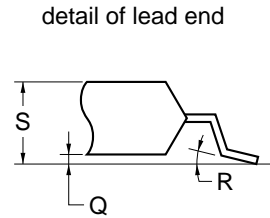
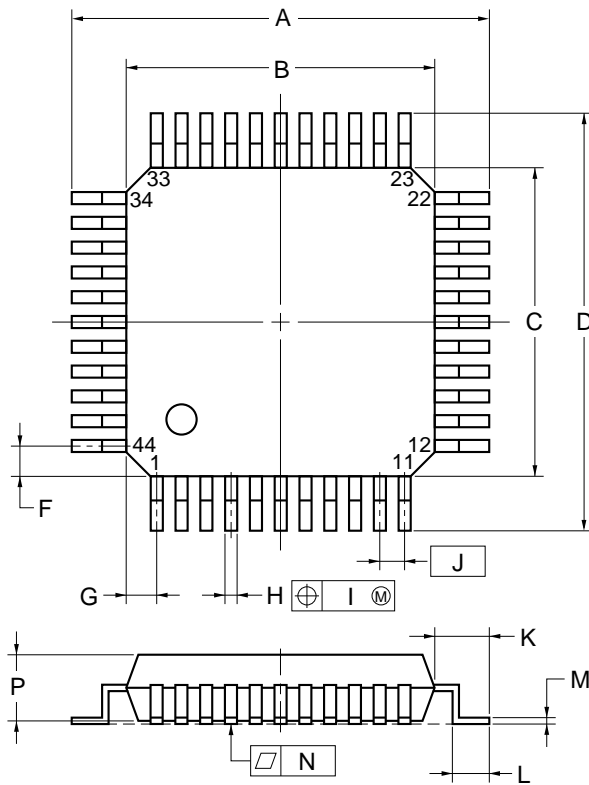
P44GB-80-3B4-3

**Remark** The shape and material of ES versions are the same as those of mass-produced versions.



μPD78P083GB(A)-3BS-MTX (Under planning)

44 PIN PLASTIC QFP (□10)



NOTE

Each lead centerline is located within 0.16 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.2±0.2	0.520 <sup>+0.008</sup> / <sub>-0.009</sub>
B	10.0±0.2	0.394 <sup>+0.008</sup> / <sub>-0.009</sub>
C	10.0±0.2	0.394 <sup>+0.008</sup> / <sub>-0.009</sub>
D	13.2±0.2	0.520 <sup>+0.008</sup> / <sub>-0.009</sub>
F	1.0	0.039
G	1.0	0.039
H	0.37 <sup>+0.08</sup> / <sub>-0.07</sub>	0.015 <sup>+0.003</sup> / <sub>-0.004</sub>
I	0.16	0.007
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	0.031 <sup>+0.009</sup> / <sub>-0.008</sub>
M	0.17 <sup>+0.06</sup> / <sub>-0.05</sub>	0.007 <sup>+0.002</sup> / <sub>-0.003</sub>
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	3° <sup>+7°</sup> / <sub>-3°</sub>	3° <sup>+7°</sup> / <sub>-3°</sub>
S	3.0 MAX.	0.119 MAX.

S44GB-80-3BS

Remark The shape and material of ES versions are the same as those of mass-produced versions.

**8. RECOMMENDED SOLDERING CONDITIONS**

It is recommended that the μPD78P083(A) be soldered under the following conditions. For details on the recommended soldering conditions, refer to information document "Semiconductor Device Mounting Technology Manual" (C10535E).

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

**Table 8-1. Soldering Conditions for Surface Mount Types**

**μPD78P083GB(A)-3B4 : 44-pin plastic QFP (10 × 10 mm)**

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or less (at 210°C or higher), Number of reflow processes: 3 or less	IR35-00-3
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or less (at 200°C or higher), Number of reflow processes: 3 or less	VP15-00-3
Wave soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or less, Number of flow processes: 1, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C or below, Flow time: 3 seconds or less (per pin row)	—

- Cautions**
1. Do not use different soldering methods together (except for partial heating method).
  2. Soldering conditions for the μPD78P083GB(A)-3BS-MTX is not fixed because this product is under planning.

**Table 8-2. Soldering Condition for Hole-Through Types**

**μPD78P083CU(A) : 42-pin plastic shrink DIP (600 mil)**

Soldering Method	Soldering Conditions
Wave Soldering (only pins)	Solder temperature: 260°C or below, Flow time: 10 seconds or less
Partial heating	Pin temperature: 300°C or below, Flow time: 3 seconds or less (per pin)

**Caution** Apply wave soldering only to the pins and be careful so as not to bring solder into direct contact with the package.

**APPENDIX A. DEVELOPMENT TOOLS**

The following development tools are available to support development of systems using the μPD78P083(A).

**Language Processing Software**

RA78K/0 <small>Notes 1, 2, 3, 4</small>	Assembler package common to the 78K/0 Series
CC78K/0 <small>Notes 1, 2, 3, 4</small>	C compiler package common to the 78K/0 Series
DF78083 <small>Notes 1, 2, 3, 4</small>	Device file used for the μPD78083 Subseries
CC78K/0-L <small>Notes 1, 2, 3, 4</small>	C compiler library source file common to the 78K/0 Series

**PROM Writing Tools**

PG-1500	PROM programmer
PA-78P083CU PA-78P083GB	Programmer adapter connected to the PG-1500
PG-1500 Controller <small>Notes 1, 2</small>	Control program for the PG-1500

**Debugging Tools**

IE-78000-R	In-circuit emulator common to the 78K/0 Series
IE-78000-R-A	In-circuit emulator common to the 78K/0 Series (for integrated debugger)
IE-78000-R-BK	Break board common to the 78K/0 Series
IE-78078-R-EM	Emulation board common to the μPD78078 Subseries
EP-78083CU-R EP-78083GB-R	Emulation probe for the μPD78083 Subseries
EV-9200G-44	Socket mounted on the target system board prepared for 44-pin plastic QFP (GB-3B4, GB-3BS-MTX type)
SM78K0 <small>Notes 5, 6, 7</small>	System simulator common to the 78K/0 Series
ID78K0 <small>Notes 4, 5, 6, 7</small>	Integrated debugger for IE-78000-R-A
SD78K/0 <small>Notes 1, 2</small>	Screen debugger for the IE-78000-R
DF78083 <small>Notes 1, 2, 4, 5, 6, 7</small>	Device file used for the μPD78083 Subseries

- Notes**
1. Based on PC-9800 series (MS-DOS™)
  2. Based on IBM PC/AT™ and its compatibles (PC DOS™/IBM DOS™/MS-DOS)
  3. Based on HP9000 series 300™ (HP-UX™)
  4. Based on HP9000 series 700™ (HP-UX), SPARCstation™ (SunOS™), and EWS4800 series (EWS-UX/V)
  5. Based on PC-9800 series (MS-DOS + Windows™)
  6. IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS + Windows)
  7. Based on NEWS™ (NEWS-OS™)

- Remarks**
1. Please refer to the **78K/0 Series Selection Guide (U11126E)** for information on the third party development tools.
  2. Use the RA78K/0, CC78K/0, SM78K0, ID78K0, and SD78K/0 in combination with the DF78083.

**OS**

MX78K/0 <small>Notes 1, 3, 4</small>	78K/0 Series common embedded OS
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**Fuzzy Inference Development Support System**

FE9000 <small>Note 1</small> /FE9200 <small>Note 2</small>	Fuzzy knowledge data creation tool
FT9080 <small>Note 1</small> /FT9085 <small>Note 3</small>	Translator
FI78K0 <small>Notes 1, 3</small>	Fuzzy inference module
FD78K0 <small>Notes 1, 3</small>	Fuzzy inference debugger

- Notes**
1. Based on PC-9800 series (MS-DOS)
  2. Based on IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS+Windows)
  3. Based on IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS)
  4. Based on HP9000 series 300 and series 700 (HP-UX), SPARCstation (SunOS), and EWS4800 series (EWS-UX/V)

**Remark** Please refer to the **78K/0 Series Selection Guide (U11126E)** for information on the third party development tools.

**APPENDIX B. RELATED DOCUMENTS**

**Documents Related to Devices**

Document Name		Document No.	
		Japanese	English
μPD78083 Subseries User's Manual		U12176J	U12176E
78K/0 Series User's Manual—Instructions		IEU-849	IEU-1372
78K/0 Series Instruction Table		U10903J	—
78K/0 Series Instruction Set		U10904J	—
μPD78083 Subseries Special Function Register Table		IEM-5599	—
78K/0 Series Application Note	Basic (III)	IEA-767	U10182E

**Caution** The contents of the documents listed above are subject to change without prior notice. Make sure to use the latest edition when starting design.

**Documents Related to Development Tools (User's Manual)**

Document Name		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K0 Assembler Package	Operation	U11802J	U11802E
	Assembly language	U11801J	U11801E
	Structured assembly language	U11789J	U11789E
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K/0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
CC78K/0 C Compiler Application Note	Programming know-how	EEA-618	EEA-1208
CC78K Series Library Source File		EEU-777	—
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) Based		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS) Based		EEU-5008	U10540E
IE-78000-R		EEU-810	U11376E
IE-78000-R-BK		EEU-867	EEU-1427
IE-78000-R-A		U10057J	U10057E
IE-78078-R-EM		U10775J	EEU-1504
EP-78083		EEU-5003	EEU-1529
SM78K0 System Simulator Windows Based	Reference	U10181J	U10181E
SM78K Series System Simulator	External parts user open interface specification	U10092J	U10092E
ID78K0 Integrated Debugger EWS Based	Reference	U11151J	—
ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E
ID78K0 Integrated Debugger	Guides	U11649J	U11649E
SD78K/0 Screen Debugger PC-9800 Series (MS-DOS) Based	Introduction	EEU-852	U10539E
	Reference	U10952J	—
SD78K/0 Screen Debugger IBM PC/AT (PC DOS) Based	Introduction	EEU-5024	EEU-1414
	Reference	U11279J	U11279E

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**Documents Related to Embedded Software (User's Manual)**

Document Name		Document No.	
		Japanese	English
78K/0 Series OS	MX78K0 Basic	EEU-5010	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, and 87AD Series Fuzzy Inference Development Support System Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

**Other Documents**

Document Name	Document No.	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	—
Guide to Quality Assurance for Semiconductor Devices	C11893J	MEI-1202
Microcontroller-Related Product Guide – Third Party Products –	U11416J	—

**Caution** The contents of the documents listed above are subject to change without prior notice. Be sure to use the latest edition when starting design.

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.



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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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