

### GRAPHICS LSI

The  $\mu$ PD72255Y is the successor to the  $\mu$ PD72254Y display controller, designed for use in navigation systems.

In addition to the display control functions and a drawing function of  $\mu$ PD72254Y, high quality alpha blending function can be applied for all window layers, and alpha blend drawing is also helpful to draw anti-aliasing line. The  $\mu$ PD72255Y provides a function for loading and displaying external video signals, and an internal D/A converter. This graphics LSI has been designed to be used to create a high quality display system for a multimedia navigation system.

The  $\mu$ PD72255Y can be connected to a host CPU having an asynchronous bus mode like a SRAM. As its display data memory (FRB), the device uses SDRAM with a 32-bit data bus.

**Remarks 1.** In this document, data lengths are defined as follows:

Byte:	8 bits
Half-word (2 bytes):	16 bits
Word (4 bytes):	32 bits
Double-word (8 bytes):	64 bits

**2.** In this document, data significance is defined as follows:

Bit 0: LSB

### ORDERING INFORMATION

Parts Number	Package
$\mu$ PD72255YF1-GA5	240-pin Plastic FBGA (16 × 16)

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Not all products and/or types are available in every country. Please check with NEC Electronics sales representative for availability and additional information.

**ELECTRICAL CHARACTERISTICS**

**Absolute Maximum Ratings (T<sub>A</sub> = 25 °C)**

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	2.5 V DV <sub>DD</sub>		-0.5 to +3.6	V
	2.5 V AV <sub>DD</sub>		-0.5 to +3.6	V
	3.3 V DV <sub>DD</sub>		-0.5 to +4.6	V
Input voltage	V <sub>I</sub>		-0.5 to +4.6	V
Output current	I <sub>o</sub>		-0.5 to DV <sub>DD</sub> + 0.3 -0.5 to AV <sub>DD</sub> + 0.3	V
Operating ambient temperature	T <sub>A</sub>		-40 to +85	°C
Storage temperature	T <sub>stg</sub>		-65 to +150	°C

**Caution** Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics. The rated values and conditions under the DC and AC characteristics correspond to the range in which the normal operation and reliability of the product can be guaranteed.

**Capacitance (T<sub>A</sub> = 25 °C)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>i</sub>	f = 1 MHz	4		10	pF
Output capacitance	C <sub>o</sub>		4		10	pF

**Remark** These values are sample values and not those actually measured.  
Input capacitance = Interface block capacitance + Package capacitance

**DC Characteristics (T<sub>A</sub> = -40 to +85 °C, 3.3 V DV<sub>DD</sub> = 3.0 to 3.6 V, 2.5 V DV<sub>DD</sub> = AV<sub>DD</sub> = 2.4 to 2.6 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V <sub>IH</sub>		2.0			V
		PCI/CPU	0.5 DV <sub>DD</sub>			V
Low-level input voltage	V <sub>IL</sub>				0.8	V
		PCI/CPU			0.3 DV <sub>DD</sub>	V
High-level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -400 μA	2.4			V
Low-level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA			0.4	V
High-level input leakage current	I <sub>LIH</sub>	V <sub>I</sub> = DV <sub>DD</sub>			10	μA
Low-level input leakage current	I <sub>LIL</sub>	V <sub>I</sub> = 0 V			-10	μA
High-level output leakage current	I <sub>LOH</sub>				10	μA
Low-level output leakage current	I <sub>LOL</sub>				-10	μA
Supply current to digital circuits	2.5V DI <sub>DD</sub>				360	mA
Supply current to digital circuits	3.5V DI <sub>DD</sub>				80	mA

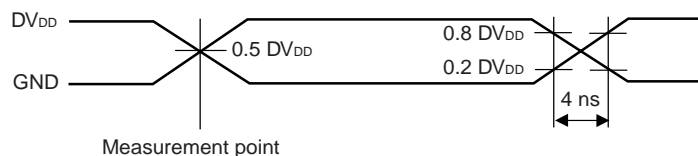
**DAC Characteristics (T<sub>A</sub> = -40 to +85 °C, 3.5 V DV<sub>DD</sub> = 3.15 to 3.45 V, 2.5 V DV<sub>DD</sub> = AV<sub>DD</sub> = 2.4 to 2.6 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current to analog circuits	AI <sub>DD</sub>	f <sub>clk</sub> = 15 MHz			50	mA
Resolution	RES		6	6	6	Bit
Differential linearity error	DLE				±1.0	LSB
Integral linearity error	ILE				±2.0	LSB
Full-scale output voltage	V <sub>FS</sub>		1.50	2.05	2.60	V
Zero-scale output voltage	V <sub>ZS</sub>		0.60	0.95	1.30	V
Output amplitude	V <sub>OPP</sub>		0.80	1.10	1.40	V
LSB output voltage	LSB			4.21		μV
Sampling clock frequency	f <sub>CLK</sub>		2.5		38	MHz

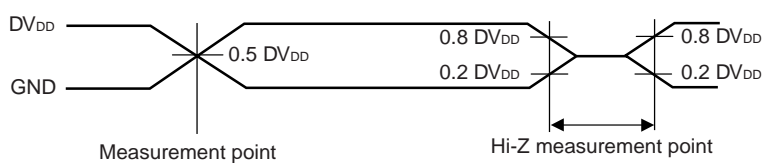
**AC Characteristics ( $T_A = -40$  to  $+85$  °C, 3.3 V  $DV_{DD} = 3.0$  to 3.6 V, 2.5 V  $DV_{DD} = 2.4$  to 2.6 V)**

Unless otherwise specified, the following voltage level is the measurement point.

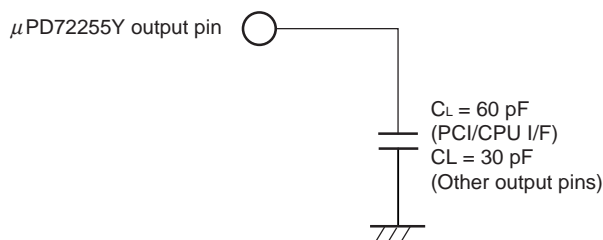
**Input waveform and measurement point for AC test**



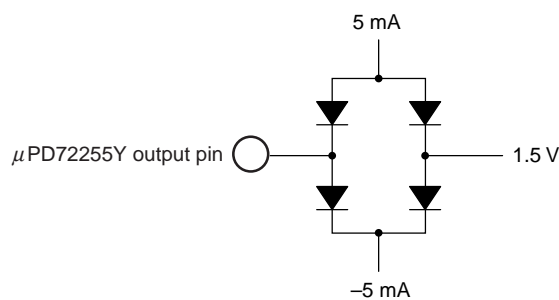
**Output measurement point for AC test**



**Test load**



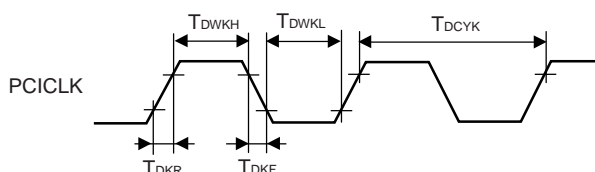
**Output floating measurement method**



(1) Input clock

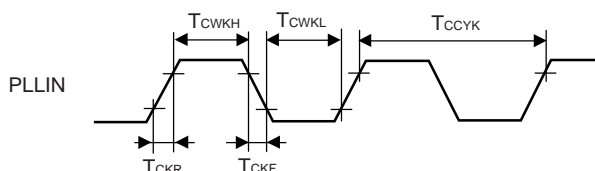
(a) PCICLK (If PCI bus function is not used, PCICLK pin must be connect to GND (Low level).)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock cycle	$T_{DCYK}$		28	30	72	ns
High-level clock width	$T_{DWKH}$		10			ns
Low-level clock width	$T_{DWKL}$		10			ns
Clock rise time	$T_{DKR}$				5	ns
Clock fall time	$T_{DKF}$				5	ns



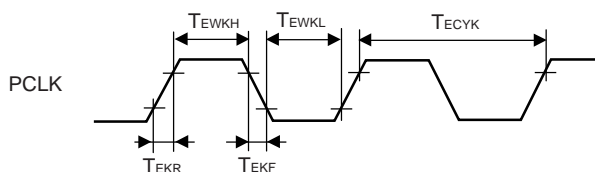
(b) PLLIN (If PLLIN clock is not used, PLLIN pin must be connect to pull-up/pull down resistors.)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock cycle	$T_{CCYK}$		28		200	ns
High-level clock width	$T_{CWKH}$		10			ns
Low-level clock width	$T_{CWKL}$		10			ns
Clock rise time	$T_{CKR}$				5	ns
Clock fall time	$T_{CKF}$				5	ns



(c) PCLK

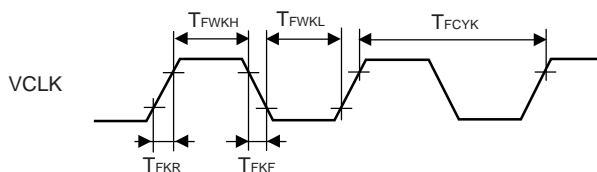
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock cycle	$T_{ECYK}$		30	69.84	119	ns
High-level clock width	$T_{EWKH}$		10			ns
Low-level clock width	$T_{EWKL}$		10			ns
Clock rise time	$T_{EKR}$				5	ns
Clock fall time	$T_{EKF}$				5	ns



Peak-to-peak jitter for PCLK: +/- 500 ps (value of SysClockSet register: 0x102 2000)

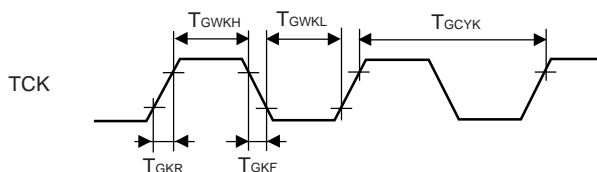
(d) VCLK (If Video Capturing function is not used, VCLK pin must be connect to GND (Low level).)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock cycle	$T_{FCYK}$		25		160	ns
High-level clock width	$T_{FWKH}$		10			ns
Low-level clock width	$T_{FWKL}$		10			ns
Clock rise time	$T_{FKR}$				5	ns
Clock fall time	$T_{FKF}$				5	ns



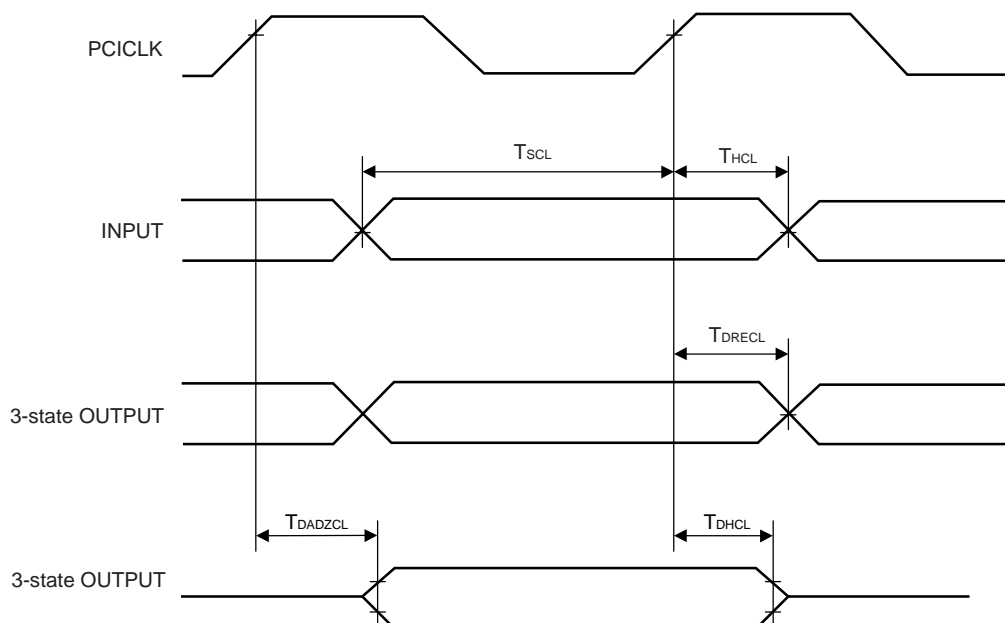
(e) TCK (If JTAG function is not used, TCK pin must be connect to GND (Low level).)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock cycle	$T_{GCYK}$		50			ns
High-level clock width	$T_{GWKH}$		10			ns
Low-level clock width	$T_{GWKL}$		10			ns
Clock rise time	$T_{GKR}$				6	ns
Clock fall time	$T_{GKF}$				6	ns



(2) CPU access timing (PCI bus mode, CPUSEL = L)

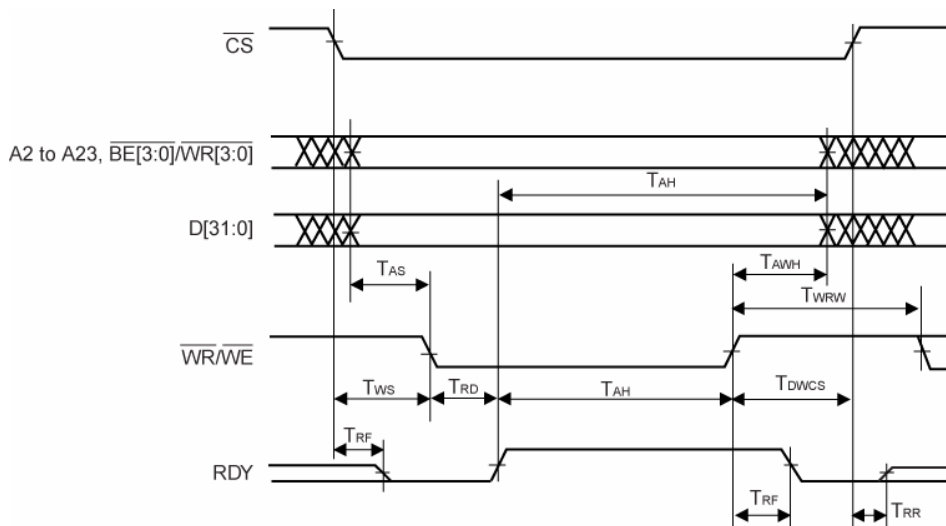
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input setup time (vs. PCICLK)	$T_{SCL}$		9			ns
Input hold time (vs. PCICLK)	$T_{HCL}$		0			ns
Output delay time	$T_{DRECL}$		4		18	ns
Output data set time (vs. PCICLK)	$T_{DADZCL}$		4		18	ns
3-state data buffer turn-off time (vs. PCICLK)	$T_{DHCL}$		4		28	ns



(3) CPU access timing (asynchronous bus mode, CPUSEL = H)

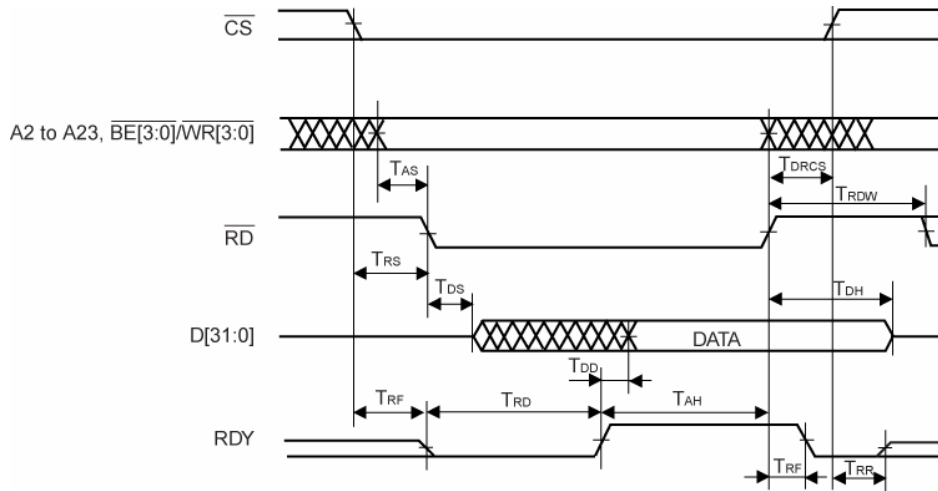
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
D[31:0], A[23:2], $\overline{\text{BE}}[3:0]/\overline{\text{WR}}[3:0]$ setup time (vs. $\overline{\text{WR}}/\overline{\text{WE}}$ , $\overline{\text{RD}}$ )	$T_{AS}$		5			ns
$\overline{\text{WR}}/\overline{\text{WE}}$ , $\overline{\text{RD}}$ , D[31:0], A[23:2], $\overline{\text{BE}}[3:0]/\overline{\text{WR}}[3:0]$ hold time (vs. RDY)	$T_{AH}$		5			ns
D[31:0], A[23:2], $\overline{\text{BE}}[3:0]/\overline{\text{WR}}[3:0]$ setup time (vs. $\overline{\text{WR}}/\overline{\text{WE}}$ )	$T_{AWH}$		5			ns
RDY fall delay time (vs. $\overline{\text{CS}}$ , $\overline{\text{WR}}/\overline{\text{WE}}$ , $\overline{\text{RD}}$ )	$T_{RF}$		3		10	ns
RDY buffer turn-off time (vs. $\overline{\text{WR}}/\overline{\text{WE}}$ )	$T_{RR}$		3		21.5	ns
RDY delay time (vs. $\overline{\text{WR}}/\overline{\text{WE}}$ , $\overline{\text{RD}}$ )	$T_{RD}$		5			ns
D[31:0] data set time (vs. $\overline{\text{RD}}$ )	$T_{DS}$		5		21.5	ns
D[31:0] buffer turn-off time (vs. $\overline{\text{RD}}$ )	$T_{DH}$		5		21.5	ns
$\overline{\text{WR}}/\overline{\text{WE}}$ High level width	$T_{WRW}$		5			ns
$\overline{\text{RD}}$ High level width	$T_{RDW}$		25			ns
$\overline{\text{CS}}-\overline{\text{WR}}/\overline{\text{WE}}$ delay time	$T_{WS}$		0			ns
$\overline{\text{WR}}/\overline{\text{WE}}-\overline{\text{CS}}$ delay time	$T_{DWCS}$		0			ns
$\overline{\text{CS}}-\overline{\text{RD}}$ delay time	$T_{RS}$		0			ns
$\overline{\text{RD}}-\overline{\text{CS}}$ delay time	$T_{DRCS}$		0			ns
Read data determination – RDY delay time	$T_{DD}$				5	ns

During write ( $\overline{\text{RD}} = \text{H}$ )



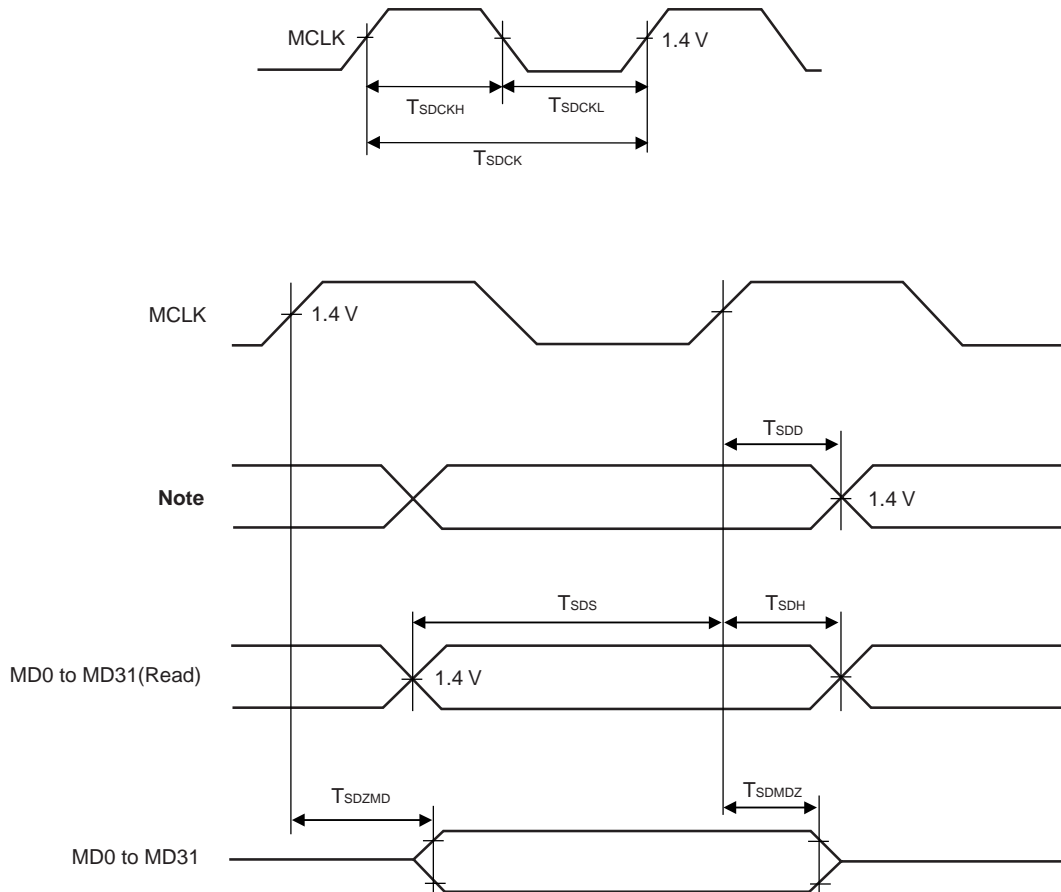


During read ( $\overline{WR} = H$ )



(4) SDRAM access timing

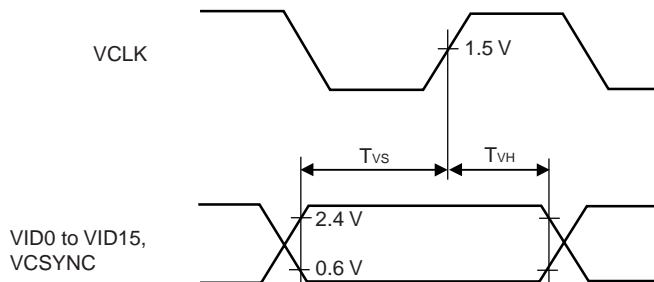
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
MCLK clock cycle time	$T_{SDCK}$		10	12.5	14	ns
MCLK high-level width	$T_{SDCH}$		3			ns
MCLK low-level width	$T_{SDCL}$		3			ns
MD0 to MD31, MA0 to MA14, MCS, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , DQM0 to DQM3, CKE output delay time	$T_{SDD}$		1.5		7.5	ns
MD0 to MD31 data set time	$T_{SDZMD}$		2.5		17	ns
MD0 to MD31 data buffer turn-off time	$T_{SDMDZ}$		2.5		17	ns
MD0 to MD31 data setup time (during read)	$T_{SDS}$		3			ns
MD0 to MD31 data hold time (during read)	$T_{SDH}$		2			ns



**Note** MD0 to MD31 (write), MA0 to MA14, MCS,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ , DQM0 to DQM3, CKE

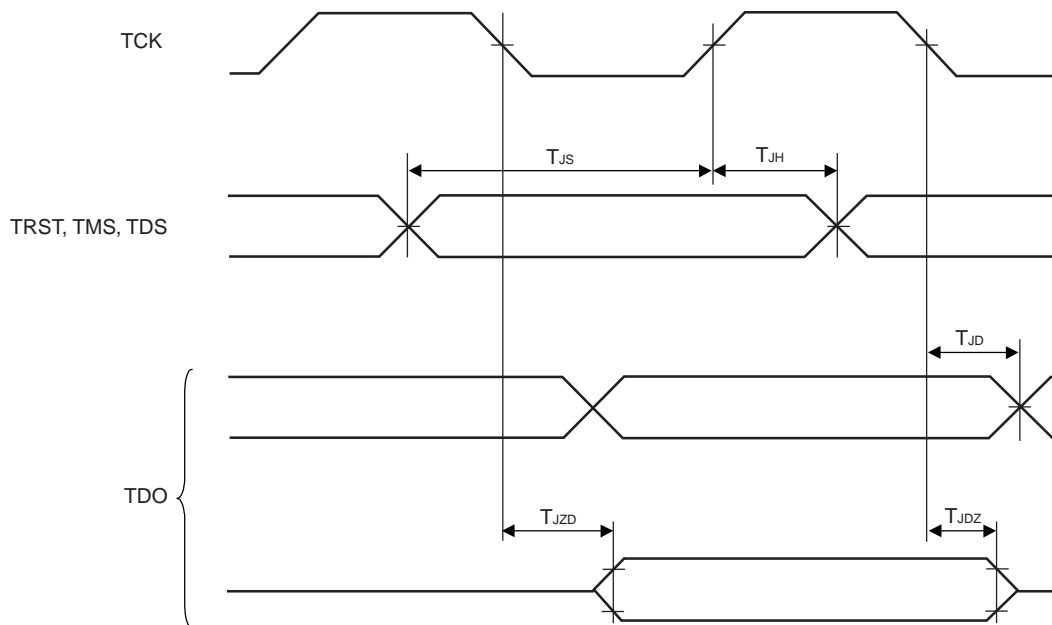
(5) Video interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
VID0 to VID15, VCSYNC setup time	$T_{Vs}$		4			ns
VID0 to VID15, VCSYNC hold time	$T_{VH}$		7			ns



(6) JTAG interface

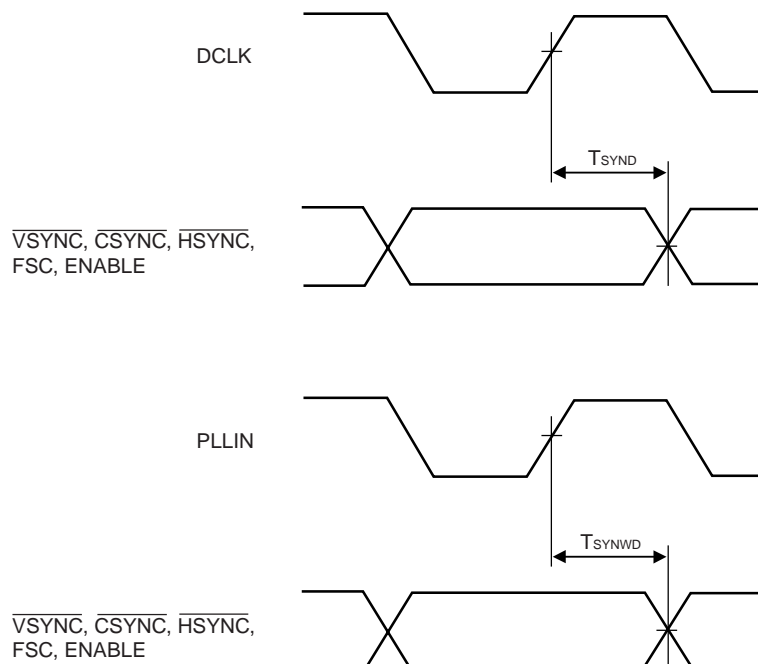
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TRST, TMS, TDI setup time	$T_{Js}$		10			ns
TRST, TMS, TDI hold time	$T_{JH}$		10			ns
TDO output delay time	$T_{JD}$		2		20	ns
TDO data set time	$T_{JZD}$		2		20	ns
TDO data buffer turn-off time	$T_{JDZ}$		2		20	ns



(7) Sync signal

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Sync signal output delay time (vs.DCLK <sup>Note</sup> )	t <sub>SYND</sub>		0	4	8	ns
Sync signal output delay time (vs.PLLIN)	t <sub>SYNWD</sub>		2	10	20	ns

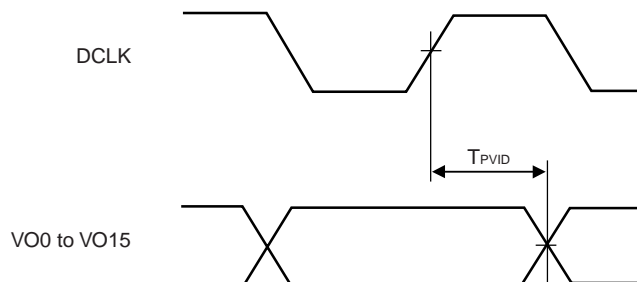
**Note** In case VoPixelClock (x1FF FB34H) bit 27 set to 0 (= shift disable (0 degree)).



(8) Digital RGB output

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
VO (digital RGB) output delay time (vs. DCLK <sup>Note</sup> )	T <sub>PVID</sub>		0	4	8	ns

**Note** In case VoPixelClock (x1FF FB34H) bit 27 set to 0 (= shift disable (0 degree)).

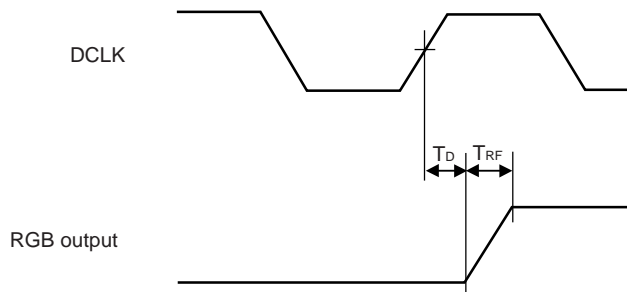


(9) Analog RGB output (design value)

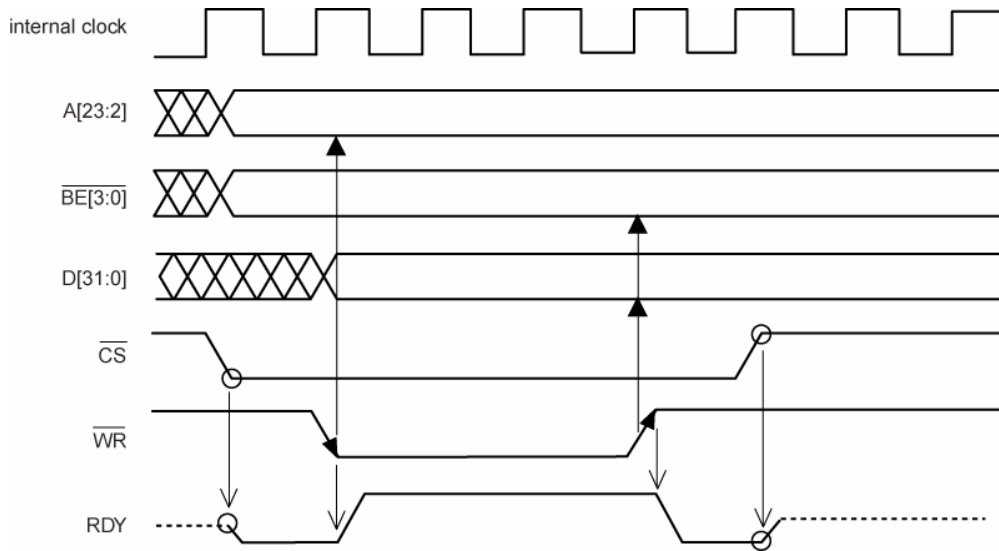
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RGB (analog RGB) output delay time <sup>Note1</sup> (vs. DCLK <sup>Note2</sup> )	T <sub>D</sub>		-10		+10	ns
RGB (analog RGB) output determination time (10% to 90%) <sup>Note1</sup>	T <sub>RF</sub>		-10		+12	ns

**Notes** 1. Reference value

2. In case VoPixelClock (x1FF FB34H) bit 27 set to 0 (= shift disable (0 degree)).

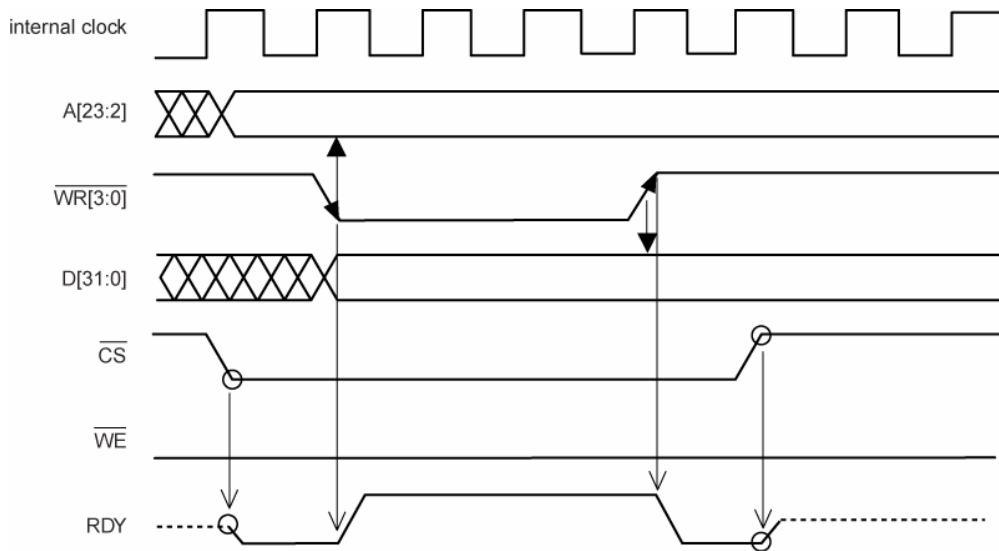


**Single Write BE Mode (When the internal write buffer is not full.)**

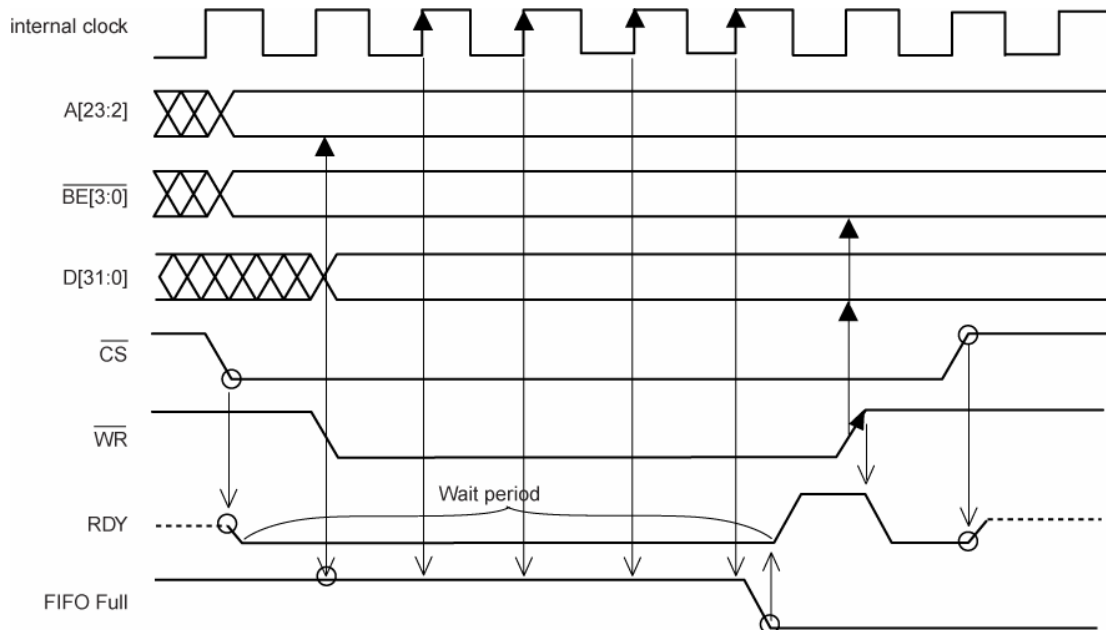


**Remark** The dotted line of RDY signifies the Hi-Z. RDY is asynchronous with internal clock. Therefore it has only analog delay with  $\overline{CS}$  and  $\overline{WR}$ . Data is fetched in  $\overline{WR}$  rising.

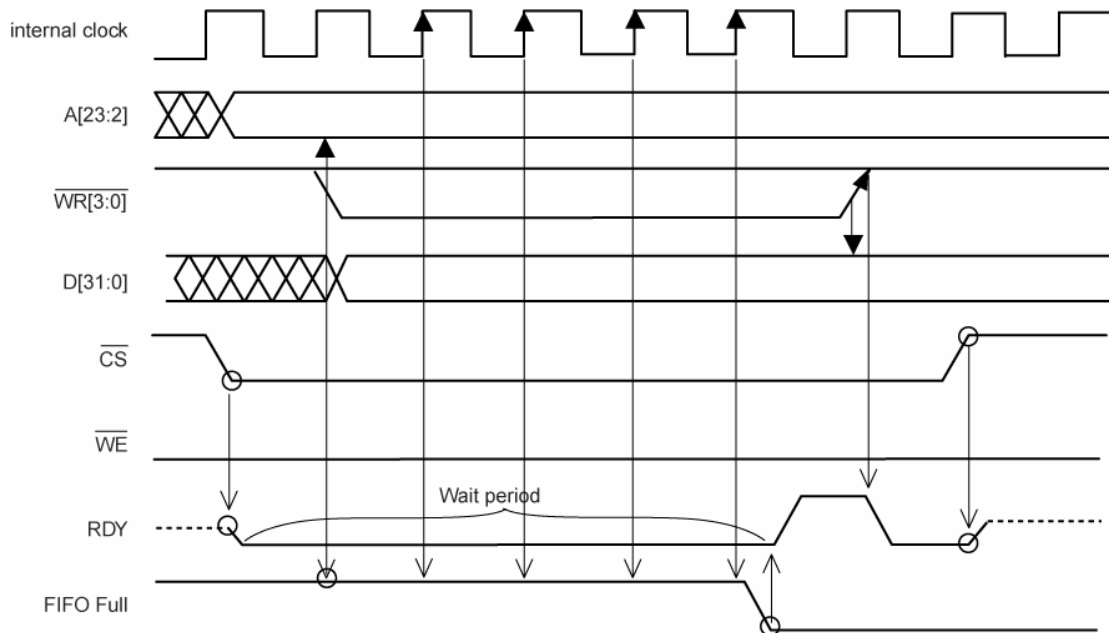
**Single Write WR Mode (When the internal write buffer is not full.)**



**Single Write BE Mode (When the internal write buffer is full. Some wait are inserted by RDY)**

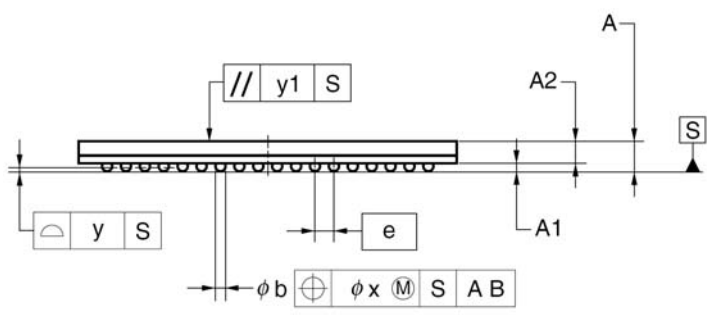
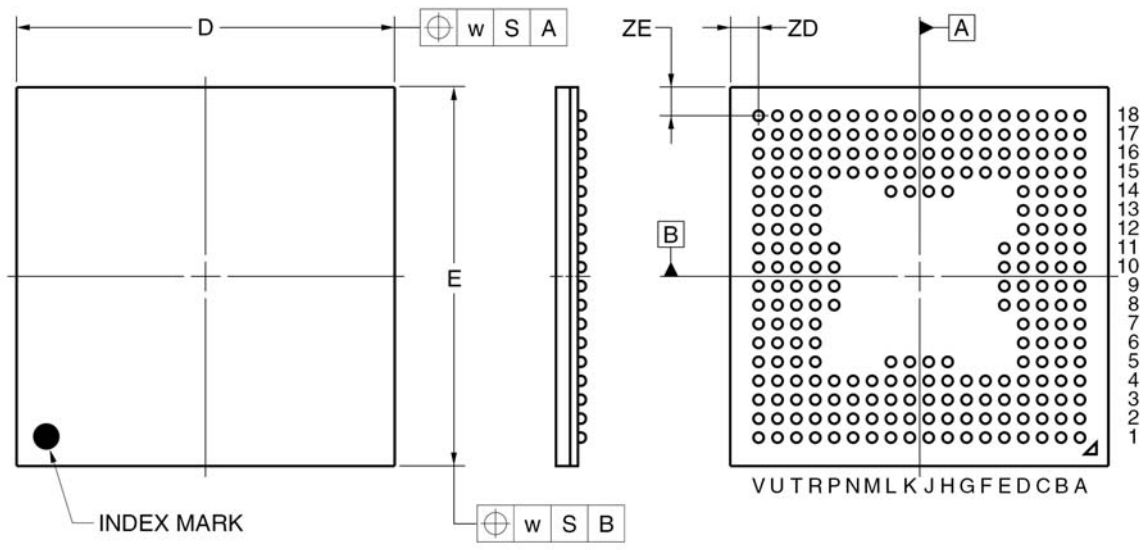


**Single Write WR Mode (When the internal write buffer is full. Some wait are inserted by RDY)**



PACKAGE DRAWING

240-PIN PLASTIC FBGA (16x16)



(UNIT:mm)

ITEM	DIMENSIONS
D	16.00±0.10
E	16.00±0.10
w	0.20
A	1.28±0.10
A1	0.35±0.06
A2	0.93
e	0.80
b	0.50 <sup>+0.05</sup> <sub>-0.10</sub>
x	0.08
y	0.10
y1	0.20
ZD	1.20
ZE	1.20

P240F1-80-GA5



**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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