

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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**256K-BIT CMOS STATIC RAM**  
**32K-WORD BY 8-BIT**

**Description**

The  $\mu$ PD43257B is a high speed, low power, and 262,144 bits (32,768 words by 8 bits) CMOS static RAM. Battery backup is available. And the  $\mu$ PD43257B has two chip enable pins (/CE1, CE2) to extend the capacity. The  $\mu$ PD43257B is packed in 28-pin PLASTIC SOP.

**Features**

- 32,768 words by 8 bits organization
- Fast access time: 70, 85 ns (MAX.)
- Low  $V_{CC}$  data retention: 2.0 V (MIN.)
- Two Chip Enable inputs: /CE1, CE2

Part number	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current		
				At operating mA (MAX.)	At standby $\mu$ A (MAX.)	At data retention $\mu$ A (MAX.) <sup>Note</sup>
$\mu$ PD43257B-xxL	70, 85	4.5 to 5.5	0 to 70	45	50	3
$\mu$ PD43257B-xxLL				45	15	2

**Note**  $T_A \leq 40$  °C,  $V_{CC} = 3.0$  V

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Ordering Information

Part number	Package	Access time ns (MAX.)	Supply current μA (MAX.)		Remark
			At standby	At data retention <sup>Note</sup>	
μPD43257BGU-70L	28-pin PLASTIC SOP (11.43 mm (450))	70	50	3	L version
μPD43257BGU-85L		85			
μPD43257BGU-70LL		70	15	2	LL version
μPD43257BGU-85LL		85			
μPD43257BGU-70L-A	28-pin PLASTIC SOP (11.43 mm (450))	70	50	3	L version
μPD43257BGU-85L-A		85			
μPD43257BGU-70LL-A		70	15	2	LL version
μPD43257BGU-85LL-A		85			

**Note** T<sub>A</sub> ≤ 40 °C, V<sub>CC</sub> = 3.0 V

**Remark** Products with -A at the end of the part number are lead-free products.

EOL Product

Pin Configurations (Marking Side)

/xxx indicates active low signal.

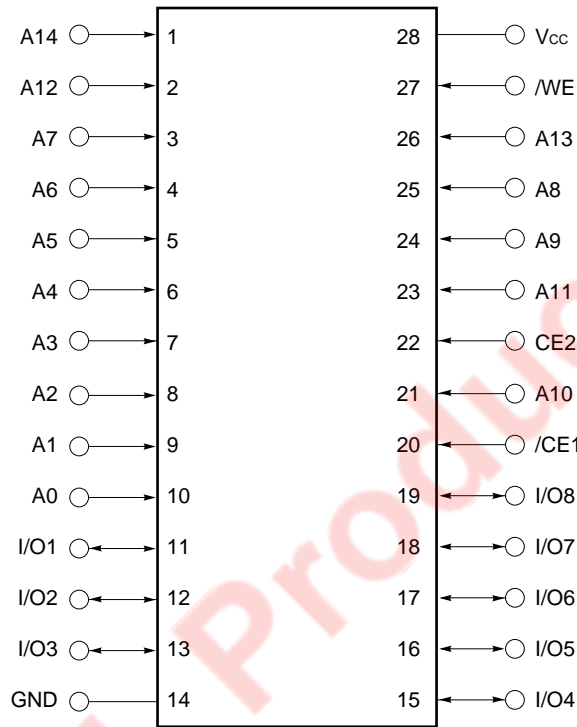
28-pin PLASTIC SOP (11.43 mm (450))

[ μPD43257BGU-xxL ]

[ μPD43257BGU-xxLL ]

[ μPD43257BGU-xxL-A ]

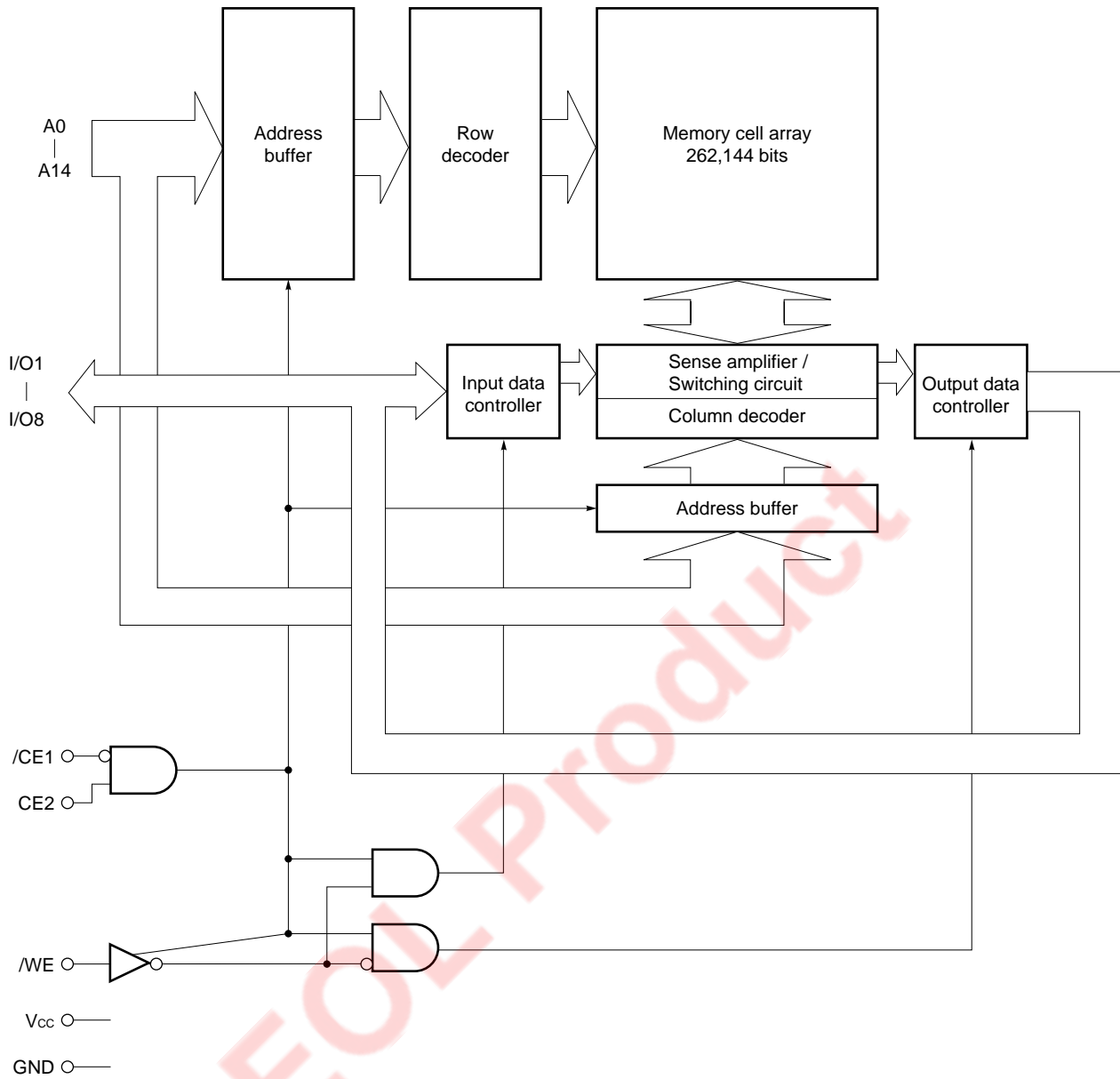
[ μPD43257BGU-xxLL-A ]



- A0 - A14 : Address inputs
- I/O1 - I/O8 : Data inputs / outputs
- /CE1 : Chip Enable 1
- CE2 : Chip Enable 2
- /WE : Write Enable
- Vcc : Power supply
- GND : Ground

**Remark** Refer to **Package Drawings** for the 1-pin marking.

Block Diagram



Truth Table

/CE1	CE2	/WE	Mode	I/O	Supply current
H	x	x	Not selected	High impedance	I <sub>SB</sub>
x	L	x			
L	H	H	Read	D <sub>OUT</sub>	I <sub>CCA</sub>
L	H	L	Write	D <sub>IN</sub>	

Remark x : V<sub>IH</sub> or V<sub>IL</sub>

**Electrical Specifications**

**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V <sub>CC</sub>		-0.5 <sup>Note</sup> to +7.0	V
Input / Output voltage	V <sub>T</sub>		-0.5 <sup>Note</sup> to V <sub>CC</sub> + 0.5	V
Operating ambient temperature	T <sub>A</sub>		0 to 70	°C
Storage temperature	T <sub>stg</sub>		-55 to +125	°C

**Note** -3.0 V (MIN.) (Pulse width : 50 ns)

**Caution** Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V <sub>CC</sub>		4.5	5.0	5.5	V
High level input voltage	V <sub>IH</sub>		2.2		V <sub>CC</sub> +0.5	V
Low level input voltage	V <sub>IL</sub>		-0.3 <sup>Note</sup>		+0.8	V
Operating ambient temperature	T <sub>A</sub>		0		70	°C

**Note** -3.0 V (MIN.) (Pulse width: 50 ns)

**Capacitance (T<sub>A</sub> = 25 °C, f = 1 MHz)**

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V			5	pF
Input / Output capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V			8	pF

- Remarks**
1. V<sub>IN</sub> : Input voltage  
V<sub>I/O</sub> : Input / Output voltage
  2. These parameters are periodically sampled and not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition	μPD43257B-xxL			μPD43257B-xxLL			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 V to V <sub>CC</sub>	-1.0		+1.0	-1.0		+1.0	μA
I/O leakage current	I <sub>LO</sub>	V <sub>I/O</sub> = 0 V to V <sub>CC</sub> , /CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> or /WE = V <sub>IL</sub>	-1.0		+1.0	-1.0		+1.0	μA
Operating supply current	I <sub>CCA1</sub>	/CE1 = V <sub>IL</sub> , CE2 = V <sub>IH</sub> , Minimum cycle time, I <sub>I/O</sub> = 0 mA	μPD43257B-70		45			45	mA
			μPD43257B-85		45		45		
	I <sub>CCA2</sub>	/CE1 = V <sub>IL</sub> , CE2 = V <sub>IH</sub> , I <sub>I/O</sub> = 0 mA			10			10	
	I <sub>CCA3</sub>	/CE1 ≤ 0.2 V, CE2 ≥ V <sub>CC</sub> - 0.2 V, Cycle = 1 MHz, I <sub>I/O</sub> = 0 mA, V <sub>IL</sub> ≤ 0.2 V, V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2 V			10			10	
Standby supply current	I <sub>SB</sub>	/CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> ,			3			3	mA
	I <sub>SB1</sub>	/CE1 ≥ V <sub>CC</sub> - 0.2 V, CE2 ≥ V <sub>CC</sub> - 0.2 V		1.0	50		0.5	15	
	I <sub>SB2</sub>	CE2 ≤ 0.2 V		1.0	50		0.5	15	
High level output voltage	V <sub>OH1</sub>	I <sub>OH</sub> = -1.0 mA	2.4			2.4			V
	V <sub>OH2</sub>	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> -0.5			V <sub>CC</sub> -0.5			
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA			0.4			0.4	V

Remarks 1. V<sub>IN</sub> : Input voltage

V<sub>I/O</sub> : Input / Output voltage

2. These DC characteristics are in common regardless of package types and access time.

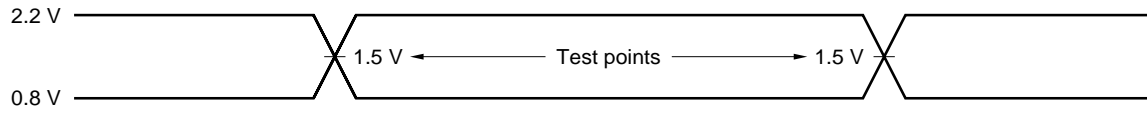


AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

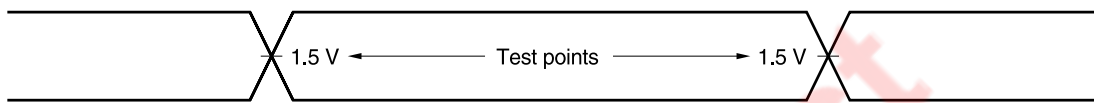
AC Test Conditions

[  $\mu$ PD43257B-70L,  $\mu$ PD43257B-85L,  $\mu$ PD43257B-70LL,  $\mu$ PD43257B-85LL ]

Input Waveform (Rise and Fall Time  $\leq 5$  ns)



Output Waveform

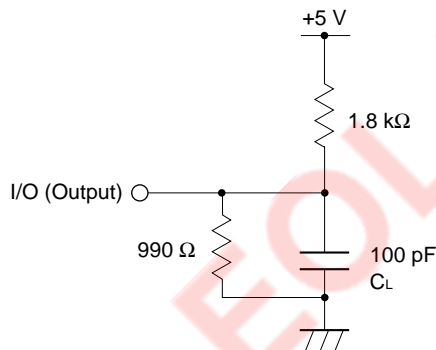


Output Load

AC characteristics with notes should be measured with the output load shown in **Figure 1** and **Figure 2**.

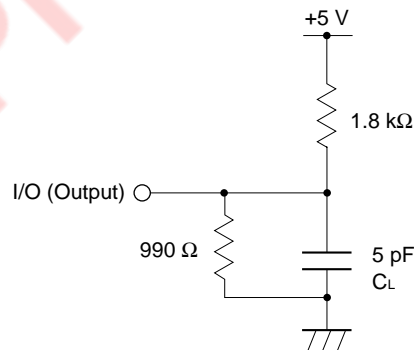
**Figure 1**

( $t_{AA}$ ,  $t_{CO1}$ ,  $t_{CO2}$ ,  $t_{OH}$ )



**Figure 2**

( $t_{LZ1}$ ,  $t_{LZ2}$ ,  $t_{HZ1}$ ,  $t_{HZ2}$ ,  $t_{WHZ}$ ,  $t_{OW}$ )



**Remark**  $C_L$  includes capacitance of the probe and jig, and stray capacitance.

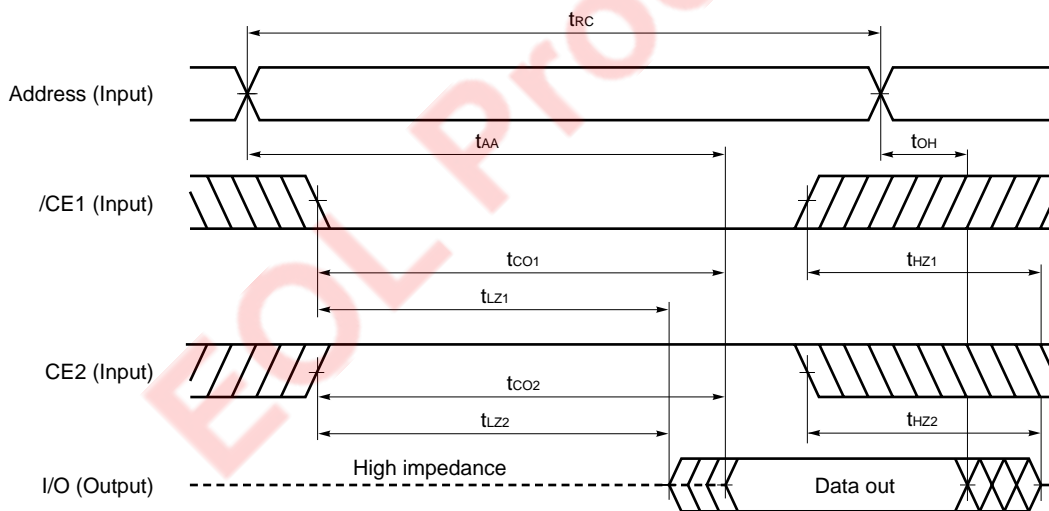
**Read Cycle**

Parameter	Symbol	μPD43257B-70		μPD43257B-85		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	$t_{RC}$	70		85		ns	
Address access time	$t_{AA}$		70		85	ns	<b>Note 1</b>
/CE1 access time	$t_{CO1}$		70		85	ns	
CE2 access time	$t_{CO2}$		70		85	ns	
Output hold from address change	$t_{OH}$	10		10		ns	
/CE1 to output in low impedance	$t_{LZ1}$	10		10		ns	<b>Note 2</b>
CE2 to output in low impedance	$t_{LZ2}$	10		10		ns	
/CE1 to output in high impedance	$t_{HZ1}$		30		30	ns	
CE2 to output in high impedance	$t_{HZ2}$		30		30	ns	

- Notes**
1. See the output load shown in **Figure 1**.
  2. See the output load shown in **Figure 2**.

**Remark** These AC characteristics are in common regardless of package types and L, LL versions.

**Read Cycle Timing Chart**



**Remark** In read cycle, /WE should be fixed to high level.

**Write Cycle**

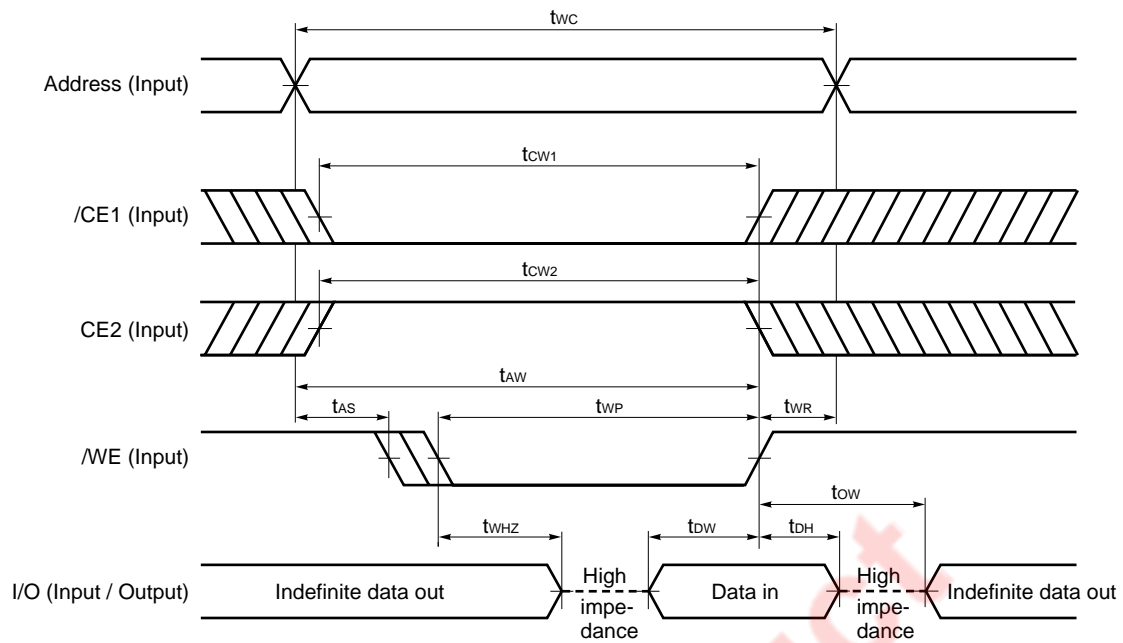
Parameter	Symbol	μPD43257B-70		μPD43257B-85		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t <sub>wc</sub>	70		85		ns	
/CE1 to end of write	t <sub>cw1</sub>	50		70		ns	
CE2 to end of write	t <sub>cw2</sub>	50		70		ns	
Address valid to end of write	t <sub>aw</sub>	50		70		ns	
Address setup time	t <sub>as</sub>	0		0		ns	
Write pulse width	t <sub>wp</sub>	55		65		ns	
Write recovery time	t <sub>wr</sub>	0		0		ns	
Data valid to end of write	t <sub>dw</sub>	30		35		ns	
Data hold time	t <sub>dh</sub>	0		0		ns	
/WE to output in high impedance	t <sub>whz</sub>		30		30	ns	<b>Note</b>
Output active from end of write	t <sub>ow</sub>	10		10		ns	

**Note** See the output load shown in **Figure 2**.

**Remark** These AC characteristics are in common regardless of package types and L, LL versions.

EOL Product

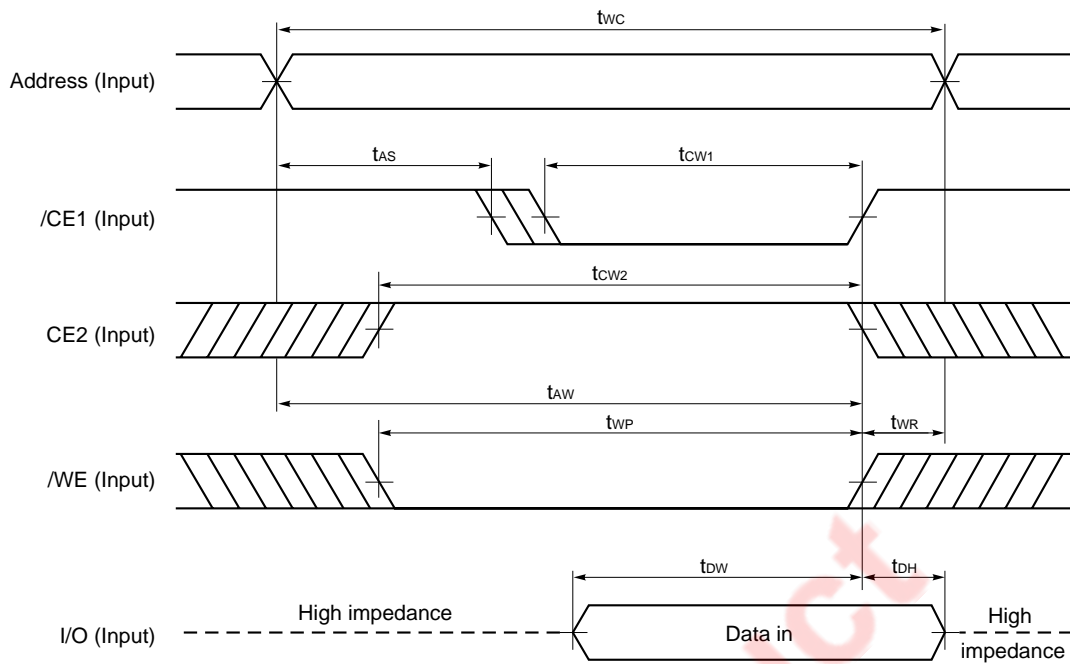
**Write Cycle Timing Chart 1 (/WE Controlled)**



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
  2. When I/O pins are in the output state, therefore the input signals must not be applied to the output.

- Remarks**
1. Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.
  2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.
  3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

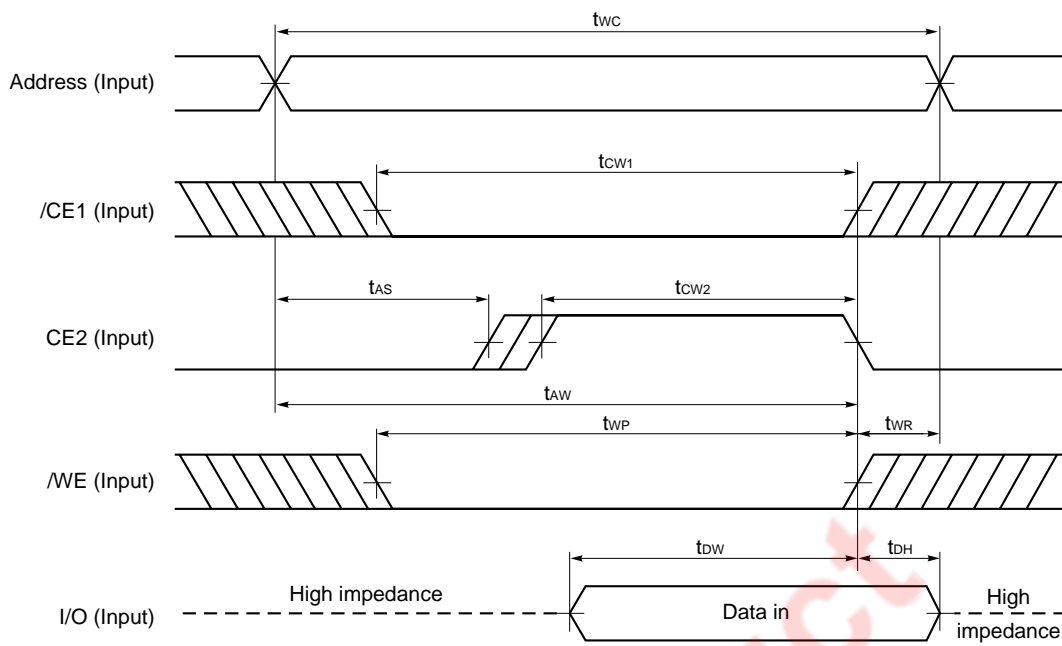
Write Cycle Timing Chart 2 (/CE1 Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
  2. When I/O pins are in the output state, therefore the input signals must not be applied to the output.

**Remark** Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.

**Write Cycle Timing Chart 3 (CE2 Controlled)**



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
  2. When I/O pins are in the output state, therefore the input signals must not be applied to the output.

**Remark** Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.

Low V<sub>CC</sub> Data Retention Characteristics (T<sub>A</sub> = 0 to 70 °C)

Parameter	Symbol	Test Condition	μPD43257B-xxL			μPD43257B-xxLL			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Data retention supply voltage	V <sub>CCDR1</sub>	/CE1 ≥ V <sub>CC</sub> – 0.2 V, CE2 ≥ V <sub>CC</sub> – 0.2 V	2.0		5.5	2.0		5.5	V
	V <sub>CCDR2</sub>	CE2 ≤ 0.2 V	2.0		5.5	2.0		5.5	
Data retention supply current	I <sub>CCDR1</sub>	V <sub>CC</sub> = 3.0 V, /CE1 ≥ V <sub>CC</sub> – 0.2 V, CE2 ≥ V <sub>CC</sub> – 0.2 V		0.5	20 <sup>Note1</sup>		0.5	7 <sup>Note2</sup>	μA
	I <sub>CCDR2</sub>	V <sub>CC</sub> = 3.0 V, CE2 ≤ 0.2 V		0.5	20 <sup>Note1</sup>		0.5	7 <sup>Note2</sup>	
Chip deselection to data retention mode	t <sub>CDR</sub>		0			0			ns
Operation recovery time	t <sub>R</sub>		5			5			ms

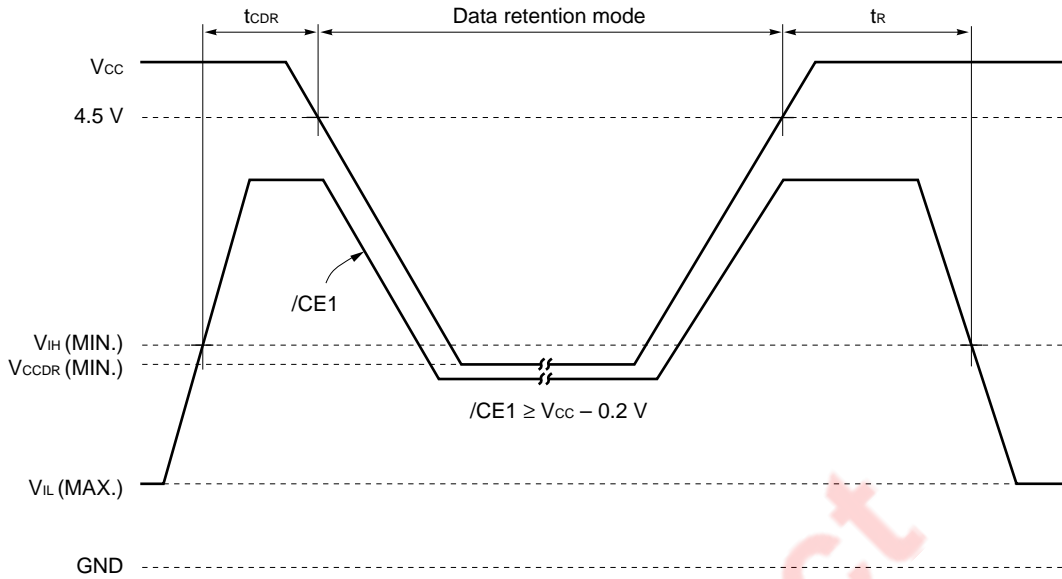
Notes 1. 3 μA (T<sub>A</sub> ≤ 40 °C)

2. 2 μA (T<sub>A</sub> ≤ 40 °C), 1 μA (T<sub>A</sub> ≤ 25 °C)

EOL Product

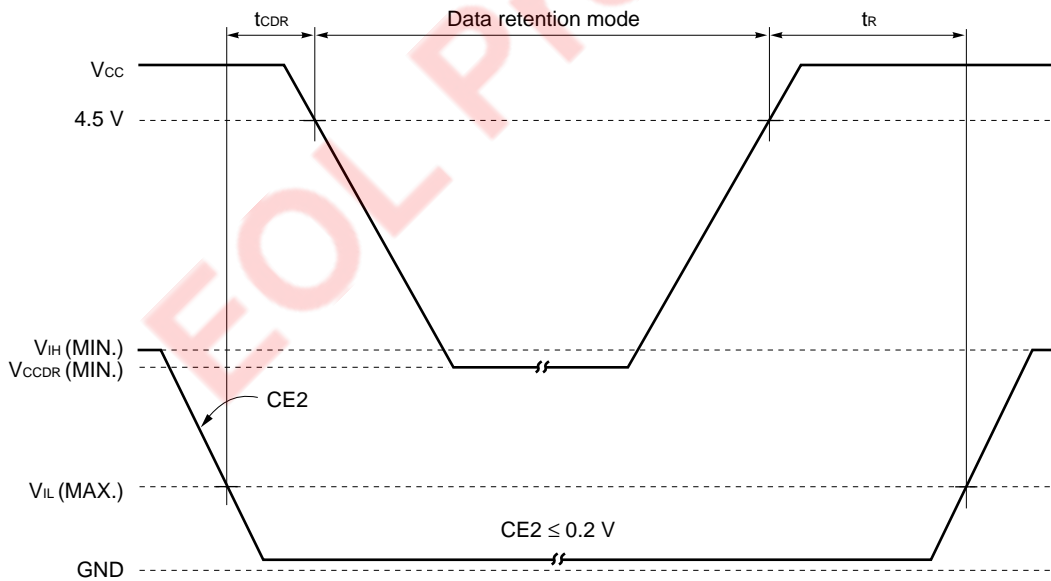
**Data Retention Timing Chart**

**(1) /CE1 Controlled**



**Remark** On the data retention mode by controlling  $/CE1$ , the input level of  $CE2$  must be  $CE2 \geq V_{CC} - 0.2 V$  or  $CE2 \leq 0.2 V$ . The other pins (Address, I/O,  $/WE$ ) can be in high impedance state.

**(2) CE2 Controlled**

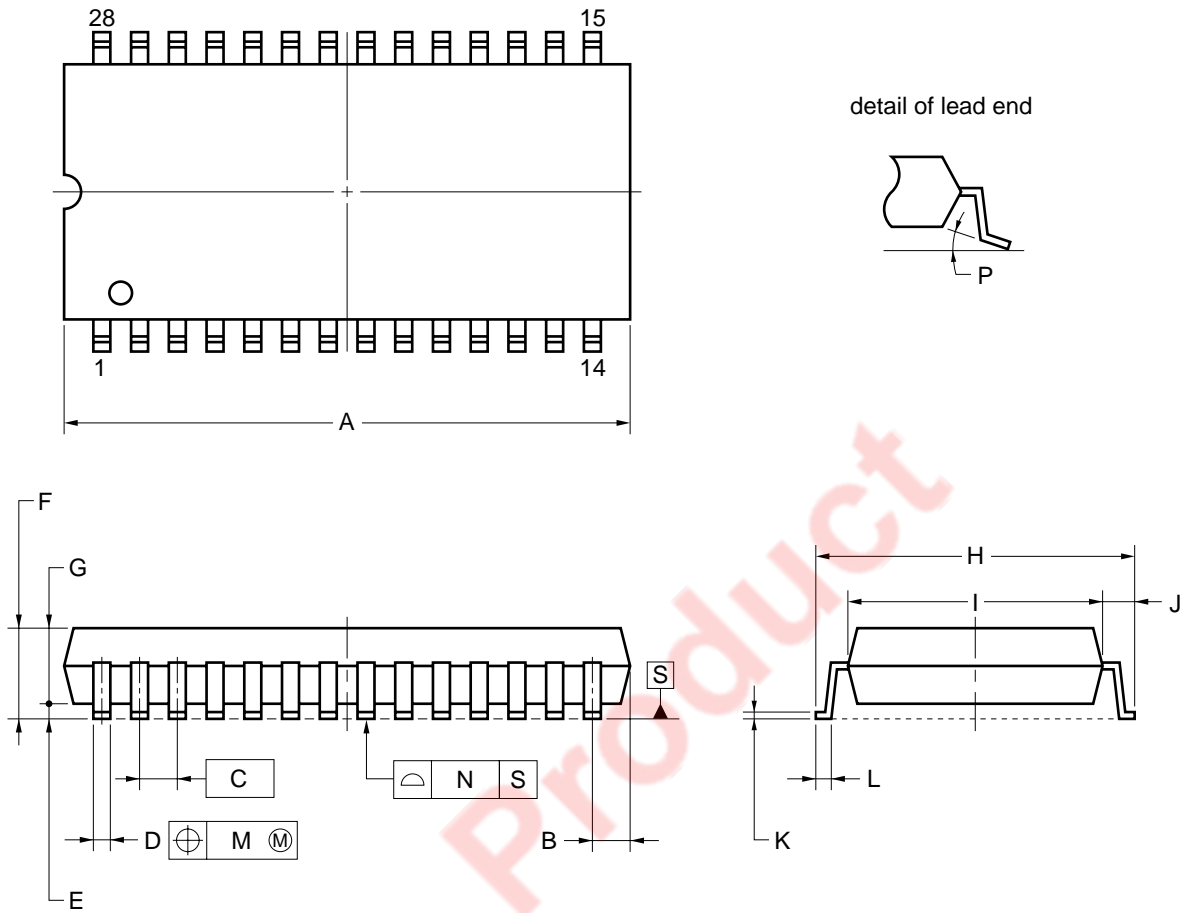


**Remark** On the data retention mode by controlling  $CE2$ , the other pins ( $/CE1$ , Address, I/O,  $/WE$ ) can be in high impedance state.



Package Drawings

28-PIN PLASTIC SOP (11.43 mm (450))



**NOTE**

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	18.0 <sup>+0.6</sup> <sub>-0.05</sub>
B	1.27 MAX.
C	1.27 (T.P.)
D	0.42 <sup>+0.08</sup> <sub>-0.07</sub>
E	0.2±0.1
F	2.95 MAX.
G	2.55±0.1
H	11.8±0.3
I	8.4±0.1
J	1.7±0.2
K	0.22±0.05
L	0.7±0.2
M	0.12
N	0.10
P	3 <sup>+7°</sup> <sub>-3°</sub>

P28GU-50-450A-4

### Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the  $\mu$ PD43257B.

### Types of Surface Mount Device

$\mu$ PD43257BGU-xxL : 28-pin PLASTIC SOP (11.43 mm (450))

$\mu$ PD43257BGU-xxLL : 28-pin PLASTIC SOP (11.43 mm (450))

$\mu$ PD43257BGU-xxL-A : 28-pin PLASTIC SOP (11.43 mm (450))

$\mu$ PD43257BGU-xxLL-A : 28-pin PLASTIC SOP (11.43 mm (450))

### Quality Grade

- A quality grade of the products is "Standard".
- Anti-radioactive design is not implemented in the products.
- Semiconductor devices have the possibility of unexpected defects by affection of cosmic ray that reach to the ground and so forth.

EOL Product

[ MEMO ]

EOL Product

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
10th edition/ Nov. 2009	through	through	Modification	–	Ordering Information revised.

EOL Product

## NOTES FOR CMOS DEVICES

**① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN).

**② HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

**③ PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

**④ STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

**⑤ POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

**⑥ INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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