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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

μPD17P005

4-BIT SINGLE-CHIP MICROCONTROLLER WITH ONE-TIME PROM AND HARDWARE FOR DIGITAL TUNING SYSTEM

DESCRIPTION

μPD17P005 is a model of μPD17005 equipped with one-time PROM instead of a mask ROM.

Since the user program can be written to the PROM of the μPD17P005, this 4-bit microcontroller is ideal for experimental or small-scale production of application systems using μPD17005 or μPD17003A (a model of μPD17005 with reduced ROM and RAM).

Also refer to the Data Sheets of the μPD17005 and μPD17003A.

The electrical characteristics (such as the supply current) of the μPD17P005 and the analog characteristics of the PLL are different from those of the μPD17005. Therefore, take these differences into consideration when designing and producing the application systems.

FEATURES

- Compatible with μPD17005 and 17003A
- Internal one-time PROM: 7932 x 16 bits
- Operating voltage range: 5 V±10%
- I^2C bus (μPD17P005GF-E00-3B9)
- QTOP™ microcontroller model available (μPD17P005GF-xxx-3B9)

ORDERING INFORMATION

PART NUMBER	PACKAGE	QUALITY GRADE
μPD17P005GF-3B9	80-pin plastic QFP (14 x 20 mm)	Standard
μPD17P005GF-E00-3B9*1	80-pin plastic QFP (14 x 20 mm)	Standard
μPD17P005GF-xxx-3B9*2	80-pin plastic QFP (14 x 20 mm)	Standard

*1: I^2C bus model

*2: QTOP microcontroller model

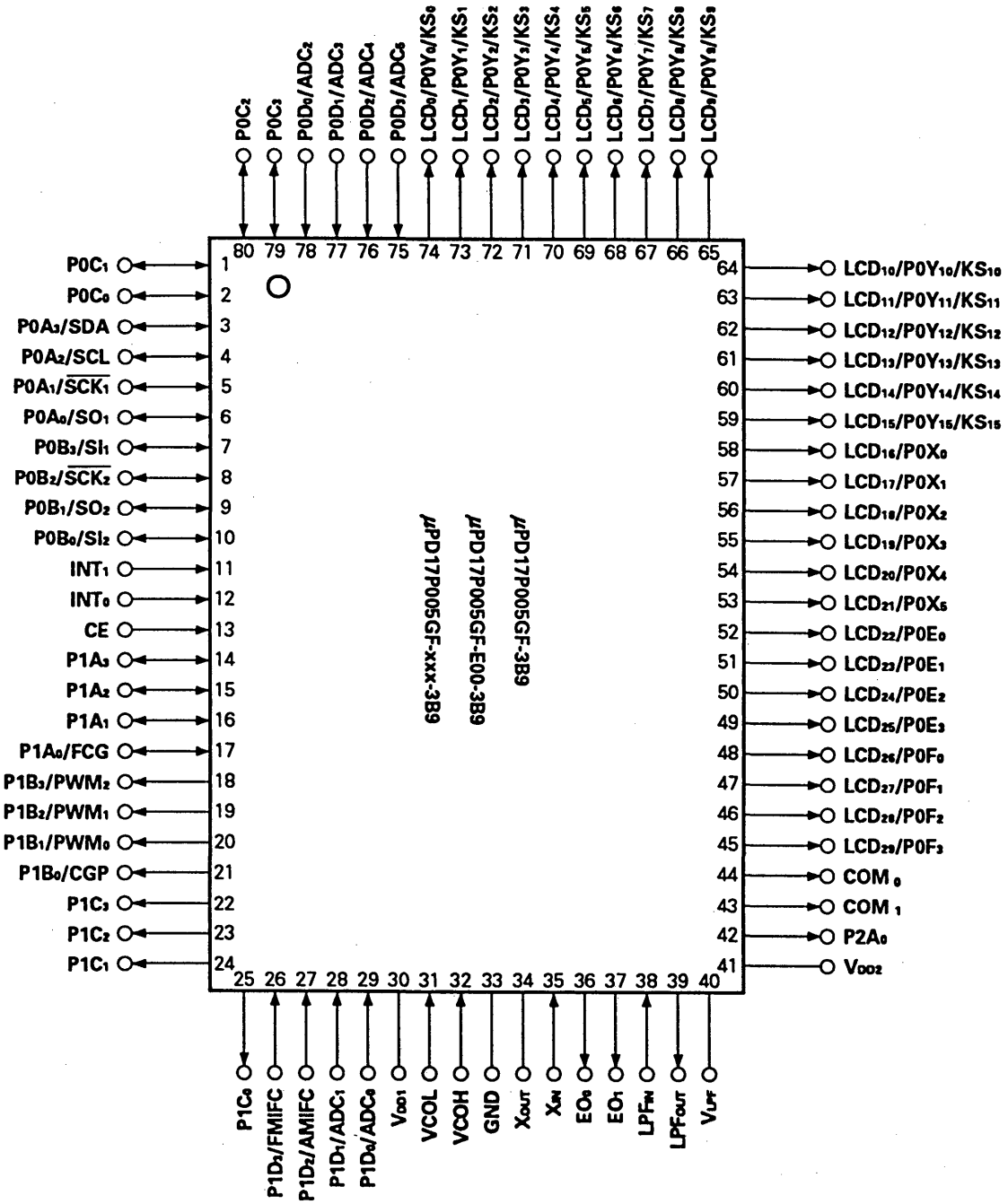
Remarks: QTOP microcontroller is the generic name of a single-chip microcontroller with a one-time PROM that is programmed, stamped, screened, and verified by NEC.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grades on the devices and their recommended applications.

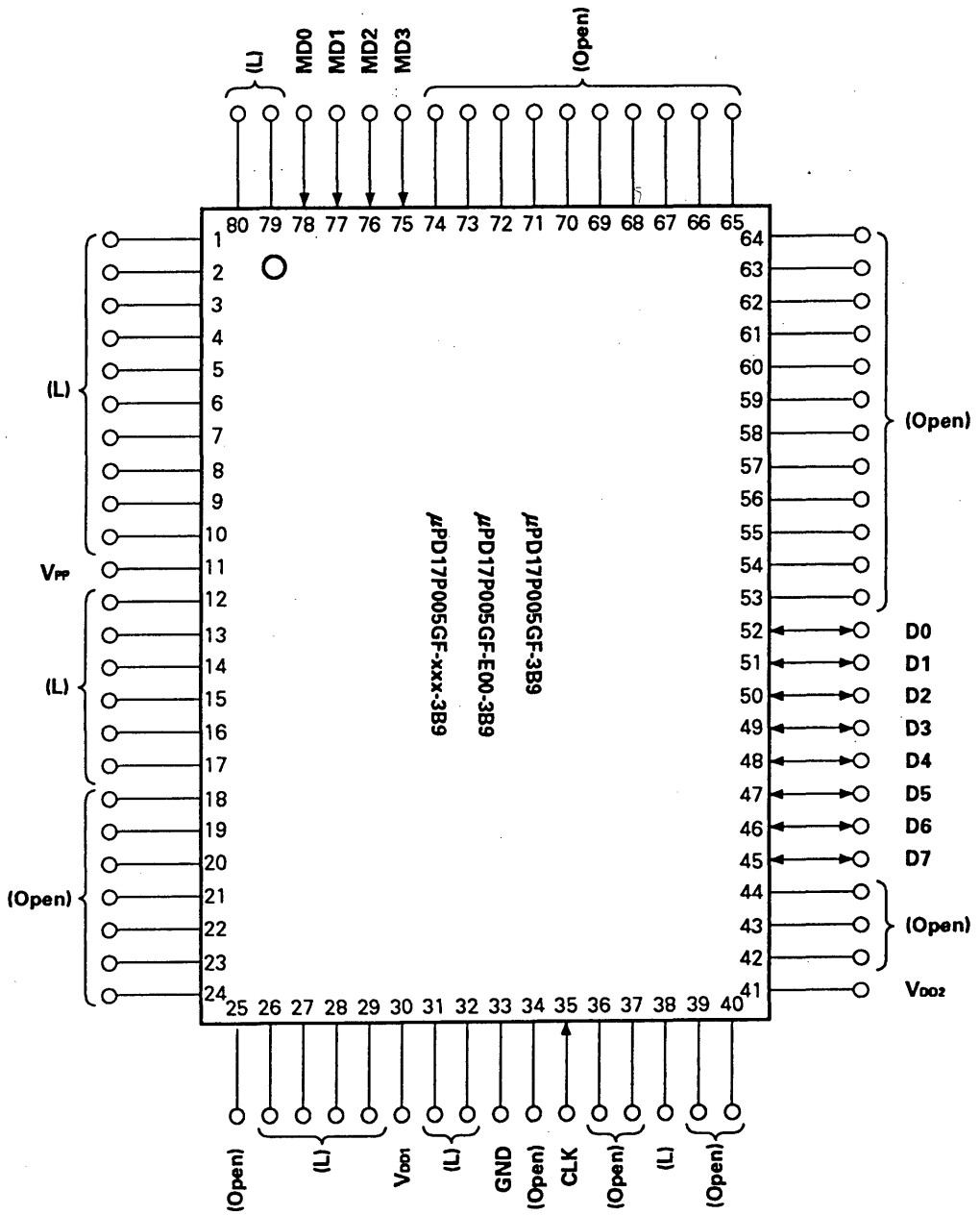
Document No. IC-2703A
(O.D.No. IC-8081A)
Date Published August 1992 P
Printed in Japan

PIN CONFIGURATION (Top View)

(1) In normal operation mode



(2) In PROM programming mode



Note: ( ) indicates the processing of the pins not used in the PROM programming mode.

L :Ground these pins through an individual resistor (470Ω)

Open :Do not connect anything to these pins.

PIN NAME

ADC_0-ADC_5	A/D converter input	$P0E_0$-$P0E_3$	Port 0E
AMIFC	Frequency counter input	$P0F_0$-$P0F_3$	Port 0F
CE	Chip enable input	$P0X_0$-$P0X_3$	Port 0X
CGP	Clock generator port	$P0Y_0$-$P0Y_3$	Port 0Y
COM_0, COM_1	LCD common signal output	$P1A_0$-$P1A_3$	Port 1A
CLK	PROM address updating clock input	$P1B_0$-$P1B_3$	Port 1B
D0-D7	PROM data I/O	$P1C_0$-$P1C_3$	Port 1C
EO_0, EO_1	Error out output	$P1D_0$-$P1D_3$	Port 1D
FCG	External gate counter input	$P2A_0$	Port 2A
FMIFC	Frequency counter input	$\overline{PWM_0}$-$\overline{PWM_2}$	D/A converter output
GND	Ground	SCK_1, SCK_2	Serial clock I/O
INT_0, INT_1	External interrupt input	SCL	Serial clock I/O
KS_0-KS_{15}	Key source signal output	SDA	Serial data I/O
LCD_0-LCD_{29}	LCD segment signal output	SI_1, SI_2	Serial data input
LPF_{IN}	LPF amplifier input	SO_1, SO_2	Serial data output
LPF_{OUT}	LPF amplifier output	VCOH	Local oscillator input, high
MD0-MD3	Operation mode select	VCOL	Local oscillator input, low
$P0A_0$-$P0A_3$	Port 0A	V_{DD1}, V_{DD2}	Positive power supply
$P0B_0$-$P0B_3$	Port 0B	V_{LPF}	LPF amplifier power source
$P0C_0$-$P0C_3$	Port 0C	V_{PP}	PROM write power source
$P0D_0$-$P0D_3$	Port 0D	X_{IN}, X_{OUT}	Main clock oscillator

BLOCK DIAGRAM

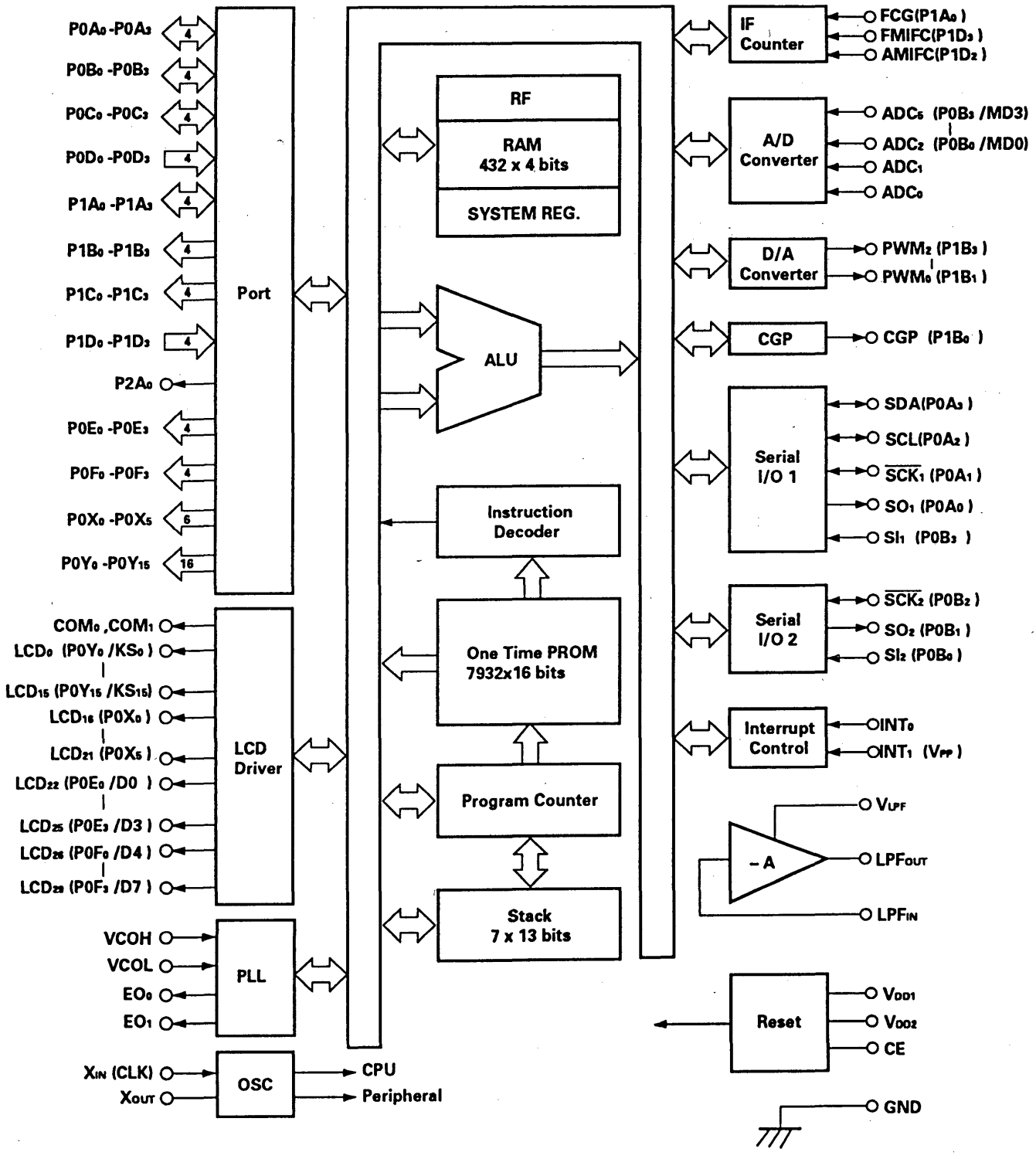


Table of Contents

1. PIN FUNCTIONS

1.1 NORMAL OPERATION MODE

PIN NO.	SYMBOL	FUNCTION	OUTPUT FORM	WHEN POWER-ON RESET
79 80 1 2	$P0C_3$ $P0C_2$ $P0C_1$ $P0C_0$	4-bit I/O port. Can be set in input or output mode in 4-bit units	CMOS push-pull	Input
3 4	$P0A_3$/SDA $P0A_2$/SCL	I/O lines of port 0A, port 0B, and serial interface. • $P0A_3$-$P0A_0$ · 4-bit I/O port · Can be set in input or output mode in 1-bit units. • $P0B_3$-$P0B_0$ · 4-bit CMOS I/O port · Can be set in input or output mode in 1-bit units. • SDA, SCL · SDA: Serial data I/O · SCL: Serial clock I/O • $\overline{SCK_1}$, SO_1, SI_1 · $\overline{SCK_1}$: Serial clock I/O · SO_1: Serial data output · SI_1: Serial data input • $\overline{SCK_2}$, SO_2, SI_2 · $\overline{SCK_2}$: Serial clock I/O · SO_2: Serial data output · SI_2: Serial data input	N-ch open-drain 5 V [$P0A_3$/SDA, $P0A_2$/SCL] CMOS push-pull [$P0A_1$, $\overline{SCK_1}$, $P0A_0$/SO_1, $P0B_3$, $P0B_2$/$\overline{SCK_2}$, $P0B_1$/SO_2, $P0B_0$]	Input [$P0A_3$-$P0A_0$, $P0B_3$-$P0B_0$]
5 6 7 8 9 10	$P0A_1$/$\overline{SCK_1}$ $P0A_0$/SO_1 $P0B_3$/SI_1 $P0B_2$/$\overline{SCK_2}$ $P0B_1$/SO_2 $P0B_0$/SI_2			
11 12	INT_1 INT_0	Edge-detectable vector interrupt input. Both rising and falling edges can be selected	—	Input
13	CE	Selects operation of μPD17P005 and inputs reset signal	—	Input
14 | 16 17	$P1A_3$ | $P1A_1$ $P1A_0$/FCG	I/O lines of port 1A and external gate counter input line • $P1A_3$-$P1A_0$ · 4-bit CMOS I/O port · Can be set in input or output mode in 1-bit units • FCG · External gate counter input	CMOS push-pull ($P1A_3$-$P1A_0$)	Input ($P1A_3$-$P1A_0$)
18 19 20 21	$P1B_3$/PWM_2 $P1B_2$/PWM_1 $P1B_1$/PWM_0 $P1B_0$/CGP	Output lines of port 1B, D/A converter, and clock generator port • $P1B_3$-$P1B_0$ · 4-bit output port • PWM_2-PWM_0 · Output of D/A converter with 8-bit resolution • CGP · Clock generator port output	N-ch open-drain 16 V [$P1B_3$/PWM_2 | $P1B_1$/PWM_0] CMOS push-pull ($P1B_0$/CGP)	Outputs undefined data ($P1B_3$-$P1B_0$)
22 | 25	$P1C_3$ | $P1C_0$	4-bit CMOS output port	CMOS push-pull	Outputs undefined data

PIN NO.	SYMBOL	FUNCTION	OUTPUT FORM	WHEN POWER-ON RESET
26 27 28 29	$P1D_3$/FMIFC $P1D_2$/AMIFC $P1D_1$/ADC_1 $P1D_0$/ADC_0	Analog input to port 1D, frequency counter, and A/D converter • $P1D_3$-$P1D_0$ · 4-bit input port • FMIFC, AMIFC · Input of frequency counter • ADC_1, ADC_0 · Analog input to A/D converter with 6-bit resolution	—	Input ($P1D_3$-$P1D_0$)
30	V_{DD1}	Positive power supply. Apply 5 V±10% to this pin in normal operation mode. Apply 6 V to write, read, or verify program memory.	—	—
31 32	VCOL VCOH	Inputs local oscillation frequency of PLL	—	Input
33	GND	Ground	—	—
34 35	X_{OUT} X_{IN}	Connect crystal oscillator for system clock oscillation across these pins.	CMOS push-pull —	—
36 37	EO_0 EO_1	Output from charge pump of PLL frequency synthesizer. Compares divided value of local oscillation frequency with phase of reference frequency, and outputs result of comparison	CMOS 3-state	High Impedance
38	LPF_{IN}	Input of amplifier for low-pass filter	—	
39	LPF_{OUT}	Output of amplifier for low-pass filter	N-ch open-drain 16 V	
40	V_{LPF}	Power to amplifier for low-pass filter	—	
41	V_{DD2}	Positive power supply. Apply 5 V±10% to this pin in normal operation mode. Apply 6 V to write, read, or verify program memory.	—	—
42	$P2A_0$	1-bit CMOS output port	CMOS push-pull	Outputs undefined data
43 44	COM_1 COM_0	Outputs common signal of LCD controller/driver	CMOS 3-value output	Low-level output
45 | 48 49 | 52 53 | 58 59 | 74	LCD_{29}/$P0F_3$ | LCD_{26}/$P0F_0$ LCD_{25}/$P0E_3$ | LCD_{22}/$P0E_0$ LCD_{21}/$P0X_5$ | LCD_{16}/$P0X_0$ LCD_{15}/$P0Y_{15}$/KS_{15} | LCD_0/$P0Y_0$/KS_0	Output lines of ports 0F, 0E, 0X, 0Y, and segment signals of LCD controller/driver, and key source signals of key matrix • $P0F_3$-$P0F_0$ · 4-bit CMOS output port • $P0E_3$-$P0E_0$ · 4-bit CMOS output port • $P0X_5$-$P0X_0$ · 6-bit CMOS output port • $P0Y_{15}$-$P0Y_0$ · 16-bit CMOS output port • LCD_{29}-LCD_0 · Segment signal output of LCD controller/driver • KS_{15}-KS_0 · Key source signal output of key matrix	CMOS push-pull	Low-level output (LCD_{29}-LCD_0)

PIN NO.	SYMBOL	FUNCTION	OUTPUT FORM	WHEN POWER-ON RESET
75 | 78	$P0D_3/ADC_5$ | $P0D_0/ADC_2$	Port 0D, analog input line to A/D converter, and key source signal return input line of LCD segment • $P0D_3$-$P0D_0$ · 4-bit input port · Connected to pull-down resistor • ADC_5-ADC_2 · Analog input to A/D converter with 6-bit resolution · Key source signal return input	—	Input with pull-down resistor ($P0D_3$-$P0D_0$)

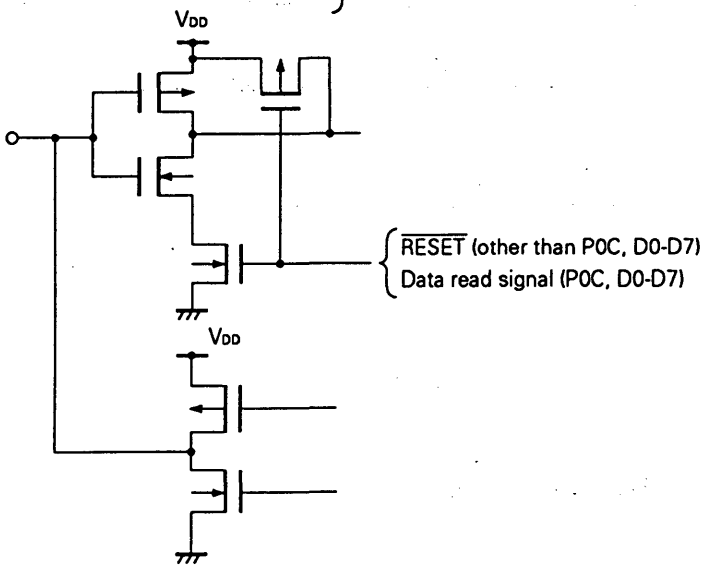
1.2 PROM PROGRAMMING MODE

PIN NO.	SYMBOL	FUNCTION	OUTPUT FORM
11	V_{PP}	Positive power supply for PROM programming. Apply 12.5 V to this pin to write, read, or verify program memory.	—
30	V_{DD1}	Positive power supply. Apply 6 V to this pin to write, read, or verify program memory.	—
33	GND	Ground	—
35	CLK	Clock input for PROM programming	—
41	V_{DD2}	Positive power supply. Apply 6 V to this pin to write, read, or verify program memory.	—
45 | 52	D7 | D0	8-bit data I/O for PROM programming	CMOS push-pull
75 | 78	MD3 | MD0	Input to select operation mode when PROM is programmed	—

Remarks: Pins other than the above are not used in the PROM programming mode. For the processing of the unused pins, refer to (2) PROM programming mode in Pin Connections.

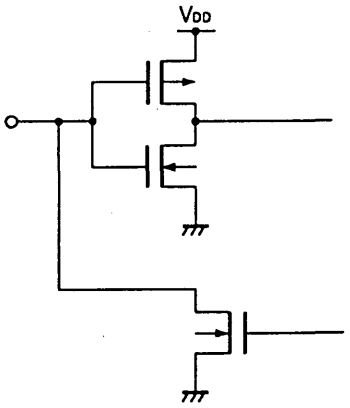
1.3 EQUIVALENT CIRCUIT OF PIN

1.3.1 P0A (P0A1/$\overline{SCK1}$, P0A0/SO1)
P0B (P0B3/SI1, P0B2/$\overline{SCK2}$, P0B1/SO2, P0B0/SI2)
P0C (P0C3, P0C2, P0C1, P0C0)*
P1A (P1A3, P1A2, P1A1, P1A0)
D0-D7* } (I/O)

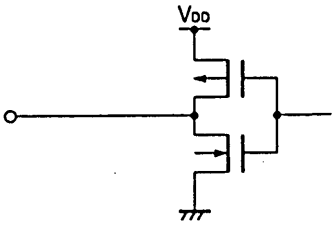


* :The $\overline{RESET}$ signal is not supplied to P0C and D0-D7.

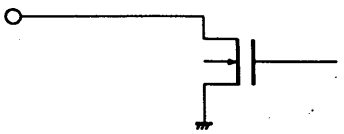
1.3.2 P0A (P0A3/SDA, P0A2/SCL) (I/O)



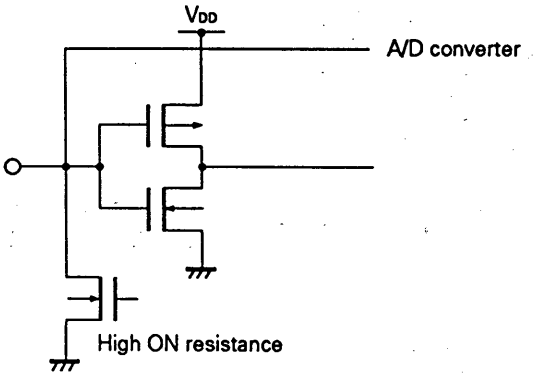
1.3.3 P1B (P1B0/CGP)
P1C (P1C3, P1C2, P1C1, P1C0)
P2A (P2A0)
LCD0/P0Y0/KS0-LCD29/P0F3 } (Output)



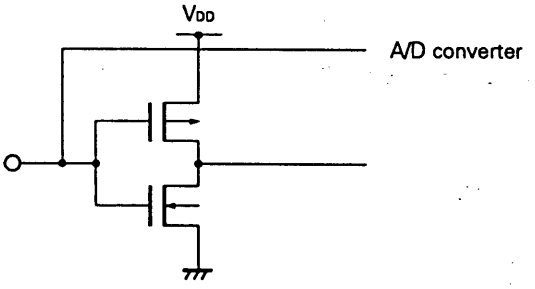
1.3.4 P1B (P1B3/PWM2, P1B2/PWM1, P1B1/PWM0) (Output)



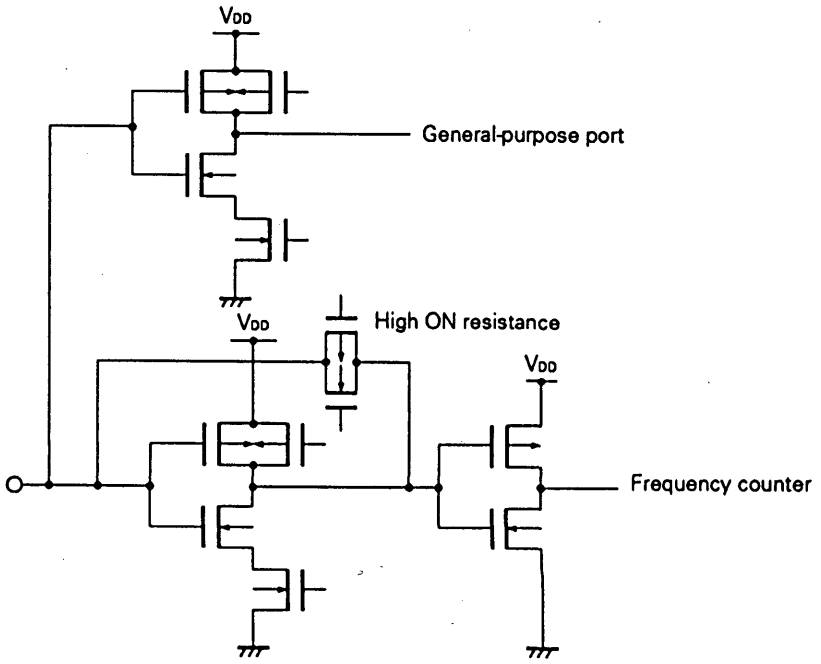
1.3.5 P0D (P0D3/ADC5/MD3, P0D2/ADC4/MD2, P0D1/ADC3/MD1, P0D0/ADC2/MD0) (Input)



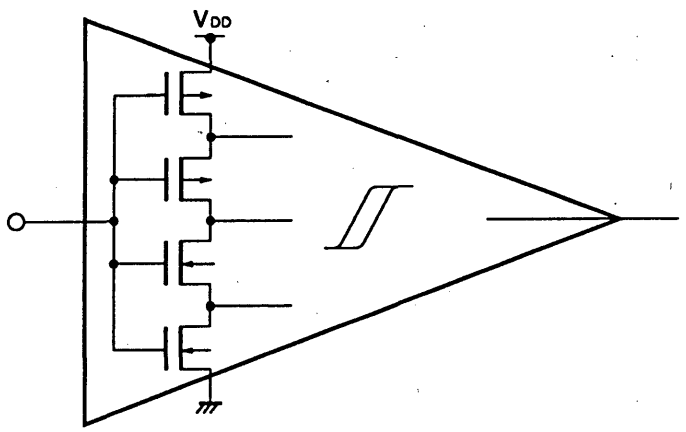
1.3.6 P1D (P1D1/ADC1, P1D0/ADC0) (Input)



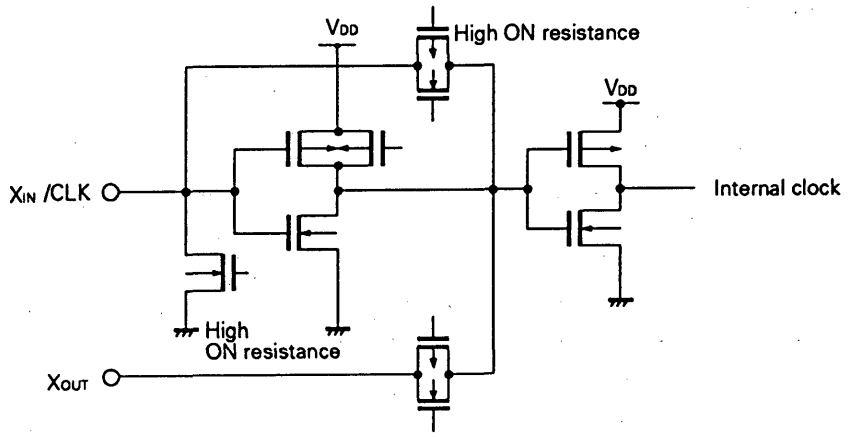
1.3.7 P1D (P1D3/FMIFC, P1D2/AMIFC) (Input)



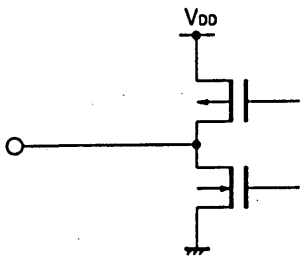
1.3.8 CE, INT_1/V_{PP}, INT_0 } (Schmitt trigger input)



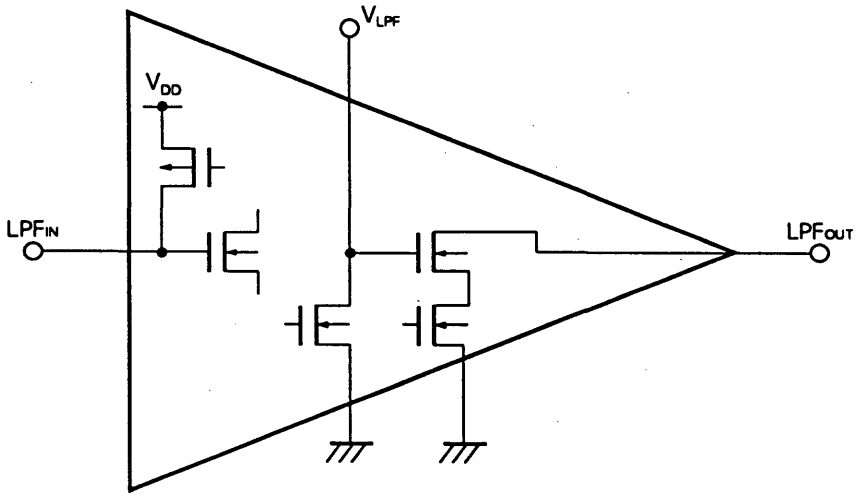
1.3.9 X_{OUT} (output), X_{IN}/CLK (input)



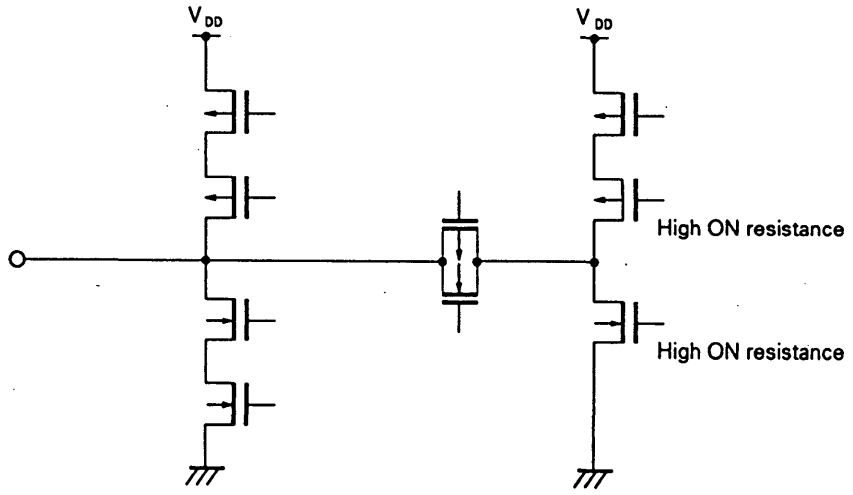
1.3.10 EO_1, EO_0 } (Output)



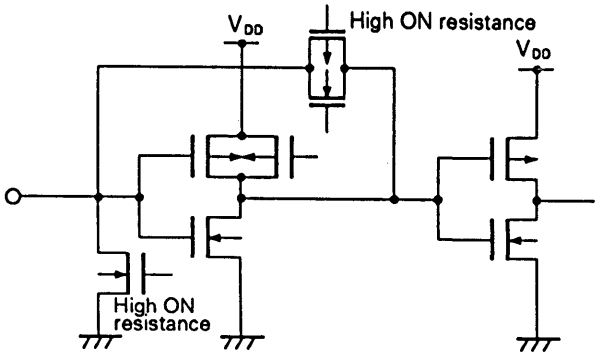
1.3.11 LPF_{IN} (input), LPF_{OUT} (output), V_{LPF}



1.3.12 COM_1, COM_0 (Output)



1.3.13 VCOH, VCOL (Input)



2. FUNCTION LIST

ITEM \ PRODUCT NAME	μPD17003A	μPD17005	μPD17P005
ROM (×16 bits)	3836 (mask ROM)	7932 (mask ROM)	7932 (PROM)
Table reference area	256	7932	
RAM (×4 bits)	320	432	
Data buffer	4		
General register	16		
System register	12 × 4 bits		
Register file	33 × 4 bits (control register)		
General-purpose port register	24 × 4 bits		
Instruction execution time	4.44 μs (at 4.5 MHz, crystal oscillator)		
Stack level	7 (stack can be manipulated)		
General-purpose port: I/O port	16 lines		
General-purpose port: Input port	8 lines		
General-purpose port: Output port	9 lines (+30: LCD segment pin)		
Clock generator port	1 line		
LCD controller/driver	· 30 segment, 2 common 1/2 duty, 1/2 bias, frame frequency 250 Hz, drive voltage V_{DD} Segment pins multiplexed with key source: 16 lines All 30 lines can be used as output port pins (4, 4, 6, and 16 lines each of which can be independently set)		
Serial interface	· 2 systems (3 channels) Serial interface 1: 2-line ... I^2C bus mode*, serial I/O mode 3-line ... Serial I/O mode Serial interface 2: 3-line ... Serial I/O mode		
D/A converter	· 8 bits × 3 lines (PWM output, output voltage: 16 V max.)		
A/D converter	· 6 bits × 6 lines (successive approximation method by software)		
Interrupt	· 5 channels (maskable interrupt) External interrupt : 2 channels (INT_0 pin, INT_1 pin) Internal interrupt : 3 channels (timer, serial interface 1, frequency counter)		
Timer	· 2 systems Timer carry (1, 5, 100, 250 ms) Timer interrupt (1, 5, 100, 250 ms)		
Reset function	· Power-ON reset (on power application) · Reset by CE pin (CE pin: low level→high level) · Power failure detection function		

*: Among the PROM models, only μPD17P005GF-E00-3B9 can use the I^2C bus mode.
For the mask ROM model, it is confirmed when an order for the custom code is received.

(con't)

ITEM \ PRODUCT NAME		μPD17003A	μPD17005	μPD17P005
PLL frequency synthesizer	Division modes	· 2 modes Direct division mode (VCOL pin 30 MHz max.) Pulse swallow method (VCOL pin 40 MHz max.) (VCOH pin 150 MHz max.)		
	Reference frequency	· 12 types selected by program 1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50, 100 kHz		
	Charge pump	· Two independent error outputs		
	Phase comparator	· Unlock can be detected through program Delay time of unlock FF selectable		
	LPF amp	· CMOS operational amp. Output withstand voltage: 16 V max.		
Frequency counter		· Frequency measurement $P1D_3$/FMIFC pin 5 to 15 MHz $P1D_2$/AMIFC pin 0.1 to 1 MHz · External gate width measurement $P1A_0$/FCG pin		
Supply voltage		· V_{DD} = 4.5 to 5.5 V (PLL and CPU operate) · V_{DD} = 3.5 to 5.5 V (PLL stops, CPU operates) · V_{DD} = 2.2 to 5.5 V (crystal oscillator stops)		
Package		80-pin plastic QFP (14 × 20 mm)		

3. WRITING, READING, AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The internal program memory of the μPD17P005 is a 15864 × 8 bit one-time PROM to which data can be electrically written. This PROM is accessed in 1-word or 16-bit units in a normal operation mode. When the program memory is written, read, or verified, the PROM is accessed in 1-word or 8-bit units. The higher 8 bits of 1 word or 16 bits are assigned to an even address, while the lower 8 bits are assigned to an odd address.

When the PROM is to be written, read, or verified, set the PROM mode and use the pins shown in Table 3-1 below.

Note that there is no address input pin. Instead, the clock signal input from the CLK pin is used to update the address.

Table 3-1 Pins Used to Write, Read, or Verify Program Memory

PIN NAME	FUNCTION
V_{PP}	Applies program voltage (12.5 V)
CLK	Inputs address updating clock
MD0-MD3	Select operation mode
D0-D7	Input/output 8-bit data
V_{DD1},V_{DD2}	Apply supply voltage (6 V)

Write the internal PROM by using the following PROM programmer and program adapter:

PROM programmer	AF-9703 (Ando Electric.)
	AF-9704 (ditto)
Program adapter	AF-9803 (ditto)

3.1 OPERATION MODE FOR WRITING, READING, AND VERIFYING PROGRAM MEMORY

The μPD17P005 is set in a mode to write, read, or verify the program memory when +6 V is applied to the V_{DD} pin and +12.5 V is applied to the VPP pin.

To set the program memory write, read, and verify modes, use the MD0 through MD3 pins as shown in Table 3-2.

The pins not used to write, read, or verify the program memory should be either opened, or connected to GND through a pull-down resistor (470 Ω). (Refer to (2) PROM programming mode in Pin Configuration.)

Table 3-2 Operation Mode When Program Memory is Written, Read, or Verified

SPECIFIES OPERATION MODE						OPERATION MODE
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5V	+6V	H	L	H	L	Clears program memoryaddressto0
		L	H	H	H	Write mode
		L	L	H	H	Read, verify modes
		H	X	H	H	Program inhibit mode

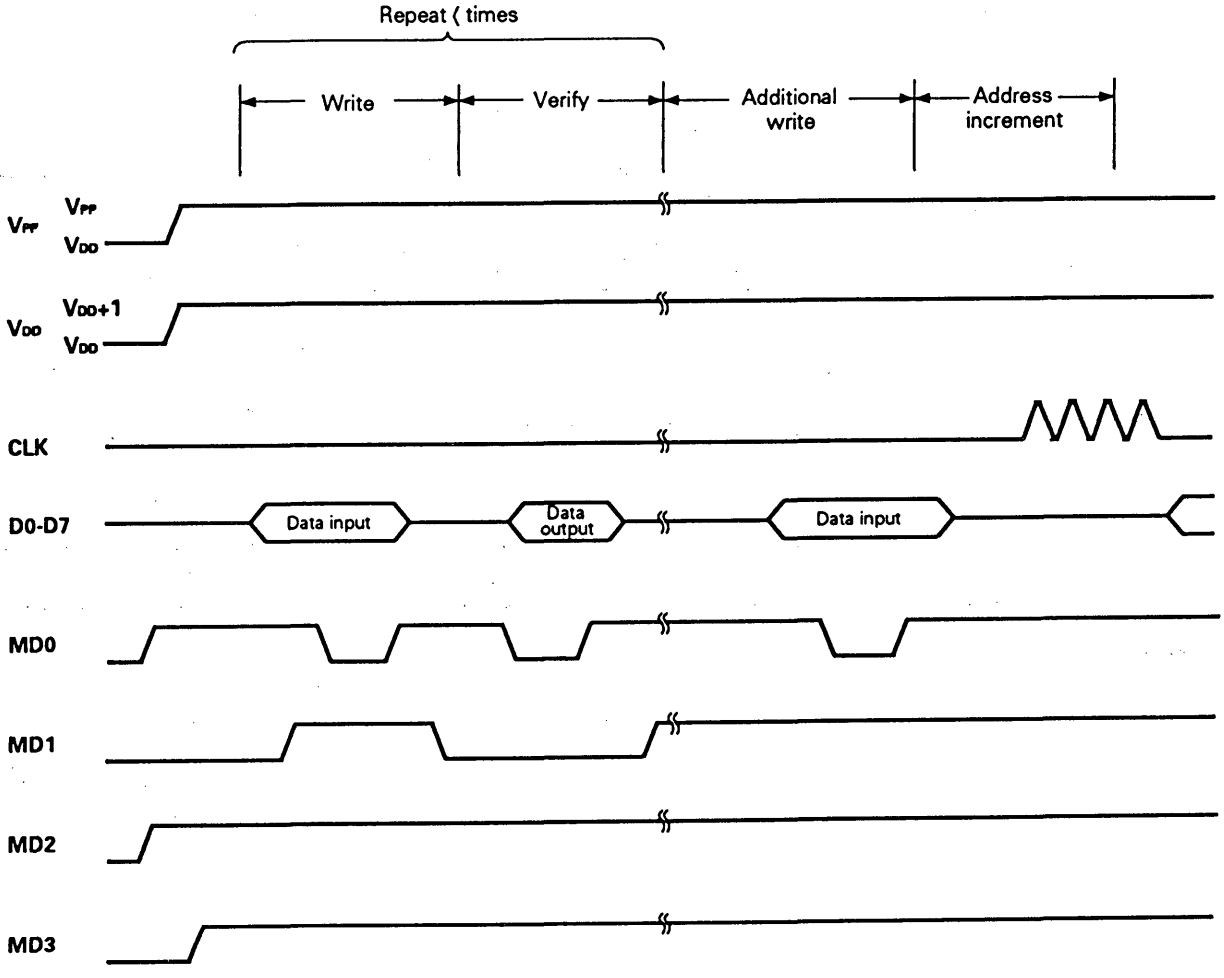
Remarks: X: L or H

3.2 WRITING PROGRAM MEMORY

The program memory can be written at high speeds in the following sequence:

(1) Pull down the unused pins to GND through a resistor. Keep the CLK pin at the low level.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait for 10 us.
(4) Set the program memory address 0 clear mode.
(5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Set the program inhibit mode.
(7) Write data in 1-ms write mode.
(8) Set the program inhibit mode.
(9) Set the verify mode. If the program memory has been correctly written, proceed to step (10). If not, repeat steps (7) through (9).
(10) Additional writing of (Number of times the program memory has been written in (7) through (9): X) × 1 ms
(11) Set the program inhibit mode.
(12) Input a pulse to the CLK pin four times to update the program memory address by one (+1).
(13) Repeat steps (7) through (12) until the last address is written.
(14) Set the program memory address 0 clear mode.
(15) Change the voltage on the V_{DD} and V_{PP} pins to 5 V.
(16) Turn off the power.

Steps (2) through (12) are illustrated below.

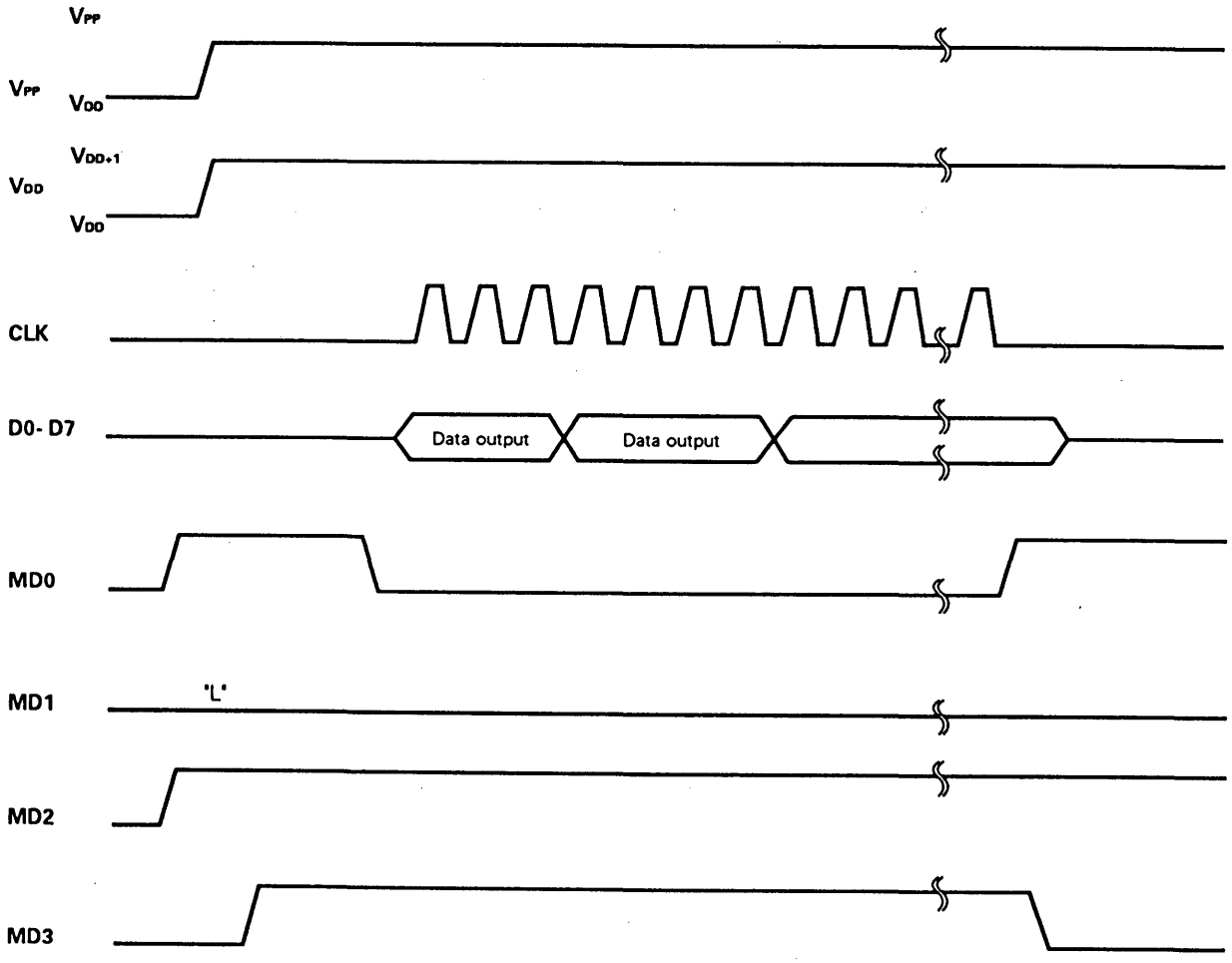


3.3 READING PROGRAM MEMORY

Read the contents of the program memory of the μPD17P005 in the following sequence:

(1) Pull down the unused pins to GND through a resistor. Keep the CLK pin at the low level.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait for 10 us.
(4) Set the program memory address 0 clear mode.
(5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Set the program inhibit mode.
(7) Set the verify mode. When the clock pulse is input to the CLK pin, data is sequentially output one address at a time with four clocks constituting one cycle.
(8) Set the program inhibit mode.
(9) Set the program memory address 0 clear mode
(10) Change the voltage on the V_{DD} and V_{PP} pins to 5 V.
(11) Turn off the power.

Steps (2) through (9) are illustrated below.



4. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (Ta = 25±2°C)

PARMETER	SYMBOL	CONDITION	RATINGS	UNIT
Supply Voltage	V_{DD}		−0.3 to +6.0	V
Input Voltage	V_I		−0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	Except $P1B_1$ - $P1B_3$, $P0A_2$, $P0A_3$, LPF_{OUT}	−0.3 to V_{DD} + 0.3	V
Output Withstand Voltage	V_{BDS1}	$P1B_1$ - $P1B_3$, LPF_{OUT}	18.0	V
	V_{BDS2}	$P0A_2$, $P0A_3$	V_{DD} + 0.3	V
High-Level Output Current	I_{OH}	1 pin	−12	mA
		Total of all pins	−20	mA
Low-Level Output Current	I_{OL}	1 pin	12	mA
		Total of all pins	20	mA
Operating Temperature	T_{opt}		−40 to +85	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD1}	PLL and CPU operate	4.5	5.0	5.5	V
Supply Voltage	V_{DD2}	PLL stops, CPU operates	3.5	5.0	5.5	V
Data Retention Voltage	V_{DDR}	Crystal oscillator stops	2.2		5.5	V
Supply Voltage Rise Time	t_{rise}	V_{DD} = 0 → 4.5 V			500	ms
Input Amplitude	V_{in1}	VCOL, VCOH	0.5		V_{DD}	V_{P-P}
	V_{in2}	AMIFC, FMIFC	0.5		V_{DD}	V_{P-P}
Output Withstand Voltage	V_{BDS}	$P1B_1$ - $P1B_3$, LPF_{OUT}			16.0	V
Operating Temperature	T_{opt}		−40		+85	°C

DC Characteristics (Ta = -40 to +85°C, V_{DD} = 4.5 to 5.5 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD1}	CPU and PLL operate	4.5	5.0	5.5	V
	V_{DD2}	CPU operates, PLL stops	3.5	5.0	5.5	V
Supply Current	I_{DD1}	CPU operates, PLL stops. X_{IN} pin Sine wave input (f_{IN} = 4.5 MHz, V_{IN} = V_{DD}), Ta = 25°C		2.8	5.6	mA
	I_{DD2}	CPU operates, PLL stops, HALT instruction is used (20 instructions executed in 1 ms) X_{IN} pin Sine wave input (f_{IN} = 4.5 MHz, V_{IN} = V_{DD}), Ta = 25°C		1.9	3.8	mA
Data Retention Voltage	V_{DDR1}	Power failure detected by timer FF; with crystal oscillator	3.5		5.5	V
	V_{DDR2}	Power failure detected by timer FF; crystal oscillator stops	2.2		5.5	V
	V_{DDR3}	Data memory (RAM) retained	2.0		5.5	V
Data Retention Current	I_{DDR1}	Crystal oscillator stops Ta = 25°C		2	15	μA
	I_{DDR2}	Crystal oscillator stops V_{DD} = 5.0 V, Ta = 25°C		2	10	μA
Intermediate Level Output Voltage	V_{OM1}	COM_0, COM_1 V_{DD} = 5 V	2.3	2.5	2.7	V
High-Level Input Voltage	V_{IH1}	$P0A_0$-$P0A_3$, $P0B_0$-$P0B_3$, $P0C_0$-$P0C_3$, $P1A_0$-$P1A_3$, $P1D_0$-$P1D_3$, CE, INT_0, INT_1	0.8 V_{DD}		V_{DD}	V
	V_{IH2}	$P0D_0$-$P0D_3$	0.6 V_{DD}		V_{DD}	V
Low-Level Input Voltage	V_{IL}	$P0A_0$-$P0A_3$, $P0B_0$-$P0B_3$, $P0C_0$-$P0C_3$, $P0D_0$-$P0D_3$, $P1A_0$-$P1A_3$, $P1D_0$-$P1D_3$, CE, INT_0, INT_1	0		0.2 V_{DD}	V
High-Level Output Current	I_{OH1}	$P0A_0$, $P0A_1$, $P0B_0$-$P0B_3$, $P0C_0$-$P0C_3$, $P1A_0$-$P1A_3$, $P1C_0$-$P1C_3$, $P1B_0$, $P2A_3$, V_{OH} = V_{DD} – 1 V	– 1.0	– 5.0		mA
	I_{OH2}	LCD_0-LCD_{29}, EO_0, EO_1 V_{OH} = V_{DD} – 1 V	– 1.0	– 4.0		mA
Low-Level Output Current	I_{OL1}	$P0A_0$-$P0A_3$, $P0B_0$-$P0B_3$, $P0C_0$-$P0C_3$, $P1A_0$-$P1A_3$, $P1C_0$-$P1C_3$, $P1B_0$, $P2A_0$, V_{OL} = 1 V	1.0	7.0		mA
	I_{OL2}	LCD_0-LCD_{29}, EO_0, EO_1 V_{OL} = 1 V	1.0	3.5		mA
	I_{OL3}	$P1B_1$-$P1B_3$ V_{OL} = 1 V	1.0	2.0		mA
	I_{OL4}	$P0A_2$, $P0A_3$ V_{OL} = 1 V	1.0	10.0		mA
High-Level Input Current	I_{IH1}	VCOH pulled down V_{IH} = V_{DD}	0.1	0.8		mA
	I_{IH2}	VCOL pulled down V_{IH} = V_{DD}	0.1	0.8		mA
	I_{IH3}	X_{IN} pulled down V_{IH} = V_{DD}	0.1	1.3		mA
	I_{IH4}	$P0D_0$-$P0D_3$ pulled down V_{IH} = V_{DD}	0.05	0.13	0.30	mA
Output Off Leakage Current	I_{L1}	$P0A_2$, $P0A_3$ V_{OH} = V_{DD}			500	nA
	I_{L2}	$P1B_1$-$P1B_3$, LPF_{OUT} V_{OH} = 16 V			500	nA
	I_{L3}	EO_0, EO_1 V_{OH} = V_{DD}, V_{OL} = 0 V			±100	nA

AC Characteristics (Ta = -40 to +85°C, V_{DD} = 4.5 to 5.5 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Fequency	f_{IN1}	VCOL MF mode, sine wave input V_{IN} = 0.3 V_{P-P}	0.5		30	MHz
	f_{IN2}	VCOL HF mode, sine wave input V_{IN} = 0.3 V_{P-P}	5		40	MHz
	f_{IN3}	VCOH, sine wave input V_{IN} = 0.3 V_{P-P}	9		150	MHz
	f_{IN4}	AMIFC, sine wave input V_{IN} = 0.5 V_{P-P}	0.1		1	MHz
	f_{IN5}	AMIFC, sine wave input V_{IN} = 0.05 V_{P-P}	0.44		0.46	MHz
	f_{IN6}	FMIFC, sine wave input V_{IN} = 0.5 V_{P-P}	5		15	MHz
	f_{IN7}	FMIFC, sine wave input V_{IN} = 0.06 V_{P-P}	10.5		10.9	MHz
A/D Converter Resolution					6	bit
A/D Converter Total Error		Ta = −10 to +50°C		±1	±1.5	LSB

Reference Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Current	I_{DD3}	CPU and PLL operate VCOH sine wave input f_{IN} = 150 MHz, V_{IN} = 0.5 V_{P-P} V_{DD} = 5 V, Ta = 25°C		15		mA
High-Level Output Current	I_{OH4}	COM_0, COM_1 V_{OH} = V_{DD} − 1 V		−0.2		mA
Intermediate Level Output Current	I_{OM1}	COM_0, COM_1 V_{OM} = V_{DD} − 1 V		−20		μA
	I_{OM2}	COM_0, COM_1 V_{OM} = 1 V		20		μA
Low-Level Output Current	I_{OL5}	COM_0, COM_1 V_{OL} = 1 V		0.2		mA

DC Programming Characteristics (T_a = 25°C, V_{DD} = 6.0±0.25 V, V_{PP} = 12.5±0.5 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
High-Level Input Voltage	V_{IH1}	Other than CLK	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	CLK	V_{DD} – 0.5		V_{DD}	V
Low-Level Input Voltage	V_{IL1}	Other than CLK	0		0.3 V_{DD}	V
	V_{IL2}	CLK	0		0.4	V
Input Leakage Current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			±10	μA
High-Level Output Voltage	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 1 mA			1.0	V
V_{DD} Supply Current	I_{DD}				30	mA
V_{PP} Supply Current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Note:Note: 1. Keep V_{PP} to within +13.5 V including the overshoot.

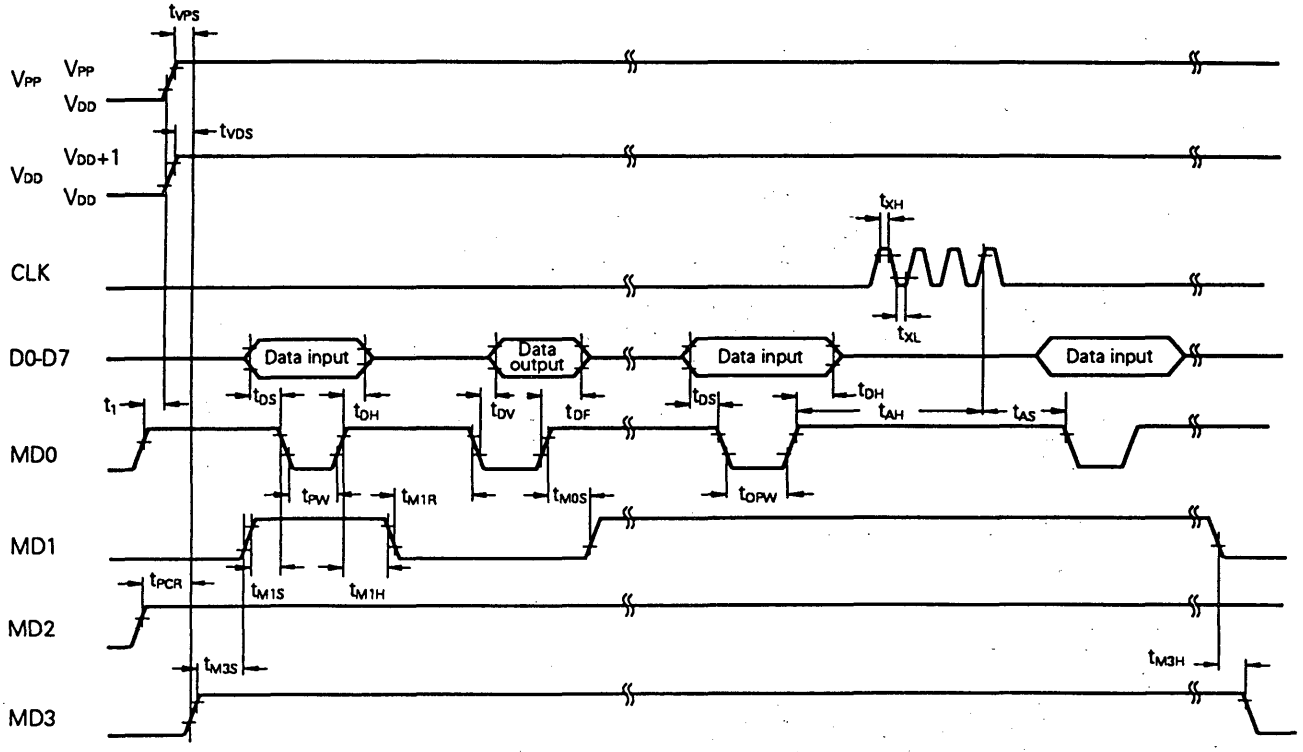
2. Apply V_{DD} before V_{PP} and turn it off after V_{PP}.

AC Programming Characteristics (T_a = 25°C, V_{DD} = 6.0±0.25 V, V_{PP} = 12.5±0.5 V)

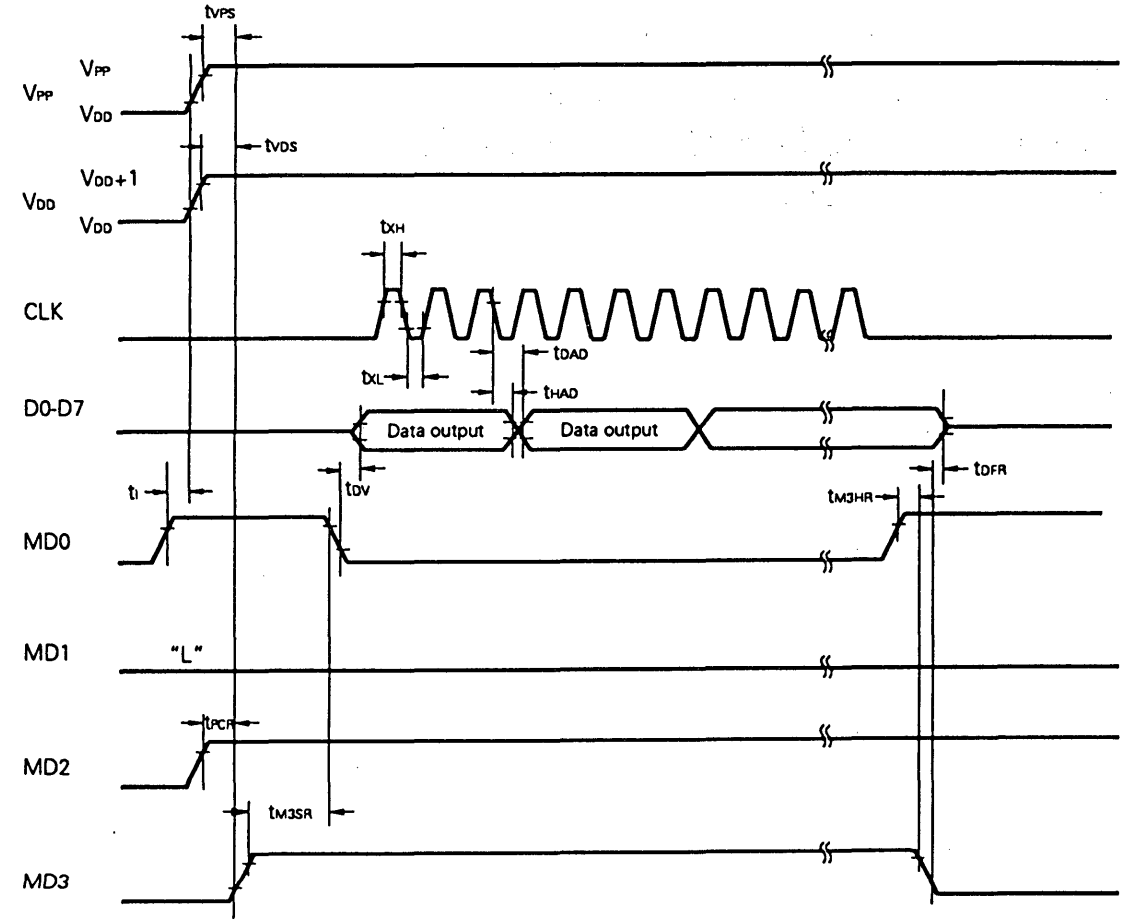
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address Setup Time* (vs. MD0↓)	t_{AS}		2			μs
MD1 Setup Time (vs. MD0↓)	t_{M1S}		2			μs
Data Setup Time (vs. MD0↓)	t_{DS}		2			μs
Address Hold Time* (vs. MD0↑)	t_{AH}		2			μs
Data Hold Time (vs. MD0↑)	t_{DH}		2			μs
MD0↑→ Data Output Float Delay Time	t_{DF}		0		130	ns
V_{PP} Setup Time (vs. MD3↑)	t_{VPS}		2			μs
V_{DD} Setup Time (vs. MD3↑)	t_{VDS}		2			μs
Initial Program Pulse Width	t_{PW}		0.95	1.0	1.05	ms
Additional Program Pulse Width	t_{OPW}		0.95		21.0	ms
MD0 Setup Time (vs. MD1↑)	t_{M0S}		2			μs
MD0↓→ Data Output Delay Time	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 Hold Time (vs. MD0↑)	t_{M1H}	$t_{M1H} + t_{M1R} \geq 50$ μs	2			μs
MD1 Recovery Time (vs. MD0↓)	t_{M1R}		2			μs
Program Counter Reset Time	t_{PCR}		10			μs
CLK Input High-, Low-Level Width	t_{XH}, t_{XL}		0.125			μs
CLK Input Frequency	f_X				4.19	MHz
Initial Mode Set Time	t_I		2			μs
MD3 Setup Time (vs. MD1↑)	t_{M3S}		2			μs
MD3 Hold Time (vs. MD1↓)	t_{M3H}		2			μs
MD3 Setup Time (vs. MD0↓)	t_{M3SR}	Program memory read	2			μs
Address*→Data Output Delay Time	t_{DAD}	Program memory read	2			μs
Address*→Data Output Hold Time	t_{HAD}	Program memory read	0		130	ns
MD3 Hold Time (vs. MD0↑)	t_{M3HR}	Program memory read	2			μs
MD3↓→ Data Output Float Delay Time	t_{DFR}	Program memory read	2			μs

*: The internal address signal is incremented (+1) at the falling edge of thernal address signal is incremented (+1) at the falling edge of the third CLK signal (with one cycle consisting of four clocks). The internal address is not connected to a pin.

Program memory write timing

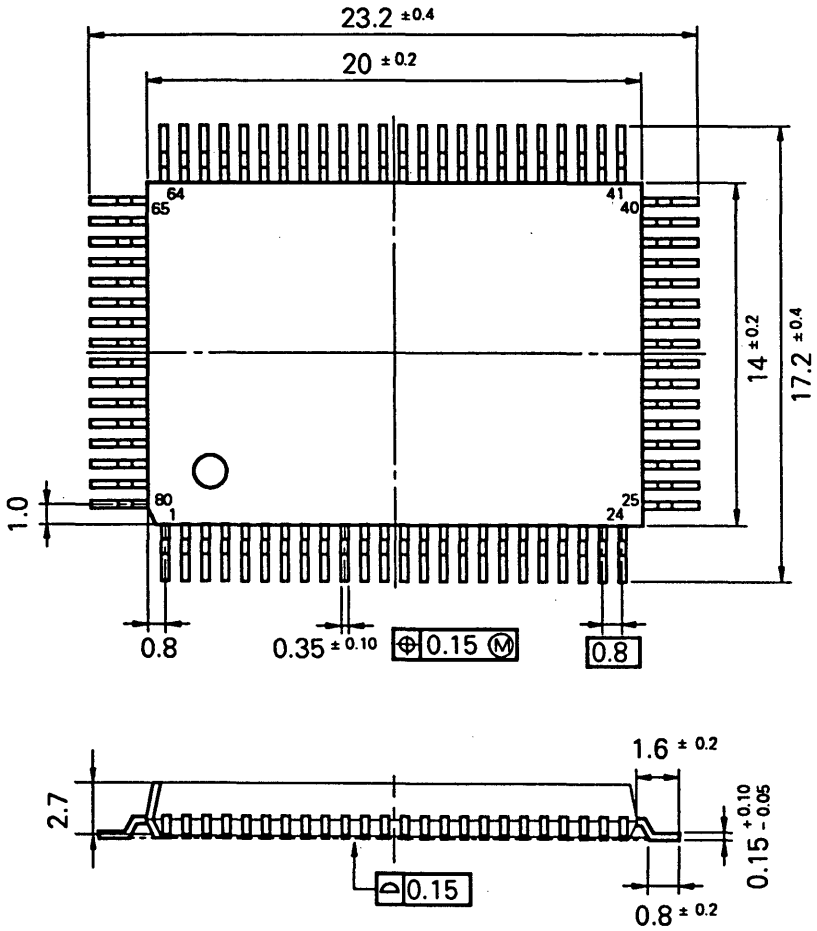


Program memory read timing

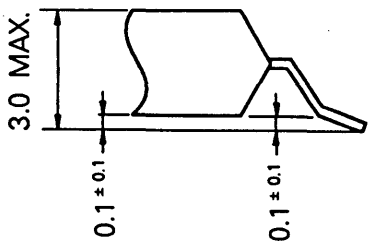


5. PACKAGE DRAWINGS

80-Pin Plastic QFP (14 × 20) (Unit: mm)



Details of tip of pin



6. RECOMMENDED SOLDERING CONDITIONS

The μPD17P005 should be soldered under the following recommended conditions. For soldering conditions other than those recommended below, consult NEC.

Table 6-1 List of Recommended Soldering Conditions

PRODUCT NAME	PACKAGE	CODE
μPD17P005GF-3B9 μPD17P005GF-E00-3B9 μPD17P005GF-xxx-3B9	80-pin plastic QFP (14 × 20 mm)	·IR30-162 ·VP15-162 ·WS60-162 ·Pin partial heating

Table 6-2 Soldering Conditions

CODE	SOLDERING METHOD	SOLDERING CONDITIONS
IR30-162	Infrared reflow	Package peak temperature: 230°C, Time: 30 seconds max. (210°C min.), Number of times: 1, Number of days*: 2 (after this, prebaking is necessary at 125°C for 16 hours)
VP15-162	VPS	Package peak temperature: 215°C, Time: 40 seconds max. (200°C min.), Number of times: 1, Number of days*: 2 (after this, prebaking is necessary at 125°C for 16 hours)
WS60-162	Wave soldering	Soldering oven temperature: 260°C max., Time: 10 seconds max., Number of times: 1, Number of days*: 2 (after this, prebaking is necessary at 125°C for 16 hours)
Pin partial heating	Pin partial heating	Pin temperature: 300°C max., Time: 10 seconds max.

*: The number of days the device can be stored after the dry pack has been opened. The storing conditions are 25°C, 65% RH max.

Note: Do not use two or more soldering methods in combination (except for the pin partial heating method).

Remarks: For details of the recommended soldering conditions, refer to **"Semiconductor Device Mounting Manual" (IEI-616).**

APPENDIX DEVELOPMENT TOOLS

The following development tools are readily available to support the development of the μPD17P005 program:

Hardware

NAME	OUTLINE	ORDER CODE
In-circuit Emulator	This in-circuit emulator is used in common with the 17K series products. When developing the program of μPD17P005, a system evaluation board (SE board) is used in combination with the in-circuit emulator. The in-circuit emulator operates with a RAM base. By connecting it to a console, the program can be added to and edited on the console. In addition, more sophisticated program development environments can be created by using the support software SIMPLEHOST™.	IE-17K IE-17K-ET*
SE board	Used to evaluate the system of μPD17P005 in stand-alone mode, or in combination with the in-circuit emulator.	SE-17010
Emulation Probe	Connects the SE board to the target system.	EP-17003GF
Conversion socket	Connects to the target system in combination with the emulation probe.	EV-9200G-80
PROM programmer	The PROM of the μPD17P005 can be programmed by using a dedicated program adapter AF-9803.	AF-9703 AF-9704 (Ando Electric)
Program adapter	Used in combination with the PROM programmer.	AF-9803 (Ando Electric)

Remarks: For the details of the PROM programmer and program adapter, consult Ando Electric.

*: Low-cost model: with external power supply

Software

NAME	OUTLINE	HOST MACHINE	OS		SUPPLY MEDIA	ORDER CODE
17K series assembler	AS17K is an assembler that can be used in common with the 17K series products. When developing the program of the μPD17P005, AS17K is used in combination with a device file (AS17005).	PC-9800 series	MS-DOS™ (Ver.3.1 to Ver.3.30C)		5"2HD	μS5A10AS17K
					3.5"2HD	μS5A13AS17K
		IBM PC/AT™	PC DOS™ (Ver. 3.1)		5"2HC	μS7B10AS17K
Device file (AS17005)	AS17005 is a device file for μPD17005 and μPD17P005, and is used in combination with an assembler for the 17K series (AS17K).	PC-9800 series	MS-DOS (Ver.3.1 to Ver.3.30C)		5"2HD	μS5A10AS17005
					3.5"2HD	μS5A13AS17005
		IBM PC/AT	PC DOS (Ver. 3.1)		5"2HC	μS7B10AS17005
Support software (SIMPLEHOST)	SIMPLEHOST is a software package that enables man-machine interface in MS-WINDOWS™ when a program is developed by using an in-circuit emulator and a personal computer.	PC-9800 series	MS-DOS (Ver. 3.1 to Ver. 3.30C)	MS-WINDOWS (Ver. 2.1 to Ver. 3.0)	5"2HD	μS5A10IE17K
					3.5"2HD	μS5A13IE17K
		IBM PC/AT	PCDOS (Ver. 3.1)		5"2HC	μS7B10IE17K

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PC/AT™ and PC DOS™ are trademarks of IBM Corporation.

[MEMO]

Note: Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2 system, provided that the system comforms to the I^2C Standard Specification as defined by Philips.