To our customers,

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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS INTEGRATED CIRCUIT

# μPD16335

## 96-Bit AC-PDP DRIVER

The μPD16335 is a high-voltage CMOS driver designed for flat display panels such as PDPs, VFDs and ELs. It consists of a 96-bit bi-directional shift register, 96-bit latch and high-voltage CMOS driver. The logic block is designed to operate using a 5-V power supply enabling direct connection to a gate array or a microcontroller. In addition, the μPD16335 achieves low power dissipation by employing CMOS structure while having a high withstand voltage output (80 V, +50/–75 mA).

### FEATURES

- Selectable by IBS pin; three 32-bit bi-directional shift register circuits configuration or six 16-bit bi-directional shift register circuits configuration
- Data control with transfer clock (external) and latch
- High-speed data transfer ($f_{max.}$ = 25 MHz min. at data fetch)
  ($f_{max.}$ = 16 MHz min. at cascade connection)
- High withstand output voltage (80 V, +50/–75 $mA_{MAX.}$)
- 5 V CMOS input interface
- High withstand voltage CMOS structure
- Capable of reversing all driver outputs by $\overline{PC}$ pin

### ORDERING INFORMATION

| Part Number | Package |
|---|---|
| μPD16335 | COB**Note** |

**Note** Please consult with an NEC sales representative about COB.

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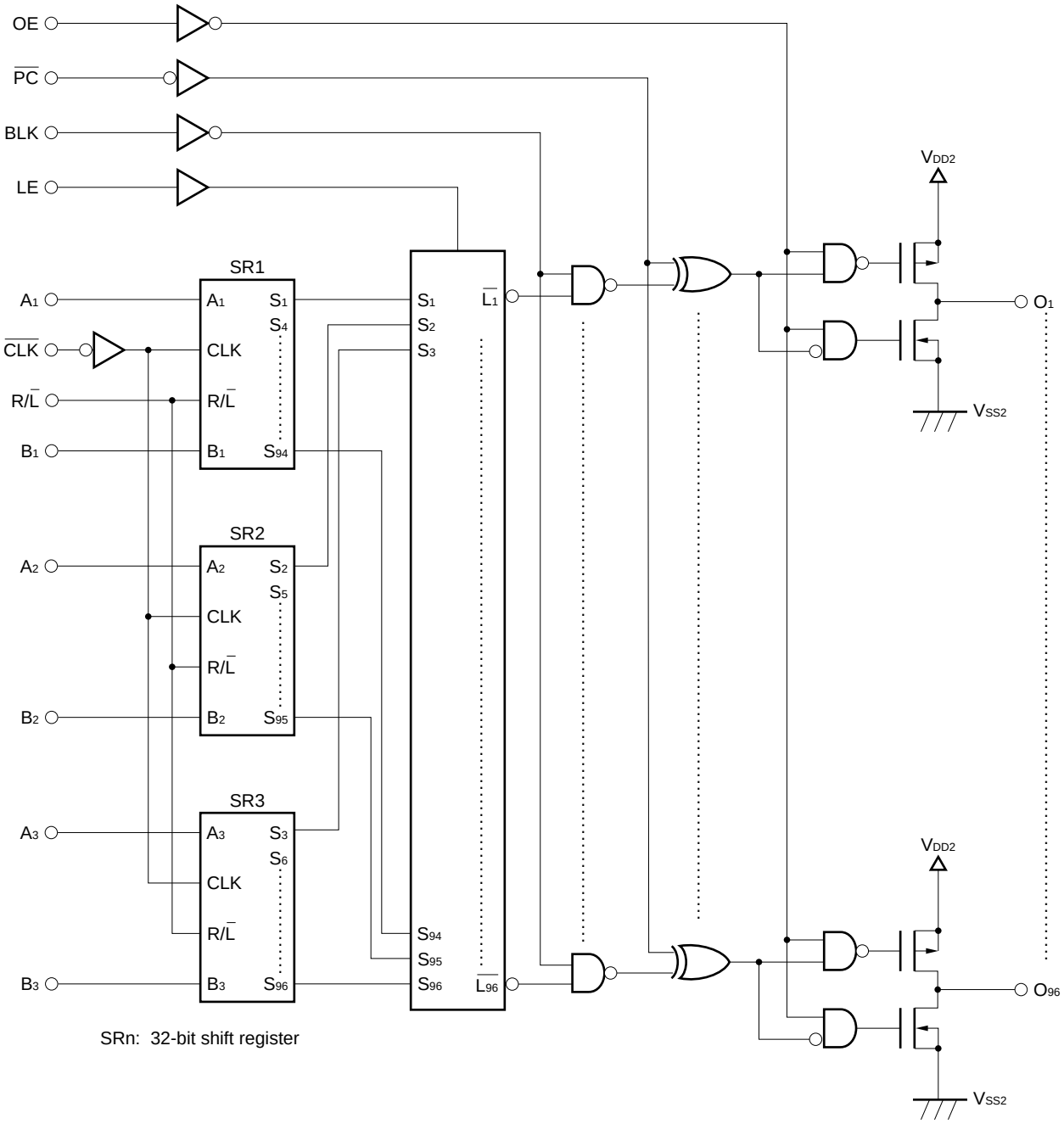
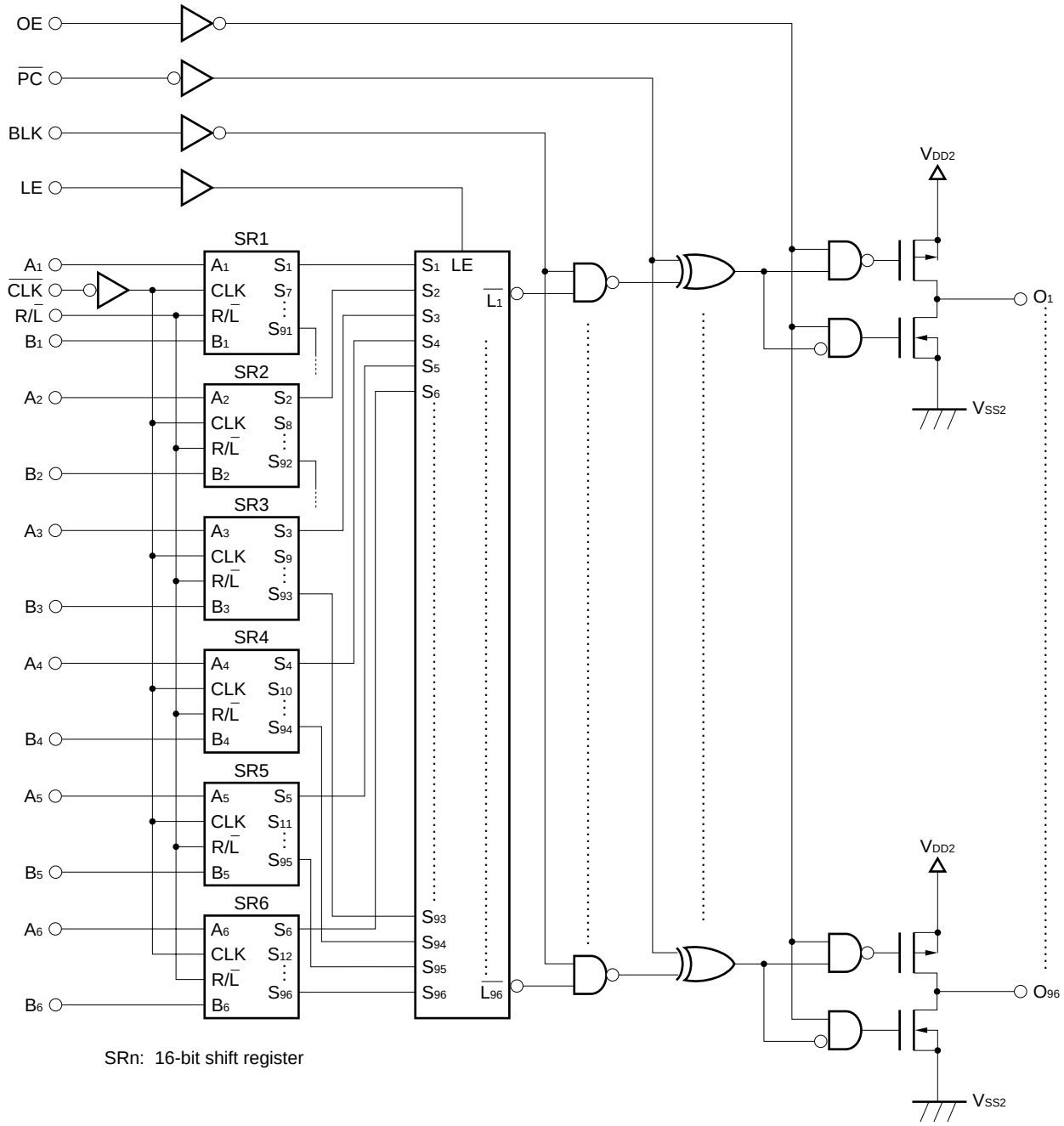
## BLOCK DIAGRAM (IBS = H, 3-BIT INPUT, 32-BIT LENGTH SHIFT REGISTER)




SRn: 32-bit shift register

## BLOCK DIAGRAM (IBS = L, 6-BIT INPUT, 16-BIT LENGTH SHIFT REGISTER)




SRn: 16-bit shift register

## PIN DESCRIPTION

| Symbol | Pin Name | Description |
|---|---|---|
| $\overline{PC}$ | Polarity change input | $\overline{PC}$ = L: All driver output invert |
| BLK | Blank input | BLK = H: All output = H or L |
| LE | Latch enable input | Data latch by rising edge of this signal. |
| OE | Output enable | Make output high impedance by input H |
| $A_1$ to $A_{3\,(6)}$ | RIGHT data input/output[Note] | When R/$\overline{L}$ = H (values in parentheses are for 6-bit input)<br>$A_1$ to $A_{3\,(6)}$: Input $B_1$ to $B_{3\,(6)}$: Output |
| $B_1$ to $B_{3\,(6)}$ | LEFT data input/output[Note] | When R/$\overline{L}$ = L (values in parentheses are for 6-bit input)<br>$A_1$ to $A_{3\,(6)}$: Output $B_1$ to $B_{3\,(6)}$: Input |
| $\overline{CLK}$ | Clock input | Shift executed on fall |
| R/$\overline{L}$ | Shift control input | Right shift mode when R/L = H<br>$SR_1$: A1 → $S_1$ ⋯ $S_{94}$ → B1 (Same direction for $SR_2$ to $SR_6$)<br>Left shift mode when R/L = L<br>$SR_1$: $B_1$ → $S_{94}$ ⋯ $S_1$ → $A_1$ (Same direction for $SR_2$ to $SR_6$) |
| IBS | Input mode switch | H: 32-bit length shift register, 3-bit input<br>L: 16-bit length shift register, 6-bit input |
| $O_1$ to $O_{96}$ | High withstand voltage output | 80 V, +50/–75 mA MAX. |
| $V_{DD1}$ | Power supply for logic block | 5 V ±10% |
| $V_{DD2}$ | Power supply for driver block | 10 to 70 V |
| $V_{SS1}$ | Logic GND | Connect to system GND |
| $V_{SS2}$ | Driver GND | Connect to system GND |

**Note** When input mode is 3-bit, set unused input and output pins "L" level.

## TRUTH TABLE 1 (Shift Register Block)

| Input | | Output | | Shift Register |
|---|---|---|---|---|
| R/$\overline{L}$ | $\overline{CLK}$ | A | B | |
| H | ↓ | Input | Output[Note 1] | Right shift execution |
| H | H or L | | Output | Hold |
| L | ↓ | Output[Note 2] | Input | Left shift execution |
| L | H or L | Output | | Hold |

**Notes 1.** The data of $S_{91}$ to $S_{93}$ ($S_{85}$ to $S_{90}$) shifts to $S_{94}$ to $S_{96}$ ($S_{91}$ to $S_{96}$) and is output from $B_1$ to $B_3$ ($B_1$ to $B_6$) at the falling edge of the clock, respectively. (Values in parentheses are for 6-bit input)

**2.** The data of $S_4$ to $S_6$ ($S_7$ to $S_{12}$) shifts to $S_1$ to $S_3$ ($S_1$ to $S_6$) and is output from $A_1$ to $A_3$ ($A_1$ to $A_6$) at the falling edge of the clock, respectively (Values in parentheses are for 6-bit input)

## TRUTH TABLE 2 (Latch Block)

| LE | Output State of Latch Block ($\overline{L_n}$) |
|---|---|
| ↑ | Latch Sn data |
| H or L | Hold latch data |

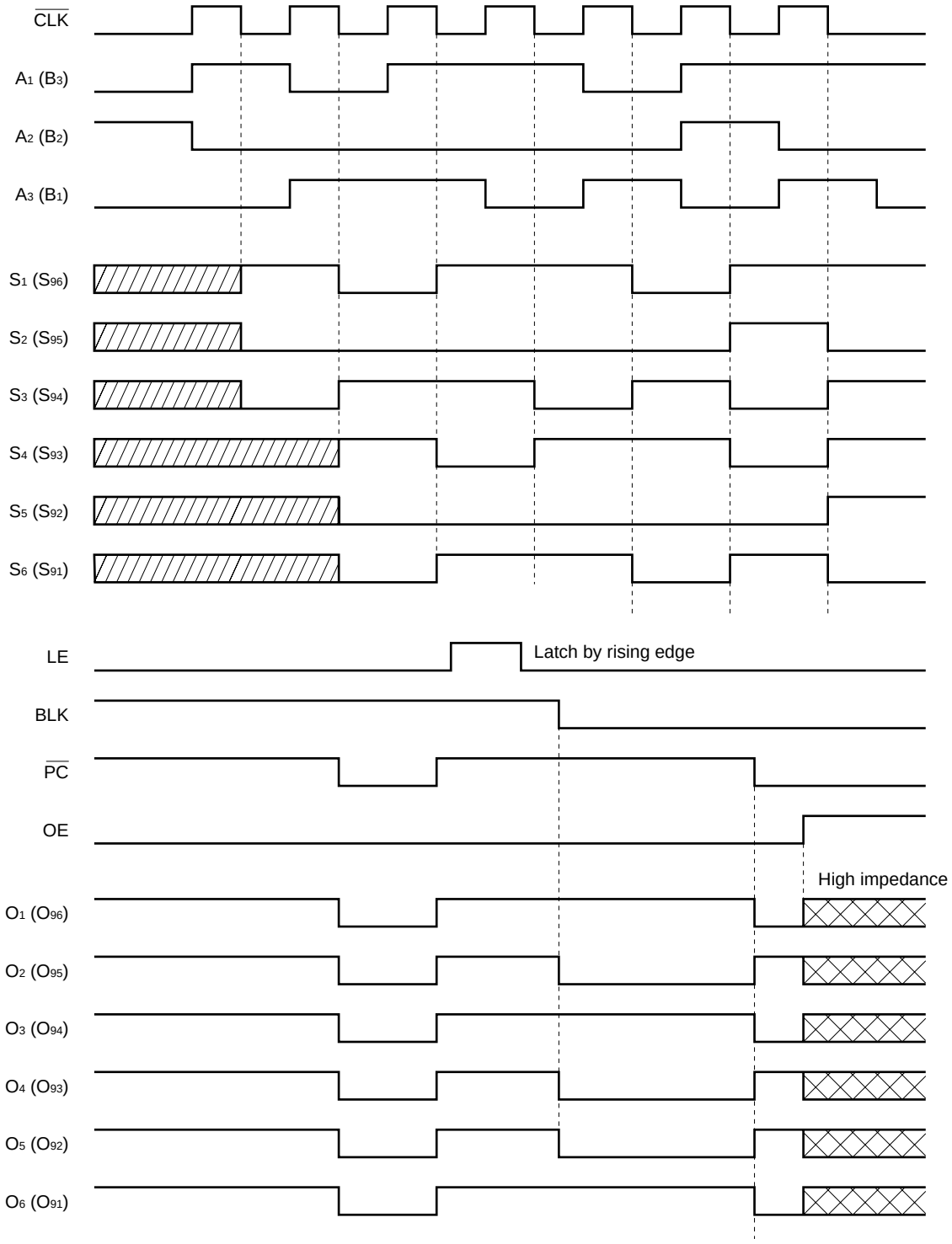
## TRUTH TABLE 3 (Driver Block)

| $\overline{L_n}$ | BLK | $\overline{PC}$ | OE | Output State of Driver Block |
|---|---|---|---|---|
| X | H | H | L | H (All driver outputs: H) |
| X | H | L | L | L (All driver outputs: L) |
| X | L | H | L | Output latch data ($\overline{L_n}$) |
| X | L | L | L | Output inverted latch data ($\overline{L_n}$) |
| X | X | X | H | Set output impedance high |

X: H or L, H: High level, L: Low level

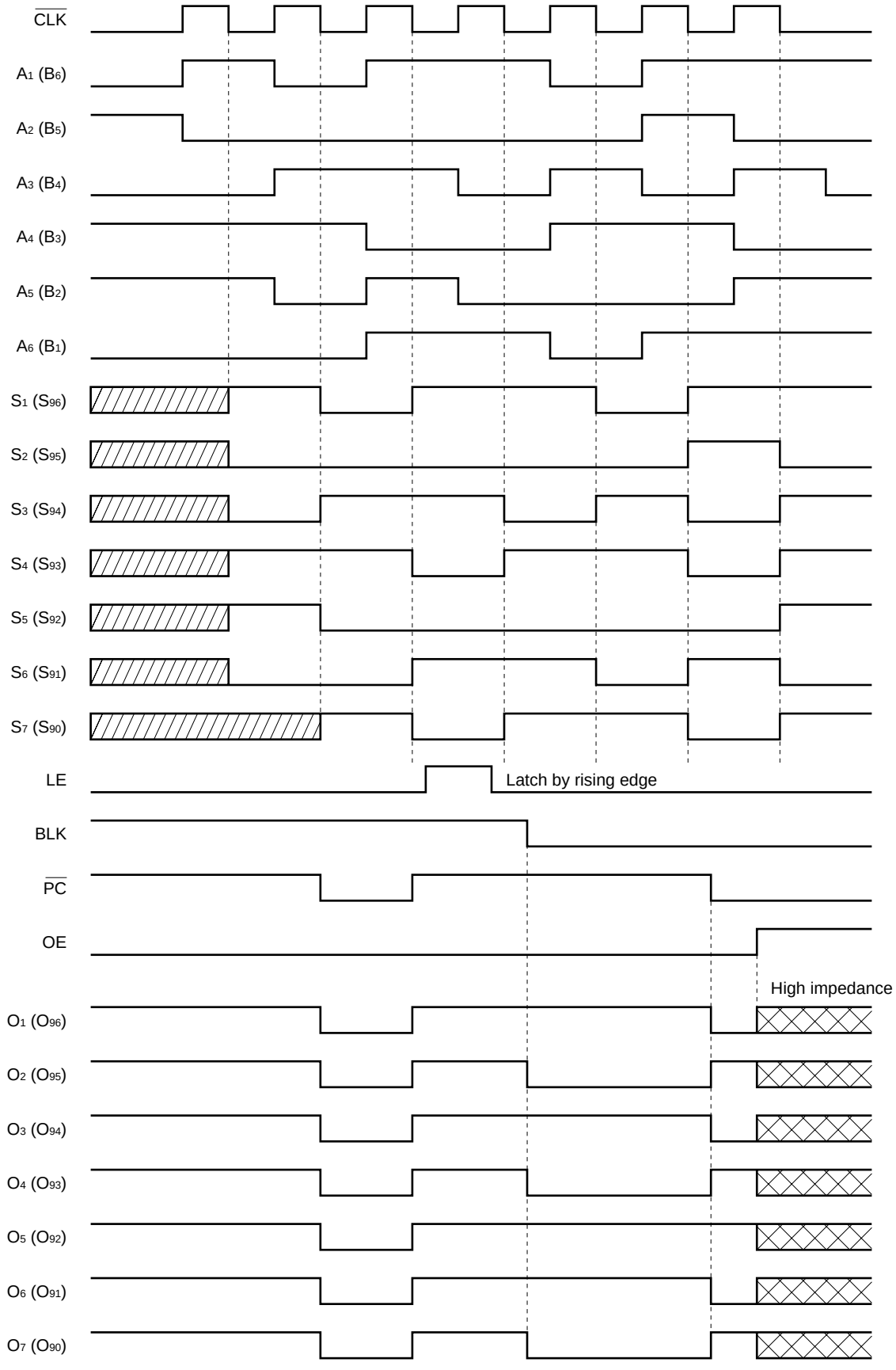
## TIMING CHART (WHEN IBS = "H": 3-BIT INPUT, RIGHT SHIFT)

Values in parentheses in the following chart are when R/$\overline{L}$ = L.



## TIMING CHART (WHEN IBS = "L": 6-BIT INPUT, RIGHT SHIFT)

Values in parentheses in the following chart are when R/$\overline{L}$ = L.



## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C, $V_{SS1}$ = $V_{SS2}$ = 0 V)

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Logic Block Supply Voltage | $V_{DD1}$ | –0.5 to +7.0 | V |
| Driver Block Supply Voltage | $V_{DD2}$ | –0.5 to +80 | V |
| Logic Block Input Voltage | $V_I$ | –0.5 to $V_{DD1}$ +0.5 | V |
| Driver Block Output Current | $I_{O2}$ | +50/–75 | mA |
| Junction Temperature | $T_j$ | ±125 | °C |
| Storage Temperature | $T_{stg.}$ | –65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS ($T_A$ = –40 to +85°C, $V_{SS1}$ = $V_{SS2}$ = 0 V)

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| Logic Block Supply Voltage | $V_{DD1}$ | 4.5 | 5.0 | 5.5 | V |
| Driver Block Supply Voltage | $V_{DD2}$ | 10 | | 70 | V |
| High-Level Input Voltage | $V_{IH}$ | 0.7 $V_{DD1}$ | | $V_{DD1}$ | V |
| Low-Level Input Voltage | $V_{IL}$ | 0 | | 0.2 $V_{DD1}$ | V |
| Driver Output Current | $I_{OH2}$ | | | –60 | mA |
| | $I_{OL2}$ | | | +40 | mA |

**Caution In order to prevent latch-up breakage, be sure to enter the power to $V_{DD1}$, logic signal and $V_{DD2}$ in that order, and turn off the power in the reverse order, keep this order also during a transition period.**

## ELECTRICAL SPECIFICATIONS ($T_A$ = 25°C, $V_{DD1}$ = 5.0 V, $V_{DD2}$ = 70 V, $V_{SS1}$ = $V_{SS2}$ = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| High-Level Output Voltage | $V_{OH1}$ | Logic, $I_{OH1}$ = –1.0 mA | 0.9 $V_{DD1}$ | | $V_{DD1}$ | V |
| Low-Level Output Voltage | $V_{OL1}$ | Logic, $I_{OL1}$ = 1.0 mA | 0 | | 0.1 $V_{DD1}$ | V |
| High-Level Output Voltage | $V_{OH21}$ | $O_1$ to $O_{96}$, $I_{OH2}$ = –1.3 mA | 69 | | | V |
| | $V_{OH22}$ | $O_1$ to $O_{96}$, $I_{OH2}$ = –13 mA | 65 | | | V |
| Low-Level Output Voltage | $V_{OL21}$ | $O_1$ to $O_{96}$, $I_{OL2}$ = 5 mA | | | 1.0 | V |
| | $V_{OL22}$ | $O_1$ to $O_{96}$, $I_{OL2}$ = 40 mA | | | 10 | V |
| Input Leakage Current | $I_{IL}$ | $V_I$ = $V_{DD1}$ or $V_{SS1}$ | | | ±1.0 | μA |
| High-Level Input Voltage | $V_{IH}$ | | 0.7 $V_{DD1}$ | | | V |
| Low-Level Input Voltage | $V_{IL}$ | | | | 0.2 $V_{DD1}$ | V |
| Static Current Dissipation | $I_{DD1}$ | Logic, $T_A$ = –40 to +85° | | | 100 | μA |
| | $I_{DD1}$ | Logic, $T_A$ = 25°C | | | 10 | μA |
| | $I_{DD2}$ | Driver, $T_A$ = –40 to +85° | | | 1000 | μA |
| | $I_{DD2}$ | Driver, $T_A$ = 25°C | | | 100 | μA |

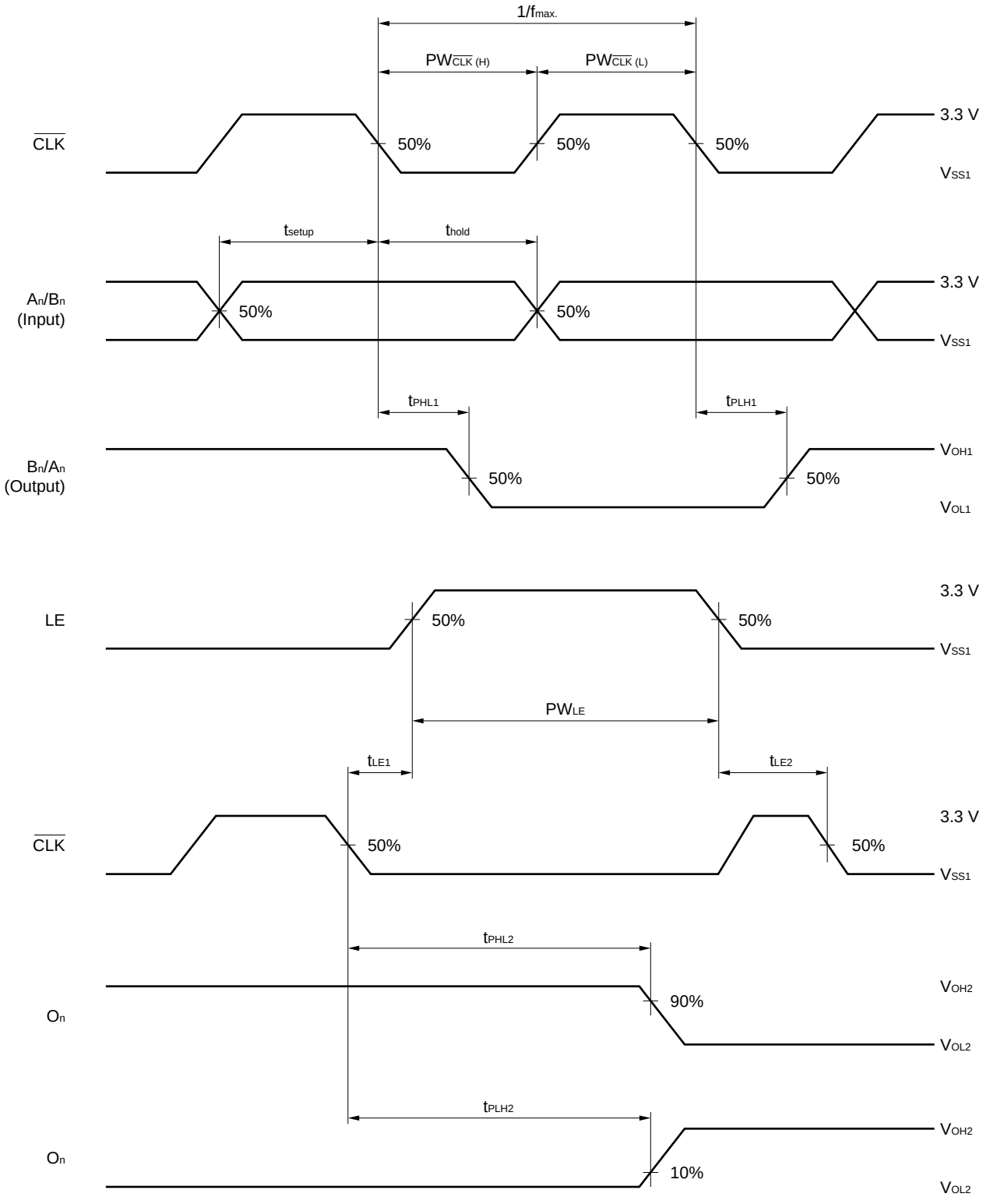
**SWITCHING CHARACTERISTICS ($T_A$ = 25°C, $V_{DD1}$ = 5.0 V, $V_{DD2}$ = 130 V, $V_{SS1}$ = $V_{SS2}$ = 0 V, logic $C_L$ = 15 pF, driver $C_L$ = 50 pF, $t_r$ = $t_f$ = 6.0 ns)**

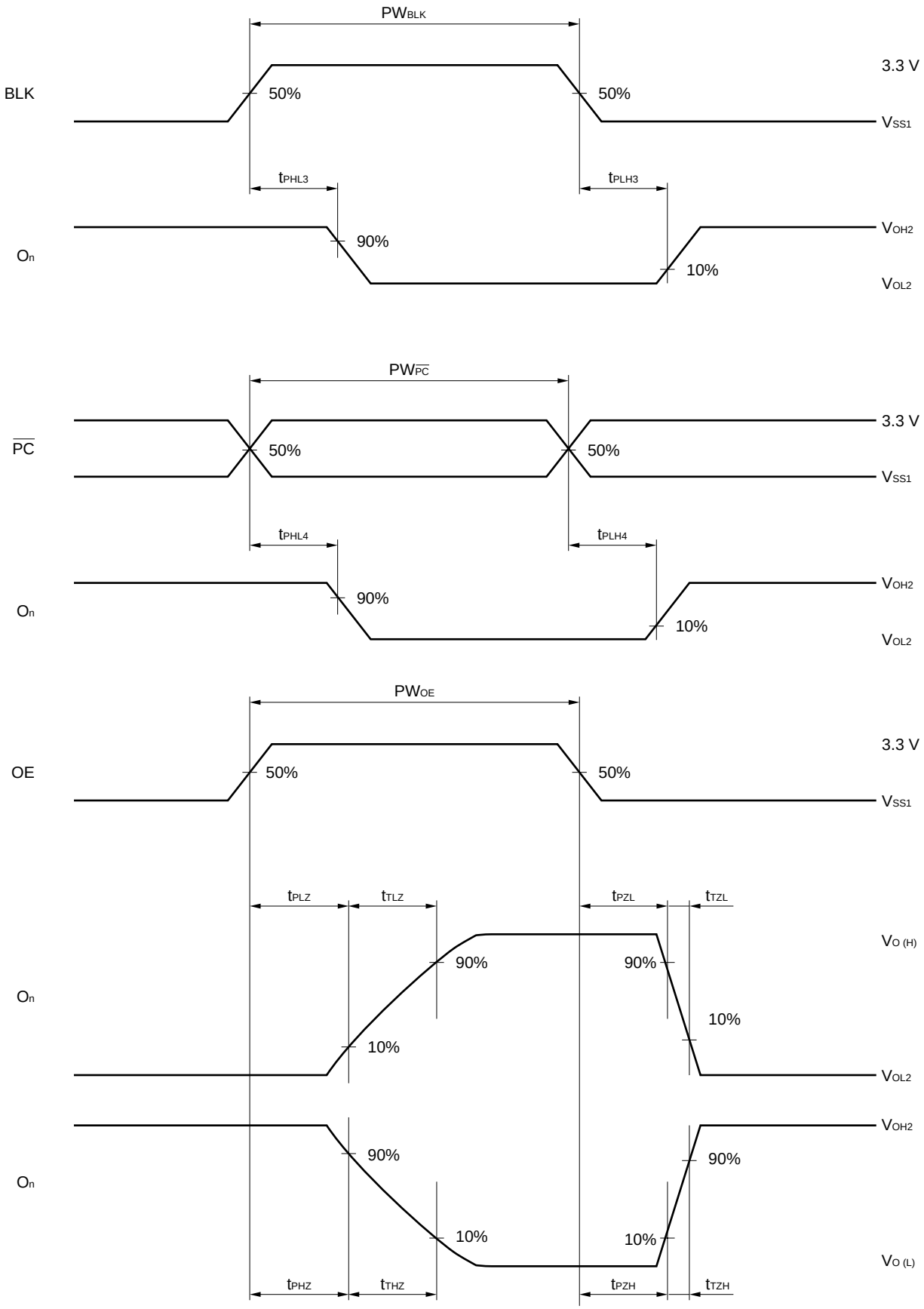
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transmission Delay Time | $t_{PHL1}$ | $\overline{CLK} \downarrow \rightarrow$ A/B | | | 55 | ns |
| | $t_{PLH1}$ | | | | 55 | ns |
| | $t_{PHL2}$ | $\overline{CLK} \uparrow$ (LE = H) $\rightarrow O_1$ to $O_{96}$ | | | 180 | ns |
| | $t_{PLH2}$ | | | | 180 | ns |
| | $t_{PHL3}$ | BLK $\rightarrow O_1$ to $O_{96}$ | | | 165 | ns |
| | $t_{PLH3}$ | | | | 165 | ns |
| | $t_{PHL4}$ | $\overline{PC} \rightarrow O_1$ to $O_{96}$ | | | 160 | ns |
| | $t_{PLH4}$ | | | | 160 | ns |
| | $t_{PHZ}$ | OE $\rightarrow O_1$ to $O_{96}$ | | | 300 | ns |
| | $t_{PZH}$ | RL = 10 kΩ | | | 180 | ns |
| | $t_{PLZ}$ | | | | 300 | ns |
| | $t_{PZL}$ | | | | 180 | ns |
| Rise Time | $t_{TLH}$ | $O_1$ to $O_{96}$ | | | 120 | ns |
| | $t_{TLZ}$ | RL = 10 kΩ | | | 3 | μs |
| | $t_{TZH}$ | $O_1$ to $O_{96}$ | | | 120 | ns |
| Fall Time | $t_{THL}$ | $O_1$ to $O_{96}$ | | | 150 | ns |
| | $t_{THZ}$ | RL = 10 kΩ | | | 3 | μs |
| | $t_{TZL}$ | $O_1$ to $O_{96}$ | | | 150 | ns |
| Maximum Clock Frequency | $f_{max.}$ | When data is read, duty 50% | 25 | | | MHz |
| | | cascade connection, Duty 50% | 16 | | | MHz |
| Input Capacitance | $C_I$ | | | | 15 | pF |

**TIMING REQUIREMENT ($T_A$ = –40 to +85°C, $V_{DD1}$ = 4.5 to 5.5 V, $V_{SS1, 2}$ = 0 V, $t_r$ = $t_f$ = 6.0 ns)**

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Clock Pulse Width | $PW_{\overline{CLK}}$ | | 20 | | | ns |
| Latch Enable Pulse Width | $PW_{LE}$ | | 20 | | | ns |
| Blank Pulse Width | $PW_{BLK}$ | | 200 | | | ns |
| $\overline{PC}$ Pulse Width | $PW_{\overline{PC}}$ | | 200 | | | ns |
| OE Pulse Width | $PW_{OE}$ | $R_L$ = 10 kΩ | 3.3 | | | μs |
| Data Setup Time | $t_{setup}$ | | 7 | | | ns |
| Data Hold Time | $t_{hold}$ | | 10 | | | ns |
| Latch Enable Time 1 | $t_{LE1}$ | | 20 | | | ns |
| Latch Enable Time 2 | $t_{LE2}$ | | 20 | | | ns |

## SWITCHING CHARACTERISTICS WAVEFORM




PWBLK
BLK
3.3 V
50%
50%
VSS1
tPHL3
tPLH3
On
90%
10%
VOH2
VOL2
PWPC
PC
3.3 V
50%
50%
VSS1
tPHL4
tPLH4
On
90%
10%
VOH2
VOL2
PWOE
OE
3.3 V
50%
50%
VSS1
tPLZ
tTLZ
tPZL
tTZL
VO (H)
On
90%
90%
10%
10%
VOL2
VOH2
On
90%
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10%
VO (L)
tPHZ
tTHZ
tPZH
tTZH

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