To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

RELIMINARY PRODUCT INFORMATION

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD161801

240 OUTPUTS TFT-LCD SOURCE DRIVER WITH RAM

DESCRIPTION

The μPD161801 is a TFT-LCD source driver that includes display RAM

This driver has 240 outputs, a display RAM capacity of 172.8 K bytes (240 pixels x 18 bits x 320 lines) and can provide a 262,144-color display.

FEATURES

- TFT-LCD driver with on-chip display RAM
- Logic power supply voltage: 1.6 to 2.7 V (Can also be generated within chip from power IC interface's power supply)
- CPU/RGB interface voltage: 1.8 to V_{DD}
- Power supply IC interface power supply voltage: 2.5 to 3.3 V
- Driver power supply voltage: 4.0 to 5.5 V
- Display RAM: 240 x 18 x 320 bits
- Driver outputs: 240 outputs
- CPU interface: Three types of interfaces selectable
  - 6-bit/16-bit/18-bit RGB interface (through mode, capture mode)
  - i80/M68 parallel interface (selectable from 8/16/18-bit)
  - 8-bit serial interface
- Colors: 262,144 colors/pixel
- On-chip timing generator
- On-chip oscillator

ORDERING INFORMATION

Part Number	Package
μPD161801P	Chip

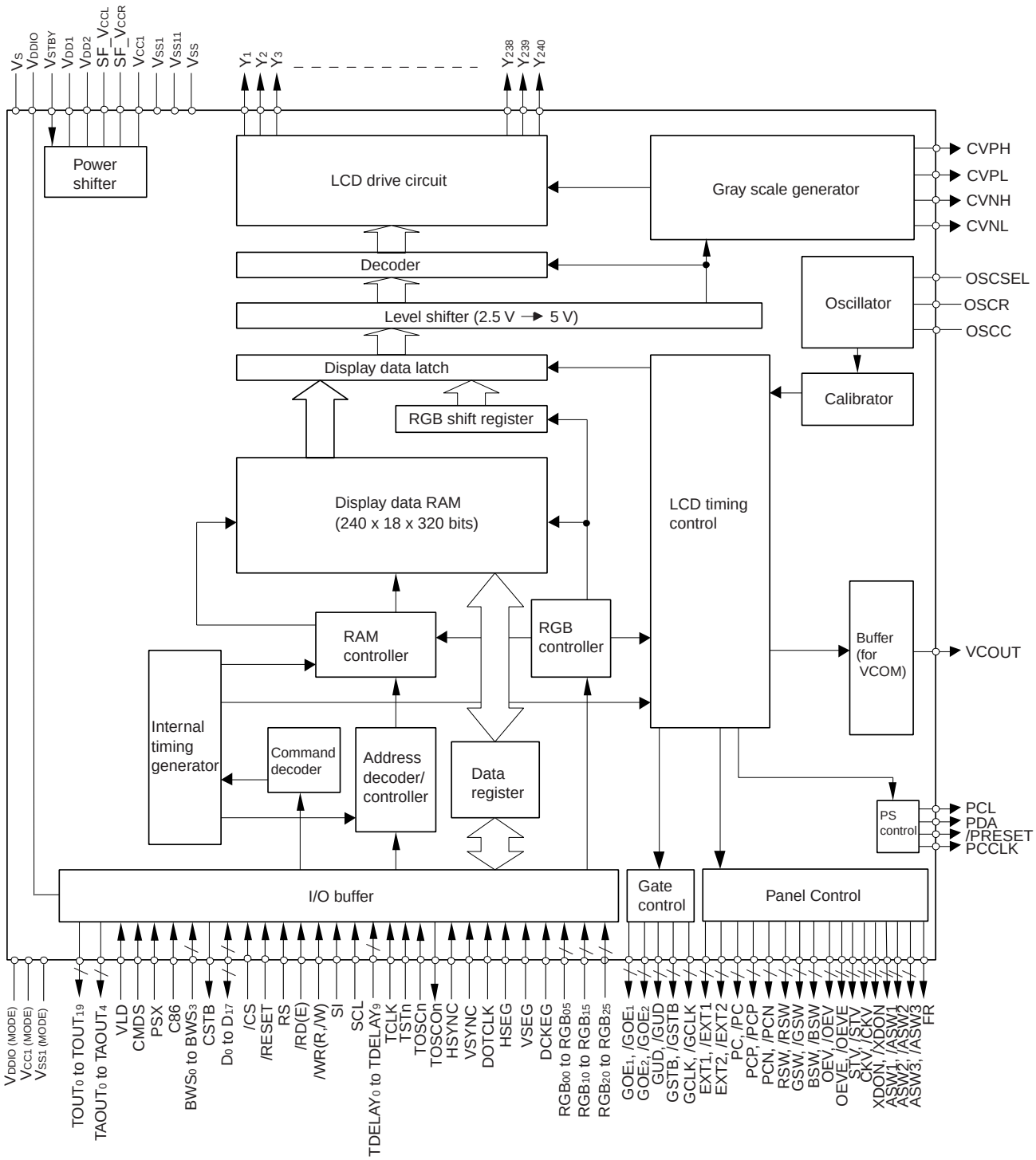
Remark Purchasing the above chip entails the exchange of documents such as a separate memorandum on product quality, so please contact one of our sales representatives.

Document No. S16650EJ2V0PM00 (2nd edition)
Date Published September 2003 NS CP(K)
Printed in Japan

The mark ★ shows major revised points.

CONTENTS

1. BLOCK DIAGRAM

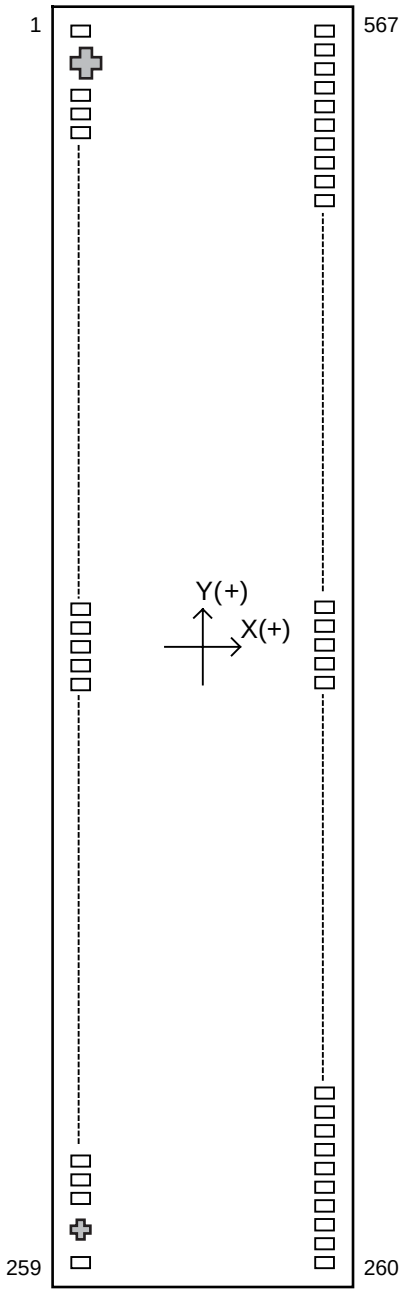


Remark /xxx indicates active low signal.

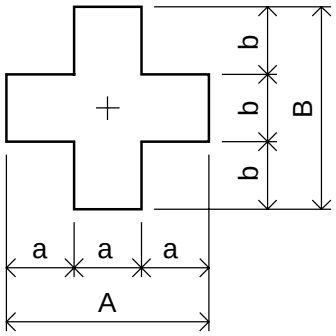
2. PIN CONFIGURATION (Pad Layout)

Chip size: 2.93 x 18.70 mm^2 (TYP.)

Bump size: 30 x 100 μm^2 (TYP.)



<Alignment Mark>



Alignment mark coordinate (mark center, unit: μm)

	X	Y
M1	−1317.00	9050.00
M2	−1317.00	−9020.00

Alignment shape of mark (unit: μm)

A	a	B	b
90	30	90	30

Table 2–1. Pad Coordinate (1/5)

No.	Pin Name	I/O	Power	Pad coordinate [μm]	
				X	Y
1	DUMMY	–	–	-1317.00	9150.00
2	DUMMY	–	–	-1317.00	8950.00
3	DUMMY	–	–	-1317.00	8890.00
4	/PRESET	Output	VCC1	-1317.00	8830.00
5	ASW3	Output	VCC1	-1317.00	8770.00
6	/ASW3	Output	VCC1	-1317.00	8710.00
7	ASW2	Output	VCC1	-1317.00	8650.00
8	/ASW2	Output	VCC1	-1317.00	8590.00
9	ASW1	Output	VCC1	-1317.00	8530.00
10	/ASW1	Output	VCC1	-1317.00	8470.00
11	STV	Output	VCC1	-1317.00	8410.00
12	/STV	Output	VCC1	-1317.00	8350.00
13	CKV	Output	VCC1	-1317.00	8290.00
14	/CKV	Output	VCC1	-1317.00	8230.00
15	OEV	Output	VCC1	-1317.00	8170.00
16	/OEV	Output	VCC1	-1317.00	8110.00
17	OEVE	Output	VCC1	-1317.00	8050.00
18	/OEVE	Output	VCC1	-1317.00	7990.00
19	XDON	Output	VCC1	-1317.00	7930.00
20	/XDON	Output	VCC1	-1317.00	7870.00
21	BSW	Output	VCC1	-1317.00	7810.00
22	/BSW	Output	VCC1	-1317.00	7750.00
23	GSW	Output	VCC1	-1317.00	7690.00
24	/GSW	Output	VCC1	-1317.00	7630.00
25	RSW	Output	VCC1	-1317.00	7570.00
26	/RSW	Output	VCC1	-1317.00	7510.00
27	GSTB	Output	VCC1	-1317.00	7450.00
28	/GSTB	Output	VCC1	-1317.00	7390.00
29	GCLK	Output	VCC1	-1317.00	7330.00
30	/GCLK	Output	VCC1	-1317.00	7270.00
31	GOE2	Output	VCC1	-1317.00	7210.00
32	/GOE2	Output	VCC1	-1317.00	7150.00
33	GOE1	Output	VCC1	-1317.00	7090.00
34	/GOE1	Output	VCC1	-1317.00	7030.00
35	GUD	Output	VCC1	-1317.00	6970.00
36	/GUD	Output	VCC1	-1317.00	6910.00
37	VCOUT	Output	VCC1	-1317.00	6850.00
38	FR	Output	VCC1	-1317.00	6790.00
39	PDA	Output	VCC1	-1317.00	6730.00
40	PCS	Output	VCC1	-1317.00	6670.00
41	PCL	Output	VCC1	-1317.00	6610.00
42	PCCLK	Output	VCC1	-1317.00	6550.00
43	PCN	Output	VCC1	-1317.00	6490.00
44	/PCN	Output	VCC1	-1317.00	6430.00
45	PCP	Output	VCC1	-1317.00	6370.00
46	/PCP	Output	VCC1	-1317.00	6310.00
47	PC	Output	VCC1	-1317.00	6250.00
48	/PC	Output	VCC1	-1317.00	6190.00
49	EXT1	Output	VCC1	-1317.00	6130.00
50	/EXT1	Output	VCC1	-1317.00	6070.00
51	EXT2	Output	VCC1	-1317.00	6010.00
52	/EXT2	Output	VCC1	-1317.00	5950.00
53	VDDIO(MODE)	–	–	-1317.00	5890.00
54	CSTB	Output	VDDIO	-1317.00	5790.00
55	/RESET	Input	VDDIO	-1317.00	5690.00
56	D17	I/O	VDDIO	-1317.00	5590.00
57	D16	I/O	VDDIO	-1317.00	5490.00
58	D15	I/O	VDDIO	-1317.00	5390.00
59	D14	I/O	VDDIO	-1317.00	5290.00
60	D13	I/O	VDDIO	-1317.00	5190.00

No.	Pin Name	I/O	Power	Pad coordinate [μm]	
				X	Y
61	D12	I/O	VDDIO	-1317.00	5090.00
62	D11	I/O	VDDIO	-1317.00	4990.00
63	D10	I/O	VDDIO	-1317.00	4890.00
64	D9	I/O	VDDIO	-1317.00	4790.00
65	D8	I/O	VDDIO	-1317.00	4690.00
66	D7	I/O	VDDIO	-1317.00	4590.00
67	D6	I/O	VDDIO	-1317.00	4490.00
68	D5	I/O	VDDIO	-1317.00	4390.00
69	D4	I/O	VDDIO	-1317.00	4290.00
70	D3	I/O	VDDIO	-1317.00	4190.00
71	D2	I/O	VDDIO	-1317.00	4090.00
72	D1	I/O	VDDIO	-1317.00	3990.00
73	D0	I/O	VDDIO	-1317.00	3890.00
74	VSS1(MODE)	–	–	-1317.00	3790.00
75	/RD	Input	VDDIO	-1317.00	3690.00
76	/WR	Input	VDDIO	-1317.00	3590.00
77	RS	Input	VDDIO	-1317.00	3490.00
78	/CS	Input	VDDIO	-1317.00	3390.00
79	VDDIO(MODE)	–	–	-1317.00	3290.00
80	SI	Input	VDDIO	-1317.00	3190.00
81	SCL	Input	VDDIO	-1317.00	3090.00
82	VSS1(MODE)	–	–	-1317.00	2990.00
83	VLD	Input	VDDIO	-1317.00	2890.00
84	VDDIO(MODE)	–	–	-1317.00	2790.00
85	VSYNC	Input	VDDIO	-1317.00	2690.00
86	HSYNC	Input	VDDIO	-1317.00	2590.00
87	DOTCLK	Input	VDDIO	-1317.00	2490.00
88	VSS1(MODE)	–	–	-1317.00	2390.00
89	RGB00	Input	VDDIO	-1317.00	2290.00
90	RGB01	Input	VDDIO	-1317.00	2190.00
91	RGB02	Input	VDDIO	-1317.00	2090.00
92	RGB03	Input	VDDIO	-1317.00	1990.00
93	RGB04	Input	VDDIO	-1317.00	1890.00
94	RGB05	Input	VDDIO	-1317.00	1790.00
95	RGB10	Input	VDDIO	-1317.00	1690.00
96	RGB11	Input	VDDIO	-1317.00	1590.00
97	RGB12	Input	VDDIO	-1317.00	1490.00
98	RGB13	Input	VDDIO	-1317.00	1390.00
99	RGB14	Input	VDDIO	-1317.00	1290.00
100	RGB15	Input	VDDIO	-1317.00	1190.00
101	RGB20	Input	VDDIO	-1317.00	1090.00
102	RGB21	Input	VDDIO	-1317.00	990.00
103	RGB22	Input	VDDIO	-1317.00	890.00
104	RGB23	Input	VDDIO	-1317.00	790.00
105	RGB24	Input	VDDIO	-1317.00	690.00
106	RGB25	Input	VDDIO	-1317.00	590.00
107	VDDIO	–	–	-1317.00	290.00
108	VDDIO	–	–	-1317.00	230.00
109	VDDIO	–	–	-1317.00	170.00
110	VDDIO	–	–	-1317.00	110.00
111	VDDIO	–	–	-1317.00	50.00
112	VDDIO	–	–	-1317.00	-10.00
113	VCC1	–	–	-1317.00	-70.00
114	VCC1	–	–	-1317.00	-130.00
115	VCC1	–	–	-1317.00	-190.00
116	VCC1	–	–	-1317.00	-250.00
117	VCC1	–	–	-1317.00	-310.00
118	VCC1	–	–	-1317.00	-370.00
119	SF_VCCL	Output	VCC1	-1317.00	-430.00
120	SF_VCCL	Output	VCC1	-1317.00	-490.00

Table 2–1. Pad Coordinate (2/5)

No.	Pin Name	I/O	Power	Pad coordinate [μm]	
				X	Y
121	SF_VCCL	Output	VCC1	-1317.00	-550.00
122	SF_VCCL	Output	VCC1	-1317.00	-610.00
123	SF_VCCL	Output	VCC1	-1317.00	-670.00
124	SF_VCCL	Output	VCC1	-1317.00	-730.00
125	VDD1	–	–	-1317.00	-790.00
126	VDD1	–	–	-1317.00	-850.00
127	VDD1	–	–	-1317.00	-910.00
128	VDD1	–	–	-1317.00	-970.00
129	VDD1	–	–	-1317.00	-1030.00
130	VDD1	–	–	-1317.00	-1090.00
131	VDD1	–	–	-1317.00	-1150.00
132	VDD1	–	–	-1317.00	-1210.00
133	SF_VCCR	Output	VCC1	-1317.00	-1270.00
134	SF_VCCR	Output	VCC1	-1317.00	-1330.00
135	SF_VCCR	Output	VCC1	-1317.00	-1390.00
136	SF_VCCR	Output	VCC1	-1317.00	-1450.00
137	SF_VCCR	Output	VCC1	-1317.00	-1510.00
138	SF_VCCR	Output	VCC1	-1317.00	-1570.00
139	VDD2	–	–	-1317.00	-1630.00
140	VDD2	–	–	-1317.00	-1690.00
141	VDD2	–	–	-1317.00	-1750.00
142	VDD2	–	–	-1317.00	-1810.00
143	VDD2	–	–	-1317.00	-1870.00
144	VDD2	–	–	-1317.00	-1930.00
145	VDD2	–	–	-1317.00	-1990.00
146	VDD2	–	–	-1317.00	-2050.00
147	VSS1	–	–	-1317.00	-2110.00
148	VSS1	–	–	-1317.00	-2170.00
149	VSS1	–	–	-1317.00	-2230.00
150	VSS1	–	–	-1317.00	-2290.00
151	VSS1	–	–	-1317.00	-2350.00
152	VSS1	–	–	-1317.00	-2410.00
153	VSS1	–	–	-1317.00	-2470.00
154	VSS1	–	–	-1317.00	-2530.00
155	VSS11	–	–	-1317.00	-2590.00
156	VSS11	–	–	-1317.00	-2650.00
157	VSS11	–	–	-1317.00	-2710.00
158	VSS11	–	–	-1317.00	-2770.00
159	VSS11	–	–	-1317.00	-2830.00
160	VSS11	–	–	-1317.00	-2890.00
161	VSS11	–	–	-1317.00	-2950.00
162	VSS11	–	–	-1317.00	-3010.00
163	VSS11	–	–	-1317.00	-3070.00
164	VSS	–	–	-1317.00	-3130.00
165	VSS	–	–	-1317.00	-3190.00
166	VSS	–	–	-1317.00	-3250.00
167	VSS	–	–	-1317.00	-3310.00
168	VSS	–	–	-1317.00	-3370.00
169	VSS	–	–	-1317.00	-3430.00
170	TAOUT0	Output	VS	-1317.00	-3490.00
171	TAOUT1	Output	VS	-1317.00	-3550.00
172	TAOUT2	Output	VS	-1317.00	-3610.00
173	TAOUT3	Output	VS	-1317.00	-3670.00
174	TAOUT4	Output	VS	-1317.00	-3730.00
175	CVNL	I/O	VS	-1317.00	-3790.00
176	CVNL	I/O	VS	-1317.00	-3850.00
177	CVNL	I/O	VS	-1317.00	-3910.00
178	CVNH	I/O	VS	-1317.00	-3970.00
179	CVNH	I/O	VS	-1317.00	-4030.00
180	CVNH	I/O	VS	-1317.00	-4090.00

No.	Pin Name	I/O	Power	Pad coordinate [μm]	
				X	Y
181	CVPL	I/O	VS	-1317.00	-4150.00
182	CVPL	I/O	VS	-1317.00	-4210.00
183	CVPL	I/O	VS	-1317.00	-4270.00
184	CVPH	I/O	VS	-1317.00	-4330.00
185	CVPH	I/O	VS	-1317.00	-4390.00
186	CVPH	I/O	VS	-1317.00	-4450.00
187	VS	–	–	-1317.00	-4660.00
188	VS	–	–	-1317.00	-4720.00
189	VS	–	–	-1317.00	-4780.00
190	VS	–	–	-1317.00	-4840.00
191	VS	–	–	-1317.00	-4900.00
192	VS	–	–	-1317.00	-4960.00
193	OSCC	–	VDD1	-1317.00	-5020.00
194	OSCR	–	VDD1	-1317.00	-5080.00
195	VSS1(MODE)	–	–	-1317.00	-5140.00
196	OSCSEL	Input	VCC1	-1317.00	-5200.00
197	CMDS	Input	VCC1	-1317.00	-5260.00
198	VCC1(MODE)	–	–	-1317.00	-5320.00
199	HSEG	Input	VCC1	-1317.00	-5380.00
200	VSEG	Input	VCC1	-1317.00	-5440.00
201	VSS1(MODE)	–	–	-1317.00	-5500.00
202	DCKEG	Input	VCC1	-1317.00	-5560.00
203	PSX	Input	VCC1	-1317.00	-5620.00
204	VCC1(MODE)	–	–	-1317.00	-5680.00
205	C86	Input	VCC1	-1317.00	-5740.00
206	BWS0	Input	VCC1	-1317.00	-5800.00
207	VSS1(MODE)	–	–	-1317.00	-5860.00
208	BWS1	Input	VCC1	-1317.00	-5920.00
209	BWS2	Input	VCC1	-1317.00	-5980.00
210	VCC1(MODE)	–	–	-1317.00	-6040.00
211	BWS3	Input	VCC1	-1317.00	-6100.00
212	VSTBY	Input	VCC1	-1317.00	-6160.00
213	VSS1(MODE)	–	–	-1317.00	-6220.00
214	TOUT19	Output	VCC1	-1317.00	-6280.00
215	TOUT18	Output	VCC1	-1317.00	-6340.00
216	TOUT17	Output	VCC1	-1317.00	-6400.00
217	TOUT16	Output	VCC1	-1317.00	-6460.00
218	TOUT15	Output	VCC1	-1317.00	-6520.00
219	TOUT14	Output	VCC1	-1317.00	-6580.00
220	TOUT13	Output	VCC1	-1317.00	-6640.00
221	TOUT12	Output	VCC1	-1317.00	-6700.00
222	TOUT11	Output	VCC1	-1317.00	-6760.00
223	TOUT10	Output	VCC1	-1317.00	-6820.00
224	TOUT9	Output	VCC1	-1317.00	-6880.00
225	TOUT8	Output	VCC1	-1317.00	-6940.00
226	TOUT7	Output	VCC1	-1317.00	-7000.00
227	TOUT6	Output	VCC1	-1317.00	-7060.00
228	TOUT5	Output	VCC1	-1317.00	-7120.00
229	TOUT4	Output	VCC1	-1317.00	-7180.00
230	TOUT3	Output	VCC1	-1317.00	-7240.00
231	TOUT2	Output	VCC1	-1317.00	-7300.00
232	TOUT1	Output	VCC1	-1317.00	-7360.00
233	TOUT0	Output	VCC1	-1317.00	-7420.00
234	VSS1(MODE)	–	–	-1317.00	-7480.00
235	TDELAY0	Input	VCC1	-1317.00	-7540.00
236	TDELAY1	Input	VCC1	-1317.00	-7600.00
237	TDELAY2	Input	VCC1	-1317.00	-7660.00
238	TDELAY3	Input	VCC1	-1317.00	-7720.00
239	TDELAY4	Input	VCC1	-1317.00	-7780.00
240	TDELAY5	Input	VCC1	-1317.00	-7840.00

Table 2–1. Pad Coordinate (3/5)

No.	Pin Name	I/O	Power	Pad coordinate [μm]	
				X	Y
241	TDELAY6	Input	VCC1	-1317.00	-7900.00
242	TDELAY7	Input	VCC1	-1317.00	-7960.00
243	TDELAY8	Input	VCC1	-1317.00	-8020.00
244	TDELAY9	Input	VCC1	-1317.00	-8080.00
245	TCLK	Input	VCC1	-1317.00	-8140.00
246	TSTVIHL	Input	VCC1	-1317.00	-8200.00
247	TSTRTST	Input	VCC1	-1317.00	-8260.00
248	TOSCSEO1	Input	VCC1	-1317.00	-8320.00
249	TOSCSEO2	Input	VCC1	-1317.00	-8380.00
250	TOSCSEI1	Input	VCC1	-1317.00	-8440.00
251	TOSCSEI2	Input	VCC1	-1317.00	-8500.00
252	TOSCI1	Input	VCC1	-1317.00	-8560.00
253	TOSCI2	Input	VCC1	-1317.00	-8620.00
254	TOSCO1	Output	VCC1	-1317.00	-8680.00
255	TOSCO2	Output	VCC1	-1317.00	-8740.00
256	VSS1(MODE)	–	–	-1317.00	-8800.00
257	DUMMY	–	–	-1317.00	-8860.00
258	DUMMY	–	–	-1317.00	-8920.00
259	DUMMY	–	–	-1317.00	-9120.00
260	DUMMY	–	–	1317.00	-9210.00
261	DUMMY	–	–	1317.00	-9150.00
262	DUMMY	–	–	1317.00	-9090.00
263	Y1	Output	VS	1317.00	-9030.00
264	Y2	Output	VS	1317.00	-8970.00
265	Y3	Output	VS	1317.00	-8910.00
266	Y4	Output	VS	1317.00	-8850.00
267	Y5	Output	VS	1317.00	-8790.00
268	Y6	Output	VS	1317.00	-8730.00
269	Y7	Output	VS	1317.00	-8670.00
270	Y8	Output	VS	1317.00	-8610.00
271	Y9	Output	VS	1317.00	-8550.00
272	Y10	Output	VS	1317.00	-8490.00
273	Y11	Output	VS	1317.00	-8430.00
274	Y12	Output	VS	1317.00	-8370.00
275	Y13	Output	VS	1317.00	-8310.00
276	Y14	Output	VS	1317.00	-8250.00
277	Y15	Output	VS	1317.00	-8190.00
278	Y16	Output	VS	1317.00	-8130.00
279	Y17	Output	VS	1317.00	-8070.00
280	Y18	Output	VS	1317.00	-8010.00
281	Y19	Output	VS	1317.00	-7950.00
282	Y20	Output	VS	1317.00	-7890.00
283	Y21	Output	VS	1317.00	-7830.00
284	Y22	Output	VS	1317.00	-7770.00
285	Y23	Output	VS	1317.00	-7710.00
286	Y24	Output	VS	1317.00	-7650.00
287	Y25	Output	VS	1317.00	-7590.00
288	Y26	Output	VS	1317.00	-7530.00
289	Y27	Output	VS	1317.00	-7470.00
290	Y28	Output	VS	1317.00	-7410.00
291	Y29	Output	VS	1317.00	-7350.00
292	Y30	Output	VS	1317.00	-7290.00
293	Y31	Output	VS	1317.00	-7230.00
294	Y32	Output	VS	1317.00	-7170.00
295	Y33	Output	VS	1317.00	-7110.00
296	Y34	Output	VS	1317.00	-7050.00
297	Y35	Output	VS	1317.00	-6990.00
298	Y36	Output	VS	1317.00	-6930.00
299	Y37	Output	VS	1317.00	-6870.00
300	Y38	Output	VS	1317.00	-6810.00

No.	Pin Name	I/O	Power	Pad coordinate [μm]	
				X	Y
301	Y39	Output	VS	1317.00	-6750.00
302	Y40	Output	VS	1317.00	-6690.00
303	Y41	Output	VS	1317.00	-6630.00
304	Y42	Output	VS	1317.00	-6570.00
305	Y43	Output	VS	1317.00	-6510.00
306	Y44	Output	VS	1317.00	-6450.00
307	Y45	Output	VS	1317.00	-6390.00
308	Y46	Output	VS	1317.00	-6330.00
309	Y47	Output	VS	1317.00	-6270.00
310	Y48	Output	VS	1317.00	-6210.00
311	Y49	Output	VS	1317.00	-6150.00
312	Y50	Output	VS	1317.00	-6090.00
313	Y51	Output	VS	1317.00	-6030.00
314	Y52	Output	VS	1317.00	-5970.00
315	Y53	Output	VS	1317.00	-5910.00
316	Y54	Output	VS	1317.00	-5850.00
317	Y55	Output	VS	1317.00	-5790.00
318	Y56	Output	VS	1317.00	-5730.00
319	Y57	Output	VS	1317.00	-5670.00
320	Y58	Output	VS	1317.00	-5610.00
321	Y59	Output	VS	1317.00	-5550.00
322	Y60	Output	VS	1317.00	-5490.00
323	Y61	Output	VS	1317.00	-5430.00
324	Y62	Output	VS	1317.00	-5370.00
325	Y63	Output	VS	1317.00	-5310.00
326	Y64	Output	VS	1317.00	-5250.00
327	Y65	Output	VS	1317.00	-5190.00
328	Y66	Output	VS	1317.00	-5130.00
329	Y67	Output	VS	1317.00	-5070.00
330	Y68	Output	VS	1317.00	-5010.00
331	Y69	Output	VS	1317.00	-4950.00
332	Y70	Output	VS	1317.00	-4890.00
333	Y71	Output	VS	1317.00	-4830.00
334	Y72	Output	VS	1317.00	-4770.00
335	Y73	Output	VS	1317.00	-4710.00
336	Y74	Output	VS	1317.00	-4650.00
337	Y75	Output	VS	1317.00	-4590.00
338	Y76	Output	VS	1317.00	-4530.00
339	Y77	Output	VS	1317.00	-4470.00
340	Y78	Output	VS	1317.00	-4410.00
341	Y79	Output	VS	1317.00	-4350.00
342	Y80	Output	VS	1317.00	-4290.00
343	Y81	Output	VS	1317.00	-4230.00
344	Y82	Output	VS	1317.00	-4170.00
345	Y83	Output	VS	1317.00	-4110.00
346	Y84	Output	VS	1317.00	-4050.00
347	Y85	Output	VS	1317.00	-3990.00
348	Y86	Output	VS	1317.00	-3930.00
349	Y87	Output	VS	1317.00	-3870.00
350	Y88	Output	VS	1317.00	-3810.00
351	Y89	Output	VS	1317.00	-3750.00
352	Y90	Output	VS	1317.00	-3690.00
353	Y91	Output	VS	1317.00	-3630.00
354	Y92	Output	VS	1317.00	-3570.00
355	Y93	Output	VS	1317.00	-3510.00
356	Y94	Output	VS	1317.00	-3450.00
357	Y95	Output	VS	1317.00	-3390.00
358	Y96	Output	VS	1317.00	-3330.00
359	Y97	Output	VS	1317.00	-3270.00
360	Y98	Output	VS	1317.00	-3210.00

Table 2–1. Pad Coordinate (4/5)

No.	Pin Name	I/O	Power	Pad coordinate [μm]	
				X	Y
361	Y99	Output	VS	1317.00	-3150.00
362	Y100	Output	VS	1317.00	-3090.00
363	Y101	Output	VS	1317.00	-3030.00
364	Y102	Output	VS	1317.00	-2970.00
365	Y103	Output	VS	1317.00	-2910.00
366	Y104	Output	VS	1317.00	-2850.00
367	Y105	Output	VS	1317.00	-2790.00
368	Y106	Output	VS	1317.00	-2730.00
369	Y107	Output	VS	1317.00	-2670.00
370	Y108	Output	VS	1317.00	-2610.00
371	Y109	Output	VS	1317.00	-2550.00
372	Y110	Output	VS	1317.00	-2490.00
373	Y111	Output	VS	1317.00	-2430.00
374	Y112	Output	VS	1317.00	-2370.00
375	Y113	Output	VS	1317.00	-2310.00
376	Y114	Output	VS	1317.00	-2250.00
377	Y115	Output	VS	1317.00	-2190.00
378	Y116	Output	VS	1317.00	-2130.00
379	Y117	Output	VS	1317.00	-2070.00
380	Y118	Output	VS	1317.00	-2010.00
381	Y119	Output	VS	1317.00	-1950.00
382	Y120	Output	VS	1317.00	-1890.00
383	Y121	Output	VS	1317.00	-1830.00
384	Y122	Output	VS	1317.00	-1770.00
385	Y123	Output	VS	1317.00	-1710.00
386	Y124	Output	VS	1317.00	-1650.00
387	Y125	Output	VS	1317.00	-1590.00
388	Y126	Output	VS	1317.00	-1530.00
389	Y127	Output	VS	1317.00	-1470.00
390	Y128	Output	VS	1317.00	-1410.00
391	DUMMY	–	–	1317.00	-1350.00
392	DUMMY	–	–	1317.00	-1290.00
393	DUMMY	–	–	1317.00	-1230.00
394	DUMMY	–	–	1317.00	-1170.00
395	DUMMY	–	–	1317.00	-1110.00
396	DUMMY	–	–	1317.00	-1050.00
397	DUMMY	–	–	1317.00	-990.00
398	DUMMY	–	–	1317.00	-930.00
399	DUMMY	–	–	1317.00	-870.00
400	DUMMY	–	–	1317.00	-810.00
401	DUMMY	–	–	1317.00	-750.00
402	DUMMY	–	–	1317.00	-690.00
403	DUMMY	–	–	1317.00	-630.00
404	DUMMY	–	–	1317.00	-570.00
405	DUMMY	–	–	1317.00	-510.00
406	DUMMY	–	–	1317.00	-450.00
407	DUMMY	–	–	1317.00	-390.00
408	DUMMY	–	–	1317.00	-330.00
409	DUMMY	–	–	1317.00	-270.00
410	DUMMY	–	–	1317.00	-210.00
411	DUMMY	–	–	1317.00	-150.00
412	DUMMY	–	–	1317.00	-90.00
413	DUMMY	–	–	1317.00	-30.00
414	DUMMY	–	–	1317.00	30.00
415	DUMMY	–	–	1317.00	90.00
416	DUMMY	–	–	1317.00	150.00
417	DUMMY	–	–	1317.00	210.00
418	DUMMY	–	–	1317.00	270.00
419	DUMMY	–	–	1317.00	330.00
420	DUMMY	–	–	1317.00	390.00

No.	Pin Name	I/O	Power	Pad coordinate [μm]	
				X	Y
421	DUMMY	–	–	1317.00	450.00
422	DUMMY	–	–	1317.00	510.00
423	DUMMY	–	–	1317.00	570.00
424	DUMMY	–	–	1317.00	630.00
425	DUMMY	–	–	1317.00	690.00
426	DUMMY	–	–	1317.00	750.00
427	DUMMY	–	–	1317.00	810.00
428	DUMMY	–	–	1317.00	870.00
429	DUMMY	–	–	1317.00	930.00
430	DUMMY	–	–	1317.00	990.00
431	DUMMY	–	–	1317.00	1050.00
432	DUMMY	–	–	1317.00	1110.00
433	DUMMY	–	–	1317.00	1170.00
434	DUMMY	–	–	1317.00	1230.00
435	DUMMY	–	–	1317.00	1290.00
436	DUMMY	–	–	1317.00	1350.00
437	DUMMY	–	–	1317.00	1410.00
438	DUMMY	–	–	1317.00	1470.00
439	DUMMY	–	–	1317.00	1530.00
440	DUMMY	–	–	1317.00	1590.00
441	DUMMY	–	–	1317.00	1650.00
442	DUMMY	–	–	1317.00	1710.00
443	DUMMY	–	–	1317.00	1770.00
444	DUMMY	–	–	1317.00	1830.00
445	DUMMY	–	–	1317.00	1890.00
446	DUMMY	–	–	1317.00	1950.00
447	DUMMY	–	–	1317.00	2010.00
448	DUMMY	–	–	1317.00	2070.00
449	DUMMY	–	–	1317.00	2130.00
450	DUMMY	–	–	1317.00	2190.00
451	DUMMY	–	–	1317.00	2250.00
452	DUMMY	–	–	1317.00	2310.00
453	Y129	Output	VS	1317.00	2370.00
454	Y130	Output	VS	1317.00	2430.00
455	Y131	Output	VS	1317.00	2490.00
456	Y132	Output	VS	1317.00	2550.00
457	Y133	Output	VS	1317.00	2610.00
458	Y134	Output	VS	1317.00	2670.00
459	Y135	Output	VS	1317.00	2730.00
460	Y136	Output	VS	1317.00	2790.00
461	Y137	Output	VS	1317.00	2850.00
462	Y138	Output	VS	1317.00	2910.00
463	Y139	Output	VS	1317.00	2970.00
464	Y140	Output	VS	1317.00	3030.00
465	Y141	Output	VS	1317.00	3090.00
466	Y142	Output	VS	1317.00	3150.00
467	Y143	Output	VS	1317.00	3210.00
468	Y144	Output	VS	1317.00	3270.00
469	Y145	Output	VS	1317.00	3330.00
470	Y146	Output	VS	1317.00	3390.00
471	Y147	Output	VS	1317.00	3450.00
472	Y148	Output	VS	1317.00	3510.00
473	Y149	Output	VS	1317.00	3570.00
474	Y150	Output	VS	1317.00	3630.00
475	Y151	Output	VS	1317.00	3690.00
476	Y152	Output	VS	1317.00	3750.00
477	Y153	Output	VS	1317.00	3810.00
478	Y154	Output	VS	1317.00	3870.00
479	Y155	Output	VS	1317.00	3930.00
480	Y156	Output	VS	1317.00	3990.00

Table 2–1. Pad Coordinate (5/5)

No.	Pin Name	I/O	Power	Pad coordinate [μm]	
				X	Y
481	Y157	Output	VS	1317.00	4050.00
482	Y158	Output	VS	1317.00	4110.00
483	Y159	Output	VS	1317.00	4170.00
484	Y160	Output	VS	1317.00	4230.00
485	Y161	Output	VS	1317.00	4290.00
486	Y162	Output	VS	1317.00	4350.00
487	Y163	Output	VS	1317.00	4410.00
488	Y164	Output	VS	1317.00	4470.00
489	Y165	Output	VS	1317.00	4530.00
490	Y166	Output	VS	1317.00	4590.00
491	Y167	Output	VS	1317.00	4650.00
492	Y168	Output	VS	1317.00	4710.00
493	Y169	Output	VS	1317.00	4770.00
494	Y170	Output	VS	1317.00	4830.00
495	Y171	Output	VS	1317.00	4890.00
496	Y172	Output	VS	1317.00	4950.00
497	Y173	Output	VS	1317.00	5010.00
498	Y174	Output	VS	1317.00	5070.00
499	Y175	Output	VS	1317.00	5130.00
500	Y176	Output	VS	1317.00	5190.00
501	Y177	Output	VS	1317.00	5250.00
502	Y178	Output	VS	1317.00	5310.00
503	Y179	Output	VS	1317.00	5370.00
504	Y180	Output	VS	1317.00	5430.00
505	Y181	Output	VS	1317.00	5490.00
506	Y182	Output	VS	1317.00	5550.00
507	Y183	Output	VS	1317.00	5610.00
508	Y184	Output	VS	1317.00	5670.00
509	Y185	Output	VS	1317.00	5730.00
510	Y186	Output	VS	1317.00	5790.00
511	Y187	Output	VS	1317.00	5850.00
512	Y188	Output	VS	1317.00	5910.00
513	Y189	Output	VS	1317.00	5970.00
514	Y190	Output	VS	1317.00	6030.00
515	Y191	Output	VS	1317.00	6090.00
516	Y192	Output	VS	1317.00	6150.00
517	Y193	Output	VS	1317.00	6210.00
518	Y194	Output	VS	1317.00	6270.00
519	Y195	Output	VS	1317.00	6330.00
520	Y196	Output	VS	1317.00	6390.00
521	Y197	Output	VS	1317.00	6450.00
522	Y198	Output	VS	1317.00	6510.00
523	Y199	Output	VS	1317.00	6570.00
524	Y200	Output	VS	1317.00	6630.00
525	Y201	Output	VS	1317.00	6690.00
526	Y202	Output	VS	1317.00	6750.00
527	Y203	Output	VS	1317.00	6810.00
528	Y204	Output	VS	1317.00	6870.00
529	Y205	Output	VS	1317.00	6930.00
530	Y206	Output	VS	1317.00	6990.00
531	Y207	Output	VS	1317.00	7050.00
532	Y208	Output	VS	1317.00	7110.00
533	Y209	Output	VS	1317.00	7170.00
534	Y210	Output	VS	1317.00	7230.00
535	Y211	Output	VS	1317.00	7290.00
536	Y212	Output	VS	1317.00	7350.00
537	Y213	Output	VS	1317.00	7410.00
538	Y214	Output	VS	1317.00	7470.00
539	Y215	Output	VS	1317.00	7530.00
540	Y216	Output	VS	1317.00	7590.00
541	Y217	Output	VS	1317.00	7650.00
542	Y218	Output	VS	1317.00	7710.00
543	Y219	Output	VS	1317.00	7770.00
544	Y220	Output	VS	1317.00	7830.00
545	Y221	Output	VS	1317.00	7890.00
546	Y222	Output	VS	1317.00	7950.00
547	Y223	Output	VS	1317.00	8010.00
548	Y224	Output	VS	1317.00	8070.00
549	Y225	Output	VS	1317.00	8130.00
550	Y226	Output	VS	1317.00	8190.00
551	Y227	Output	VS	1317.00	8250.00
552	Y228	Output	VS	1317.00	8310.00
553	Y229	Output	VS	1317.00	8370.00
554	Y230	Output	VS	1317.00	8430.00
555	Y231	Output	VS	1317.00	8490.00
556	Y232	Output	VS	1317.00	8550.00
557	Y233	Output	VS	1317.00	8610.00
558	Y234	Output	VS	1317.00	8670.00
559	Y235	Output	VS	1317.00	8730.00
560	Y236	Output	VS	1317.00	8790.00
561	Y237	Output	VS	1317.00	8850.00
562	Y238	Output	VS	1317.00	8910.00
563	Y239	Output	VS	1317.00	8970.00
564	Y240	Output	VS	1317.00	9030.00
565	DUMMY	–	–	1317.00	9090.00
566	DUMMY	–	–	1317.00	9150.00
567	DUMMY	–	–	1317.00	9210.00

	X [μm]	Y [μm]
Alignment Mark 1 (M1)	-1317.00	9050.00
Alignment Mark 1 (M2)	-1317.00	-9020.00
Alignment Mark 2 (M3)		

3. PIN FUNCTIONS

3.1 Power Supply System Pins (1/2)

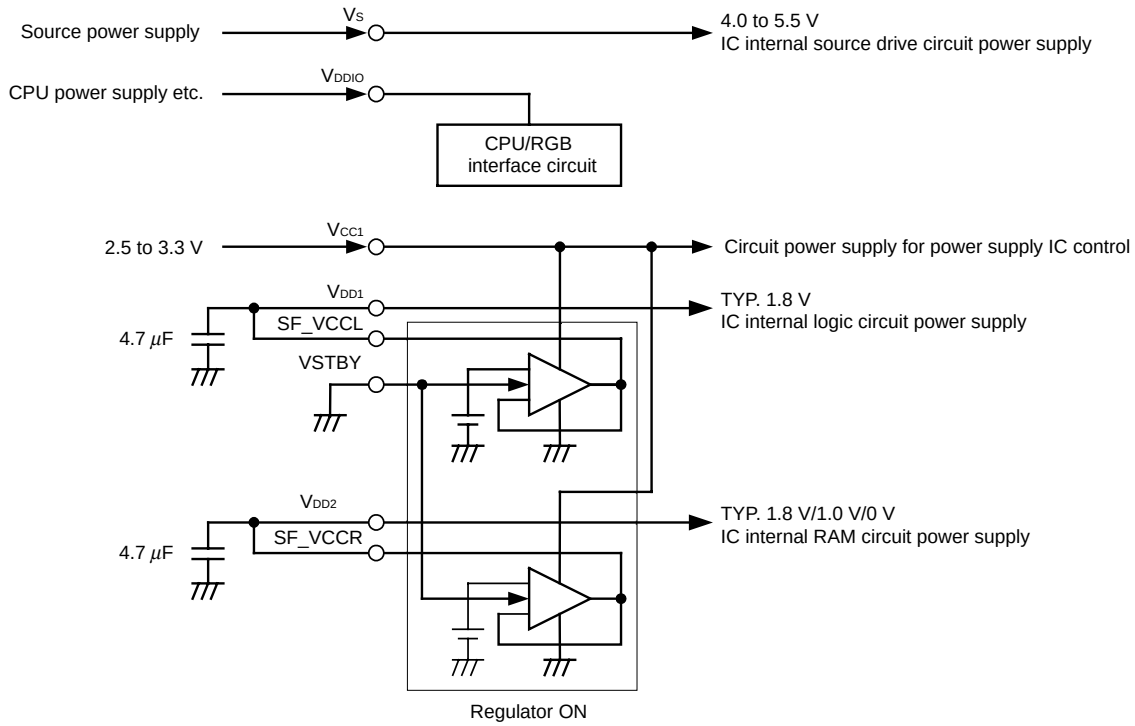
Symbol	Pin Name	Pad No.	I/O	Function
V_{DD1}	Power supply for logic	125 to 132	–	This is the power supply pin for the logic. When VSTBY = L, there is no need to apply a power supply voltage. The voltage that is input from the power supply control pin (V_{CC1}) is used to generate the logic's power supply voltage within the chip. However, the interface with the CPU must be implemented using V_{DDIO}. Also, no power is supplied to the V_{DD1} pin, but it should be connected to the SF_VCCL pin and a 4.7 μF capacitor should be connected between it and the GND pin. Refer to **Figure 3–1**.
SF_VCCL	Internal logic power supply generation amplifier output	119 to 124	Output	If using 3 power supplies (VSTBY = L), be sure to connect a capacitor between this pin and a GND connection. For details, refer to **Figure 3–1**. If using 4 power supplies (VSTBY = H), leave this pin open.
V_{DD2}	Power supply for display RAM	139 to 146	–	This power supply pin is used for the display RAM circuits. When VSTBY = L, there is no need to apply a power supply voltage. The voltage that is input from the power supply control pin (V_{CC1}) is used to generate the logic's power supply voltage within the chip. Also, no power is supplied to the V_{DD2} pin, but it should be connected to the SF_VCCR pin and a 1 μF capacitor should be connected between it and the GND pin. For details, refer to **Figure 3–1**.
SF_VCCR	Display RAM circuit power supply generation amplifier output	133 to 138	Output	In the case of 3 power-supply supply system (VSTBY = L), connect a capacitor between grounds. For details, refer to **Figure 3–1**. In the case of 4 power-supply supply system (VSTBY = H), leave it open.
V_{DDIO}	CPU/RGB interface power supply	107 to 112	–	This is the CPU/RGB interface's power supply pin. Be sure to input a power supply that has the same potential as the IC connected to the CPU/RGB interface.
V_{CC1}	Interface and power supply pin for power supply IC control	113 to 118	–	This is the power supply pin for the power IC control circuit. Be sure to input a power supply that has the same potential as the connected IC.
V_S	Driver and gate control for power supply	187 to 192	–	Power supply pin for driver circuit.
V_{SS11}	Ground pin for logic	155 to 163	–	Ground pin for logic circuit
V_{SS1}	Ground pin for interface and power supply IC	147 to 154	–	Ground pin for power supply IC of control circuit and logic interface circuit.
V_{SS}	Ground pin for driver and gate control	164 to 169	–	Ground pin for driver circuit power supply IC control circuit
VSTBY	Logic power supply generation control	212	Input	This pin is used to select whether or not to supply voltage to the logic's power supply. VSTBY = L: Supply voltage to V_{DD1}, V_{DD2}, SF_VCCL, and SF_VCCR is not required. VSTBY = H: Supply voltage to V_{DD1} and V_{DD2} is required.

(2/2)

Symbol	Pin Name	Pad No.	I/O	Function
$V_{DDIO(MODE)}$	Mode setting pull-up power supply	53, 79, 84	–	Pull-up power supply pin for mode setting
$V_{CC1\ (MODE)}$	Mode setting pull-up power supply	198, 204, 210	–	Pull-up power supply pin for mode setting
$V_{SS1\ (MODE)}$	Mode setting pull-down power supply	74, 82, 88, 195, 201, 207, 213, 234, 256	–	Pull-down power supply pin for mode setting

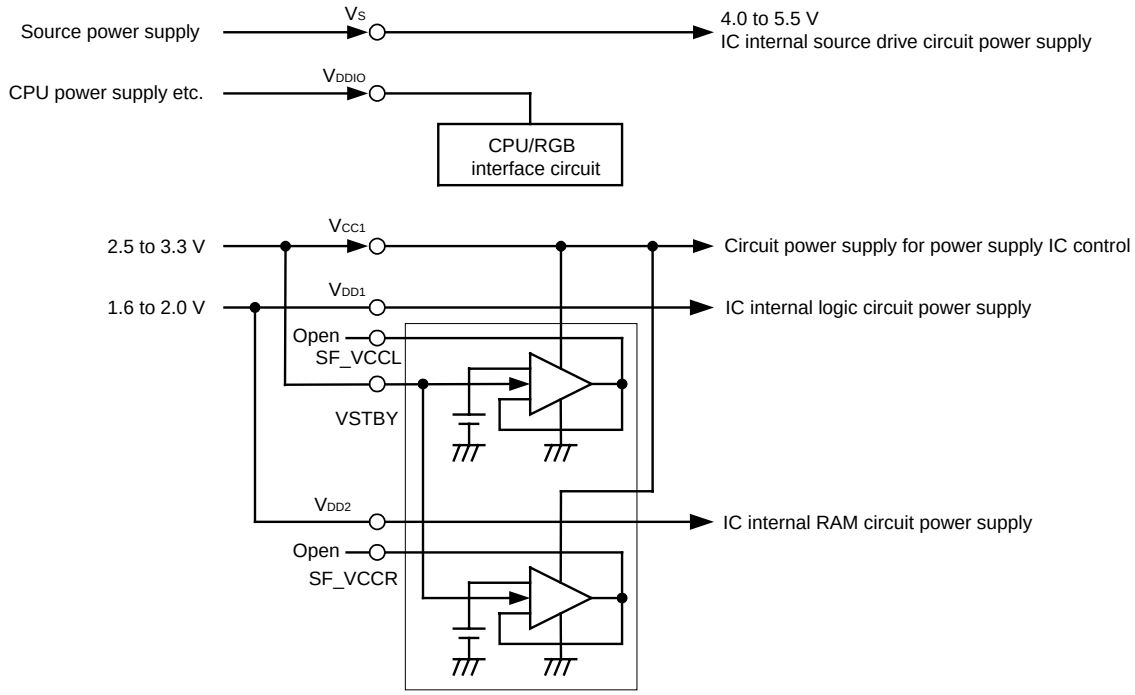
Figure 3–1. Supplies for Power Supply

[At the time of IC regulator circuit use for logic circuits: V_{CC1} = 2.5 to 3.3 V single power supply input]



Regulator ON

[At the time of IC regulator circuit unused for logic circuits: V_{DD1}, V_{DD2} = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V]



Regulator OFF

3.2 Logic System Pins

(1/2)

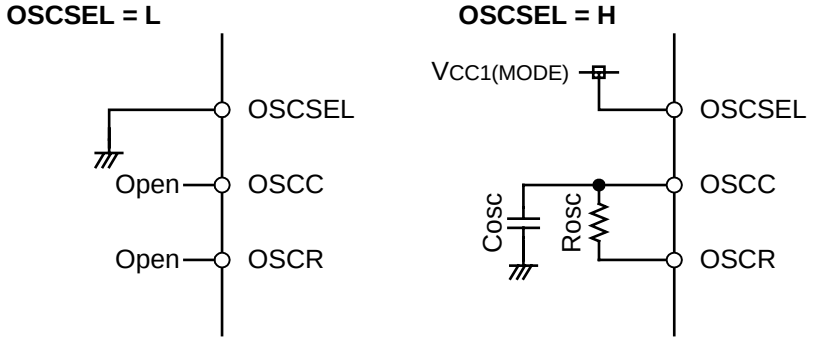
<table>
<tr><th>Symbol</th><th>Pin Name</th><th>Pad No.</th><th>I/O</th><th>Function</th></tr>
<tr><td>BWS0</td><td>CPU interface bus width selection</td><td>206</td><td>Input</td><td rowspan="2">This pin selects the bus width of the i80/M68 interface (it is invalid for the RGB interface).
<table><tr><th>BWS0</th><th>BWS1</th><th>i80/M68, Serial Interface Bus Width</th></tr><tr><td>L</td><td>L</td><td>18 bits</td></tr><tr><td>L</td><td>H</td><td>16 bits</td></tr><tr><td>H</td><td>L</td><td>Prohibited</td></tr><tr><td>H</td><td>H</td><td>8 bits parallel or serial interface</td></tr></table></td></tr>
<tr><td>BWS1</td><td>CPU interface bus width selection</td><td>208</td><td>Input</td></tr>
<tr><td>BWS2</td><td>RGB interface bus width selection</td><td>209</td><td>Input</td><td rowspan="2">This pin selects the bus width of the RGB interface (it is invalid for the CPU interface).
<table><tr><th>BWS2</th><th>BWS3</th><th>RGB Interface Bus Width</th></tr><tr><td>L</td><td>L</td><td>18 bits</td></tr><tr><td>L</td><td>H</td><td>16 bits</td></tr><tr><td>H</td><td>L</td><td>6 bits</td></tr><tr><td>H</td><td>H</td><td>Prohibited</td></tr></table></td></tr>
<tr><td>BWS3</td><td>RGB interface bus width selection</td><td>211</td><td>Input</td></tr>
<tr><td>PSX</td><td>CPU interface mode selection</td><td>203</td><td>Input</td><td>This pin selects the mode of the CPU interface.
L: i80/M68 interface only, H: Serial interface only</td></tr>
<tr><td>/CS</td><td>Chip select</td><td>78</td><td>Input</td><td>This pin is used for chip select signals. When /CS = L, the chip is active and can perform data I/O operations including command and data I/O.</td></tr>
<tr><td>/RESET</td><td>Reset</td><td>55</td><td>Input</td><td>When /RESET is L, an internal reset is initialized. The reset operation is executed at the /RESET signal level. Be sure to perform reset via this pin at power application.</td></tr>
<tr><td>/RD
(E)</td><td>Read
(Enable)</td><td>75</td><td>Input</td><td>When i80 series parallel data transfer (/RD) has been selected, the signal at this pin is used to enable read operations. Data is output to the data bus only when this pin is low.
When M68 series parallel data transfer (E) has been selected, the signal at this pin is used to enable read/write operations.</td></tr>
<tr><td>/WR
(R,/W)</td><td>Write
(Read/write)</td><td>76</td><td>Input</td><td>When i80 series parallel data transfer (/WR) has been selected, the signal at this pin is used to enable write operations.
When M68 series parallel data transfer (R,/W) has been selected, this pin is used to determine the direction of data transfer.
L: Write, H: Read</td></tr>
<tr><td>C86</td><td>Select interface</td><td>205</td><td>Input</td><td>This pin is used to switch between interface modes (i80 series CPU or M68 series CPU).
L: Selects i80 series CPU mode, H: Selects M68 series CPU mode</td></tr>
<tr><td>D_0 to D_{17}</td><td>Data bus</td><td>73 to 56</td><td>I/O</td><td>These pins comprise 18-bit bi-directional data.
When the chip is not selected, D_0 to D_{17} are in Hi-Z (high impedance) mode.</td></tr>
<tr><td>SI</td><td>Serial input</td><td>80</td><td>Input</td><td>This pin is data input of serial interface.</td></tr>
<tr><td>SCL</td><td>Serial clock</td><td>81</td><td>Input</td><td>This pin is clock input of serial interface.</td></tr>
<tr><td>RS</td><td>Data/command selection</td><td>77</td><td>Input</td><td>When parallel data transfer has been selected, this pin is usually connected to the least significant bit of the standard CPU address bus and is used to distinguish between data from display data and commands.
RS = L: Indicates that data from D_0 to D_{17} is commands.
RS = H: Indicates that data from D_0 to D_{17} is display data.</td></tr>
</table>

(2/2)

Symbol	Pin Name	Pad No.	I/O	Function
HSYNC	Horizontal sync signal	86	Input	This is the horizontal sync signal of the RGB interface.
VSYNC	Vertical sync signal	85	Input	This is the vertical sync signal of the RGB interface.
DOTCLK	Dot clock	87	Input	This is the dot clock signal of the RGB interface.
HSEG	HSYNC polarity selection	199	Input	This selects polarity of the horizontal sync signal of the RGB interface. HSEG = L: Low active HSEG = H: High active
VSEG	VSYNC polarity selection	200	Input	This selects polarity of the vertical sync signal of the RGB interface. VSEG = L: Low active VSEG = H: High active
DCKEG	DOTCLK polarity selection	202	Input	This selects polarity of the dot clock signal of the RGB interface. DCKEG = L: High active (this pin is latched up at rising edge) DCKEG = H: High level (this pin is latched up at falling edge)
RGB_{00} to RGB_{05}, RGB_{10} to RGB_{15}, RGB_{20} to RGB_{25}	Data bus	89 to 94, 95 to 100, 101 to 106	Input	These pins are RGB interface data signal.
CSTB	GSTB logic signal	54	Output	This pin outputs STB signal for gate driver leveled by interface power supply voltage (V_{DDIO}). This output signal is reverse signal of GSTB.
★ VLD	RAM write enable signal	83	Input	This signal sets the data as valid during a RAM write operation. This signal can be used only when the RGB interface is in capture mode. VLD = L: Capture input data is valid (no write to RAM) VLD = H: Capture input data is invalid (write to RAM)
OSCSEL	Oscillator circuit selection	196	Input	The oscillation circuit of the inside reference clock for liquid crystal drive of IC is selected. OSCSEL = L: Internal oscillation circuit selection OSCSEL = H: External oscillation circuit selection
OSCR	Resistance Connection for Oscillator	194	–	Resistance of T.B.D. Ω is connected between OSCC pins at the time (OSCSEL = H) of external oscillation circuit selection. Leave it open at the time (OSCSEL = L) of internal oscillation circuit selection.
OSCC	Capacitor connection for oscillator	193	–	At the time (OSCSEL = H) of external oscillation circuit selection, resistance of T.B.D. Ω is connected between OSCR pins, and the capacitor of T.B.D. μF is connected between grounds. Leave it open at the time (OSCSEL = L) of internal oscillation circuit selection.
★ CMDS	CMDS	197	Input	Connect to V_{SS1}.

Remark T.B.D. (To be determined.)

[Example of the oscillator circuit connection]



3.3 Gate Driver Control Pins

3.3.1 Gate driver control 1

Symbol	Pin Name	Pad No.	I/O	Function
GOE1	OE1 output for gate control	33	Output	This pin is output enable pin for gate control. Signal is outputted to the timing set as R79 and R80. For details, refer to **5.4 Display Timing Generator.**
/GOE1	OE1 output for gate control	34	Output	This pin outputs inverted GOE1 signal.
GOE2	OE2 output for gate control	31	Output	This pin is output enable pin for gate control. For details, refer to **5.4 Display Timing Generator.**
/GOE2	OE2 output for gate control	32	Output	This pin outputs inverted GOE2 signal.
GSTB	STB output for gate control	27	Output	This pin is output strove pin for gate control. Timing signal for output, refer to **5.4 Display Timing Generator.**
/GSTB	STB output for gate control	28	Output	This pin outputs inverted GSTB signal.
GCLK	CLK output for gate control	29	Output	This pin is the CLK output for the gate control. Timing signal for output, refer to **5.4 Display Timing Generator.**
/GCLK	CLK output for gate control	30	Output	This pin outputs inverted GCLK signal.
PC	Panel control output	47	Output	This pin is output control pin for panel. Signal is outputted to the timing set as R81 and R82. For details, refer to **5.4 Display Timing Generator.**
/PC	Panel control output	48	Output	This pin outputs inverted PC signal.
PCP	Pre-charge control output	45	Output	This pin is the pre-charge control output for panel. Timing signal for output, refer to **5.4 Display Timing Generator.**
/PCP	Pre-charge control output	46	Output	This pin outputs inverted PCP signal.

3.3.2 Gate driver control 2

Symbol	Pin Name	Pad No.	I/O	Function
PCN	Pre-discharge control output	43	Output	This pin is the pre-discharge control output for panel. Timing signal for output, refer to **5.4 Display Timing Generator.**
/PCN	Pre-discharge control output	44	Output	This pin outputs inverted PCN signal.
EXT1	Reserve signal for panel control	49	Output	This pin is extended signal for panel control. Signal is outputted to the timing set as R89 and R90. Timing signal for output, refer to **5.4 Display Timing Generator.**
/EXT1	Reserve signal for panel control	50	Output	This pin outputs inverted EXT1 signal.
EXT2	Reserve signal for panel control	51	Output	This pin is extended signal for panel control. Signal is outputted to the timing set as R91 and R92. Timing signal for output, refer to **5.4 Display Timing Generator.**
/EXT2	Reserve signal for panel control	52	Output	This pin outputs inverted EXT2 signal.
GUD	Control signal for gate scan direction	35	Output	This pin is gate scan direction control signal. Timing signal for output, refer to **5.4 Display Timing Generator.**
/GUD	Control signal for gate scan direction	36	Output	This pin outputs inverted GUD signal.
OEV	OE1 output for gate control	15	Output	This pin is output enable pin for gate control. Signal is outputted to the timing set as R79 and R80. Timing signal for output, refer to **5.4 Display Timing Generator**.
/OEV	OE1 output for gate control	16	Output	This pin outputs inverted OEV signal.
OEVE	OE2 output for gate control	17	Output	This pin is output enable pin for gate control. Timing signal for output, refer to **5.4 Display Timing Generator**.
/OEVE	OE2 output for gate control	18	Output	This pin outputs inverted OEVE signal.
STV	Start signal output for gate control	11	Output	This pin is start signal pin for gate control. Timing signal for output, refer to **5.4 Display Timing Generator**.
/STV	Start signal output for gate control	12	Output	This pin outputs inverted STV signal.
CKV	CLK output for gate control	13	Output	This pin is clock output signal pin for gate control. Timing signal for output, refer to **5.4 Display Timing Generator**.
/CKV	CLK output for gate control	14	Output	This pin outputs inverted CKV signal.
XDON	Panel control output	19	Output	This pin is control output pin for panel. Signal is outputted by set-up of RXDON (R77).
/XDON	Panel control output	20	Output	This pin outputs inverted XDON signal.

3.4 RGB Multi-plectra Switch Control Pins

3.4.1 RGB Multi-plectra Switch Control

Symbol	Pin Name	Pad No.	I/O	Function
RSW	Multi-plectra control signal	25	Output	This pin is panel of multi-plectra control signal. Signal is outputted to the timing set as R83 and R84. For details, refer to **5.4 Display timing generator**.
/RSW	Multi-plectra control signal	26	Output	This pin outputs inverted RSW signal.
GSW	Multi-plectra control signal	23	Output	This pin is panel of multi-plectra control signal. Signal is outputted to the timing set as R85 and R86. For details, refer to **5.4 Display timing generator**.
/GSW	Multi-plectra control signal	24	Output	This pin outputs inverted GSW signal.
BSW	Multi-plectra control signal	21	Output	This pin is panel of multi-plectra control signal. Signal is outputted to the timing set as R87 and R88. For details, refer to **5.4 Display timing generator**.
/BSW	Multi-plectra control signal	22	Output	This pin outputs inverted BSW signal.

3.4.2 Multi-plectra Switch Control

Symbol	Pin Name	Pad No.	I/O	Function
ASW1	Multi-plectra control signal	9	Output	This pin is panel of multi-plectra control signal. Signal is outputted to the timing set as R83 and R84. For details, refer to **5.4 Display timing generator**.
/ASW1	Multi-plectra control signal	10	Output	This pin outputs inverted ASW1 signal.
ASW2	Multi-plectra control signal	7	Output	This pin is panel of multi-plectra control signal. Signal is outputted to the timing set as R85 and R86. For details, refer to **5.4 Display timing generator**.
/ASW2	Multi-plectra control signal	8	Output	This pin outputs inverted ASW2 signal.
ASW3	Multi-plectra control signal	5	Output	This pin is panel of multi-plectra control signal. Signal is outputted to the timing set as R87 and R88. For details, refer to **5.4 Display timing generator**.
/ASW3	Multi-plectra control signal	6	Output	This pin outputs inverted ASW3 signal.

3.5 External IC (μPD161861, etc.) Control Pins

Symbol	Pin Name	Pad No.	I/O	Function
PCS	Chip select signal output	40	Output	This is a chip selection output pin for serial interfaces for power supply IC control. Connect with chip selection input pins, such as the external power supply IC. Set-up of R38 to R42, and R60 to R65 starts an output. For details, refer to **5.1.8 Serial interface for power supply IC control**.
PCL	Serial clock signal output	41	Output	This is a serial clock output pin for serial interfaces for power supply IC control. Connect with serial clock input pins, such as the external power supply IC. Set-up of R38 to R42, and R60 to R65 starts an output. For details, refer to **5.1.8 Serial interface for power supply IC control**.
PDA	Serial data output	39	Output	This is a serial data pin for serial interfaces for power supply IC control. Connect with serial data input pins, such as the external power supply IC. Set-up of R38 to R42, and R60 to R65 starts an output. For details, refer to **5.1.8 Serial interface for power supply IC control**.
/PRESET	Reset output	4	Output	This is a reset signal output pin for power supplies IC. The reset signal inputted from RESET pin is outputted on the incoming signal level (V_{CC1}) of the external power supply IC. Connect with reset input pins, such as the external power supply IC.
PCCLK	Power supply IC DC/DC converter clock output	42	Output	The reference clock for the DC/DC converter circuits of a power supply IC is outputted. Oscillation frequency is divided cycle and outputted by the divided cycle ratio set up by DC4 and DC3 (R72). Use this pin, connecting with standard clock inputs for DC/DC converter circuits, such as a power supply IC.

3.6 Driver Pins

Symbol	Pin Name	Pad No.	I/O	Function
Y_1 to Y_{240}	Source output	263 to 390, 453 to 564	Output	These pins are source output pins
VCOUT	Common timing output	37	Output	Common timing signal is outputted from V_{CC1}-V_{SS}, V_{P-P}. Usually, it is used such as shifting this timing output signal to the voltage level to need.
FR	Frame signal output	38	Output	This pin outputs frame polarity signal. With VCOUT, the signal of inversion polarity is outputted in V_{CC1} to V_{SS} when RXDON (R77 • D_2) = 0 setup. When RXDON = 1 setup, operation set as DSCGn (R72 • D_5 to D_0) is performed.
CVPH, CVPL, CVNH, CVNL	Basis power supply pin for γ-corrected power supplies	184 to 186, 181 to 183, 178 to 180, 175 to 177	–	This is operational amplifier output pin for the γ-corrected power supplies. Normally, this pin connects capacitor of T.B.D. μF. When unused the amplifier for γ-correction, leave it open.

3.7 Test or Other Pins

Symbol	Pin Name	Pad No.	I/O	Function
$TOUT_0$ to $TOUT_{19}$, TOSCO1, TOSCO2, $TAOUT_0$ to $TAOUT_4$	Test output	233 to 214, 254 to 255, 170 to 174	Output	This is output pin when IC is in test mode. Normally, leave it open.
$TDELAY_0$ to $TDELAY_9$	Test input	235 to 244	Input	This is input pin when IC is in test mode. Normally, connected it to V_{SS1}.
TSTRTST, TSTVIHL, TOSCI1, TOSCI2, TOSCSEI1, TOSCSEI2, TOSCSEO1, TOSCSEO2, TCLK	Test input	247, 246, 252, 253, 250, 251 248, 249, 245	Input	These input pins are to set up test mode of IC. Normally, fixed it to V_{SS}.
DUMMY	Dummy	1 to 3, 257 to 262, 391 to 452, 565 to 567	–	Dummy pin

4. PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The I/O circuit types of each pin and recommended connection of unused pins are described below.

(1/2)

Pin Name	I/O	Power Supply	Recommended Connection of Unused Pins		Note
			Parallel Interface	Serial Interface	
PSX	Input	V_{CC1}	Mode setting pin		O
BWS_0 to BWS_3	Input	V_{CC1}	Mode setting pin		O
VSTBY	Input	V_{CC1}	Mode setting pin		O
/RESET	Input	V_{DDIO}	Always reset on power application		–
/CS	Input	V_{DDIO}	Connect to V_{DDIO}		–
/RD (E), /WR	Input	V_{DDIO}	Connect to V_{DDIO} (when i80 series interface)	Connect to V_{DDIO} or V_{SS1}	–
C86	Input	V_{CC1}	Mode setting pin	Connect to V_{CC1} or V_{SS1}	O
D_0 to D_{17}	I/O	V_{DDIO}	–	Connect to V_{SS1}	–
SI, SCL	Input	V_{DDIO}	Connect to V_{DDIO}	–	–
HSYNC	Input	V_{DDIO}	Connect to V_{DDIO} or V_{SS1}		–
VSYNC	Input	V_{DDIO}	Connect to V_{DDIO} or V_{SS1}		–
DOTCLK	Input	V_{DDIO}	Connect to V_{DDIO} or V_{SS1}		O
HSEG	Input	V_{CC1}	Mode setting pin		O
VSEG	Input	V_{CC1}	Mode setting pin		O
DCKEG	Input	V_{CC1}	Mode setting pin		–
RGB_{00} to RGB_{05}, RGB_{10} to RGB_{15}, RGB_{20} to RGB_{25}	Input	V_{DDIO}	Connect to V_{DDIO} or V_{SS1}		O
RS	Input	V_{DDIO}	Register setting pin		–
CSTB	Output	V_{DDIO}	Leave open		–
OSCSEL	Input	V_{CC1}	Mode setting pin		O
OSCR	–	V_{DD1}	Leave open		–
OSCC	–	V_{DD1}	Leave open		–
GOE_1, /GOE_1	Output	V_{CC1}	Leave open		–
GOE_2, /GOE_2	Output	V_{CC1}	Leave open		–
GSTB, /GSTB	Output	V_{CC1}	Leave open		–
GCLK, /GCLK	Output	V_{CC1}	Leave open		–
PC, /PC	Output	V_{CC1}	Leave open		–
PCP, /PCP	Output	V_{CC1}	Leave open		–
PCN, /PCN	Output	V_{CC1}	Leave open		–
EXT1, /EXT1	Output	V_{CC1}	Leave open		–
EXT2, /EXT2	Output	V_{CC1}	Leave open		–
RSW, /RSW	Output	V_{CC1}	Leave open		–
GSW, /GSW	Output	V_{CC1}	Leave open		–
BSW, /BSW	Output	V_{CC1}	Leave open		–
GUD, /GUD	Output	V_{CC1}	Leave open		–
STV, /STV	Output	V_{CC1}	Leave open		–
CKV, /CKV	Output	V_{CC1}	Leave open		–

(2/2)

Pin Name	I/O	Power Supply	Recommended Connection of Unused Pins		Note
			Parallel Interface	Serial Interface	
OEV, /OEV	Output	V_{CC1}	Leave open		–
OEVE, /OEVE	Output	V_{CC1}	Leave open		–
XDON, /XDON	Output	V_{CC1}	Leave open		–
PCS	Output	V_{CC1}	Connect power supply IC etc. with exterior IC. Leave it open when in unused.		–
PCL	Output	V_{CC1}	Connect power supply IC etc. with exterior IC. Leave it open when in unused.		–
PDA	Output	V_{CC1}	Connect power supply IC etc. with exterior IC. Leave it open when in unused.		–
PCCLK	Output	V_{CC1}	Connect power supply IC etc. with exterior IC. Leave it open when in unused.		–
/PRESET	Output	V_{CC1}	Connect power supply IC etc. with exterior IC. Leave it open when in unused.		–
VCOUT	Output	V_{CC1}	Leave open		–
FR	Output	V_{CC1}	Leave open		–
CVNL, CVNH, CVPL, CVPH	Output	V_S	Always connect to the capacitor of T.B.D. μF. However, this pin can be left open if not using any amplifier for γ-correction.		–
$TOUT_0$ to $TOUT_{19}$	Output	V_{CC1}	Leave open		–
TOSCO1, TOSCO2	Output	V_{CC1}	Leave open		–
$TAOUT_0$ to $TAOUT_4$	Output	V_S	Leave open		–
TSTRTST	Input	V_{CC1}	Connect to V_{SS1}		–
TSTVIHL	Input	V_{CC1}	Connect to V_{SS1}		–
TOSCI1, TOSCI2	Input	V_{CC1}	Connect to V_{SS1}		–
TOSCSEO1, TOSCSEO2	Input	V_{CC1}	Connect to V_{SS1}		–
TOSCSEI1, TOSCSEI2	Input	V_{CC1}	Connect to V_{SS1}		–
$TDELAY_0$ to $TDELAY_9$	Input	V_{CC1}	Connect to V_{SS1}		–
TCLK	Input	V_{CC1}	Connect to V_{SS1}		–

Note Connect to V_{DD1} or V_{SS1}, depending on the mode selected.

5. DESCRIPTION OF FUNCTIONS

5.1 CPU Interface

5.1.1 Selection of interface type

The μPD161801 is able to transfer data via an RGB interface (18-/16-/6-bit) or via either of two CPU interfaces: the i80/M68 parallel interface (18-/16-/8-bit) or a serial interface (8-bit). The following modes can be selected for these CPU interfaces, as set via the PSX, BSW0, and BSW1 pins. Also, the RGB interface becomes valid when NWRGB (R25:D_2) = 1, at which time the bus width is selected according to the BWS2 and BSW3 pin settings.

Although the i80/M68 parallel interface and the serial interface allow writing to both the display data RAM and the registers, the RGB interface can be used only to overwrite the display data RAM.

Table 5–1. CPU Interface Bus Width Selection

PSX	BWS0	BWS1	Mode	/CS	RS	/RD (E)	/WR (R, /W)	C86	D_{17}, D_{16}	D_{15} to D_8	D_7 to D_0	SI, SCL
L	L	L	18-bit parallel	/CS	RS	/RD (E)	/WR (R, /W)	C86	D_{17}, D_{16}	D_{15} to D_8	D_7 to D_0	Hi-Z Note
	L	H	16-bit parallel	/CS	RS	/RD (E)	/WR (R, /W)	C86	Hi-Z Note	D_{15} to D_8	D_7 to D_0	Hi-Z Note
	H	H	8-bit parallel	/CS	RS	/RD (E)	/WR (R, /W)	C86	Hi-Z Note	Hi-Z Note	D_7 to D_0	Hi-Z Note
H	H	H	8-bit serial	/CS	RS	X	Hi-Z Note	X	Hi-Z Note	Hi-Z Note	Hi-Z Note	SI, SCL
Other than above			Setting prohibited									

Remark X: Don't care

Note Hi-Z: High impedance

Table 5–2. RGB Interface Bus Width Selection

BWS2	BWS3	Mode	RGB_{01} to RGB_{05}	RGB_{00}	RGB_{10} to RGB_{15}	RGB_{21} to RGB_{25}	RGB_{20}
L	L	18-bit parallel	RGB_{01} to RGB_{05}	RGB_{00}	RGB_{10} to RGB_{15}	RGB_{21} to RGB_{25}	RGB_{20}
L	H	16-bit parallel	RGB_{01} to RGB_{05}	Hi-Z Note	RGB_{10} to RGB_{15}	RGB_{21} to RGB_{25}	Hi-Z Note
H	L	6-bit parallel	Hi-Z Note	Hi-Z Note	Hi-Z Note	RGB_{21} to RGB_{25}	RGB_{20}
H	H	Setting prohibited					

Note Hi-Z: High impedance

5.1.2 Selection of data transfer mode

When the 18-bit parallel interface is selected, the length of 1 pixel is fixed to 18 bits. With the 16-bit or 8-bit parallel interface, however, the length of 1 pixel can be selected from 18 or 16 bits (1 pixel = 16 bits when DTX1 = 0, and 1 pixel = 18 bits when DTX1 = 1).

If the 16-bit or 8-bit parallel interface is selected, therefore, several modes of transferring data to the display RAM are selectable. The mode is selected by using the DTX1 register.

[16-bit parallel interface]

<When 1 pixel = 18 bits (DTX1 = 1)>

<1> 16-bit data transfer + 2-bit data transfer

1 pixel = 18-bit data is divided into 16-bit data and 2-bit data for transfer, as shown in Figure 5–3.

<When 1 pixel = 16 bits (DTX1 = 0)>

<2> 16-bit data transfer

Display data of 1 pixel is transferred by one transmission as shown in Figure 5–4. Because 1 pixel is 16 bits long, the number of display colors is limited to 65,536.

[8-bit parallel interface]

< When 1 pixel = 18 bits (DTX1 = 1)>

<1> Transferring 6-bit data three times

1 pixel = 18-bit data is divided into three 6-bit data for transfer, as shown in Figure 5–6.

<Where 1 pixel = 16 bits (DTX1 = 0)>

<2> Transferring 8-bit twice

1 pixel is divided into two 8-bit data for transfer, as shown in Figure 5–7. Because 1 pixel is 16 bits long, the number of display colors is limited to 65,536.

1 pixel of the μPD161801 display RAM consists of 18 bits. If the 16-bit parallel interface is used to transfer 16 bits as 1 pixel (DTX1 = 0), therefore, the data transferred by the CPU (16 bits) runs short by 2 bits, and these 2 bits must be made up for.

For how to do this, refer to **Figures 5–4**, **5–5** and **5–7**.

Table 5–3. Interfaces and Data Transfer Modes

PSX	BWS0	BWS1	BWS2	BWS3	Interface Mode		DTX1	Number of Data of 1 Pixel	Mode of Transferring 1-Pixel Data
L	L	L	L/H Note1	L/H Note1	18-bit parallel		X	18-bit	18-bit transfer
		H			16-bit parallel		1		16-bit + 2-bit transfer
							0	16-bit	16-bit transfer
	H	H			8-bit parallel		1	18-bit	Transferring 6 bits three times
							0	16-bit	Transferring 8 bits twice
H	X	X			8-bit serial		X	16-bit	Transferring 8 bits twice
L/H Note2	H	H	L	L	RGB	18-bit	0/1 Note2	18-bit	18-bit transfer
			L	H		16-bit		16-bit	16-bit transfer
			H	L		6-bit		18-bit	Transferring 6 bits three times

Remark X: Don't care (0 or 1)

Notes 1. The RGB interface that is shared with the i80/M68 parallel interface or serial interface is selected by inputting a low or high level to this pin.

2. The i80/M68 parallel interface or serial interface that is shared with the RGB interface is selected by inputting a low or high level to this pin.

Figure 5–1. Relationship between Bus Data and Display RAM Data (18-bit parallel interface)

Data bus side

18-bit data																	
D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Figure 5–2. Relationship between Bus Data and Display RAM Data (18-bit RGB interface)

Data bus side

18-bit data																	
RGB_{25}	RGB_{24}	RGB_{23}	RGB_{22}	RGB_{21}	RGB_{20}	RGB_{15}	RGB_{14}	RGB_{13}	RGB_{12}	RGB_{11}	RGB_{10}	RGB_{05}	RGB_{04}	RGB_{03}	RGB_{02}	RGB_{01}	RGB_{00}
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Figure 5–3. Relationship between Bus Data and Display RAM Data (1-pixel/18-bit mode [DTX1 = 1], 16-bit parallel interface)

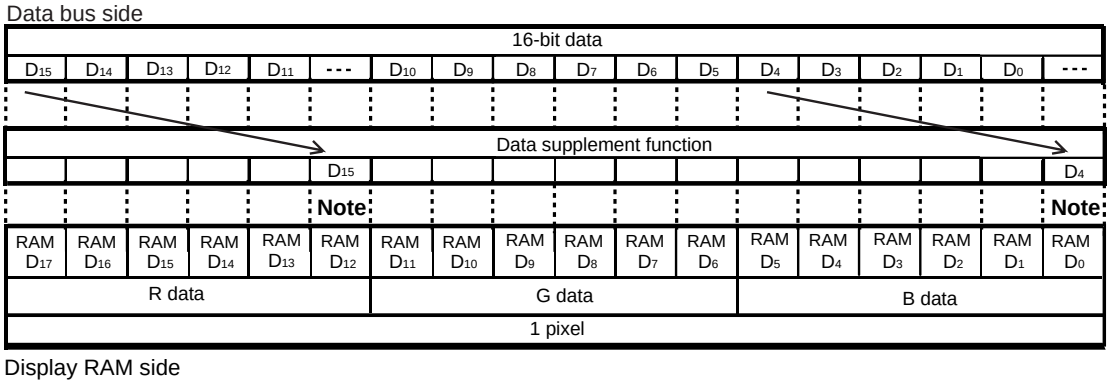
Data bus side

16-bit data																2-bit data	
D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_1	D_0
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

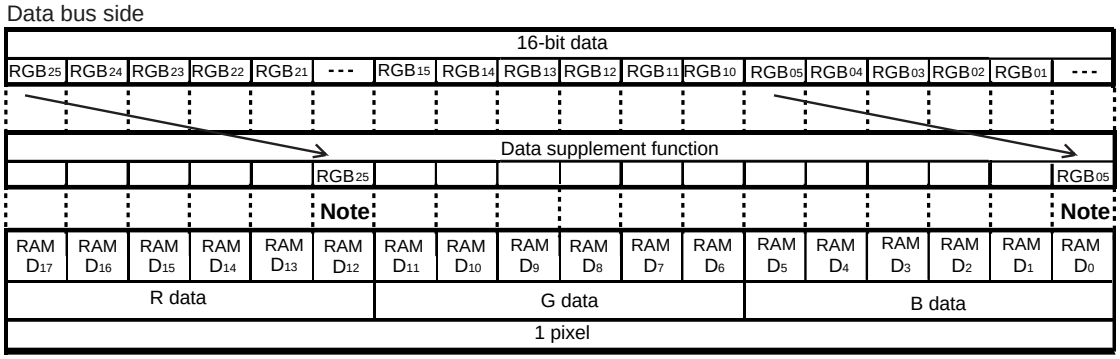
Caution Data D_2 to D_{15} of the second word are treated as invalid data when the 16-bit parallel interface is used.

Figure 5–4. Relationship between Bus Data and Display RAM Data
(1-pixel/16-bit mode [DTX1 = 0], 16-bit parallel interface)



Note When In used 16-bit parallel interface, display RAM data D_{12} and D_0 are supplemented by D_{15} and D_4 of bus data respectively, and written to the display RAM as 18-bit data.

Figure 5–5. Relationship between Bus Data and Display RAM Data (16-bit RGB interface)



Note When In used 16-bit parallel interface, display RAM data D_{12} and D_0 are supplemented by RGB_{25} and RGB_{05} of bus data respectively, and written to the display RAM as 18-bit data.

Figure 5–6. Relationship between Bus Data and Display RAM Data
(1-pixel/18-bit mode [DTX1 = 1], 8-bit parallel interface)

Data bus side

6-bit data						6-bit data						6-bit data					
D_5	D_4	D_3	D_2	D_1	D_0	D_5	D_4	D_3	D_2	D_1	D_0	D_5	D_4	D_3	D_2	D_1	D_0
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Caution Display data D_6 and D_7 of the 8-bit parallel interface are treated as invalid data.

Figure 5–7. Relationship between Bus Data and Display RAM Data
(1-pixel/16-bit mode [DTX1 = 0], 8-bit parallel interface, 8-bit serial interface)

Data bus side

8-bit data									8-bit data								
D_7	D_6	D_5	D_4	D_3	---	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	---
Data supplement function																	
					D_7												D_4
					Note												**Note**
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Note When In used 8-bit parallel interface mode, display RAM data D_0 and D_{12} are supplemented by bit D_7 of the first byte of the bus data and bit D_4 of the second byte of the bus data, and written to the display RAM as 18-bit data.

Figure 5–8. Relationship between Bus Data and Display RAM Data (6-bit RGB interface)

Data bus side

6-bit data						6-bit data						6-bit data					
RGB_{25}	RGB_{24}	RGB_{23}	RGB_{22}	RGB_{21}	RGB_{20}	RGB_{25}	RGB_{24}	RGB_{23}	RGB_{22}	RGB_{21}	RGB_{20}	RGB_{25}	RGB_{24}	RGB_{23}	RGB_{22}	RGB_{21}	RGB_{20}
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Figure 5–9. 16-bit Parallel Interface Data Transfer (1-pixel/18-bit mode [DTX1 = 1])

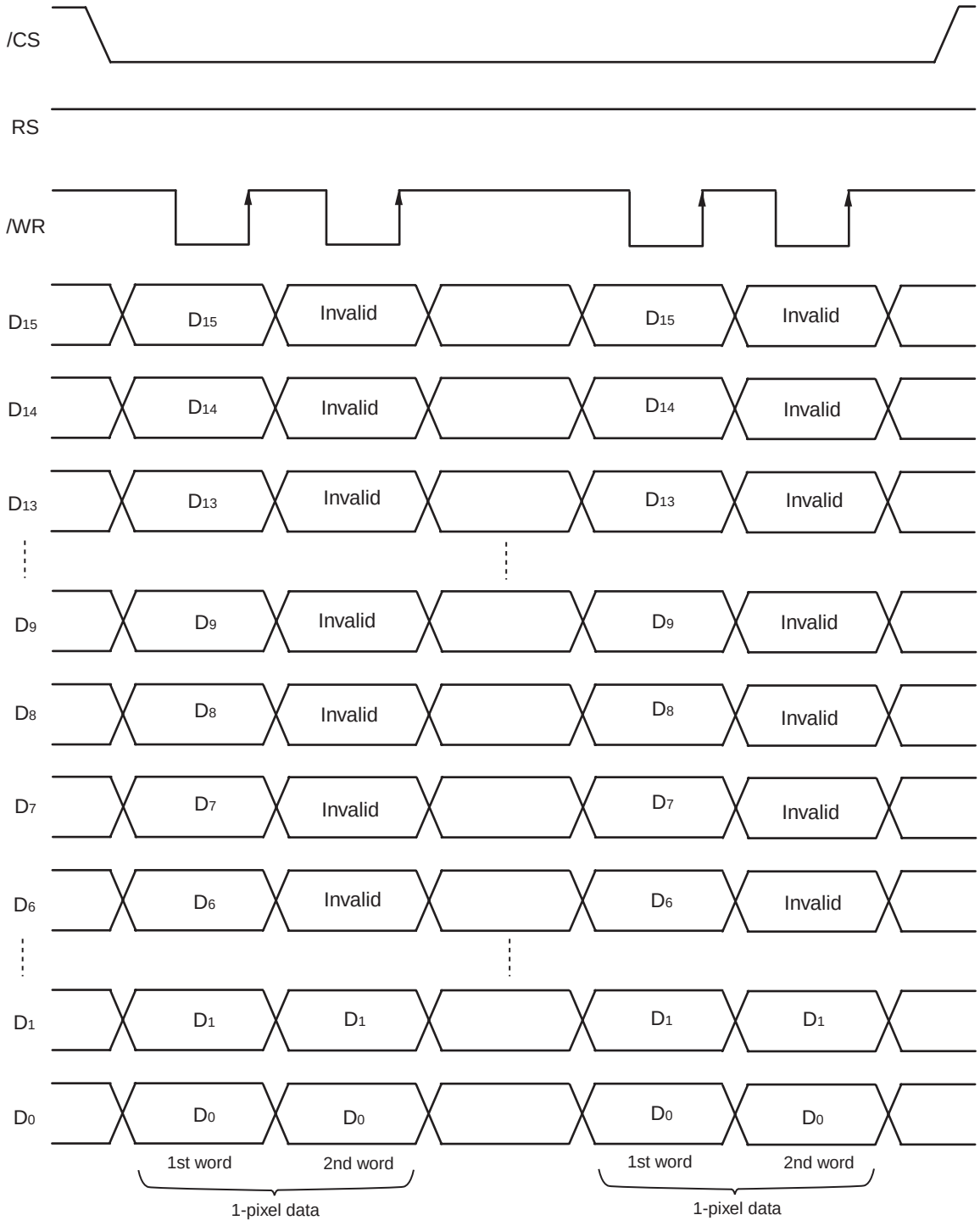


Figure 5–10. 8-bit Parallel Interface Data Transfer (1-pixel/16-bit mode [DTX1 = 0])

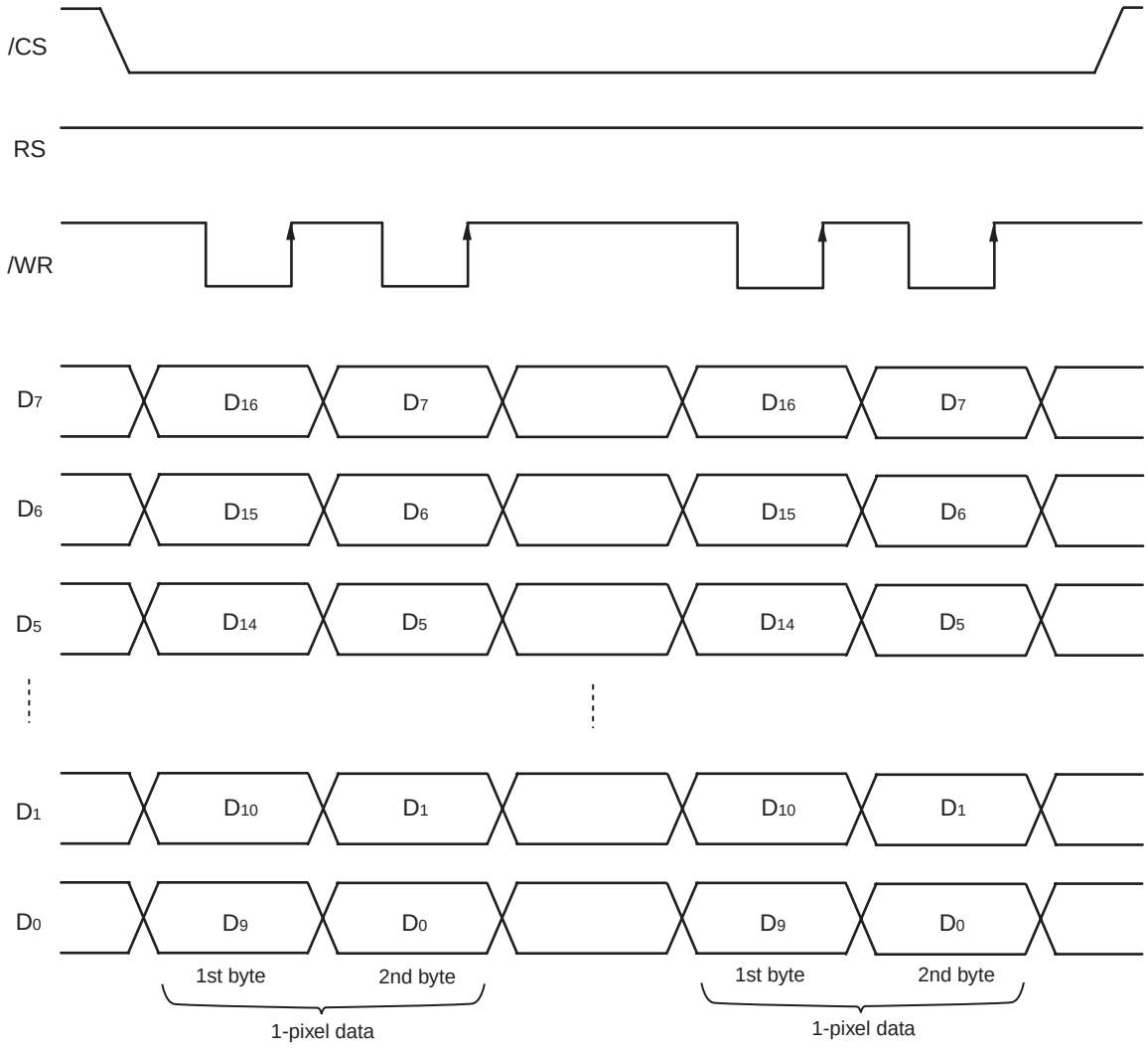
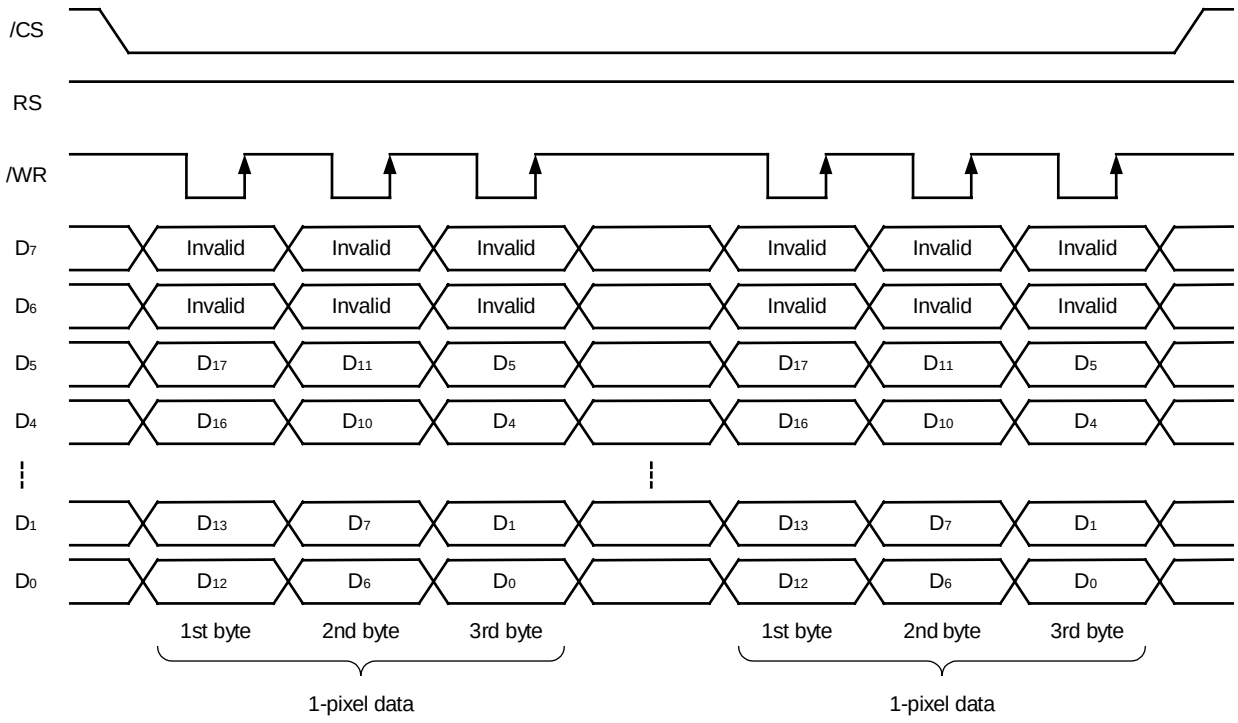


Figure 5–11. 8-bit Parallel Interface Data Transfer (1-pixel/18-bit mode [DTX1 = 1])



5.1.3 RGB interface

The μPD161801 can be directly connected to the RGB interface when bit D_2 of the RGB interface control register (R25 of NWRGB (D_2 bit)) is set to 1.

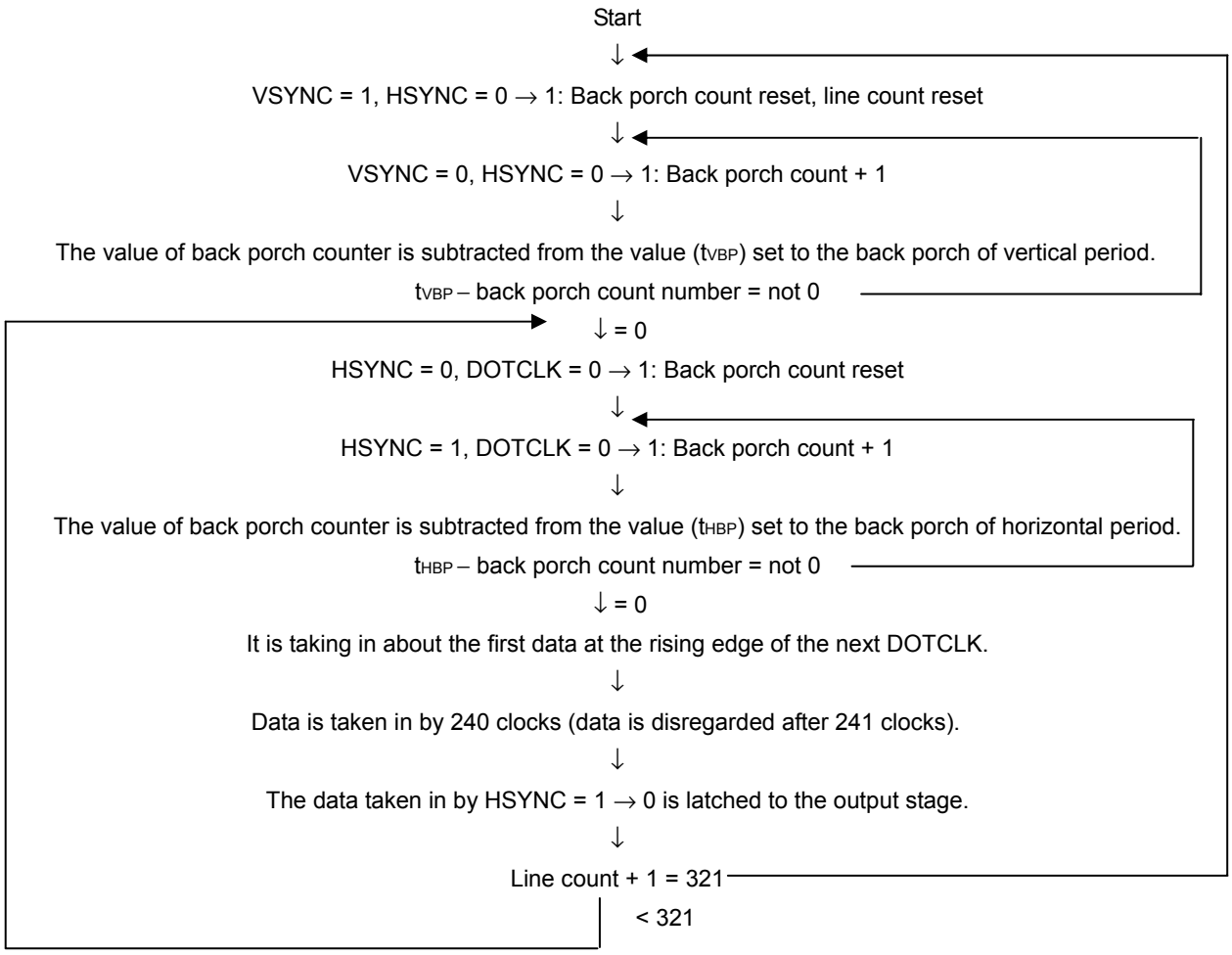
The HSYNC and VSYNC signals establish synchronization in the horizontal and vertical direction, respectively, and data input to the data bus (RGB_{00} to RBG_{05}, RGB_{10} to RGB_{15}, and RGB_{20} to RGB_{25}) is latched in synchronization with DOTCLK. For the electrical specifications, refer to **8. ELECTRICAL SPECIFICATIONS**.

When the RGB interface is selected, the display output timing can be selected from <HSYNC/VSYNC/DOTCLK> or <internal oscillation clock>. It can also be selected whether the data input from the RGB interface is to be written to the display RAM or not.

The mode in which the data input from the RGB interface is not written to the display data RAM and is used for display output is called the through mode (the display output timing is generated by HSYNC/VSYNC/DOTCLK).

The mode in which the data input from the RGB interface is written to the display data RAM for display output is called the capture mode. In the capture mode, the display output timing can be selected from <HSYNC/VSYNC/DOTCLK > or <internal oscillation clock>.

Movement of the μPD161801 when making display output timing into <HSYNC/VSYNC/DOTCLK> is as follows.



Remark VSYNC and HSYNC are both active low and DOTCLK latches data at the rising edge.

In addition, an RGB data invalid mode is also available. In this mode, data input from a motion picture chip via the RGB interface is ignored. Note that only data input from the RGB interface is ignored in this mode and that access from the i80/M68 parallel interface and serial interface is possible.

However, mode selection operates D_0 to D_2 bits of RGB interface control register (R25) on shown as follows.

Table 5–4. RGB Interface Mode Selection

R25			RGB Interface		
D_2	D_1	D_0	Mode Name	Display Output Timing Clock	Writing from RGB Interface to Display Data RAM
1	0	0/1	Through mode	HSYNC/VSYNC/DOTCLK	No
1	1	1	Capture mode	HSYNC/VSYNC/DOTCLK	Yes
1	1	0		Internal oscillation clock	
0	X	1	RGB data invalid mode	HSYNC/VSYNC/DOTCLK	No
		0		Internal oscillation clock	

Remark X: Don't care

When capture mode is selected, DOTCLK is used as a write-in signal to a display data RAM. In addition, X addresses of an address pointer are reset by the HSYNC signal, and an increment is carried out by DOTCLK. Y address is reset by the VSYNC signal and an increment is carried out by the level synchronized signal.

The blanking period can be set by the horizontal back porch register and vertical back porch register. The active levels of HSYNC and VSYNC can be set. In addition, the active level of DOTCLK can also be set. In the through mode, however, the scroll function, partial function, and window access mode cannot be used.

Caution During through mode, the first line of the gate scan is shown as blank. The second and subsequent lines are displayed in accordance with data input from an external source, and so they appear as described below.

Since 320 lines are used as display lines, through mode should not be selected.

Table 5–5. Relation between input data and output display during through mode

Gate Scan	Display Output
First line	Blank
Second line	Data input as first line is displayed
Third line	Data input as second line is displayed
:	:
320th line	Data input as 319th line is displayed

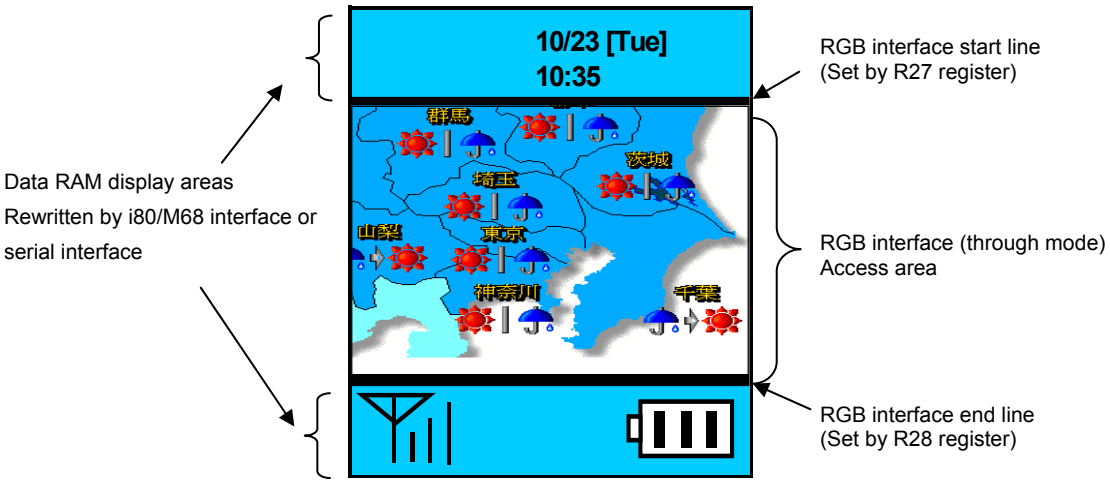
[Example of using RGB interface]

<Through mode>

In the through mode, the area to be displayed by the RGB interface is specified by the RGB interface start line register (R27) and RGB interface end line register (R28). The data written to the display data RAM are displayed in areas other than the RGB interface area.

In the through mode, the display data RAM and registers can be accessed (written or read) by the i80/M68 interface or serial interface when an access is made by the RGB interface.

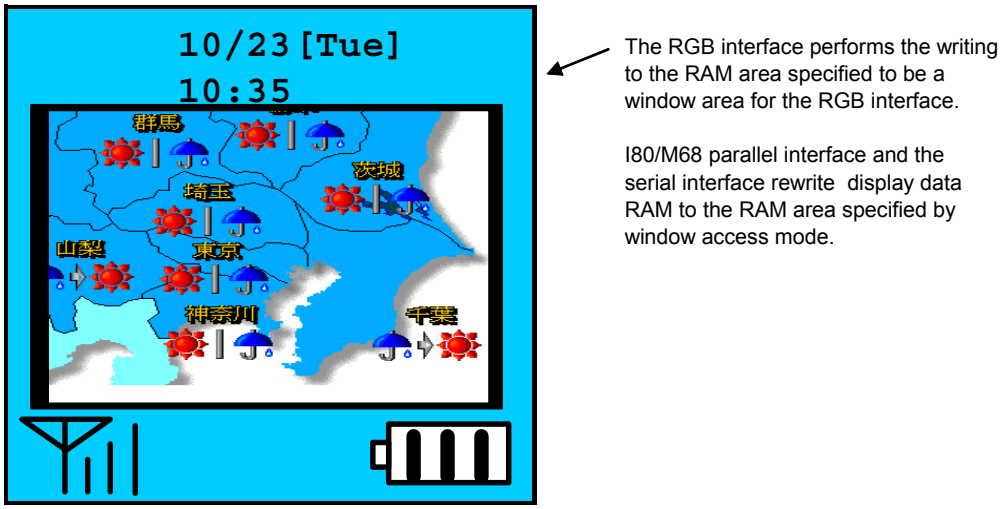
Therefore, an operation such as rewriting the time or antenna by a base band IC while inputting motion picture data from a DSP via the RGB interface can be performed.



<Capture mode>

In the capture mode, the area set in the window access mode is written by the RGB interface (R29 to R32).

Even in this mode, the i80/M68 parallel interface or serial interface, which are shared with the RGB interface, can be used. Note, however, that data can be written to a register while the RGB interface is accessed, but that the RAM cannot be accessed. Make sure that only one of these accesses is made (shift to the RGB data invalid mode so that motion picture data is not input).

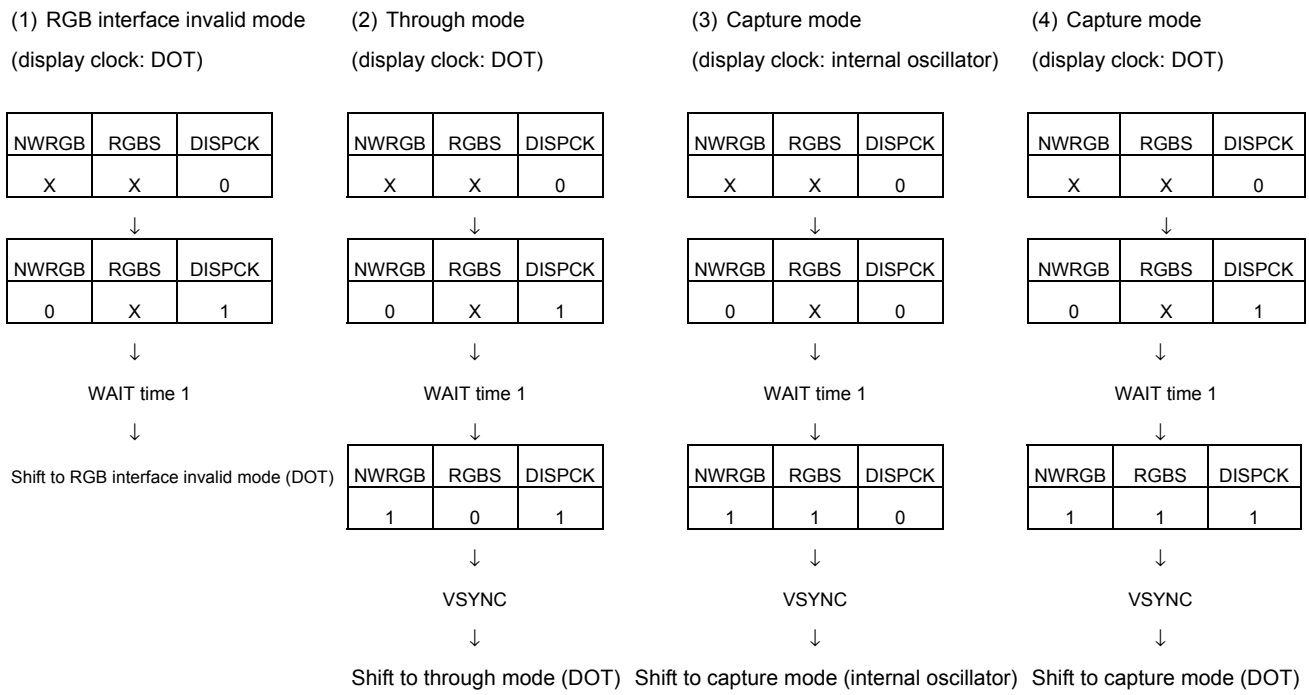


<Notes on using RGB interface>

<1> Be sure to input data from the RGB interface every frame.

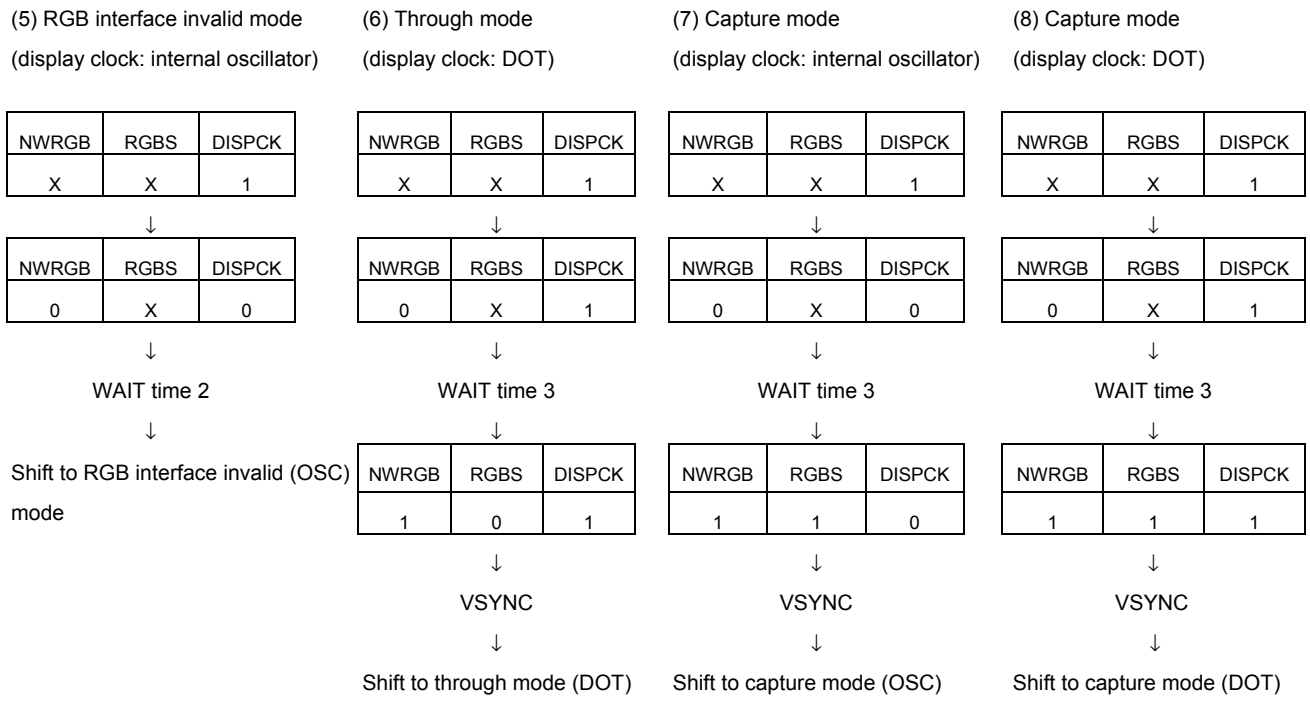
<2> When changing the mode (e.g., from the through mode to the capture mode, and vice versa), issue defined mode of selection command after once always setting RGB invalid mode. For more details, refer to sequence in the below.

<3> It is a shift flow from the time of internal oscillation use (DISPCK = 0) to each mode as a display clock.



Remark WAIT time 1: Set sufficient time of one or more frames.

<4> It is a shift flow from the time of DOTCLK use (DISPCK = 1) to each mode as a display clock.



Remarks 1. WAIT time 2: External clock for two frames is required.

2. WAIT time 3: External clock + VSYNC for one frame is required.

<5> Data (back porch period is included) of one line should be set within the period of HSYNC to HSYNC.

<6> Data (back porch period is included) of one frame should be set within the period of VSYNC to VSYNC.

<7> Do not set access to R25 register into standby mode.

<8> High-speed RAM write mode cannot be used.

<9> INC (D_2 bit of R5) function cannot be used about the writing to the display data RAM at the time of capture mode. However, ADX and an ADR function can be used.

<10> A setup of R6 to R11 is invalid at the time of RGB interface mode (since these are set up of CPU interface).

<11> The period from "the DOTCLK standup after falling of HSYNC" to "the standup of DOTCLK after a HSYNC standup" should not start VSYNC. For more details, refer to the next **Figure 5–12**, **5–13**.

Figure 5–12. Example of HSYNC, VSYNC, DOTCLK Input Timing (both HSYNC and VSYNC are low active)

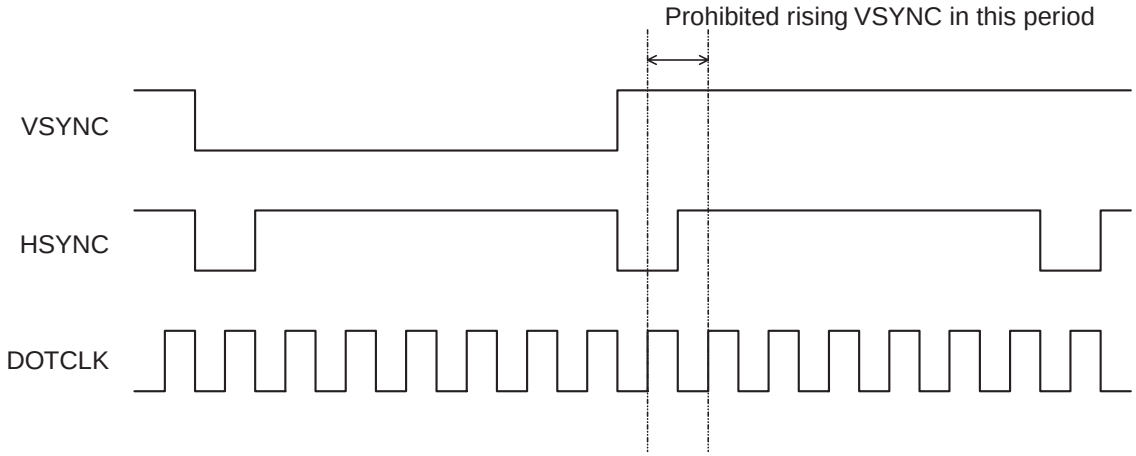
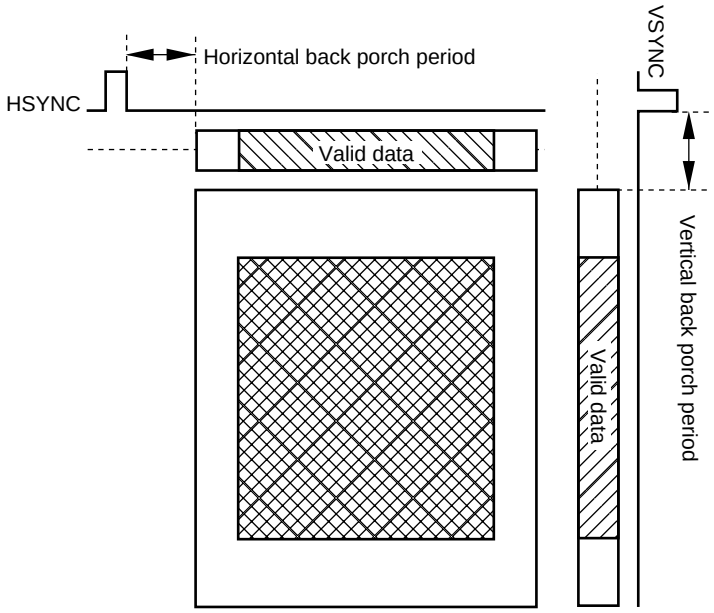


Figure 5–13. HSYNC and VSYNC Input Image Figure (when both HSYNC and VSYNC are high active)



5.1.4 i80/M68 Parallel interface

When the parallel interface has been selected, setting the C86 pin as either H or L enables a direct connection to an i80 series or M68 series CPU (see Table 5–6 below).

Table 5–6.

C86	Mode	/RD (E)	/WR (R, /W)	BWS0	BWS1	D_{17}, D_{16}	D_{15} to D_8	D_7 to D_0
H	M68 series CPU	E	R, /W	L	L	D_{17}, D_{16}	D_{15} to D_8	D_7 to D_0
				L	H	Hi-Z Note	D_{15} to D_8	D_7 to D_0
				H	H	Hi-Z Note	Hi-Z Note	D_7 to D_0
				H	L	Setting prohibited		
L	i80 series CPU	/RD	/WR	L	L	D_{17}, D_{16}	D_{15} to D_8	D_7 to D_0
				L	H	Hi-Z Note	D_{15} to D_8	D_7 to D_0
				H	H	Hi-Z Note	Hi-Z Note	D_7 to D_0
				H	L	Setting prohibited		

Note Hi-Z: High impedance. Leave it open.

The data bus signal is identified according to the combination of the RS, /RD (E), and /WR (R, /W) signals, as shown in the following Table 5–7.

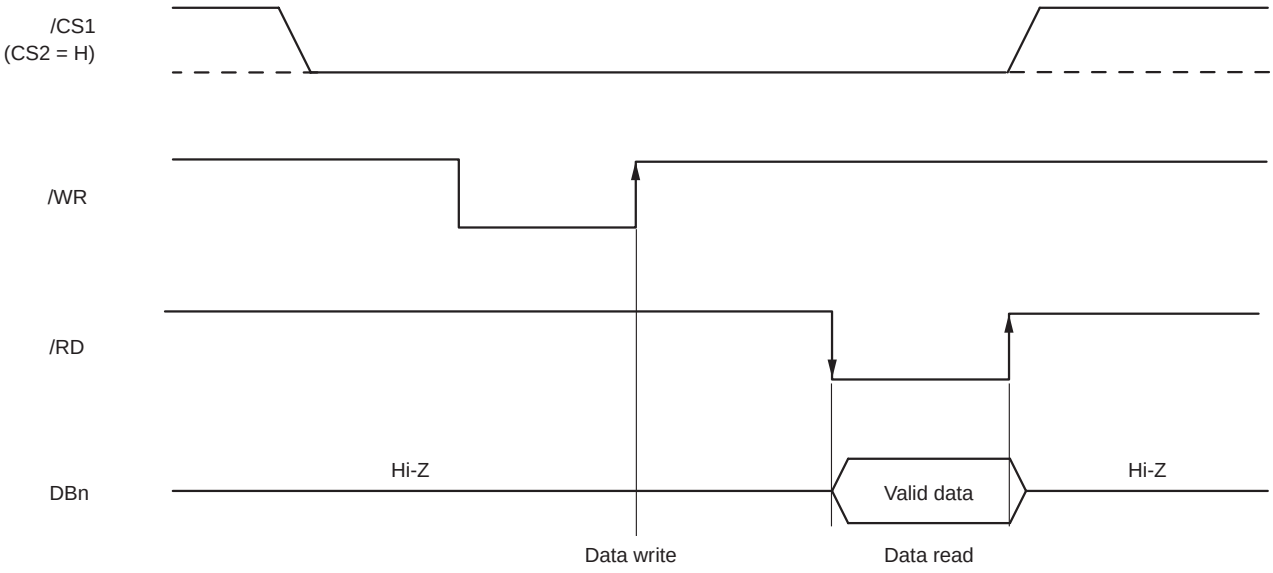
Table 5–7.

Common	M68 series CPU	i80 series CPU		Function
RS	R, /W	/RD	/WR	
H	H	L	H	Read display data
H	L	H	L	Write display data
L	H	L	H	Prohibited
L	L	H	L	Write command

(1) i80 Series Parallel Interface

When i80 series parallel data transfer has been selected, data is written to the μPD161801 at L period of the /WR signal. The data is output to the data bus when the /RD signal is L.

Figure 5–14. i80 Series Interface Data Bus Status

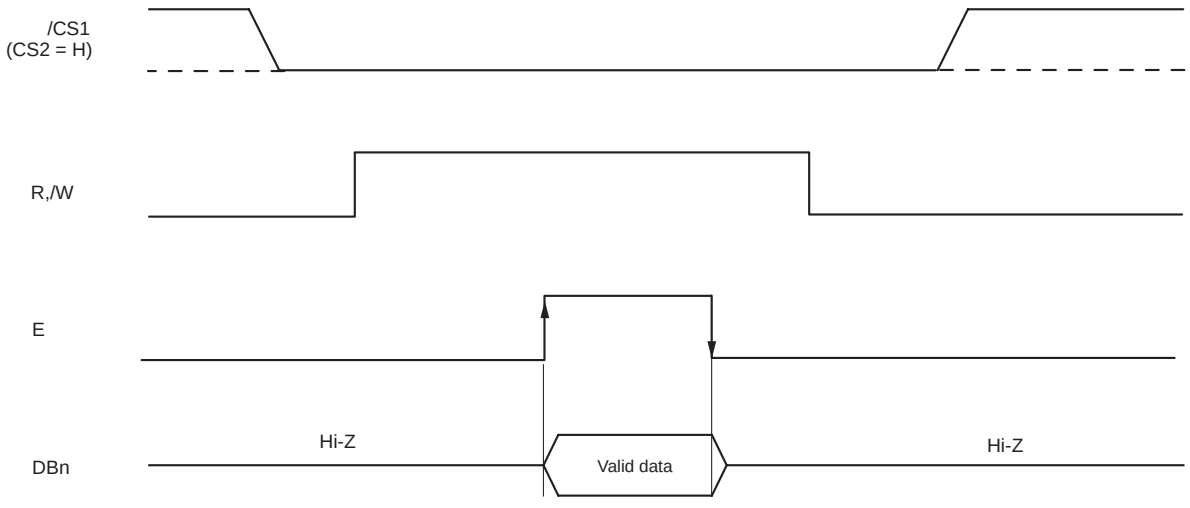


Remark Hi-Z: High impedance

(2) M68 Series Parallel Interface

When M68 series parallel data transfer has been selected, data is written at the H period of the E signal when the R,/W signal is L. In a data read operation, data is output at the rising edge of the E signal in a period when the R,/W signal is H. The data bus is released (Hi-Z) at the falling edge of the E signal.

Figure 5–15. M68 Series Interface Data Bus Status (when data read)



Remark Hi-Z: High impedance

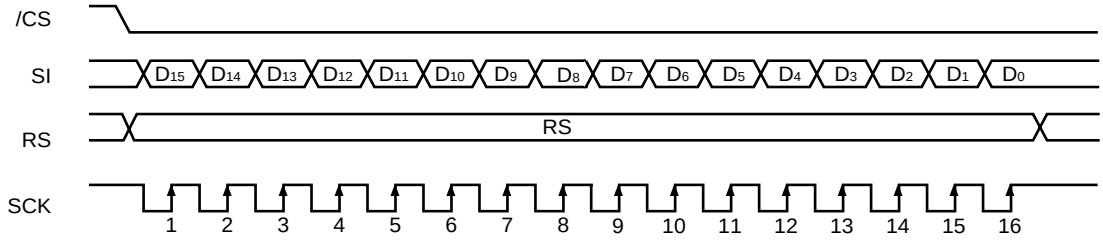
5.1.5 Serial interface

When the serial interface has been selected, if the chip is active (/CS = L), serial data input (SI) and serial clock input (SCL) can be received. Serial data is read from D_{15} and then from D_{14} to D_0 on the rising edge of the serial clock, via the serial input pin. This data is synchronized on the sixteenth serial clock's rising edge and is then converted to parallel data for processing.

RS input is used to judge serial input data as display data when RS = H the data is display data and when RS = L the data is command data. When the chip enters active mode, RS input is read at the rising edge after every sixteenth serial clock and is then used to judge the serial input data.

The serial interface signal chart is shown below.

Figure 5–16. Serial Interface Signal Chart



Remarks 1. If the chip is not active, the shift register and counter are reset to their initial settings.

2. The data read function is disabled during serial interface mode.

3. When using SCL wiring, take care concerning the possible effects of terminating reflection and noise from external sources. Our recommends checking operation with the actual device.

5.1.6 Chip select

The μPD161801 has a chip select pin (/CS). The CPU parallel interface and serial interface can be used only when /CS = L. When the chip select pin is inactive, D_0 to D_{17} are set to high impedance (invalid) and input of RS, /RD, or /WR is not active.

Therefore, keep the chip select pin active for 1 cycle period of data transfer (until a read/write operation has been completed once in the parallel interface mode).

It is not necessary to keep the chip select signal active when successively transferring data. It may be non-active between data transfer operations.

However, note that it is necessary to continue making chip selection active during "a register specification + register value setup" and transmission of "higher rank 8-bit+ low rank 8-bit of RAM" of 16-bit in the case of a serial interface.

5.1.7 Access to display data RAM and internal registers

Figures 5–17 to 5–19 show read/write accesses to the display data RAM and write accesses to internal registers 8-, 16-, and 18-bit parallel interface modes and serial interface mode.

Note that the both display data RAM and registers are not read in the serial interface mode.

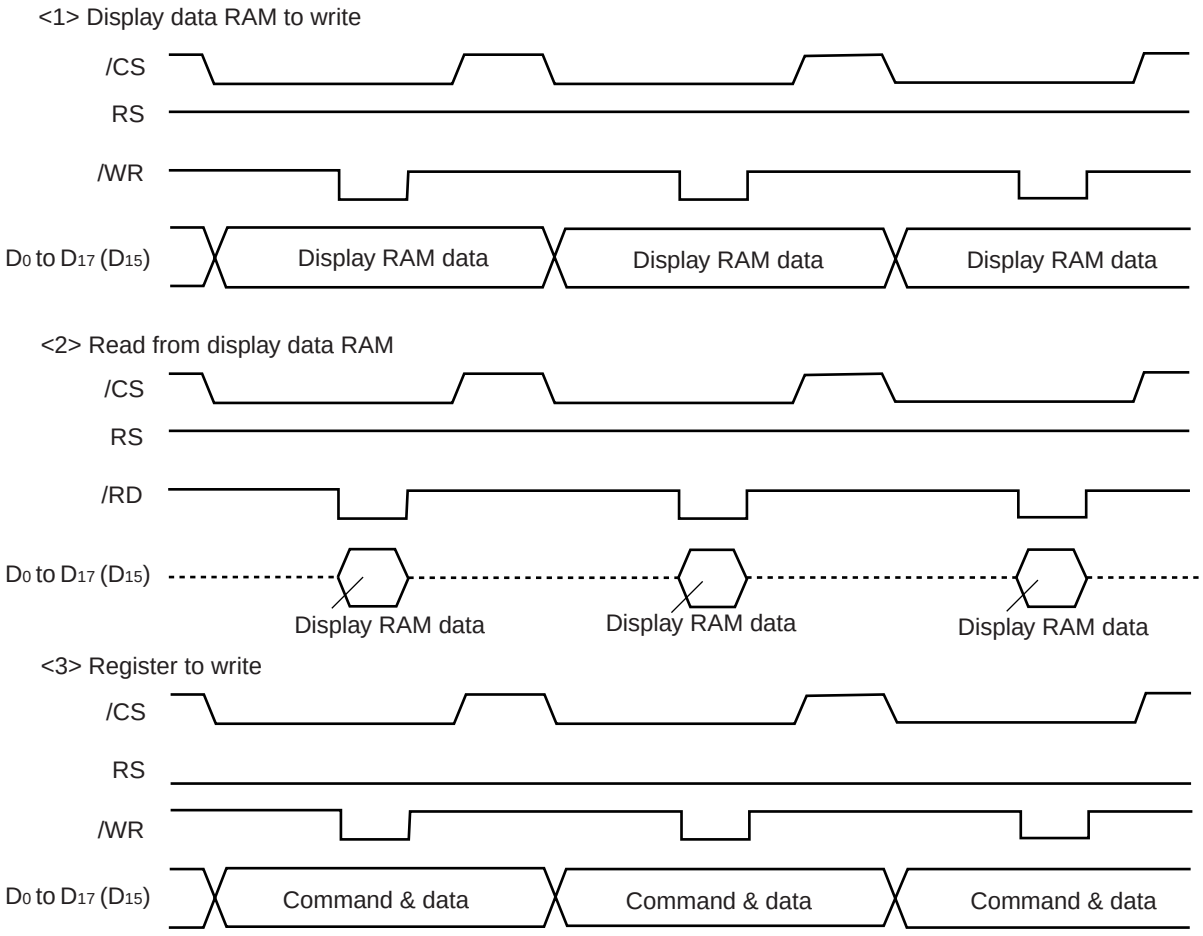
When the CPU accessed the μPD161801, the CPU only has to satisfy the standard requirement of the cycle time (t_{CYC}) and can transfer data at high speeds. Usually, it is not necessary for the CPU to take WAIT time into consideration.

In parallel interface, a high-speed RAM write function, as well as the ordinary RAM write function, is provided for writing data to the display data RAM. By using the high-speed write function, data can be written to the display RAM at an access speed two times faster than that of the ordinary RAM write function. Therefore, applications, such as motion picture display where the display data must be rewritten at high speeds, can be supported. For details, refer to **5.2.4 High-speed RAM write mode**.

No dummy data is necessary for writing data. Dummy data is necessary only when display data is read. This relationship is shown in Figure 5–27.

However, note that even when in write mode of data at high speed for data read mode of read cycle time, this mode equals to normal mode.

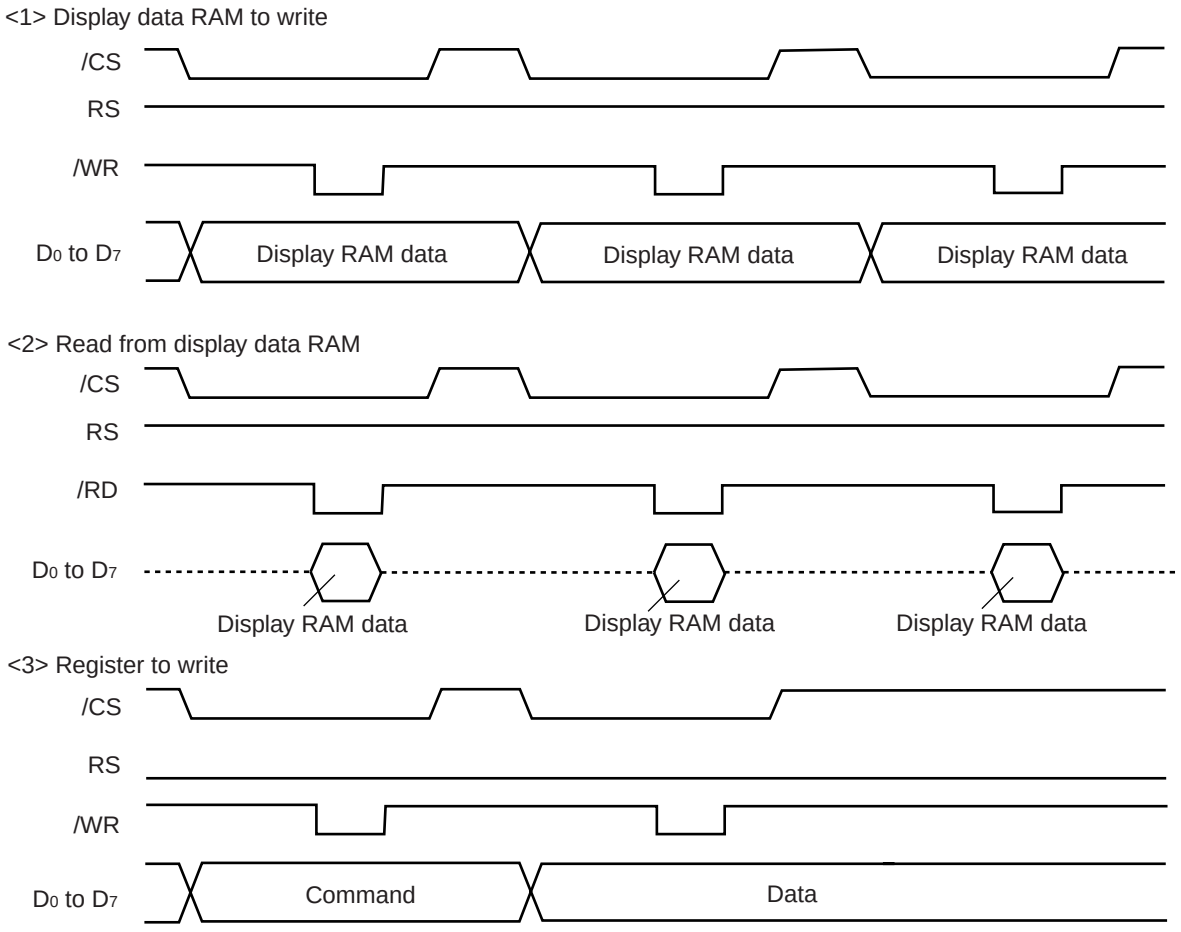
Figure 5–17. Read/Write in 16-/18-Bit Parallel Interface Mode



Cautions 1. While setting the writing to a register, set it the fixed input of the low level to RS pin. While setting the writing to a register, in the case of 16/18-bit parallel interface, 1 cycle period of write cycle is pointed out.

2. While setting the writing to a display data RAM, set it the fixed input of the high level to RS pin. While setting the writing to a display data RAM, in the case of 16/18-bit parallel interface, 1 cycle period of write cycle is pointed out. However, input signal to RS pin fix up to high level until 2-pixel data transfer ends the writing to a display data RAM at the time of high-speed RAM write mode use.

Figure 5–18. Read/Write in 8-Bit Parallel Interface Mode

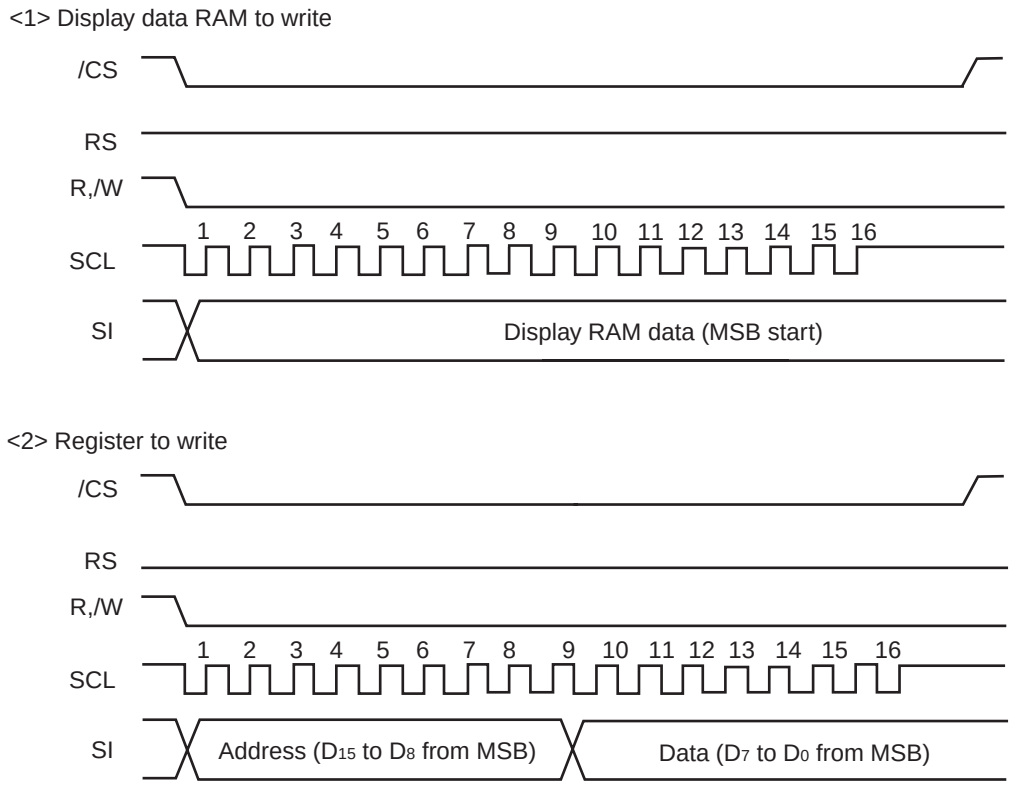


Cautions 1. While setting the writing to a register, set it the fixed input of the low level to RS pin. While setting the writing to a register, "register address specification " + "register data setup" is pointed out.

2. While setting the writing to display data RAM, set it the fixed input of the high level to RS pin. While setting the writing to display data RAM, a "data transfer for 1 pixel" period is pointed out.

3. When use 8-bit parallel interface, RS pin always start transfer after hard reset release, after set up 100 ns MIN. input of high level.

Figure 5–19. Write in Serial Interface Mode

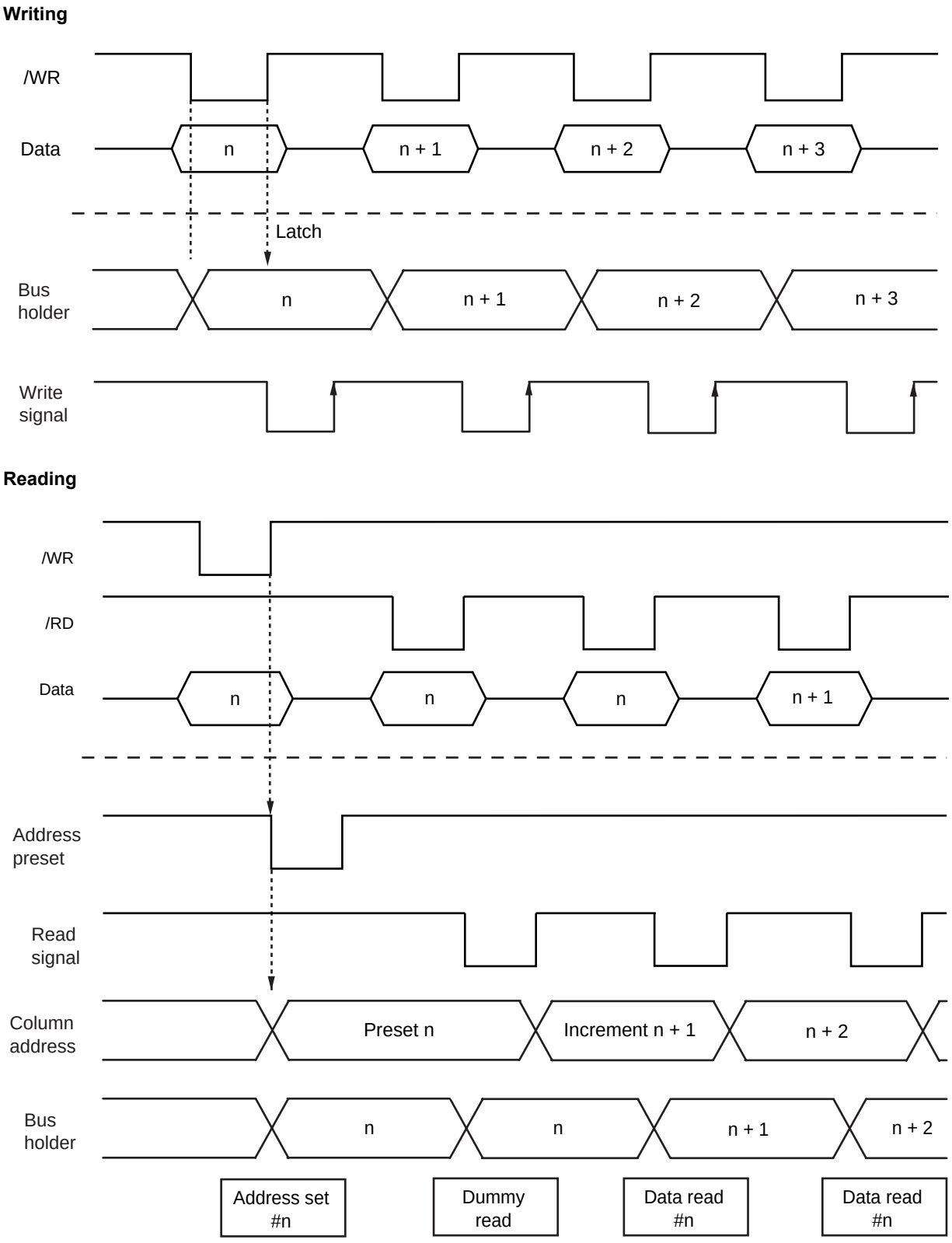


Cautions 1. It is necessary to continue making a tip selection active during "register address specification + register data setting" and transmission of "higher rank 8-bit + low rank 8-bit of RAM" of 16-bit.

2. The period of "register address" + "register data" fix the output to RS pin to low level at the time of the writing to a register.

3. Fix it to the output to RS pin to high level during a 1-pixel data transferring period at the time of the writing to display data RAM.

Figure 5–20. Image of Internal Access to Display RAM



5.1.8 Serial interface for power supply IC control

The μPD161801 builds in the 16-bit serial interface function, in order to perform control for the external connection IC of a power supply IC etc. The following registers and pins are assigned as an object for this function.

Transfer operation is as follows.

Pin Name		Pin Function
PCS	Chip select	When data is written in the register for power supply control, it will become active "L" and the output of data will be started. Moreover, after data transfer is completed, it returns to inactive "H".
PCL	Serial clock	Serial clock output pin
PDA	Serial data	Serial data output pin. Data is outputted in falling of PCL clock signal.

Power supply IC control register list

Rn	Register	RS	R,/W	Data Bit							
				DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8
				DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
R38	Power supply IC control register 1	0	0	0	0	1	0	0	1	1	0
				PSD17	PSD16	PSD15	PSD14	PSD13	PSD12	PSD11	PSD10
R39	Power supply IC control register 2	0	0	0	0	1	0	0	1	1	1
				PSD27	PSD26	PSD25	PSD24	PSD23	PSD22	PSD21	PSD20
R40	Power supply IC control register 3	0	0	0	0	1	0	1	0	0	0
				PSD37	PSD36	PSD35	PSD34	PSD33	PSD32	PSD31	PSD30
R41	Power supply IC control register 4	0	0	0	0	1	0	1	0	0	1
							DC1	DC0			
R42	Power supply IC control register 5	0	0	0	0	1	0	1	0	1	0
				PSD57	PSD56	PSD55	PSD54	PSD53	PSD52	PSD51	PSD50
R60	Power supply IC control register 6	0	0	0	0	1	1	1	1	0	0
				PSD67	PSD66	PSD65	PSD64	PSD63	PSD62	PSD61	PSD60
R61	Power supply IC control register 7	0	0	0	0	1	1	1	1	0	1
				PSD77	PSD76	PSD75	PSD74	PSD73	PSD72	PSD71	PSD70
R62	Power supply IC control register 8	0	0	0	0	1	1	1	1	1	0
				PSD87	PSD86	PSD85	PSD84	PSD83	PSD82	PSD81	PSD80
R63	Power supply IC control register 9	0	0	0	0	1	1	1	1	1	1
				PSD97	PSD96	PSD95	PSD94	PSD93	PSD92	PSD91	PSD90
R64	Power supply IC control register 10	0	0	0	1	0	0	0	0	0	0
				PSDA7	PSDA6	PSDA5	PSDA4	PSDA3	PSDA2	PSDA1	PSDA0
R65	Power supply IC control register 11	0	0	0	1	0	0	0	0	0	1
				PSDB7	PSDB6	PSDB5	PSDB4	PSDB3	PSDB2	PSDB1	PSDB0

<Transfer operation>

By 3-line serial interface, data is transferred per 16 bits. Shift operation of serial interface is performed after chip select signal output (PCS = L) synchronizing with falling of a serial clock (PCL). The data format to the external connection IC serves as data which is set the 1st byte of transfer data as a command (register number), and is set as a command the 2nd byte. Transfer is performed at MSB first.

The start trigger of serial data transfer is the writing of the data to above-mentioned "power supply IC control" each control register. Writing of the data to each control register starts an output from PCS, PCL, and PDA automatically.

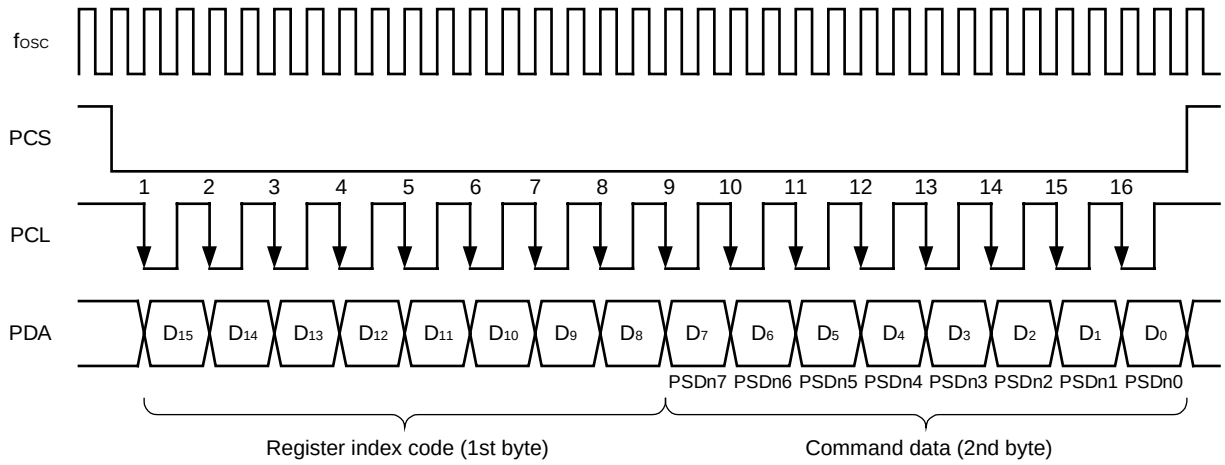
After reset command is inputted, IC connected to the μPD161801, such as a power supply IC, needs to recognize the 1st byte of data transferred to be a command (index register), and needs to recognize the 2nd byte of data to be data (data register) to a command.

In addition, when performing the writing to the register for power supply control continuously, after pre-serial data transmission is completed, it is necessary to perform.

The continuation writing to a power supply control register should set and perform weight time of minimum 250 μs.

When the data to the register for power supply control is written in during serial data transfer, the data transfer written in data and the register during transfer is not guaranteed.

Figure 5–21. Serial Interface Timing Chart for Power Supply IC Control



5.2 Display Data RAM

This RAM stores dot data for display and consists of 4,320 bits (240 x 18) x 320 bits. Any address of this RAM can be accessed by specifying an X address and an Y address.

Display data RAM construction refers to **Figure 5–22**.

Figure 5–22. Display Data RAM

D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
R data						G data						B data					
Pixel 1 (= 1 X address)																	

LCD panel	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8	
	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8	
	000H	001H	002H	003H	004H	005H	006H	007H	

5.2.1 X address circuit

The X address of the display data RAM is specified by using the X address register (R6) as shown in Figure 5–24. The specified X address is incremented by one each time display data is written or read.

In the X address increment mode, the X address is incremented up to 0EFH. If more display data is written or read, the Y address is incremented, and the X address returns to 000H.

The relationship between the X address and source output can be inverted by the ADX flag of control register 1 as shown in Figure 5–23. After switched ADX, the input data can be rotated 90 degrees and displayed by changing the ADR function and address increment direction between X and Y.

5.2.2 Y address circuit

The Y address of the display data RAM is specified by using the Y address register (R7) as shown in Figure 5–24.

The Y address is incremented each by one when one each time display is written or read and X address is incremented to last address.

When the Y address has been incremented up to 13FH and the X address up to the final address, if further display data is read or written, the X and Y addresses return to 000H.

As shown in Figure 5–23, the relationship between the Y address and gate output can be inverted by the ADR flag of the control register. The data written to the display can be rotated 90 degrees and output by changing the ADX function and address increment direction between X and Y.

Table 5–8. Data Access Control (R5) Setting

INC	Setting
0	Time of data access X directions an address continuing an increment or a decrement is carried out.
1	Time of data access Y directions an address continuing an increment or a decrement is carried out.

Caution When the access direction is changed, be sure to access Display RAM from INC after setting up X address register (R6) and Y address register (R7).

Figure 5–23. Example of 90-Degree Rotation

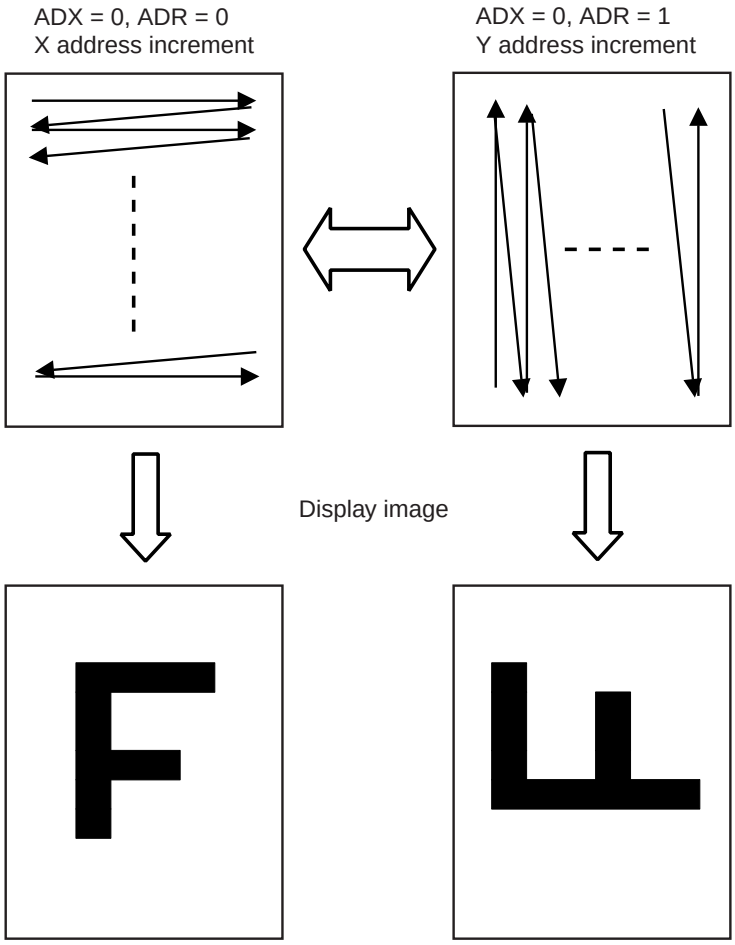


Figure 5–24. The μPD161801 RAM Addressing

(1) ADX = 0

Source output	Y_1			Y_2			---	---	Y_{239}			Y_{240}		
X-address	000H			001H			---	---	0EEH			0EFH		
	D_{17} to D_{12}	D_{11} to D_6	D_5 to D_0	D_{17} to D_{12}	D_{11} to D_6	D_5 to D_0			D_{17} to D_{12}	D_{11} to D_6	D_5 to D_0	D_{17} to D_{12}	D_{11} to D_6	D_5 to D_0

Y-address	
ADR = 0	*ADR = 1*
000H	13FH
001H	13EH
078H	07BH
079H	07AH
07AH	079H
07BH	078H
13EH	001H
13FH	000H

Display area

(2) ADX = 1

Source output	Y_1			Y_2			---	---	Y_{239}			Y_{240}		
X-address	0EFH			0EEH			---	---	001H			000H		
	D_{17} to D_{12}	D_{11} to D_6	D_5 to D_0	D_{17} to D_{12}	D_{11} to D_6	D_5 to D_0			D_{17} to D_{12}	D_{11} to D_6	D_5 to D_0	D_{17} to D_{12}	D_{11} to D_6	D_5 to D_0

Y-address	
ADR = 0	*ADR = 1*
000H	13FH
001H	13EH
078H	07BH
079H	07AH
07AH	079H
07BH	078H
13EH	001H
13FH	000H

Display area

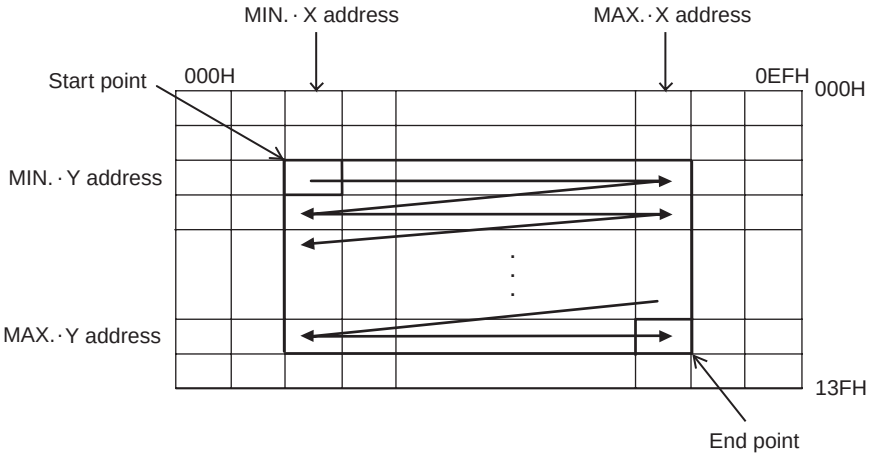
5.2.3 Arbitrary address area access (window access mode (WAS))

With the μPD161801, any area of the display RAM selected by the MIN.·X/Y address registers (R8 and R10) and MAX.·X/Y address registers (R9 and R11) can be accessed.

First, select the area to be accessed by using the MIN.·X/Y address registers and MAX.·X/Y address registers. When WAS of data access control register (R5) is set to 1, the window access mode is then selected. The address scanning setting is also valid in this mode, in the same manner as when data is normally written to the display RAM. In addition, data can be written from any address by specifying the X address register (R6) and Y address register (R7).

The data input from the RGB interface in the through mode of the RGB interface cannot be used in the window access mode.

Figure 5–25. Example of Incrementing Address when in Window Access Mode



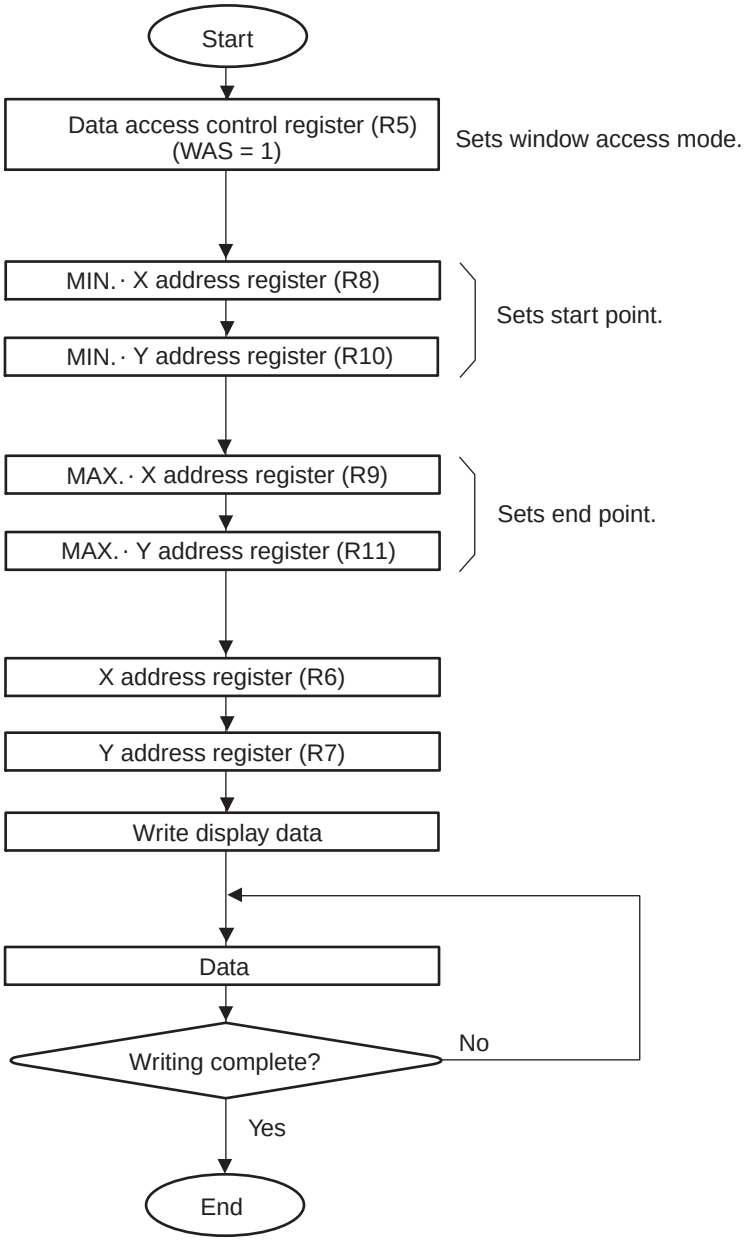
Cautions 1. When using the window access mode, the relationship between the start point and end point shown in the table below must be established.

Item	Address Relationship
X address	000H ≤ MIN.·X address ≤ X address (R6) MAX.·X address ≤ 0EFH
Y address	000H ≤ MIN.·Y address ≤ Y address (R7) MAX.·Y address ≤ 13FH

2. If invalid address data is set as the MIN./MAX.· address, operation is not guaranteed.

3. Do not specify any value other than the address value 2n – 2 (n = 1 to 120) for the X address in the high-speed RAM access mode. The operation is not guaranteed if invalid address data is set.

Figure 5–26. Example of Sequence in Window Access Mode



5.2.4 High-speed RAM write mode

With the μPD161801, two types of access modes can be selected for accessing the display RAM.

The μPD161801 has a high-speed RAM write function, as well as an ordinary RAM write function. By using the high-speed write function, data can be written to the display RAM at an access speed two times faster than that of the ordinary RAM write function. Therefore, applications, such as motion picture display where the display data must be rewritten at high speeds, can be supported.

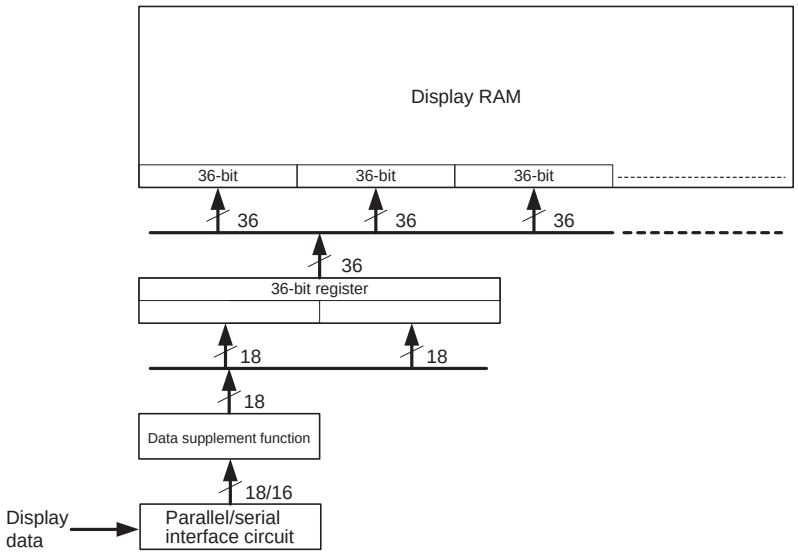
When the high-speed RAM write mode is selected by using BSTR of the data access control register (R5), data is temporarily stored in an internal register of the μPD161801. When data of 36 bits (18 bits x 2) has been stored in the register, it is written to the display RAM. It is also possible to write the next data to the internal register while the first data is being written to the RAM.

In the high-speed RAM write mode, however, the CPU must transmit data in units of 2 pixel data (1-pixel/18-bit mode: 36-bit, 1-pixel/16-bit mode: 32-bit) have been written to the internal register. If data of less than 2-pixel data is transmitted in the high-speed RAM write mode, this data is not written to the display RAM. Therefore, CPU data is not reflected on the LCD display even if it is transmitted. In this case, the data that is not reflected remains stored in the register. When the next data is transferred, it is written to the register from where the preceding data is stored.

However, if the RS signal is changed (RS = L) in the middle of data transfer, and then asserted active again and when the display data write is set, the register is initialized. Consequently, the data stored in the register is lost.

It is therefore recommended to transmit display data in 2-pixel units when using the high-speed RAM write mode.

Figure 5–27. Image of Operation in High-speed RAM Write Mode



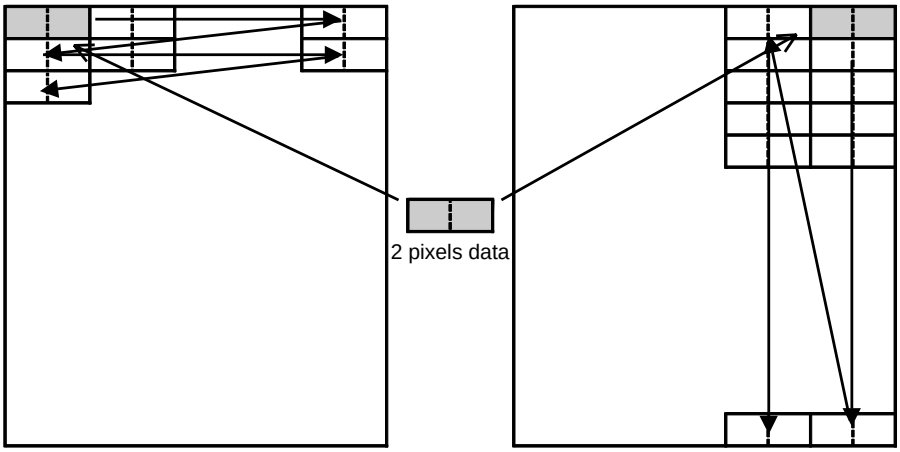
Cautions 1. Do not specify any value other than the address value 2n – 2 (n = 1 to 120) for the X address register (R6) in the high-speed RAM access mode. The operation is not guaranteed if invalid address data is set.

2. Burst mode cannot be used about each mode of 8-bit parallel interface, serial interface, and RGB interface.

3. This write-in mode is effective only at the time of 16-/18-bit parallel interface package data transfer mode.

Note that it writes in 2 pixels at a time perpendicularly at the time of Y address increment mode as shown in Figure. 5–28.

Figure 5–28. Image of Operation Accompanying Difference in the Direction of an Address Increment at the Time of High-speed RAM Write Mode



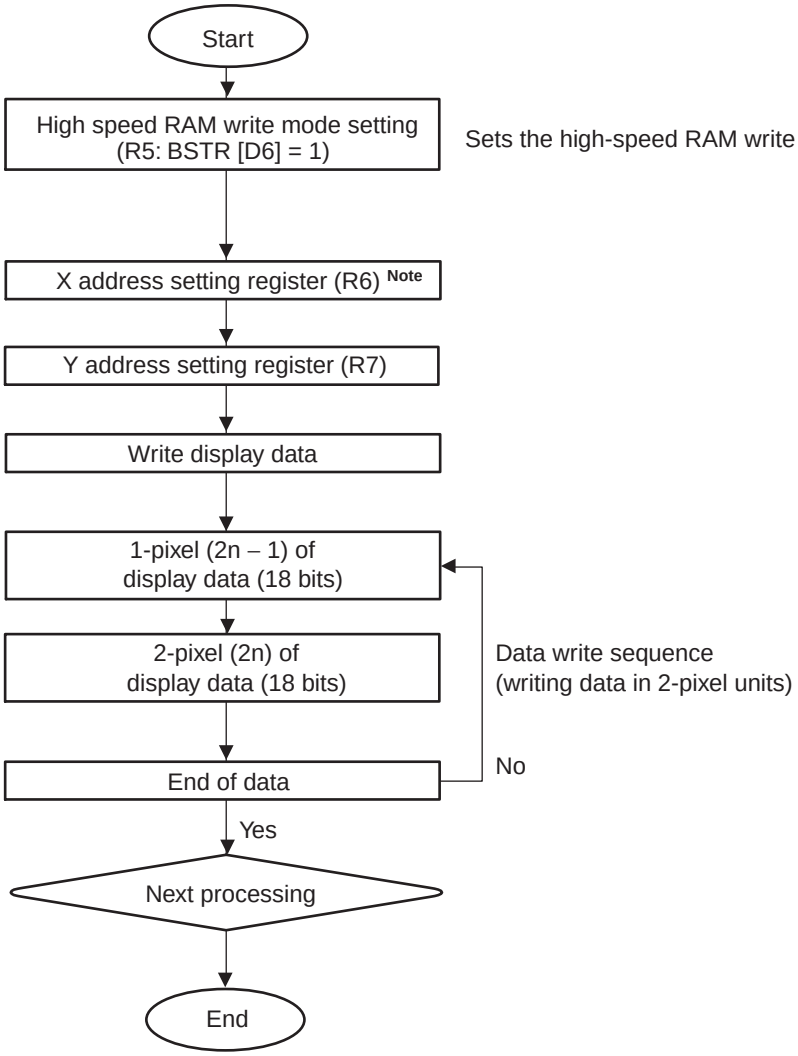
X address increment mode
(D_2 of R5 = 0)

Writing is set in the direction of
X address every 2 pixels.

Y address increment mode
(D_2 of R5 = 1)

Writing is set in the direction of
Y address every 2 pixels.

Figure 5–29. Example of Sequence in High-Speed RAM Write Mode (when 18-Bit Parallel Interface)



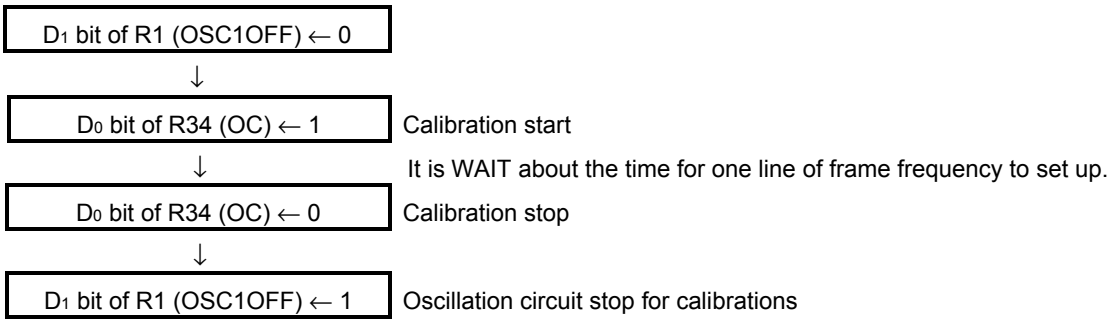
Remark n: n ≥ 1

Note Do not specify any value other than the address value 2n – 2 (n = 1 to 120) for the X address (R6) in the high-speed RAM access mode. The operation is not guaranteed if invalid address data is set.

5.3 Oscillator

The μPD161801 can select from built-in oscillation circuit (OSCSEL = L: type with built-in CR), or an external oscillation circuit (OSCSEL = H: CR external) the oscillation circuit which generates display clock by setup of an OSCSEL pin.

The μPD161801 also has two CR oscillators (with external R), which generate the display clock. One oscillation circuit (OSC2) is used in order to generate liquid crystal display output timing, and another oscillation circuit (OSC1) is used for it at the time of calibration execution of frame frequency. A calibration execution flow is shown below.



Since the oscillation circuit for calibrations comes to unnecessary after calibration execution, in order to lower power consumption, suspend an oscillation ("1" is set to OSC1OFF of D_1 bit of R1). In addition, when set calibration again once performing a calibration, start oscillation operation again.

Moreover, the frame frequency by which the calibration was carried out is eliminated by command reset. Therefore, when command reset is input, set a calibration again.

Be sure to connect the capacitor of T.B.D. μF to an OSCR pin with resistance of T.B.D. μF at an OSCC pin at the time (OSCSEL = H) of external oscillation circuit selection. When internal oscillator has been selected, leave both pins open.

5.4 Display Timing Generator

The display timing generator generates the timing signals for the internal timing of the source driver and for the panel gate.

5.4.1 1-line period timing

The μPD161801 has two drive system timing output circuits. Following preparation of these drive system timing output is carried out, and a usually different timing signal at the time of a drive and a partialness drive is generated.

	Timing Circuit 1	Timing Circuit 2	Remark
Gate circuit clock signal	GCLK	CKV	Fixed timing
Gate circuit start pulse signal	GSTB	STV	Fixed timing
Multi-plectra switch signal 1	RSW	ASW1	R83, R84
Multi-plectra switch signal 2	GSW	ASW2	R85, R86
Multi-plectra switch signal 3	BSW	ASW3	R87, R88
Gate output enable signal 1	GOE_1	OEV	R79, R80
Gate output enable signal 2	GOE_2	OEVE	RGOE2, ROEVE [R77]
Extended timing signal 1	EXT1		R89, R90
Extended timing signal 2	EXT2		R91, R92
Pre-charge signal P	PC		R81, R82

The clock set up by the calibration function is being used for the clock of one-line period, and it is generating all timing by using 40 clocks as a base.

Calibration function is assigning 40 clocks and is adjusting frame frequency to within a time of the one line period set up by calibration time (t_{cal}).

Moreover, the number of clocks of one-line period can be set up by the one-line period clock setting register (R76). The number of clocks set up by R76 is inserted as dummy clock from one-line period 38 clock.

Figure 5–30. 1-line Driving Period 1

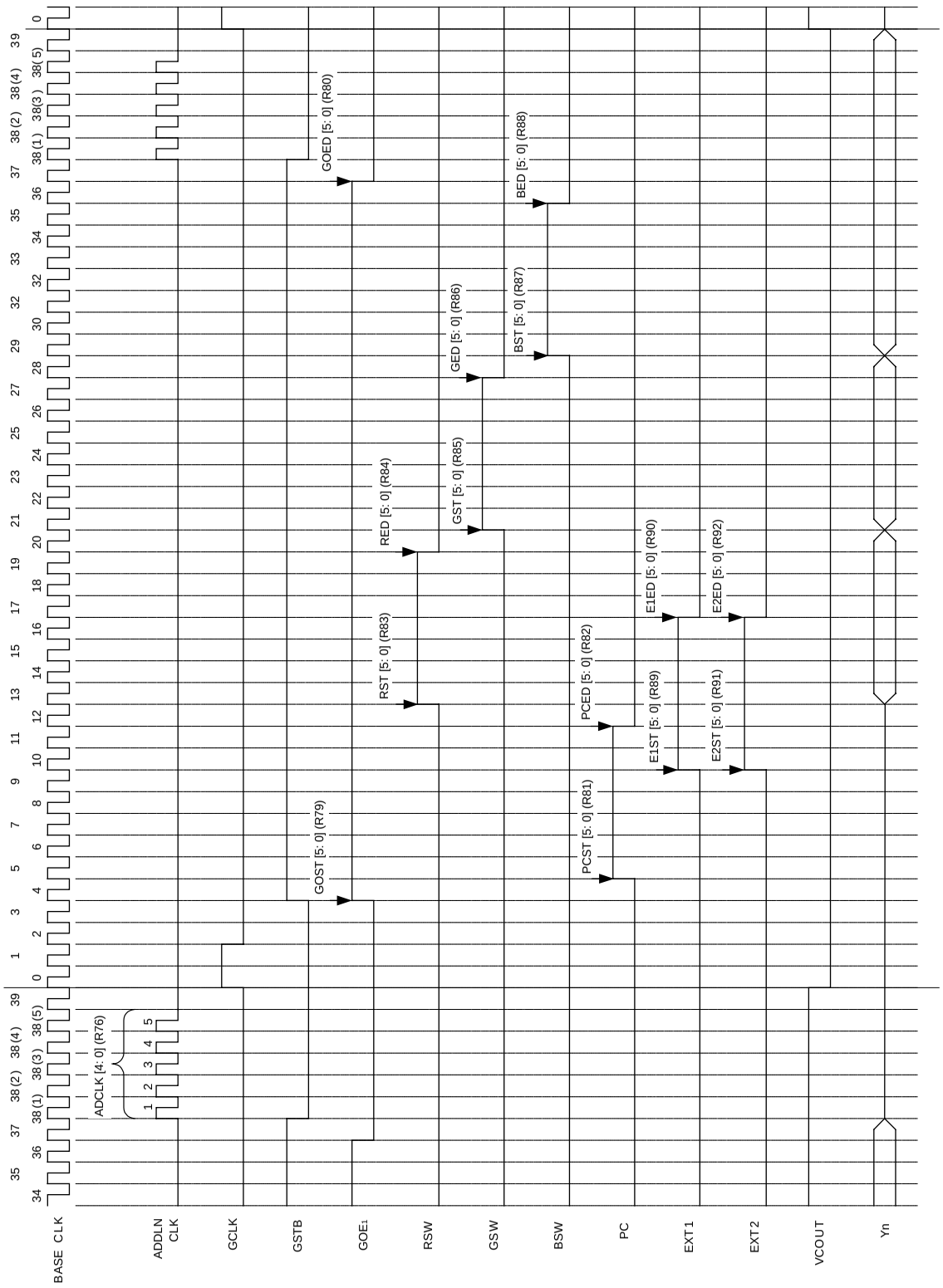
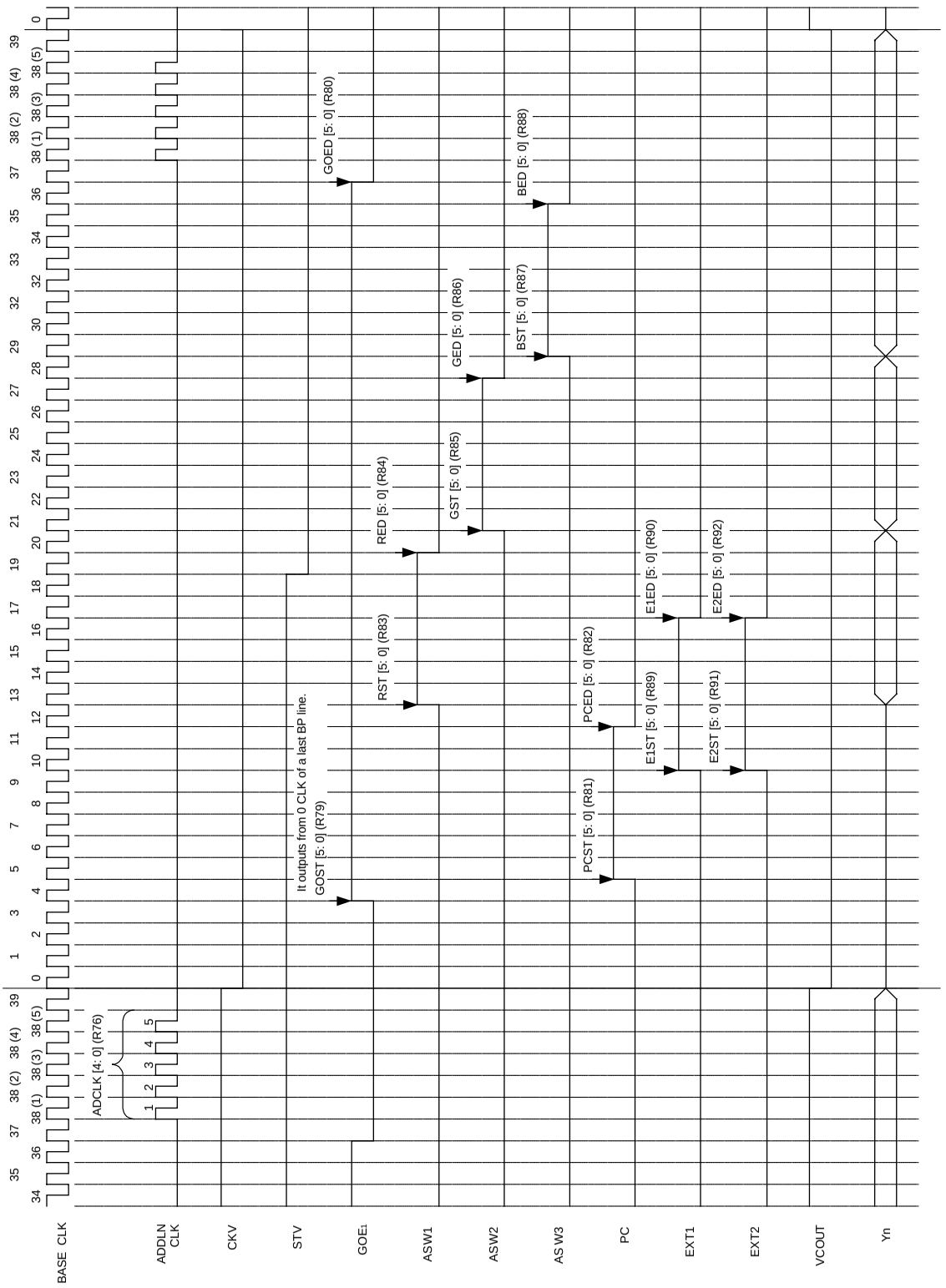


Figure 5–31. 1-line Driving Period 2

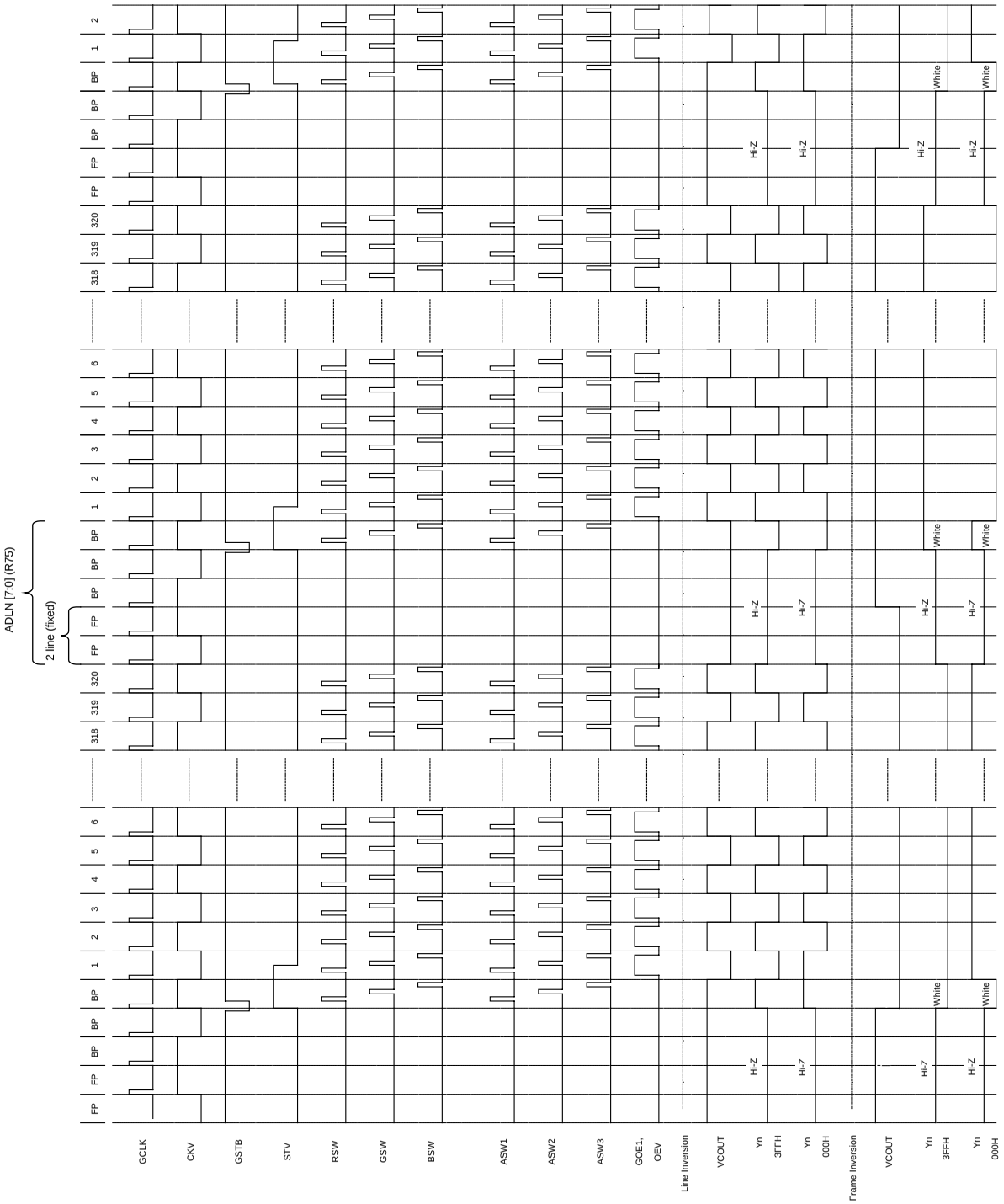


5.4.2 1-frame period timing

The μPD161801 has two driving system timing output circuits. For details, refer to the **5.4.1 1-line period timing**.

Those signals are the timing at the time of ON/OFF and a standby setup etc., and are controlled by different timing control flag. Refer to **5.8 Power Supply Sequence** and **5.9 Standby and Power Supply OFF Sequence**.

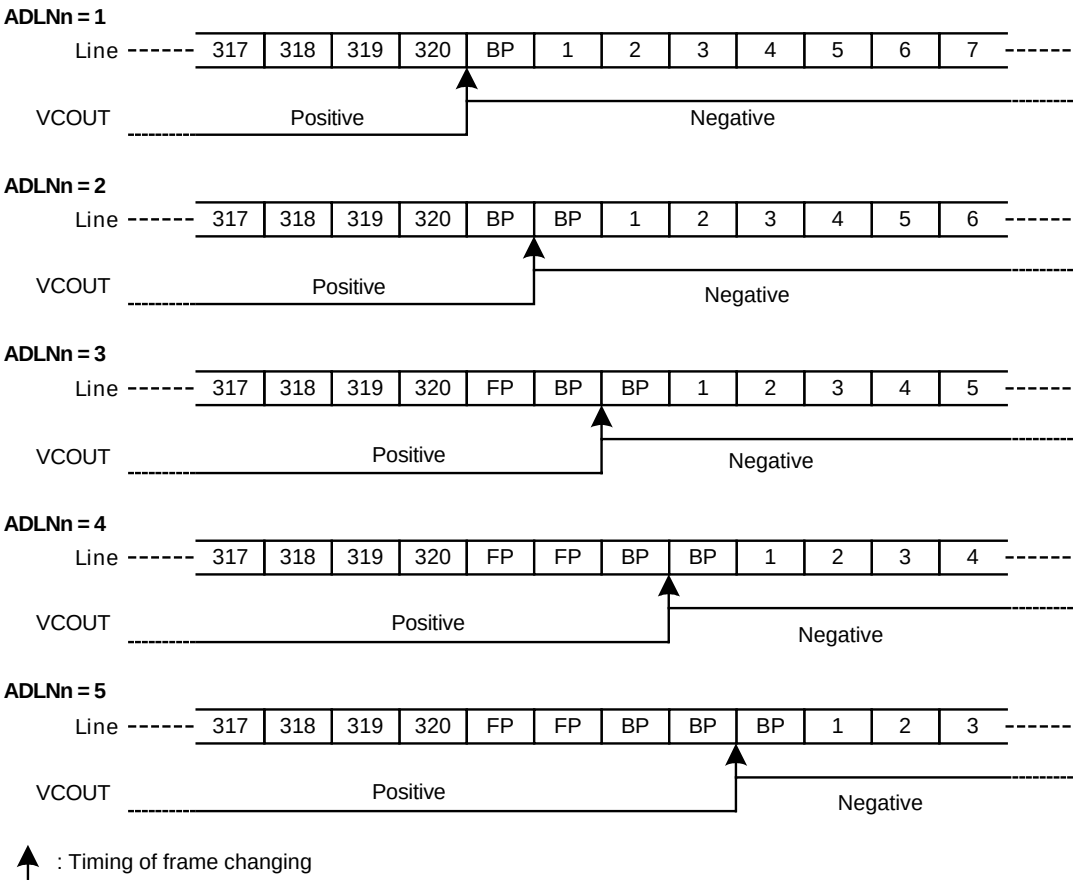
Figure 5–32. 1-frame Driving Period 2



Moreover, the one-frame period is constituted by 320 line + front porch period (FP) + back porch (BP), and the number of lines of a FP + BP period can be set up by the blanking period line setting register (R75: ADLNn). At this time, a frame changes and timing is performed during the back porch of the 1st line. Refer to the following Table and Figure 5–33.

ADLN7	ADLN6	ADLN5	ADLN4	ADLN3	ADLN2	ADLN1	ADLN0	Setting Line Number	
								FP	BP
0	0	0	0	0	0	0	0	Prohibited	
0	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	1	0	0	2
0	0	0	0	0	0	1	1	2	1
0	0	0	0	0	1	0	0	2	2
0	0	0	0	0	1	0	1	2	3
				⋮				⋮	⋮
1	1	1	1	1	1	1	0	2	252
1	1	1	1	1	1	1	1	2	253

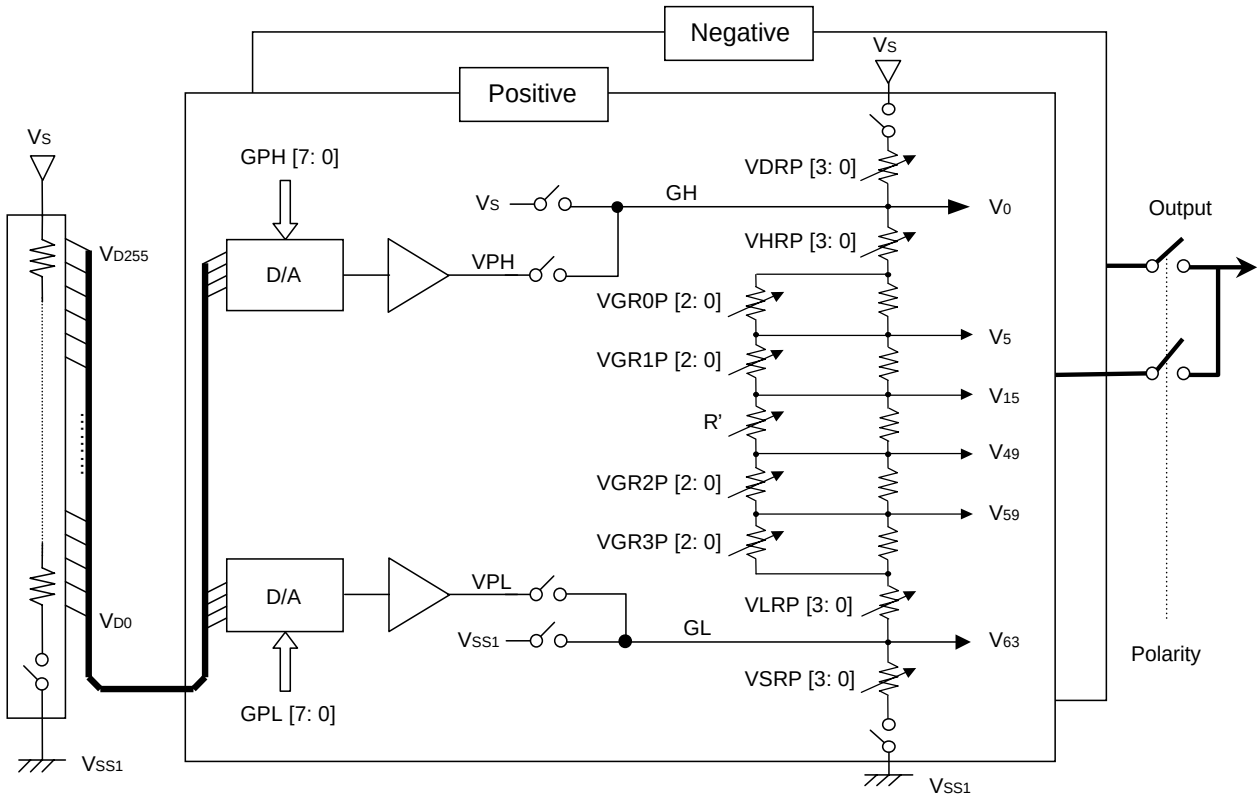
Figure 5–33. ADLNn Setting and Frame Change Rate



5.5 γ- Curve Correction Power Supply Circuit

The μPD161801 includes a γ-curve correction power supply circuit. If the internal γ-curve correction matches the LCD characteristics, no external components are necessary. In addition, this circuit can adjust inclination of γ- and amplitude by register setup while building in each γ-correction resistance by the side of a positive polarity and negative polarity.

Figure 5–34. γ- Curve Correction Power Supply Block Diagram
(The following circuit is in each by the side of positive-/negative-polarity)



5.5.1 Amplitude adjustment with internal amplifier

Amplitude adjustment can select two ways, the method of adjusting with internal amplifier, and the method of adjusting by internal resistance. Each register of R44 (GPH [7:0]), R45 (GNH [7:0]), R46 (GPL [7:0]), and R47 (GNL [7:0]) performs adjustment with amplifier. Refer to **Figure 5–35**.

Figure 5–35. Amplitude Adjustment

(This figure is a circuit by the side of positive-polarity. Use GPH reading it as GNH, GPL to GNL, VPH to VNH, and VPL to VNL if negative-polarity side's reading)

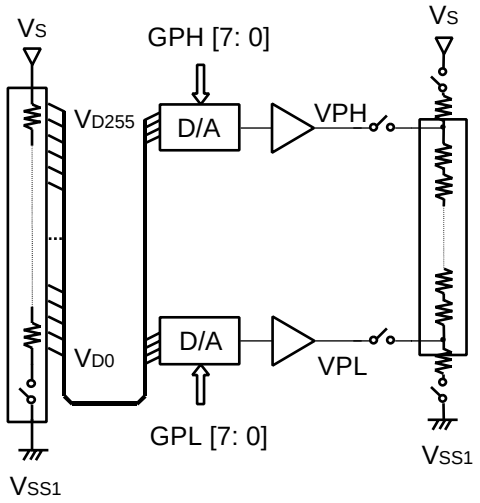
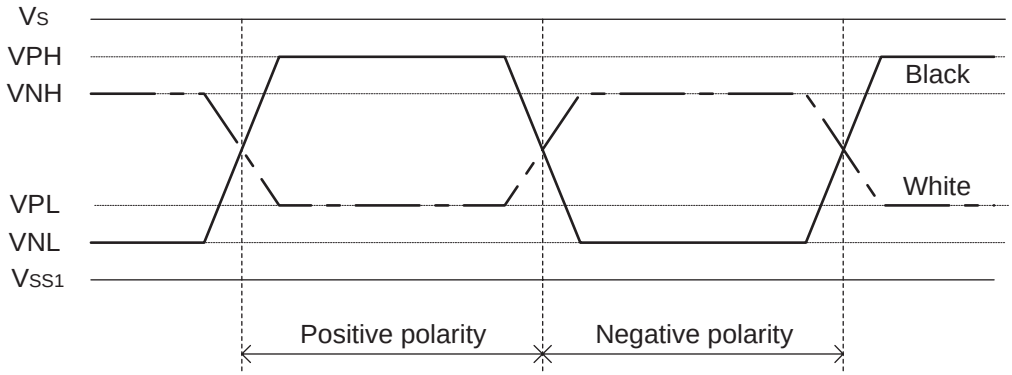


Figure 5–36. Relationship of TFT Drive Voltage (normally white)



	Drive Level	Setting Register	
VPH	Positive polarity, black	Contrast value setting register 1	R44
VNH	Negative polarity, white	Contrast value setting register 2	R45
VPL	Positive polarity, white	Contrast value setting register 3	R46
VNL	Negative polarity, black	Contrast value setting register 4	R47

The value of each amplifier output can be expressed as follows and the value of β can be set as shown in Table 5–9 and 5–10 by using the contrast value registers (R44, R45, R46, and R47)

VNL, VPL, VNH, VPH = (β ÷ 256) x V_S

Caution The usable range in which each output level of VPH, VNH, VPL, and VNL can be set depends on the γ-curve.

Table 5–9. γ- Contrast Value Setting and Electronic Volume Register β Setting 1 (VPH, VNL)

R44	GPH7	GPH6	GPH5	GPH4	GPH3	GPH2	GPH1	GPH0	β value Setting or
R45	GNH7	GNH6	GNH5	GNH4	GNH3	GNH2	GNH1	GNH0	Status Setting
000H	0	0	0	0	0	0	0	0	Fixed to V_S (amplifier OFF)
001H	0	0	0	0	0	0	0	1	255
002H	0	0	0	0	0	0	1	0	254
003H	0	0	0	0	0	0	1	1	253
⋮				⋮					⋮
0FEH	1	1	1	1	1	1	1	0	2
0FFH	1	1	1	1	1	1	1	1	1

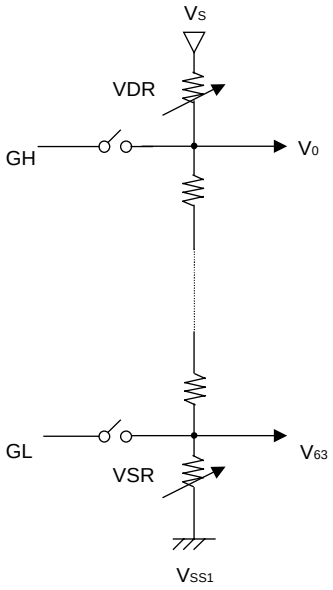
Table 5–10. γ- Contrast Value Setting and Electronic Volume Register β Setting 2 (VPL, VNL)

R46	GPL7	GPL6	GPL5	GPL4	GPL3	GPL2	GPL1	GPL0	β value Setting or
R47	GNL7	GNL6	GNL5	GNL4	GNL3	GNL2	GNL1	GNL0	Statement Setting
000H	0	0	0	0	0	0	0	0	Fixed to V_{SS1} (amplifier OFF)
001H	0	0	0	0	0	0	0	1	1
002H	0	0	0	0	0	0	1	0	2
003H	0	0	0	0	0	0	1	1	3
⋮				⋮					⋮
0FEH	1	1	1	1	1	1	1	0	254
0FFH	1	1	1	1	1	1	1	1	255

5.5.2 Amplitude adjustment by built-in resistance

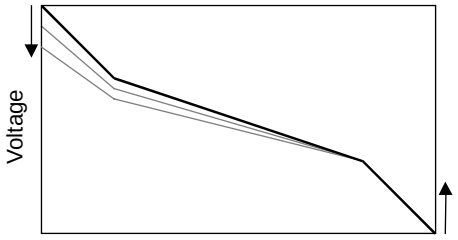
The 4-bit data set as registers R48 and R52 sets amplitude adjustment by built-in resistance. Refer to **Figure 5–37**.

Figure 5–37. Amplitude Adjustment



VDRP [3: 0] (VSRP [3: 0])				VDRP
0	0	0	0	Short (0)
0	0	0	1	4R
0	0	1	0	8R
0	0	1	1	12R
0	1	0	0	16R
0	1	0	1	20R
0	1	1	0	24R
0	1	1	1	28R
1	0	0	0	32R
1	0	0	1	36R
1	0	1	0	40R
1	0	1	1	44R
1	1	0	0	48R
1	1	0	1	52R
1	1	1	0	56R
1	1	1	1	60R

VDRN [3: 0] (VSRN [3: 0])				VDRN
0	0	0	0	Short (0)
0	0	0	1	4R
0	0	1	0	8R
0	0	1	1	12R
0	1	0	0	16R
0	1	0	1	20R
0	1	1	0	24R
0	1	1	1	28R
1	0	0	0	32R
1	0	0	1	36R
1	0	1	0	40R
1	0	1	1	44R
1	1	0	0	48R
1	1	0	1	52R
1	1	1	0	56R
1	1	1	1	60R

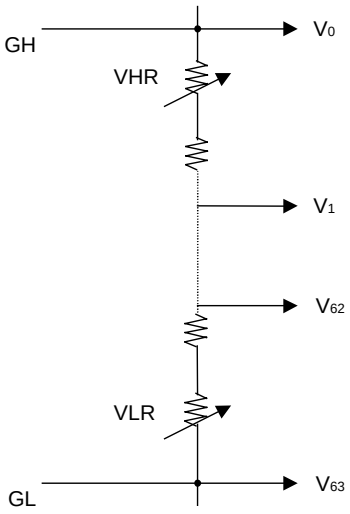


Scale data

5.5.3 Inclination adjustment

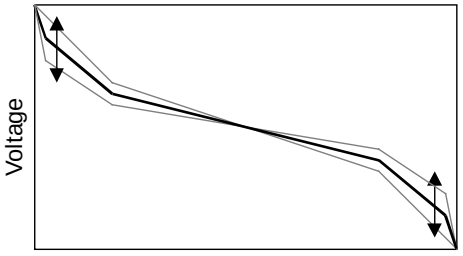
Internal resistance also adjusts inclination adjustment. R49 and R53 registers set adjustment. Refer to **Figure 5–38**.

Figure 5–38. Inclination Adjustment



VHRP [3: 0] (VLRP [3: 0])				VHRP
0	0	0	0	0R
0	0	0	1	4R
0	0	1	0	8R
0	0	1	1	12R
0	1	0	0	16R
0	1	0	1	20R
0	1	1	0	24R
0	1	1	1	28R
1	0	0	0	32R
1	0	0	1	36R
1	0	1	0	40R
1	0	1	1	44R
1	1	0	0	48R
1	1	0	1	52R
1	1	1	0	56R
1	1	1	1	60R

VHRN [3: 0] (VLRN [3: 0])				VHRN
0	0	0	0	0R
0	0	0	1	4R
0	0	1	0	8R
0	0	1	1	12R
0	1	0	0	16R
0	1	0	1	20R
0	1	1	0	24R
0	1	1	1	28R
1	0	0	0	32R
1	0	0	1	36R
1	0	1	0	40R
1	0	1	1	44R
1	1	0	0	48R
1	1	0	1	52R
1	1	1	0	56R
1	1	1	1	60R

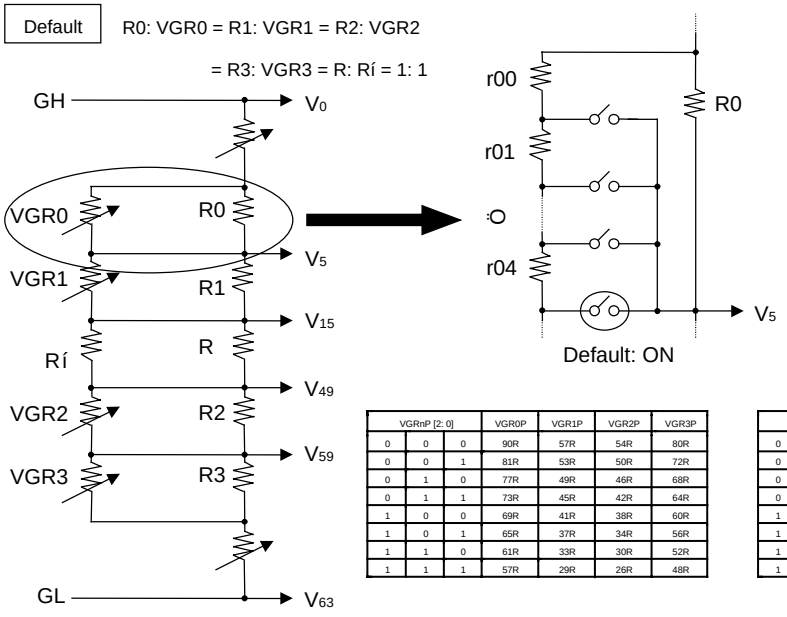


Scale data

5.5.4 Fine tuning adjustment

Internal resistance also sets fine tuning. Please adjust by R50, R51, R54 and R55 register. Refer to **Figure 5–39**.

Figure 5–39. Fine Tuning



VGRnP [2: 0]			VGR0P	VGR1P	VGR2P	VGR3P
0	0	0	90R	57R	54R	80R
0	0	1	81R	53R	50R	72R
0	1	0	77R	49R	46R	68R
0	1	1	73R	45R	42R	64R
1	0	0	69R	41R	38R	60R
1	0	1	65R	37R	34R	56R
1	1	0	61R	33R	30R	52R
1	1	1	57R	29R	26R	48R

VGRnN [2: 0]			VGR0N	VGR1N	VGR2N	VGR3N
0	0	0	80R	54R	57R	90R
0	0	1	72R	50R	53R	81R
0	1	0	68R	46R	49R	77R
0	1	1	64R	42R	45R	73R
1	0	0	60R	38R	41R	69R
1	0	1	56R	34R	37R	65R
1	1	0	52R	30R	33R	61R
1	1	1	48R	26R	29R	57R

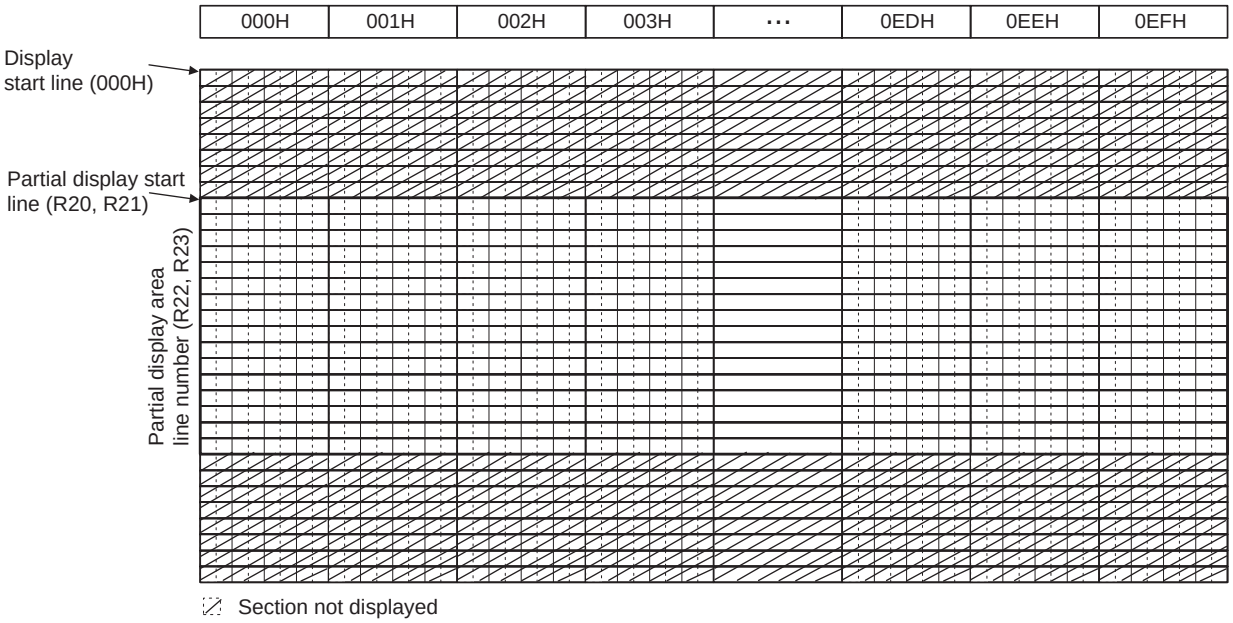
5.6 Partial Display Mode

The μPD161801 is provided with a function that allows sections within the screen to be displayed separately (partial display mode). The start line of the area to be displayed in partial display mode is set using the partial display area start line register (R20, R21), the number of lines in the area to be displayed is set using the partial non-display area line count register (R22, R23), and the color of the area not to be displayed is set using the partial non-display area setting register (R17). If "1" is set in the partial display area line count registers (R22, R23), the partial display areas each become 1 line. If "0" is set, there are no partial display areas but only normal display areas.

The non-display area indicated by R20 and R22 is called Partial 1, and the non-display area indicates by R21 and R23 is called Partial 2. The Partial 2 setting is enabled only when the Partial 1 setting has been performed (when R22 ≠ 0). Therefore, to set only one area as a non-display area, perform only the setting for Partial 1.

Low power consumption cannot be achieved if only the partial mode is set. If low power consumption is required, the mode must be switched to the 8-color mode.

Figure 5–40. Partial Display Mode



Cautions 1. The "scroll step count register (R16)" command is ignored in the partial display mode.

2. The specified partial areas must not directly overlap, and the Partial 1 area and Partial 2 area must be separated by at least one line. If the areas overlap, only the Partial 1 settings are valid, and partial display is not performed for the Partial 2 area. In addition, the last line (320 lines: 13FH) and the start line (1 line: 000H) have become continuously in address. Therefore, partial the non-displaying area for 1 line is required also among these lines.

3. When setting the partial display areas, be sure to observe the following relationship.

"000H" ≤ R20 (R21)

R22 (R23) ≤ "13FH"

5.6.1 Partial display, non-display area driving

The μPD161801 can select drive of a non-displaying area by setting of PT1, PT0 [R78] and GSM at the time of a partial display as follows.

Table 5–11. Driving Output Pin and State of Driving (1/2)

GSM	PT1	PT0	GOE1	R/G/BSW	Sn		Remark
					Non-display start 2 line	Other non-display line	
0	0	0	Normal output	Normal output	8 color	←	Normal partial driving
	0	1	L level fixed	Normal output	8 color	←	
	1	0	L level fixed	Normal output	V_{SS}	←	
	1	1	L level fixed	Normal output	White level display	Hi-Z	Non-refresh driving 1
1	0	0	L level fixed	Normal output	Hi-Z	Hi-Z	Non-refresh driving 2
	Except above		Prohibited setting				

Table 5–12. Driving Output Pin and State of Driving (2/2)

GSM	PT1	PT0	OEV	ASW1 to ASW3		Sn		Remark
				Non-display start 2 line	Other non-display line	Non-display start 2 line	Other non-display line	
0	0	0	Normal output	Normal output	Normal output	8-color white display	←	Normal partial driving
	0	1	L level fixed	Normal output	Normal output	8-color white display	←	
	1	0	L level fixed	Normal output	Normal output	V_{SS}	←	
	1	1	L level fixed	Normal output	L level fixed	White level display	Hi-Z	Non-refresh driving 1
1	0	0	L level fixed	Normal output	Normal output	Hi-Z	Hi-Z	Non-refresh driving 2
	Except above		Prohibited setting					

5.6.2 Partial display, non-display area, and normal partial driving

During partial display mode or when GSM = 0, the μPD161801 is set to normal partial drive mode whenever the settings for PT1 and PT0 are anything other than PT1 = 1 and PT0 = 1.

Normal partial drive mode is the output mode for non-display areas set via the PT1 and PT0 bits, and each frame is driven during this mode. When the settings for PT1 and PT0 are anything other than PT1 = 0 and PT0 = 0, the OEV signal is fixed at low level output so the displayed data in the panel's non-display area cannot be overwritten.

Figure 5–41. Normal Partial Driving Waveform (1/2)

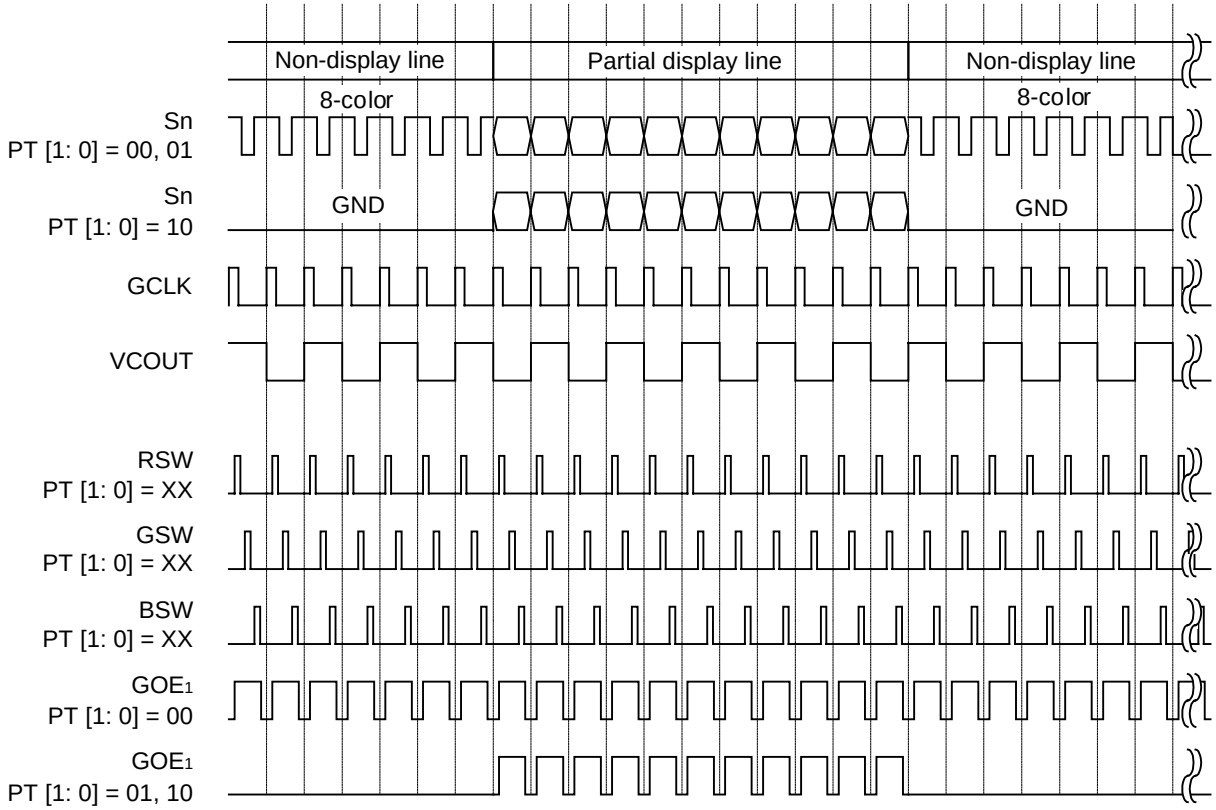
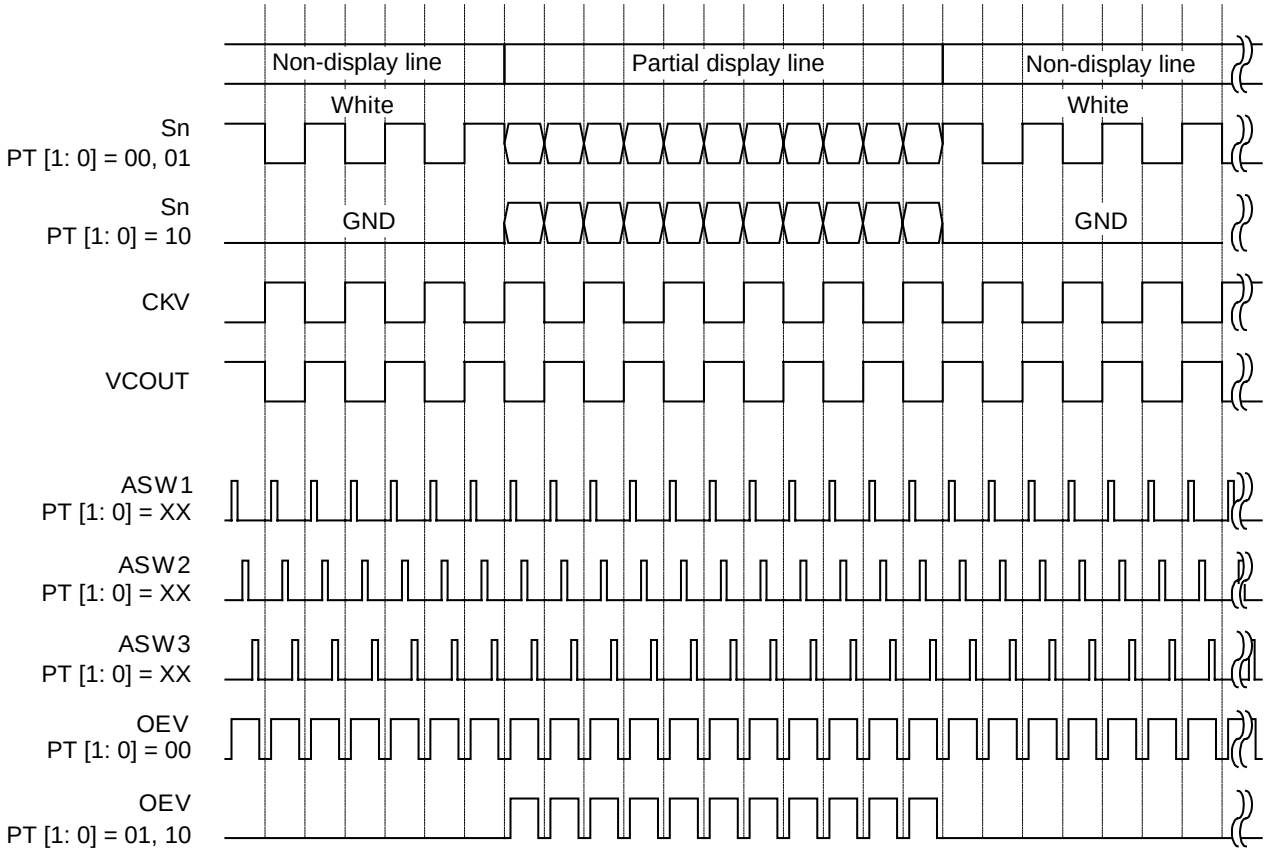


Figure 5–41. Normal Partial Driving Waveform (2/2)



5.6.3 Partial display, non-display area, and non-refresh driving

The μPD161801 can select the non-refreshing drive of a partial a non-displaying area by setting it as GSM = 0, PT1 = 1, PT0 = 1 or GSM = 1, PT1 = 0 and PT0 = 0 at the time of partial display.

This drive is the cycle set up by REFM [2:0] (R68: D_6 to D_4) with REFB [3:0] (R68: D_3 to D_0) in the non-refreshing frame which stops a source output and operation of a gate, and the refreshment frame which carries out a source white level output (normally white panel) and a gate usual scan, and drives partial a non-displaying area.

Figure 5–42. Non-refresh Driving, Frame Cycle Switching Timing

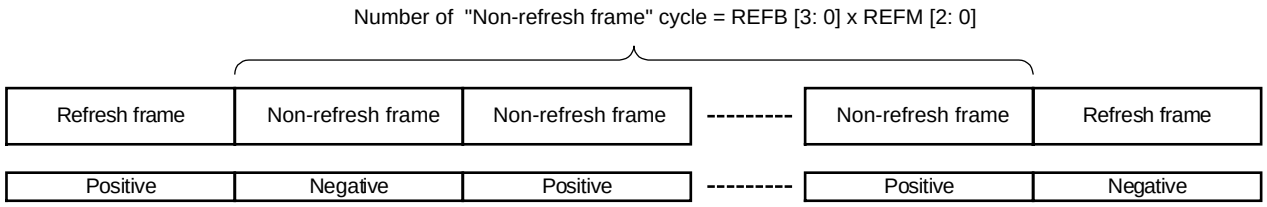


Table 5–13. Non-refresh Driving Frame Basic Cycle

REFB3	REFB2	REFB1	REFB0	Setting Value
0	0	0	0	Only non-refresh driving cycle
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
1	1	1	0	14
1	1	1	1	15

Table 5–14. Non-refresh Driving Frame Basic Cycle Multiple Setting

REFM2	REFM1	REFM0	Setting Value
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

Figure 5–43. Example of Non-refresh Driving Output Waveform (PT1 = 0, PT0 = 0) (1/2)

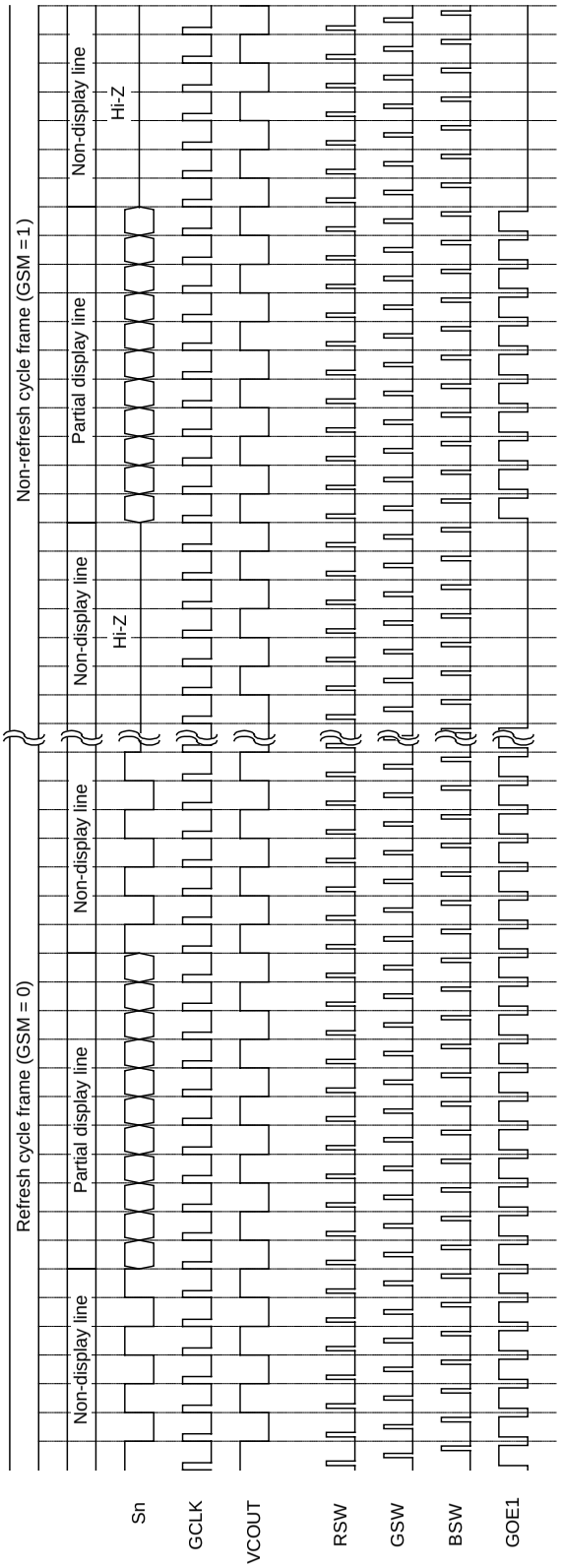


Figure 5–43. Example of Non-refresh Driving Output Waveform (PT1 = 0, PT0 = 0) (2/2)

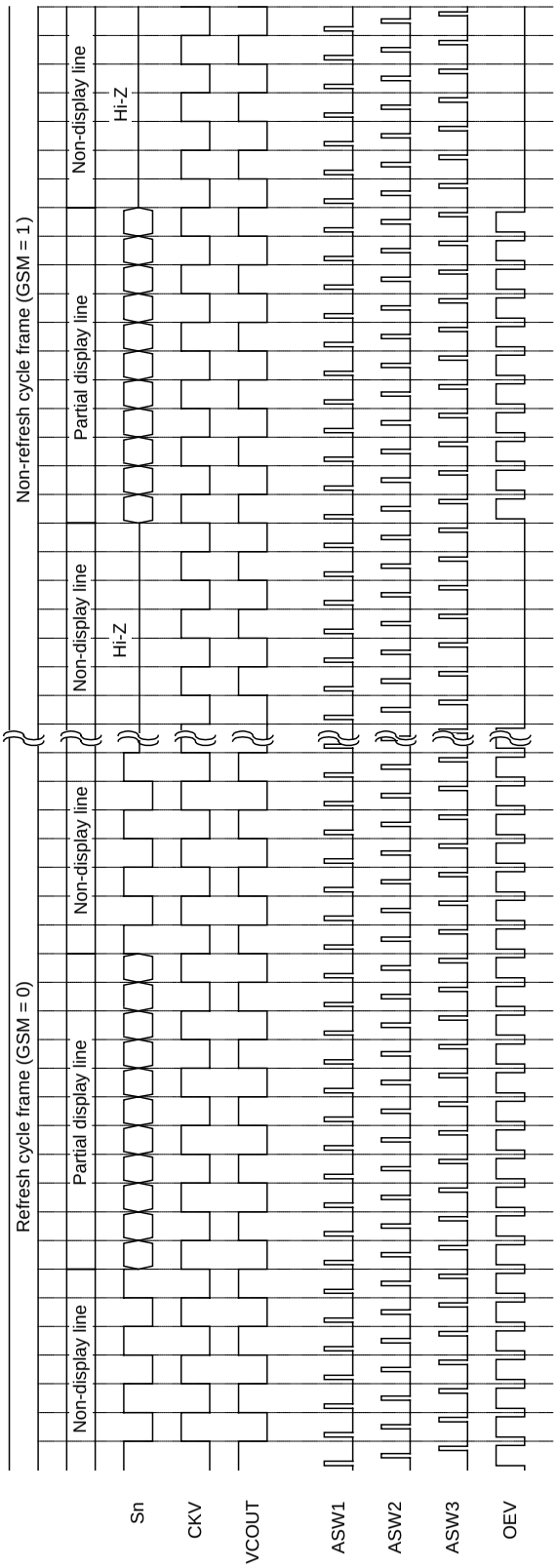


Figure 5–44. Example of Non-refresh Driving Output Waveform (GSM = 0, PT1 = 1, PT0 = 1) (1/2)

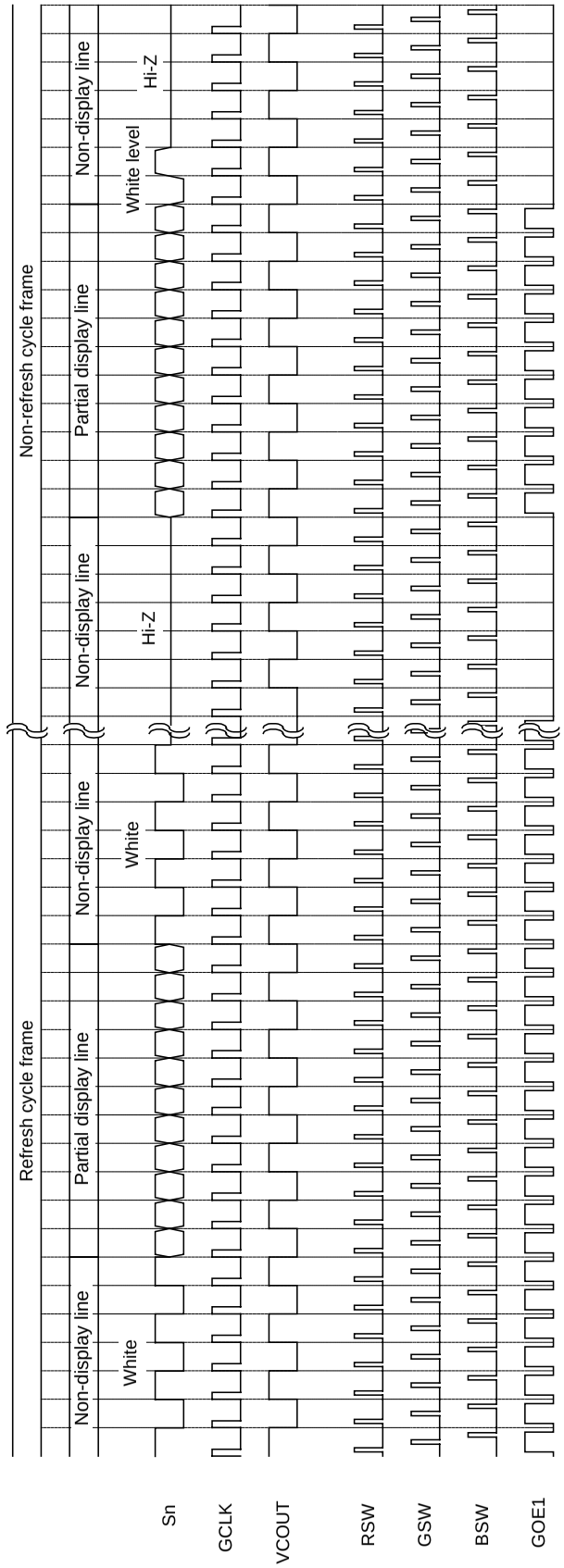
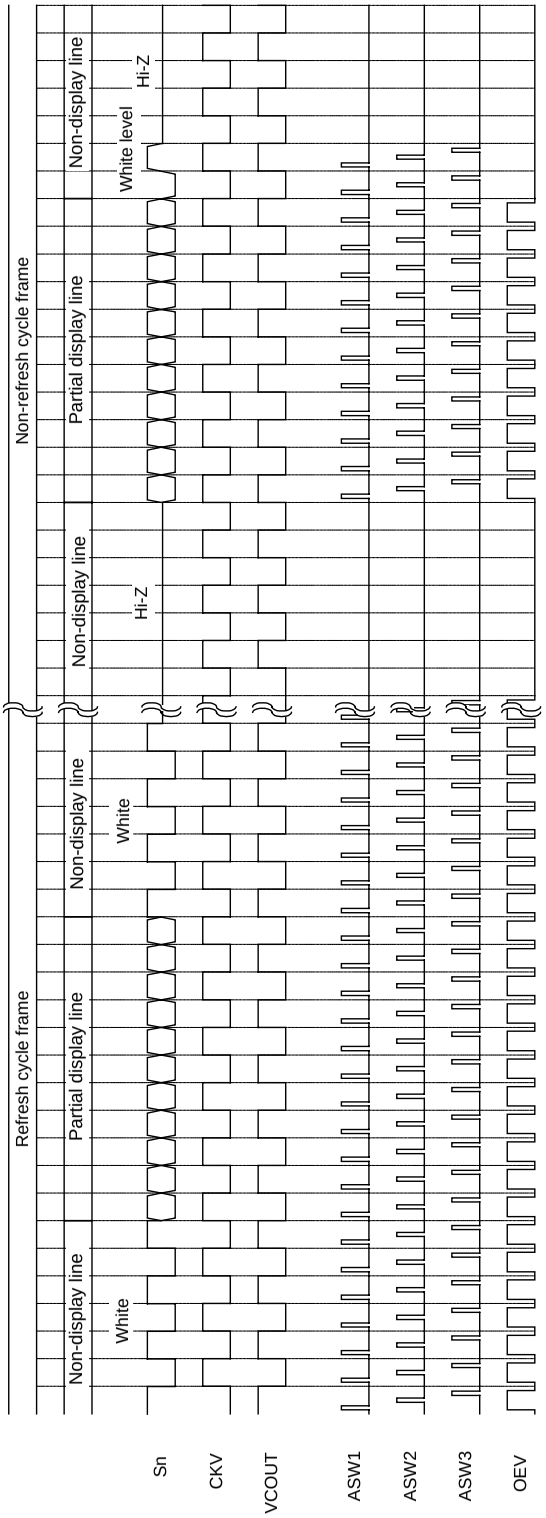


Figure 5–44. Example of Non-refresh Driving Output Waveform (GSM = 0, PT1 = 1, PT0 = 1) (2/2)



The following sequence is recommended to avoid display malfunction when switching from normal display mode to partial display mode and vice versa.

(1) Recommended sequence for switching from normal display mode to partial display mode

DISPn = 1	R0	D_7	<1> Display OFF
↓			
PGX setting	R17	D_2 ⋮ D_0	<2> Partial OFF area color register setting Note1
↓			
Display data overwrite (for partial display)			<3> Display data overwrite Note1
↓			
P1SLn, P2SLn setting	R20, R21	D_7 ⋮ D_0	<4> Partial display area start line setting Note1
↓			
P1AWn, P2AWn setting	R22, R23	D_7 ⋮ D_0	<5> Partial display area line count setting Note1
↓			
DTY = 1, COLOR = 1	R0	D_4, D_2	<6> Partial display mode, 8-color mode Note2
↓			
DISPn = 0	R0	D_7	<7> Display ON

Notes 1. <2> to <5> can be executed in any order.

2. <6> must be executed after <4> and <5> have been set.

(2) Recommended sequence for switching from partial display mode to normal display mode

DISPn = 1	R0	D_7	<1> Display OFF
↓			
Display data overwrite (for normal display)			<2> Display data overwrite Note
↓			
DTY = 0, COLOR = 0	R0	D_4, D_2	<3> Normal display mode, 260,000-color mode Note
↓			
DISPn = 0	R0	D_7	<4> Display ON

Note <2> to <3> can be executed in any order.

(3) Recommended sequence for switching from partial display mode to partial display mode (switching the partial display area)

DISPn = 1	R0	D_7	<1> Display OFF
↓			
(Display data overwrite)			<2> Display data overwrite Note1, 2
↓			
P1SLn, P2SLn setting	R20, R21	D_7 ⋮ D_0	<3> Partial display area start line setting Note1
↓			
P1AWn, P2AWn setting	R22, R23	D_7 ⋮ D_0	<4> Partial display area line count setting Note1
↓			
DTY = 1	R0	D_4	<5> Partial display mode Note3
↓			
DISPn = 0	R0	D_7	<6> Display ON

Notes 1. <2> to <4> can be executed in any order.

2. Execute <2> only when necessary.

3. <5> must be executed after <3> and <4> have been set.

(4) Partial display setting examples

Setting A-1

Register	Setting Value	Details of Setting Value
Partial display area start line register (R20, R21)	000H	Specifies Y address 000H
Partial display area line count register (R22, R23)	09FH	Sets an area of 160 lines

Setting A-2

Register	Setting Value	Details of Setting Value
Partial display area start line register (R20, R21)	0A0H	Specifies Y address 0A0H
Partial display area line count register (R22, R23)	09FH	Sets an area of 160 lines

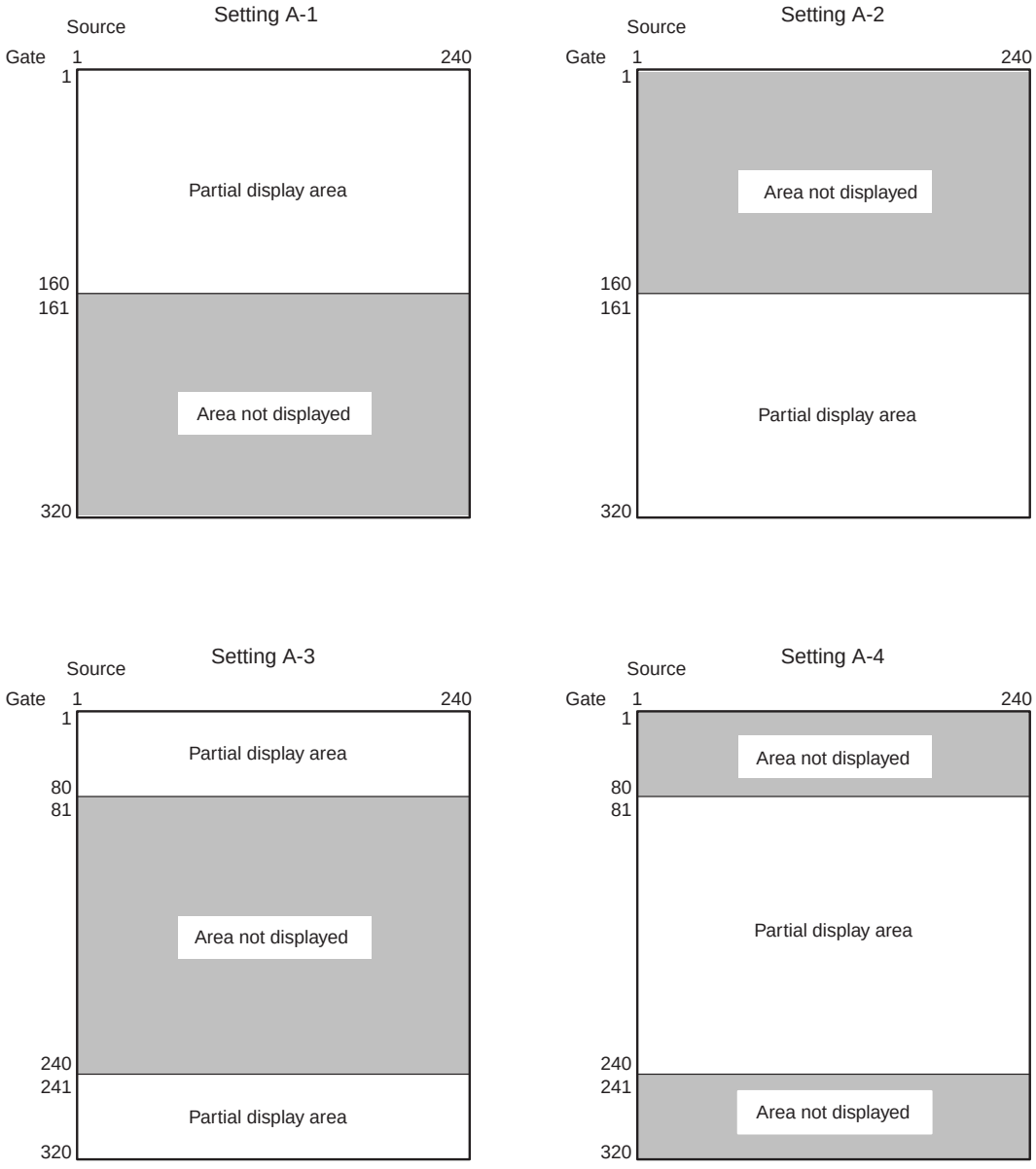
Setting A-3

Register	Setting Value	Details of Setting Value
Partial display area start line register (R20, R21)	0EFH	Specifies Y address 0EFH
Partial display area line count register (R22, R23)	09FH	Sets an area of 160 lines

Setting A-4

Register	Setting Value	Details of Setting Value
Partial display area start line register (R20, R21)	050H	Specifies Y address 050H
Partial display area line count register (R22, R23)	09FH	Sets an area of 160 lines

Figure 5–45. Partial Display Setting



5.7 Screen Scroll

The μPD161801 has a screen scroll function. Any area of the screen can be scrolled by using the scroll area start line register (R14), scroll area line count register (R15), and scroll step count register (R16) to set the Y address of the top line of the area to be scrolled, the count of lines of the area to be scrolled, and the scroll step number, respectively.

Note that in partial mode, the screen scroll function is disabled.

Table 5–15. Scroll Area Start Line Register (R14)

SSL8	SSL7	SSL6	SSL5	SSL4	SSL3	SSL2	SSL1	SSL0	Start Line Y Address
0	0	0	0	0	0	0	0	0	000H
0	0	0	0	0	0	0	0	1	001H
0	0	0	0	0	0	0	1	0	002H
0	0	0	0	0	0	0	1	1	003H
				↓					↓
1	0	0	1	1	1	1	0	1	13DH
1	0	0	1	1	1	1	1	0	13EH
1	0	0	1	1	1	1	1	1	13FH

Table 5–16. Scroll Area Line Count Register (R15)

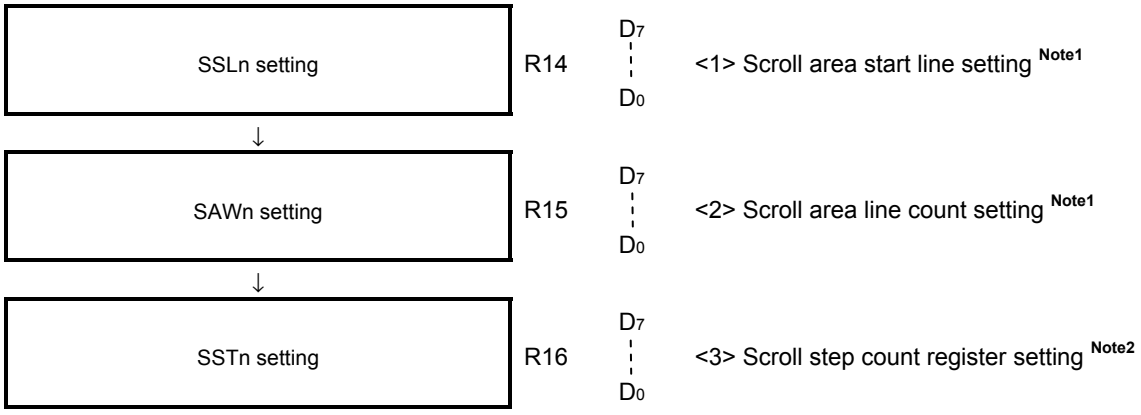
SAW8	SAW7	SAW6	SAW5	SAW4	SAW3	SAW2	SAW1	SAW0	Scroll Area Line Number
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	0	1	1	4
				↓					↓
1	0	0	1	1	1	1	0	1	318
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320

Table 5–17. Scroll Step Count Register (R16)

SST8	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0	Scroll Area Line Number
0	0	0	0	0	0	0	0	0	0 (No scroll)
0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1	3
				↓					↓
1	0	0	1	1	1	1	0	1	317
1	0	0	1	1	1	1	1	0	318
1	0	0	1	1	1	1	1	1	319

Scrolling must be set using the following sequence.

(1) Recommended scroll sequence



Notes 1. <1> to <2> can be executed in any order.

2. <3> must be executed after <1> and <2> have been set.

Remark Set SSTn to 000H to disable the scroll operation. No particular sequence is required for this.

Cautions 1. If the sum of the values of SSLn and SAWn is 320 (13FH) or over, it is invalid (no scroll operation).

2. Set the step number SSTn so that it does not exceed the line number SAWn. If a value exceeding SAWn is set, it will be invalid (no scroll operation).

(2) Scroll setting examples

Setting A-1

Register	Setting Value	Details of Setting Value
Scroll area start line register (R14)	000H	Sets Y address 000H
Scroll area line count register (R15)	13FH	Sets an area of 320 lines

Setting A-2

Register	Setting Value	Details of Setting Value
Scroll area start line register (R14)	000H	Sets Y address 000H
Scroll area line count register (R15)	09FH	Sets an area of 160 lines

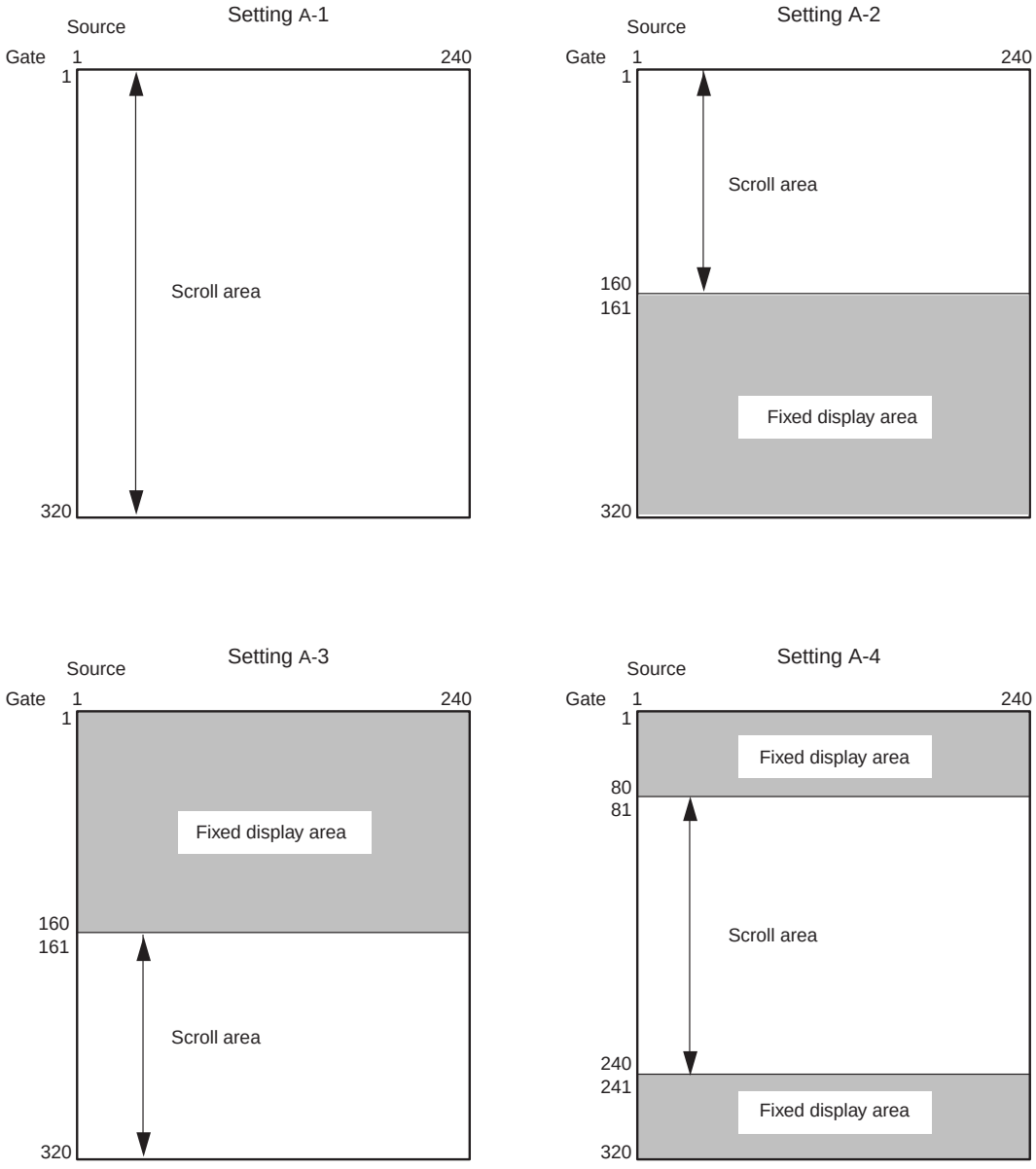
Setting A-3

Register	Setting Value	Details of Setting Value
Scroll area start line register (R14)	0A0H	Sets Y address 0A0H
Scroll area line count register (R15)	09FH	Sets an area of 160 lines

Setting A-4

Register	Setting Value	Details of Setting Value
Scroll area start line register (R14)	050H	Sets Y address 050H
Scroll area line count register (R15)	09FH	Sets an area of 160 lines

Figure 5–46. Display Scroll Setting



(3) Scroll setting flowchart example

Start

↓

R14 — Scroll area start line register setting

RS	D15 / D7							D8 / D0
L	X	0	0	0	1	1	1	1
	D7	D6	D5	D4	D3	D2	D1	D0

Caution D_7 to D_0 are the data for scroll area start line.

↓

R15 — Scroll area line count register setting

RS	D15 / D7							D8 / D0
L	X	0	0	1	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0

Caution D_7 to D_0 are the data for scroll area line count.

↓

R16 — Scroll step count register setting (1 step)

RS	D15 / D7							D8 / D0
L	X	0	0	1	0	0	0	1
	0	0	0	0	0	0	0	1

↓

R6 — X address register

RS	D15 / D7							D8 / D0
L	X	0	0	0	0	1	1	0
	D7	D6	D5	D4	D3	D2	D1	D0

Caution D_7 to D_0 depend on application condition.

↓

R7 — Y address register assignment

RS	D15 / D7							D8 / D0
L	X	0	0	0	0	1	1	1
	D7	D6	D5	D4	D3	D2	D1	D0

Caution D_7 to D_0 depend on application condition.

↓

Display data Re-write scrolling area 1 (Start)

RS	D15 / D7							D8 / D0
H	D15	D14	D13	D12	D11	D10	D9	D8
	D7	D6	D5	D4	D3	D2	D1	D0

Caution D_{15} to D_0 are display memory data.

↓

Display data Re-write scrolling area 2

RS	D15 / D7							D8 / D0
H	D15	D14	D13	D12	D11	D10	D9	D8
	D7	D6	D5	D4	D3	D2	D1	D0

Caution D_{15} to D_0 are display memory data.

↓
↓
↓

Display data Re-write scrolling area n (End)

RS	D15 / D7							D8 / D0
H	D15	D14	D13	D12	D11	D10	D9	D8
	D7	D6	D5	D4	D3	D2	D1	D0

Caution D_{15} to D_0 are display memory data.

↓

↓

Scroll step count register setting (2 steps) — R16

RS: D_{15} … D_8 / D_7 … D_0

RS								
L	X	0	0	1	0	0	1	0
	0	0	0	0	0	0	0	1

↓

X address register — R6

RS: D_{15} … D_8 / D_7 … D_0

RS								
L	X	0	0	0	0	1	1	0
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 to D_0 depend on application condition.

↓

Y address register assignment — R7

RS: D_{15} … D_8 / D_7 … D_0

RS								
L	X	0	0	0	0	1	1	1
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 to D_0 depend on application condition.

↓

Display data Re-write scrolling area 1 (Start)

RS: D_{15} … D_8 / D_7 … D_0

RS								
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} to D_0 are display memory data.

↓

Display data Re-write scrolling area 2

RS: D_{15} … D_8 / D_7 … D_0

RS								
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} to D_0 are display memory data.

↓
↓
↓

Display data Re-write scrolling area n (End)

RS: D_{15} … D_8 / D_7 … D_0

RS								
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} to D_0 are display memory data.

(Repeat)

↓
↓
↓

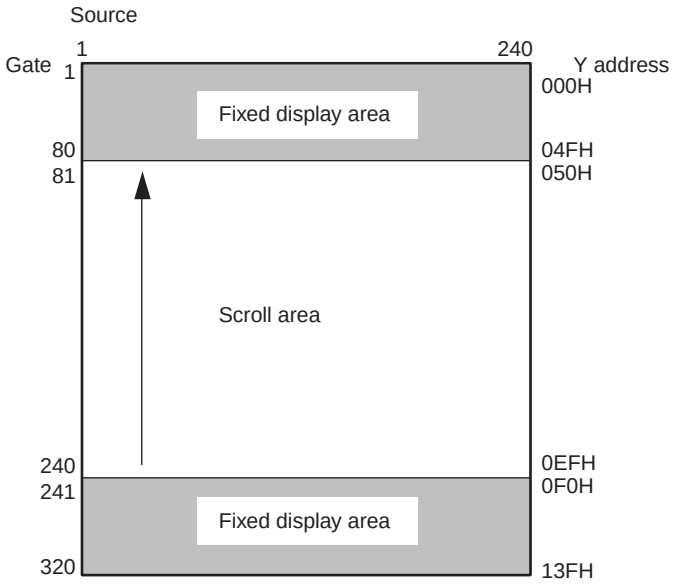
Next transaction

(4) Scroll function example

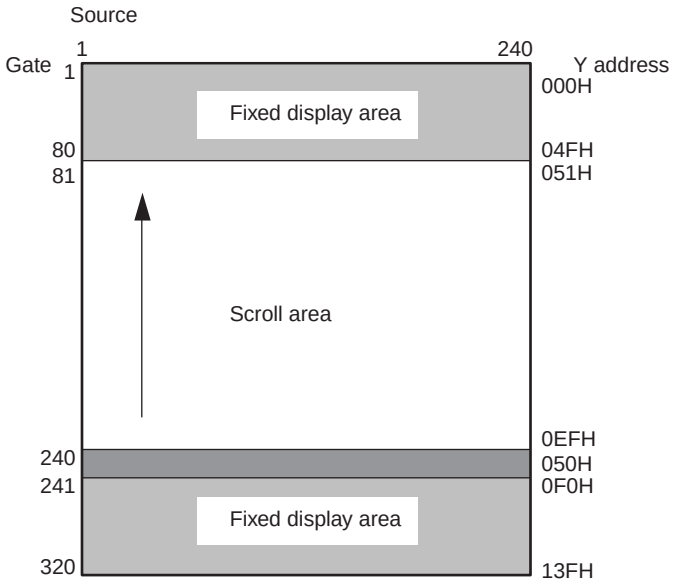
Scroll area start line register (R14): 03CH

Scroll area line count register (R15): 077H

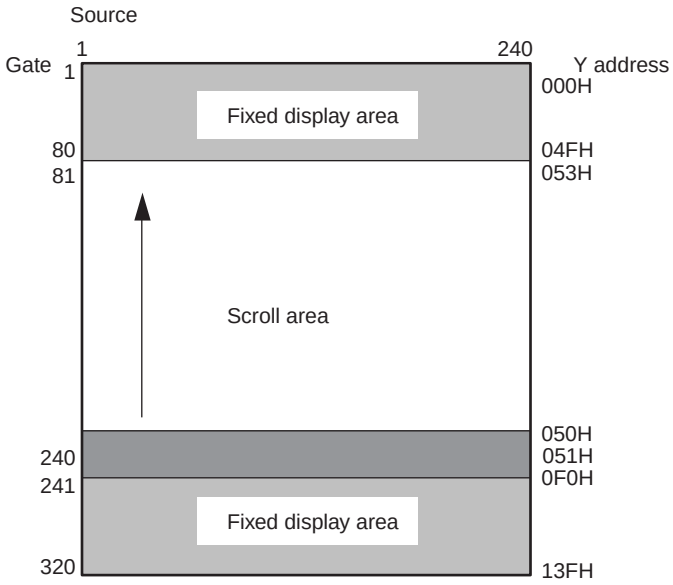
(a) Scroll step count register setting (R16): 000H



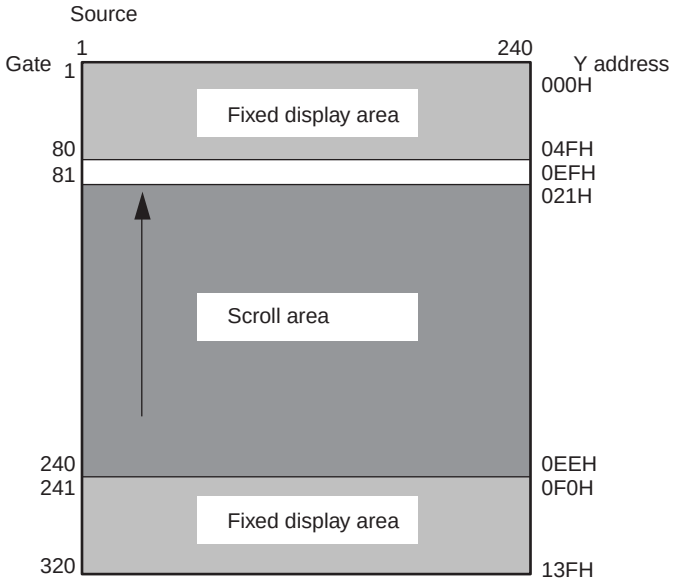
(b) Scroll step count register setting (R16): 001H



(c) Scroll step count register setting (R16): 002H



(d) Scroll step count register setting (R16): 076H

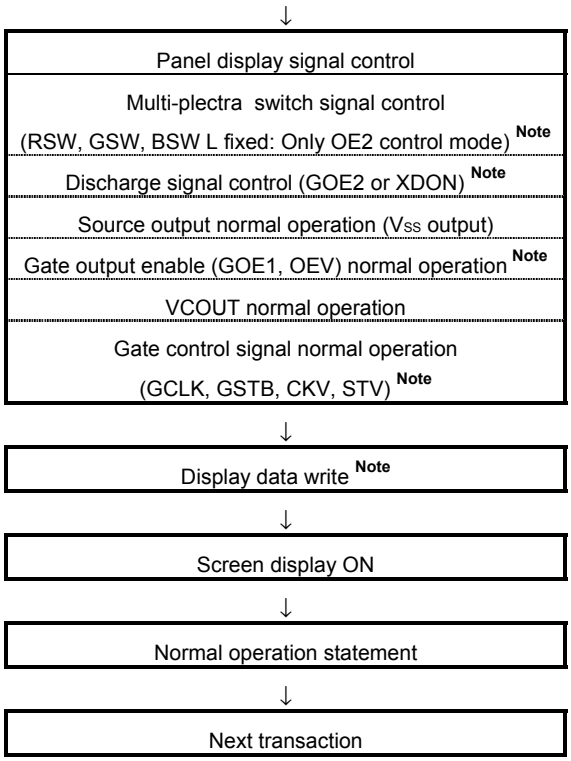


5.8 Power Supply Sequence

The power ON supply sequence of the μPD161801 recommends the sequence shown below.

Power ON	
↓	
WAIT	Power supply voltage stable time
↓	
Hard reset (/RESET ”L” pulse input)	
↓	
RAM address offset	RMODS (R2) = “1”
	By hard reset, the initial value is "0". When using it by "0" setup, it is not necessary to perform this processing.
↓	
Command reset	CRES (R3) = “1”
	All register setup except R2 is to a default state.
↓	
Stand-by mode	
↓	
SRAM power ON	R78 RMST [1:0] =1, 0
↓	
WAIT time (10 ms)	SRAM power supply rising wait time
	It is SRAM power supply circuit rising wait time with built-in IC.
↓	
Display RAM data output "0" data mask release	R78 RMMSK = ”1”
↓	
Sleep mode state	Display OFF, oscillation stop, logic power supply ON, SRAM power supply ON
↓	
Oscillator circuit operation start	R1 OSC2OFF = ”0”
↓	
Power supply IC control (power supply ON)	R38 to R42, R60 to R65
	(Sequence changes with use power supply IC. Refer to the specifications of the power supply IC currently used.)
↓	
WAIT time Note	Power supply rising wait time
	It is the power supply rising wait time of the power supply IC to "Display ON".
↓	

Note Set up the control system register flag of the signal actually used on a panel.



Note Set up the control system register flag of the signal actually used on a panel.

5.9 Stand-by Power Supply OFF Sequence

The stand-by power supply OFF sequence is described below.

5.9.1 Stand-by controlled by STBY flag

The μPD161801 has a stand-by function. When the STBY bit of the control register 1 (R0) is set to 1 while changing the total output of a gate into an ON state in the dummy period of one frame, it is outputted to V_{SS}, and VCOUTn is outputted to V_{SS}, and discharge of the electric charge of a panel is carried out. After the output of gate is in ON state, automatically stopping oscillator (OSC2OFF = 1), regulator OFF for the μPD161801 and DC/DC converter OFF (DCON control) become perfect stand-by mode.

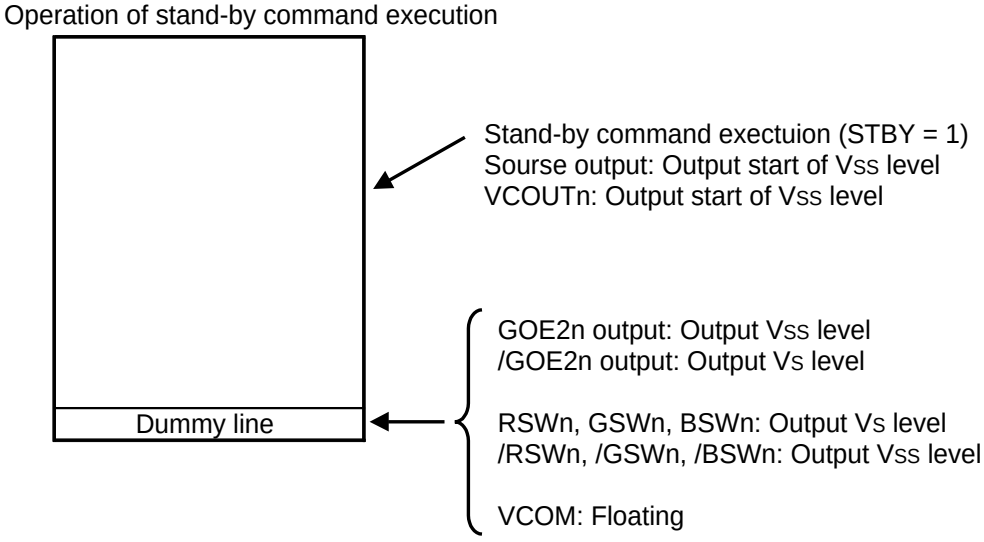
As for control of power supply IC, it is possible to use and control the serial interface pin for control for power supply IC (PCS, PCL and PDA). For details, refer to the specifications of IC used about the OFF sequence/ON sequence of power supply IC.

(1) Stand-by sequence

R0 of STBY bit = 1
↓
(WAIT in one frame period)
↓
Power supply IC control (controlling by serial interface for power supply IC control)
(regulator OFF, DC/DC converter OFF)
↓
Stand-by statement

Caution In the inside of stand-by mode (STBY = 1), regardless of setup of OSC2OFF bit of R1, oscillator for LCD display stops and, after stand-by mode release, oscillator for LCD display starts an oscillation according to a setup of an OSC2OFF bit automatically.

Figure 5–47. Outline of Operation at the Time of Stand-by Execution



(2) Stand-by release sequence

In case of transfer normal mode from stand-by mode, against stand-by sequence, it executes in order.

Under stand-by

↓

OSC2FF = '0' (oscillator start)

↓

Power supply IC control (controlling by serial interface for power supply IC control)

(regulator ON, DC/DC converter ON)

↓

(power ON rising WAIT time)

↓

STBY = 0

5.9.2 Standby-by command input control

When VSTBY = low (power supply to V_{DD1} and V_{DD2} is from internal regulator), the μPD161801 can be freely switched (via input of a mode selection command) from the normal operation mode shown in Figure 5–48 to sleep mode, deep sleep mode, or stand-by mode.

These modes are organized as shown below to enable reduction of power consumption.

	State of Internal Operation the μPD161801				
	Logic Power Supply	Command Massage	SRAM Power Supply	SRAM State	Oscillation
Normal operation	O	Good	O	Normal operation	Operation
Sleep mode	O	Good	O	Normal operation	Stop
Deep sleep mode	O	Good	Δ	Data maintenance	Stop
Stand-by mode	O	Good	X	Data cancellation	Stop

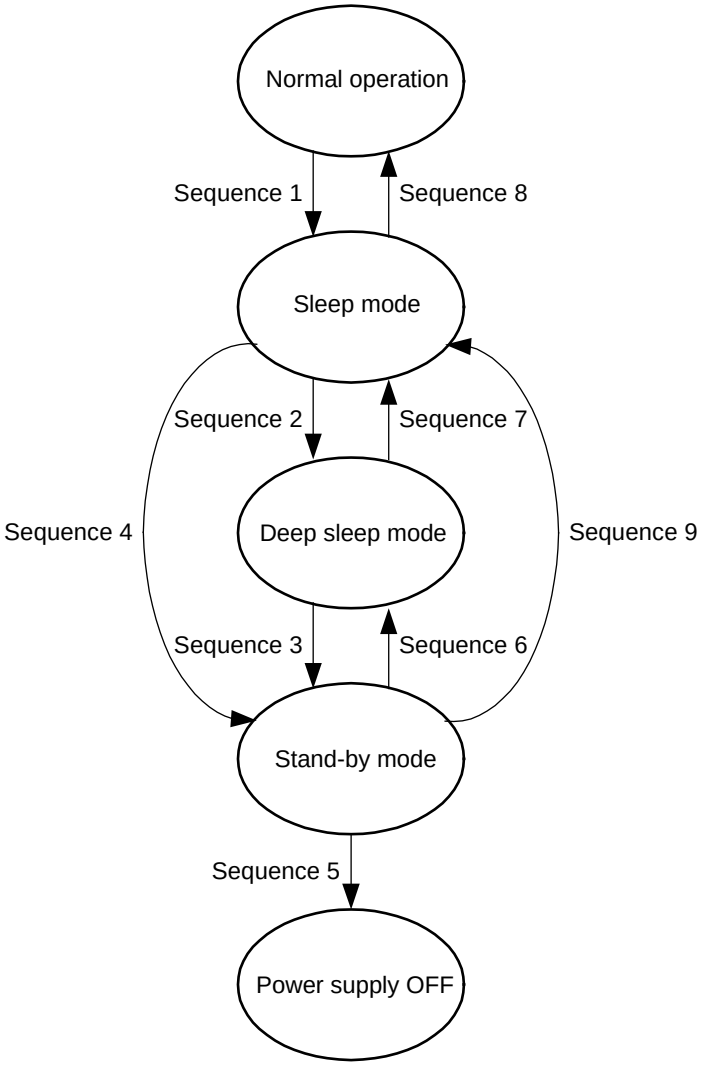
Remark O: Supply, Δ: Low power supply, X: Supply stop

Current consumption current: Normal operation > Sleep mode > Deep sleep mode > Stand-by mode

Setting a sequence, such as for stopping the power IC's power supply, enables module-based reduction of power consumption.

When VSTBY = High has been set, the SRAM power supply voltage supplied to V_{DD2} from an external source remains the same (whether in deep sleep mode or standby mode). Therefore, the amount of power consumed in deep sleep mode and stand-by mode is the same as in sleep mode.

Figure 5–48. IC State Changes



Caution When using the VSTBY = High setting, the settings at sequence 2, 3, 6 and 7 cannot be made.

<Sequence 1>

Normal operation statement	Display ON
↓	
Screen display OFF	R0 DISP1 = ”1”
↓	
WAIT time	Over 1-frame cycle time
↓	
Panel display signal control 1	
Source output stop (Vss output)	R77 RSOUT = ”0”
Gate output stop (GOE1, OEV) signal stop Note1	R77 RGOE1 = ”0” or ROEV = ”0”
VCOUT stop	R93 RVCOT = ”0”
Gate control signal stop (GCLK, GSTB, CKV, STV) Note1	R93 RGCLK = ”0”, RGSTB = ”0” or RCKV = ”0”, RSTV = ”0”
↓	
WAIT time	Over 1-frame cycle time Note2
↓	
Panel discharge control 1	
Discharge control signal (GOE2 or XDON) Note1	R77 RGOE2 = ”1” or RXDON = ”1”
↓	
WAIT time	**Note2**
↓	
Panel discharge control 2	
Multi-plectra switch signal control (RSW, GSW, BSW L fixed: Only OE2 control) Note1	R93 RGBW = ”0”
↓	
Power supply IC control (power supply OFF)	R38 to R42, R60 to R65 (sequence changes with use power supplies IC. Refer to the specifications of the power supply IC currently used.)
↓	
Oscillator stop	R1 OSC2OFF = ”1”
↓	
Sleep mode statement	Display OFF, oscillator stop, logic power supply ON, SRAM power supply ON
↓	
Next transaction	

This sequence is shown in illustration and changes with use panels. It is after checking the specification of the panel used about a sequence enough evaluation. It recommends as following condition after considering.

Notes 1. Set up the control system register flag of the signal actually used on a panel.

2. WAIT time is after checking the characteristic of a use panel, and specification enough evaluation.

<Sequence 2>

Sleep mode	Display OFF, oscillator stop, logic power supply ON, SRAM power supply ON
↓	
Display RAM data output ”0” data mask Note1	R78 RMMSK = ”0”
↓	
SRAM power supply low power mode	R78 RMST [1:0] = 0, 1
↓	
Deep sleep mode Note2	Display OFF, oscillator stop, logic power supply ON, SRAM power supply low power

Notes 1. When it set as a deep sleep mode state, be sure to input the following command. When this processing is not performed but it shifts to a deep sleep mode (RMST [1:0] = 0, 1), problems, such as an increase in penetration current, may occur.

2. Deep sleep mode state is operating the SRAM power supply for display data in the low power mode, and attains low power consumption. Although the data written to display RAM at this time is held, operation of write/read of display data cannot be performed. Note that no-guarantee about operation of IC at the time of accessing display RAM at the time of a deep sleep mode.

Caution Do not set this sequence when VSTB = High.

<Sequence 3>

Deep sleep mode	Display OFF, oscillator stop, logic power supply ON, SRAM power supply low power
↓	
SRAM power supply OFF	R78 RMST [1:0] = 0, 0
↓	
Stand-by mode Note	Display OFF, oscillator stop, logic power supply ON, SRAM power supply OFF

Note Stand-by mode state is stopping supply of the SRAM power supply for display data, and is attaining further low power consumption. The data written to display RAM at this time is canceled. After stand-by mode setup, when usually changing in operation again, it is necessary to write in display data again.

Caution Do not set this sequence when VSTB = High.

<Sequence 4>

Sleep mode	Display OFF, oscillator stop, logic power supply ON, SRAM power supply ON
↓	
Display RAM data output ”0” data mask Note1	R78 RMMSK = ”0”
↓	
SRAM power supply OFF	R78 RMST [1:0] = 0, 0
↓	
Stand-by mode Note2	Display OFF, oscillator stop, logic power supply ON, SRAM power supply OFF

Notes 1. When it set as a deep sleep mode state, be sure to input the following command. When this processing is not performed but it shifts to a deep sleep mode (RMST [1:0] = 0, 1), problems, such as an increase in penetration current, may occur.

2. Stand-by mode state is stopping supply of the SRAM power supply for display data, and is attaining further low power consumption. The data written to display RAM at this time is canceled. After stand-by mode setup, when usually changing in operation again, it is necessary to write in display data again.

Caution When VSTBY = High has been set, the SRAM power supply voltage supplied to V_{DD2} from an external source remains the same (even in stand-by mode). Therefore, the amount of power consumed in stand-by mode is the same as in sleep mode.

<Sequence 5>

Stand-by mode	Display OFF, oscillator stop, logic power supply ON, SRAM power supply OFF
↓	
<System power supply OFF>	

Safely, since system power supply is turned off, after setting it as stand-by mode, it recommends turning OFF system power supply.

<Sequence 6>

Stand-by mode [Note]	Display OFF, oscillator stop, logic power supply ON, SRAM power supply OFF
↓	
SRAM power supply low power mode	R78 RMST [1:0] = 0, 1
↓	
Deep sleep mode	Display OFF, oscillator stop, logic power supply ON, SRAM power supply low power

Note Stand-by mode state is stopping supply of the SRAM power supply for display data, and is attaining further low power consumption. The data written to display RAM at this time is canceled. After stand-by mode setup, when usually changing in operation again, it is necessary to write in display data again.

Caution Do not set this sequence when VSTB = High.

<Sequence 7>

Deep sleep mode [Note1]	Display OFF, oscillator stop, logic power supply ON, SRAM power supply Low Power
↓	
SRAM power supply low power mode	R78 RMST [1:0] = 0, 1
↓	
WAIT time (10 ms) [Note2]	SRAM power supply rising WAIT time It is SRAM power supply circuit rising WAIT time with built-in IC.
↓	
Display RAM data output ”0” data mask release [Note2]	R78 RMMSK = ”1”
↓	
Sleep mode	Display OFF, oscillator stop, logic power supply ON, SRAM power supply ON

Notes 1. Deep sleep mode state is operating the SRAM power supply for display data in the low power mode, and attains low power consumption. Although the data written to display RAM at this time is held, operation of write/read of display data cannot be performed. Note that no-guarantee about operation of IC at the time of accessing display RAM at the time of a deep sleep mode.

2. From deep sleep mode, sleep mode or when it usually returns to operation, input the following command. When display ON is carried out, all LCD displays will be "0" data outputs, without canceling a setup of this command.

Caution Do not set this sequence when VSTB = High.

<Sequence 8>

Sleep mode statement	Display OFF, oscillator stop, logic power supply ON, SRAM power supply ON
↓	
Oscillator circuit operation start	R1 OSC2OFF = ”0”
↓	
Power supply IC control (power supply ON)	R38 to R42, R60 to R65 (sequence changes with use power supplies IC. Refer to the specifications of the power supply IC currently used.)
↓	
WAIT time Note	Power supply rising WAIT time It is the power supply rising WAIT time of the power supply IC to "Display ON."
↓	
Panel display signal control	
Multi-plectra switch signal control (RSW, GSW, BSW L fixed: Only OE2 control) Note	R93 RGBW= ” 1”
Discharge control signal (GOE2 or XDON) Note	R77 RGOE2 = ”0” or RXDON=”0”
Source output normal operation (V_{SS} output)	R77 RSOUT = ”1”
Gate output stop (GOE1, OEV) normal operation Note	R77 RGOE1 = ”1” or ROEV = ”1”
VCOUT stop	R93 RVCOT = ”1”
Gate control signal stop (GCLK, GSTB, CKV, STV) Note	R93 RGCLK = ”1”, RGSTB = ”1” or RCKV = ”1”, RSTV = ”1”
↓	
Screen display ON	R0 DISP1 = ”0”, DISP0 = ”0”
↓	
Normal operation statement	Display ON
↓	
Next transaction	

Notes Set up the control system register flag of the signal actually used on a panel.

<Sequence 9>

Stand-by mode	Display OFF, oscillator stop, logic power supply ON, SRAM power supply OFF
↓	
SRAM power supply ON	R78 RMST [1:0] = 1, 0
↓	
WAIT time (10 ms)	SRAM power supply rising WAIT time It is SRAM power supply circuit rising WAIT time with built-in IC.
↓	
Display RAM data output ”0” data mask release	R78 RMMSK = ”1”
↓	
Sleep mode	Display OFF, oscillator stop, logic power supply ON, SRAM power supply ON
↓	
Display data write Note	

Note Stand-by mode state is stopping supply of the SRAM power supply for display data, and is attaining further low power consumption. The data written to display RAM at this time is canceled. After stand-by mode setup, when usually changing in operation again, it is necessary to write in display data again.

Caution When VSTBY = High has been set, the SRAM power supply voltage supplied to V_{DD2} from an external source remains the same (even in stand-by mode). Therefore, the amount of power consumed in stand-by mode is the same as in sleep mode.

6. RESET

If the /RESET input becomes L or the reset command is input, the internal timing generator is initialized. The reset command will also initialize each register to its default value. These default values are listed in the table below (Register number is an estimate. Understand that there is a case where it changes later).

(1/2)

Register		/RESET Pin Note1	Reset Command	Default Value
Control register 1	R0	X	O	080H
Control register 2	R1	X	O	003H
RAM address offset register	R2	O	X	000H
Command reset register	R3	X	O	000H
Data access control register	R5	X	O	000H
X address register	R6	X	O	000H
Y address register	R7	X	O	000H
MIN. ·X address register	R8	X	O	000H
MAX. ·X address register	R9	X	O	0EFH
MIN. ·Y address register	R10	X	O	000H
MAX. ·Y address register	R11	X	O	13FH
Scroll area start line register	R14	X	O	000H
Scroll area line count register	R15	X	O	000H
Scroll step count register	R16	X	O	000H
Partial non-display area setting register	R17	X	O	000H
Partial 1 display area start line register	R20	X	O	000H
Partial 2 display area start line register	R21	X	O	000H
Partial 1 display area line count register	R22	X	O	000H
Partial 2 display area line count register	R23	X	O	000H
RGB interface control register	R25	X	O	000H
RGB interface back poach period register	R26	X	O	012H
RGB interface through mode start line register	R27	X	O	000H
RGB interface through mode end line register	R28	X	O	000H
RGB interface capture mode window access MIN. ·X address register	R29	X	O	000H or 10FH Note2
RGB interface capture mode window access MAX. ·X address register	R30	X	O	0EFH or 0FFH Note2
RGB interface capture mode window access MIN. ·Y address register	R31	X	O	000H
RGB interface capture mode window access MAX. ·Y address register	R32	X	O	13FH
Calibration register Note3	R34	X	O	000H
Power supply IC control register 1 to 5	R38 to R42	X	O	000H
γ-resistance-connection changing register	R43	X	O	000H

Remark O: Default value set, X: Default value not set

(2/2)

Register		/RESET Pin [Note1]	Reset Command	Default Value
γ-amplitude adjustment register 1 to 4	R44 to R47	X	O	005H
γ-characteristic adjustment P1 register	R48	X	O	011H
γ-characteristic adjustment P2 register	R49	X	O	077H
γ-characteristic adjustment P3 register	R50	X	O	044H
γ-characteristic adjustment P4 register	R51	X	O	044H
γ-characteristic adjustment N1 register	R52	X	O	011H
γ-characteristic adjustment N2 register	R53	X	O	077H
γ-characteristic adjustment N3 register	R54	X	O	044H
γ-characteristic adjustment N4 register	R55	X	O	044H
Output amplitude power supply setup register for 8-color displays	R56	X	O	000H
γ-reference voltage generator capability setting register	R59	X	O	044H
Power supply IC control register 6 to 11	R60 to R65	X	O	000H
AMP drive method change register	R66	X	O	000H
Partial display/non-display area refresh cycle register	R68	X	O	000H
RGB switch open timing register	R72	X	O	000H
Blanking period line setting register	R75	X	O	001H
1 line period clock setting register	R76	X	O	001H
Panel signal control register 1	R77	X	O	000H
Pre-charge polarity select register	R78	X	O	000H
GOE1 start timing register	R79	X	O	004H
GOE1 end timing register	R80	X	O	025H
Pre-charge start timing register	R81	X	O	005H
Pre-charge end timing register	R82	X	O	005H
R switch start timing register	R83	X	O	00DH
R switch end timing register	R84	X	O	014H
G switch start timing register	R85	X	O	015H
G switch end timing register	R86	X	O	01CH
B switch start timing register	R87	X	O	01DH
B switch end timing register	R88	X	O	024H
Extended signal 1 start timing register	R89	X	O	009H
Extended signal 1 end timing register	R90	X	O	009H
Extended signal 2 start timing register	R91	X	O	009H
Extended signal 2 end timing register	R92	X	O	009H
Panel signal control register 2	R93	X	O	000H
★ Interface adjustment register	R98	X	O	000H
Test mode		O	O	–

Remark O: Default value set, X: Default value not set

Notes 1. The internal counters are initialized only by a reset from the /RESET pin. Be sure to perform reset via the /RESET pin at power application.

2. With setting value of RAM address offset register (R2), a default value change as show in the below table.

R2 Setting Value	Default Value	
	R29	R30
000H	000H	0EFH
001H	010H	0FFH

3. The following value is set as the calibration setting time, t_{cal}, in a reset by reset command.

$t_{cal} = 1/f_{OSC2} \times 40$ (f_{OSC2} returns to initial frequency)

Caution The contents of RAM are saved in the case of both reset by /RESET pin and reset by reset command. Note that the RAM contents are unfixed immediately after the power is turned on.

7. COMMAND

7.1 Command List

(Register number is an estimate. Understand that there is a case where it changes later).

Display data access

RAM Access	RS	R,/W	Data Bit								
			DB_{17}	DB_{16}	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9
			DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
18-bit parallel interface											
Display data read 1	1	1	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9
			D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display data write 1	1	0	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9
			D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
16-bit parallel interface (1-pixel/16-bit mode [DTX = 0])											
Display data read 2	1	1	**Hi-Z**	**Hi-Z**	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{11}	D_{10}
			D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1
Display data write 2	1	0	–	–	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{11}	D_{10}
			D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1
16-bit parallel interface (1-pixel/18-bit mode [DTX = 1])											
Display data read 3	1	1	**Hi-Z**	**Hi-Z**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
			D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9
			(D_8)	(D_7)	(D_6)	(D_5)	(D_4)	(D_3)	(D_2)	(D_1)	(D_0)
Display data write 3	1	0	**Hi-Z**	**Hi-Z**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
			D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9
			(D_8)	(D_7)	(D_6)	(D_5)	(D_4)	(D_3)	(D_2)	(D_1)	(D_0)

Remark Hi-Z: High impedance, X: Invalid data

Caution When the 16-bit parallel interface is used in 1-pixel/18-bit mode (DTX = H), data access of two words per pixel is required.

18-bit parallel interface mode, DB_{17}, DB_{16} = 0 (1/5)

Rn	Register	RS	R,/W	Data Bit							
				DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8
				DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
R0	Control register 1	0	0	0	0	0	0	0	0	0	0
				DISP1	DISP0	INV	DTY	STBY	COLOR		GSM
R1	Control register 2	0	0	0	0	0	0	0	0	0	1
				ADX	ADR	0	GUD	LTS1	LTS0	OSC1OFF	OSC2OFF
R2	RAM address offset register	0	0	0	0	0	0	0	0	1	0
											RMOFS
R3	RESET	0	0	0	0	0	0	0	0	1	1
											CRES
R5	Data access control register	0	0	0	0	0	0	0	1	0	1
				DTX1	BSTR	0	WAS	0	INC	0	0
R6	X address register (1 word)	0	0	0	0	0	0	0	1	1	0
				0	0	0	0	0	0	0	0
	X address register (2 word)			X	X	X	X	X	X	X	X
				XA_7	XA_6	XA_5	XA_4	XA_3	XA_2	XA_1	XA_0
R7	Y address register (1 word)	0	0	0	0	0	0	0	1	1	1
				0	0	0	0	0	0	0	0
	Y address register (2 word)			X	X	X	X	X	X	X	YA_8
				YA_7	YA_6	YA_5	YA_4	YA_3	YA_2	YA_1	YA_0
R8	MIN. ·X address register (1 word)	0	0	0	0	0	0	1	0	0	0
				0	0	0	0	0	0	0	0
	MIN. ·X address register (2 word)			X	X	X	X	X	X	X	X
				XMIN7	XMIN6	XMIN5	XMIN4	XMIN3	XMIN2	XMIN1	XMIN0
R9	MAX. ·X address register (1 word)	0	0	0	0	0	0	1	0	0	1
				0	0	0	0	0	0	0	0
	MAX. ·X address register (2 word)			X	X	X	X	X	X	X	X
				XMAX7	XMAX6	XMAX5	XMAX4	XMAX3	XMAX2	XMAX1	XMAX0
R10	MIN. ·Y address register (1 word)	0	0	0	0	0	0	1	0	1	0
				0	0	0	0	0	0	0	0
	MIN. ·Y address register (2 word)			X	X	X	X	X	X	X	YMIN8
				YMIN7	YMIN6	YMIN5	YMIN4	YMIN3	YMIN2	YMIN1	YMIN0
R11	MAX. ·Y address register (1 word)	0	0	0	0	0	0	1	0	1	1
				0	0	0	0	0	0	0	0
	MAX. ·Y address register (2 word)			X	X	X	X	X	X	X	YMAX8
				YMAX7	YMAX6	YMAX5	YMAX4	YMAX3	YMAX2	YMAX1	YMAX0
R14	Scroll area start line register (1 word)	0	0	0	0	0	0	1	1	1	0
				0	0	0	0	0	0	0	0
	Scroll area start line register (2 word)			X	X	X	X	X	X	X	SSL8
				SSL7	SSL6	SSL5	SSL4	SSL3	SSL2	SSL1	SSL0
R15	Scroll area line count register (1 word)	0	0	0	0	0	0	1	1	1	1
				0	0	0	0	0	0	0	0
	Scroll area line count register (2 word)			X	X	X	X	X	X	X	SAW8
				SAW7	SAW6	SAW5	SAW4	SAW3	SAW2	SAW1	SAW0

18-bit parallel interface mode, DB_{17}, DB_{16} = 0 (2/5)

Rn	Register	RS	R,/W	Data Bit							
				DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8
				DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
R16	Scroll step count register (1 word)	0	0	0	0	0	1	0	0	0	0
				0	0	0	0	0	0	0	0
	Scroll step count register (2 word)			X	X	X	X	X	X	X	SST8
				SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0
R17	Partial non-display area setting register	0	0	0	0	0	1	0	0	0	1
								PSEL	PGR	PGG	PGB
R20	Partial 1 display area start line register (1 word)	0	0	0	0	0	1	0	1	0	0
				0	0	0	0	0	0	0	0
	Partial 1 display area start line register (2 word)			X	X	X	X	X	X	X	P1SL8
				P1SL7	P1SL6	P1SL5	P1SL4	P1SL3	P1SL2	P1SL1	P1SL0
R21	Partial 2 display area start line register (1 word)	0	0	0	0	0	1	0	1	0	1
				0	0	0	0	0	0	0	0
	Partial 2 display area start line register (2 word)			X	X	X	X	X	X	X	P2SL8
				P2SL7	P2SL6	P2SL5	P2SL4	P2SL3	P2SL2	P2SL1	P2SL0
R22	Partial 1 display area line count register (1 word)	0	0	0	0	0	1	0	1	1	0
				0	0	0	0	0	0	0	0
	Partial 1 display area line count register (2 word)			X	X	X	X	X	X	X	P1AW8
				P1AW7	P1AW6	P1AW5	P1AW4	P1AW3	P1AW2	P1AW1	P1AW0
R23	Partial 2 display area line count register (1 word)	0	0	0	0	0	1	0	1	1	1
				0	0	0	0	0	0	0	0
	Partial 2 display area line count register (2 word)			X	X	X	X	X	X	X	P2AW8
				P2AW7	P2AW6	P2AW5	P2AW4	P2AW3	P2AW2	P2AW1	P2AW0
R25	RGB interface control register	0	0	0	0	0	1	1	0	0	1
									NWRGB	RGBS	DISPCK
R26	RGB back poach period setting register	0	0	0	0	0	1	1	0	1	0
				HBP3	HBP2	HBP1	HBP0	VBP3	VBP2	VBP1	VBP0
R27	RGB through mode display start line register (1 word)	0	0	0	0	0	1	1	0	1	1
				0	0	0	0	0	0	0	0
	RGB through mode display start line register (2 word)			X	X	X	X	X	X	X	RGBST8
				RGBST7	RGBST6	RGBST5	RGBST4	RGBST3	RGBST2	RGBST1	RGBST0
R28	RGB through mode display end line register (1 word)	0	0	0	0	0	1	1	1	0	0
				0	0	0	0	0	0	0	0
	RGB through mode display end line register (2 word)			X	X	X	X	X	X	X	RGBED8
				RGBED7	RGBED6	RGBED5	RGBED4	RGBED3	RGBED2	RGBED1	RGBED0
R29	RGB capture mode window access MIN. ·X address register (1 word)	0	0	0	0	0	1	1	1	0	1
				0	0	0	0	0	0	0	0
	RGB capture mode window access MIN. ·X address register (2 word)			X	X	X	X	X	X	X	X
				CAPXMIN7	CAPXMIN6	CAPXMIN5	CAPXMIN4	CAPXMIN3	CAPXMIN2	CAPXMIN1	CAPXMIN0

18-bit parallel interface mode, DB_{17}, DB_{16} = 0 (3/5)

Rn	Register	RS	R,/W	Data Bit							
				DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8
				DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
R30	RGB capture mode window access MAX. ·X address register (1 word)	0	0	0	0	0	1	1	1	1	0
				0	0	0	0	0	0	0	0
	RGB capture mode window access MAX. ·X address register (2 word)			X	X	X	X	X	X	X	X
				CAPXMAX7	CAPXMAX6	CAPXMAX5	CAPXMAX4	CAPXMAX3	CAPXMAX2	CAPXMAX1	CAPXMAX0
R31	RGB capture mode window access MIN. ·Y address register (1 word)	0	0	0	0	0	1	1	1	1	1
				0	0	0	0	0	0	0	0
	RGB capture mode window access MIN. ·Y address register (2 word)			X	X	X	X	X	X	X	CAPYMIN8
				CAPYMIN7	CAPYMIN6	CAPYMIN5	CAPYMIN4	CAPYMIN3	CAPYMIN2	CAPYMIN1	CAPYMIN0
R32	RGB capture mode window access MAX. ·Y address register (1 word)	0	0	0	0	1	0	0	0	0	0
				0	0	0	0	0	0	0	0
	RGB capture mode window access MAX. ·Y address register (2 word)			X	X	X	X	X	X	X	CAPYMAX8
				CAPYMAX7	CAPYMAX6	CAPYMAX5	CAPYMAX4	CAPYMAX3	CAPYMAX2	CAPYMAX1	CAPYMAX0
R34	Calibration register	0	0	0	0	1	0	0	0	1	0
											OC
R38	Power supply IC control register 1	0	0	0	0	1	0	0	1	1	0
				PSD17	PSD16	PSD15	PSD14	PSD13	PSD12	PSD11	PSD10
R39	Power supply IC control register 2	0	0	0	0	1	0	0	1	1	1
				PSD27	PSD26	PSD25	PSD24	PSD23	PSD22	PSD21	PSD20
R40	Power supply IC control register 3	0	0	0	0	1	0	1	0	0	0
				PSD37	PSD36	PSD35	PSD34	PSD33	PSD32	PSD31	PSD30
R41	Power supply IC control register 4	0	0	0	0	1	0	1	0	0	1
				PSD47	PSD46	PSD45	PSD44	PSD43	PSD42	PSD41	PSD40
R42	Power supply IC control register 5	0	0	0	0	1	0	1	0	1	0
				PSD57	PSD56	PSD55	PSD54	PSD53	PSD52	PSD51	PSD50
R43	γ-resistance-connection changing register	0	0	0	0	1	0	1	0	1	1
							GSEL				GONSEL
R44	γ-amplitude adjustment register 1	0	0	0	0	1	0	1	1	0	0
				GPH7	GPH6	GPH5	GPH4	GPH3	GPH2	GPH1	GPH0
R45	γ-amplitude adjustment register 2	0	0	0	0	1	0	1	1	0	1
				GNH7	GNH6	GNH5	GNH4	GNH3	GNH2	GNH1	GNH0
R46	γ-amplitude adjustment register 3	0	0	0	0	1	0	1	1	1	0
				GPL7	GPL6	GPL5	GPL4	GPL3	GPL2	GPL1	GPL0
R47	γ-amplitude adjustment register 4	0	0	0	0	1	0	1	1	1	1
				GNL7	GNL6	GNL5	GNL4	GNL3	GNL2	GNL1	GNL0
R48	γ-characteristic adjustment P1 register	0	0	0	0	1	1	0	0	0	0
				VDRP3	VDRP2	VDRP1	VDRP0	VSRP3	VSRP2	VSRP1	VSRP0
R49	γ-characteristic adjustment P2 register	0	0	0	0	1	1	0	0	0	1
				VLRP3	VLRP2	VLRP1	VLRP0	VHRP3	VHRP2	VHRP1	VHRP0
R50	γ-characteristic adjustment P3 register	0	0	0	0	1	1	0	0	1	0
					VGR1P2	VGR1P1	VGR1P0		VGR0P2	VGR0P1	VGR0P0
R51	γ-characteristic adjustment P4 register	0	0	0	0	1	1	0	0	1	1
					VGR3P2	VGR3P1	VGR3P0		VGR2P2	VGR2P1	VGR2P0

18-bit parallel interface mode, DB_{17}, DB_{16} = 0 (4/5)

Rn	Register	RS	R,/W	Data Bit							
				DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8
				DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
R52	γ-characteristic adjustment N1 register	0	0	0	0	1	1	0	1	0	0
				VDRN3	VDRN2	VDRN1	VDRN0	VSRN3	VSRN2	VSRN1	VSRN0
R53	γ-characteristic adjustment N2 register	0	0	0	0	1	1	0	1	0	1
				VLRN3	VLRN2	VLRN1	VLRN0	VHRN3	VHRN2	VHRN1	VHRN0
R54	γ-characteristic adjustment N3 register	0	0	0	0	1	1	0	1	1	0
					VGR1N2	VGR1N1	VGR1N0		VGR0N2	VGR0N1	VGR0N0
R55	γ-characteristic adjustment N4 register	0	0	0	0	1	1	0	1	1	1
					VGR3N2	VGR3N1	VGR3N0		VGR2N2	VGR2N1	VGR2N0
R56	Output amplitude power supply setup register for 8-color displays	0	0	0	0	1	1	1	0	0	0
										GV8S1	0
R59	γ-reference voltage generator capability setting register	0	0	0	0	1	1	1	0	1	1
				WHP	WI2	WI1	WI0	BHP	BI2	BI1	BI0
R60	Power supply IC control register 6	0	0	0	0	1	1	1	1	0	0
				PSD67	PSD66	PSD65	PSD64	PSD63	PSD62	PSD61	PSD60
R61	Power supply IC control register 7	0	0	0	0	1	1	1	1	0	1
				PSD77	PSD76	PSD75	PSD74	PSD73	PSD72	PSD71	PSD70
R62	Power supply IC control register 8	0	0	0	0	1	1	1	1	1	0
				PSD87	PSD86	PSD85	PSD84	PSD83	PSD82	PSD81	PSD80
R63	Power supply IC control register 9	0	0	0	0	1	1	1	1	1	1
				PSD97	PSD96	PSD95	PSD94	PSD93	PSD92	PSD91	PSD90
R64	Power supply IC control register 10	0	0	0	1	0	0	0	0	0	0
				PSDA7	PSDA6	PSDA5	PSDA4	PSDA3	PSDA2	PSDA1	PSDA0
R65	Power supply IC control register 11	0	0	0	1	0	0	0	0	0	1
				PSDB7	PSDB6	PSDB5	PSDB4	PSDB3	PSDB2	PSDB1	PSDB0
R66	AMP drive method change register	0	0	0	1	0	0	0	0	1	0
										LMD1	0
R68	Partial display/non-display area refresh cycle register	0	0	0	1	0	0	0	1	0	0
					REFM2	REFM1	REFM0	REFB3	REFB2	REFB1	REFB0
R72	RGB switch open timing register	0	0	0	1	0	0	1	0	0	0
				DC4	DC3		DSCG4	DSCG3	DSCG2	DSCG1	DSCG0
R75	Blanking period line setting register	0	0	0	1	0	0	1	0	1	1
				ADLN7	ADLN6	ADLN5	ADLN4	ADLN3	ADLN2	ADLN1	ADLN0
R76	1 line period clock setting register	0	0	0	1	0	0	1	1	0	0
							ADCK4	ADCK3	ADCK2	ADCK1	ADCK0
R77	Panel signal control register 1	0	0	0	1	0	0	1	1	0	1
						RSOUT	RGOE2	RGOE1	RXDON	ROEVE	ROEV
R78	Pre-charge polarity select register	0	0	0	1	0	0	1	1	1	0
					RMMSK	RMST1	RMST0	PT1	PT0	REV	0
R79	GOE1 start timing register	0	0	0	1	0	0	1	1	1	1
						GOST5	GOST4	GOST3	GOST2	GOST1	GOST0
R80	GOE1 end timing register	0	0	0	1	0	1	0	0	0	0
						GOED5	GOED4	GOED3	GOED2	GOED1	GOED0

18-bit parallel interface mode, DB_{17}, DB_{16} = 0 (5/5)

Rn	Register	RS	R,/W	Data Bit							
				DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8
				DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
R81	Pre-charge start timing register	0	0	0	1	0	1	0	0	0	1
						PCST5	PCST4	PCST3	PCST2	PCST1	PCST0
R82	Pre-charge end timing register	0	0	0	1	0	1	0	0	1	0
						PCED5	PCED4	PCED3	PCED2	PCED1	PCED0
R83	R switch start timing register	0	0	0	1	0	1	0	0	1	1
						RST5	RST4	RST3	RST2	RST1	RST0
R84	R switch end timing register	0	0	0	1	0	1	0	1	0	0
						RED5	RED4	RED3	RED2	RED1	RED0
R85	G switch start timing register	0	0	0	1	0	1	0	1	0	1
						GST5	GST4	GST3	GST2	GST1	GST0
R86	G switch end timing register	0	0	0	1	0	1	0	1	1	0
						GED5	GED4	GED3	GED2	GED1	GED0
R87	B switch start timing register	0	0	0	1	0	1	0	1	1	1
						BST5	BST4	BST3	BST2	BST1	BST0
R88	B switch end timing register	0	0	0	1	0	1	1	0	0	0
						BED5	BED4	BED3	BED2	BED1	BED0
R89	Extended signal 1 start timing register	0	0	0	1	0	1	1	0	0	1
						E1ST5	E1ST4	E1ST3	E1ST2	E1ST1	E1ST0
R90	Extended signal 1 end timing register	0	0	0	1	0	1	1	0	1	0
						E1ED5	E1ED4	E1ED3	E1ED2	E1ED1	E1ED0
R91	Extended signal 2 start timing register	0	0	0	1	0	1	1	0	1	1
						E2ST5	E2ST4	E2ST3	E2ST2	E2ST1	E2ST0
R92	Extended signal 2 end timing register	0	0	0	1	0	1	1	1	0	0
						E2ED5	E2ED4	E2ED3	E2ED2	E2ED1	E2ED0
R93	Panel signal control register 2	0	0	0	1	0	1	1	1	0	1
				0	RVCOT	RGBSW	RGSTB	RGCLK	RASW	RSTV	RCKV
★ R98	Interface adjustment register	0	0	0	1	1	0	0	0	1	0
				0	0						

Cautions 1. Input unfixed (0 or 1) in blank area.

2. Access is prohibited about the register is not in the above register.

7.2 Command Explanation

(Register number is an estimate. Understand that there is a case where it changes later).

(1/13)

Register	Bit	Symbol	Function
R0	D_7	DISP1	This command performs the same output as when all data is 1, independently of the internal RAM data (white display in the case of normally white). This command is executed, after it has been transferred, when the next line is output. 0: Normal operation 1: Ignores data of RAM and outputs all data as 1. DISP1 takes precedence over DISP0. When DISP1 = 1, DISP0 = 1 is ignored.
	D_6	DISP0	This command performs the same output as when all data is 0, independently of the internal RAM data (black display in the case of normally white). This command is executed, after it has been transferred, when the next line is output. 0: Normal operation 1: Ignores data of RAM and outputs all data as 0.
	D_5	INV	This command selects a line inversion function and a frame inversion function. Execution in the mode set by this command is from the timing outputs the following line data. 0: Line inversion 1: Frame inversion
	D_4	DTY	This pin selects the partial function. When the partial function s selected in the 260,000-color mode, set the partial OFF area color setting register (R27) to 000H. In the 8-color mode, the partial off area color can be set to any value from 000H to 007H. The power consumption cannot be reduced with the partial function. To reduce the power consumption, select the 8-color mode. This command is executed following transfer from the time the next line data is output. 0: Normal display mode 1: Partial display mode
	D_3	STBY	This bit selects the stand-by function. When the stand-by function is selected, a display OFF operation is executed, the amplifiers, and oscillator at each output circuit are stopped. After executing the stand-by function using this bit, set the regulator for gate power supply IC to OFF and set the DC/DC converter to OFF. For the sequence, refer to the preliminary product information of the power supply IC etc. Note that when releasing stand-by, perform the opposite operation, after setting the DC/DC converter to ON and setting the regulators of the gate IC and power supply IC to ON, execute the normal operation command. 0: Normal operation 1: Stand-by function (Display read OFF from RAM, stop VCOM, display OFF = source output becomes V_{SS})
	D_2	COLOR	This pin switches the 260,000-color mode and the 8-color mode. When the 8-color mode is selected, low power supply can be selected in order to stop the amplifier at each output circuit. In the 8-color mode, the value of the MSB of the internal RAM data is used as the color data. This command is executed following transfer from the time the next line data is output. 0: 260,000-color mode (18-bit/pixels) 1: 8-color mode (3-bit/pixels)
	D_0	GSM	Sets output of the gate scanning signal during partial display. If this bit is set to 1, the gate scan of the lines set in the partial non-display area is stopped. 0: Normal mode 1: Stops gate scanning in partial non-display area

(2/13)

<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td rowspan="8">R1</td><td>D_7</td><td>ADX</td><td>Addressing of X address is inverted. For more details, refer to Figure 5–24.</td></tr>
<tr><td>D_6</td><td>ADR</td><td>Addressing of Y address is inverted. For more details, refer to Figure 5–24.</td></tr>
<tr><td>D_4</td><td>GUD</td><td>This pin can be used when changing the direction of gate scan of a panel.
A display is possible for a vertical contrary by changing the direction of gate scan of a panel also in the time of the through mode of RGB interface using the output signal from this pin.
0: GUD pin L output
1: GUD pin H output
The signal change timing is the same as frame change timing. About frame change timing, refer to 5.4.2 1-frame period timing.</td></tr>
<tr><td>D_3</td><td>LTS1</td><td rowspan="2">Selects set time of calibration.
The calibration function adjusts the frame frequency by setting time of one line. This command can select the set time of a line from the following:
<table><tr><th>LTS1</th><th>LTS0</th><th>1-line time</th><th>1-line frequency</th></tr><tr><td>0</td><td>0</td><td>t_{cal} x 1</td><td>Normal operation x 1</td></tr><tr><td>0</td><td>1</td><td>t_{cal} x 2</td><td>Normal operation x 2</td></tr><tr><td>1</td><td>0</td><td>t_{cal} x 4</td><td>Normal operation x 4</td></tr><tr><td>1</td><td>1</td><td>t_{cal} x 8</td><td>Normal operation x 8</td></tr></table>Remark t_{cal}: Calibration set time = 1 ÷ Frame frequency ÷ Number of displayed lines</td></tr>
<tr><td>D_2</td><td>LTS0</td></tr>
<tr><td>D_1</td><td>OSC1OFF</td><td>This is oscillator circuit stop bit for calibration. This command is stop when in stand-by mode.
0: Oscillator operation
1: Oscillator stop</td></tr>
<tr><td>D_0</td><td>OSC2OFF</td><td>This is oscillator circuit stop bit for LCD display. This command is stop when in stand-by mode.
0: Oscillator operation
1: Oscillator stop</td></tr>
<tr><td>R2</td><td>D_0</td><td>RMOFS</td><td>Offset is applied to the address value of X addresses of the display RAM. The relation between X addresses and an output is set up as follows.
0: Offset OFF, 000H (0) to 0EFH (239)
1: Offset ON, 020H (0) to 0FFH (239)</td></tr>
<tr><td>R3</td><td>D_0</td><td>CRES</td><td>Command reset function. Be sure to execute this bit after power ON.
Command reset automatically clears this bit following execution (RES = 1H). Therefore, it is not necessary to set 0 (select normal operation) again by software. Moreover, since the time required for the value of this bit to change (1 → 0) following command reset execution is extremely short, it is not necessary to secure time until the next command is set following command reset setting.
0: Normal operation
1: Command reset</td></tr>
</table>

(3/13)

Register	Bit	Symbol	Function
R5	D_7	DTX1	The data bus of the display data at the time of 16-bit parallel data transfer inputted is set. DTX1 = L: 1-pixel/16-bit mode DTX1 = H: 1-pixel/18-bit mode
	D_6	BSTR	Sets the write mode for writing data to the display RAM. If the high-speed RAM write mode is selected, data is written to the display RAM in 2-pixel units inside the IC. When selecting the high-speed RAM write mode, be sure to write data to the display RAM in 2-pixel units. 0: Normal write mode (18-bit access) 1: High-speed RAM write mode (36-bit access)
	D_4	WAS	Window access mode setting When the window access mode is set, the address is increment/decrement only in the range set by the MIN. ·X address setting register (R8), MAX. ·X address setting register (R9), MIN. ·Y address setting register (R10), and MAX. ·Y address setting register (R11). 0: Normal operation 1: Window access mode
	D_2	INC	This bit selects the direction in which the address is to be increment. 0: Increments X address 1: Increments Y address
R6	D_7 to D_0	XAn	This register sets the X address of the display RAM. Set 000H to 0EFH.
R7	D_8 to D_0	YAn	This register sets the Y address of the display RAM. Set 000H to 13FH.
R8	D_7 to D_0	XMINn	Sets the minimum value of the X address in the window access mode. The X address is incremented up to the maximum value set by the MAX. ·X address register (R9), and then initialized to the address value set by this command. Set 000H to 0EFH.
R9	D_7 to D_0	XMAXn	Sets the maximum value of the X address in the window access mode. The X address is incremented up to the maximum value set by the MIN. ·X address register (R8), and then initialized to the address value set by this command. Set 000H to 0EFH.
R10	D_8 to D_0	YMINn	Sets the minimum value of the Y address in the window access mode. The Y address is incremented up to the maximum value set by the MAX. ·Y address register (R11), and then initialized to the address value set by this command. Set 000H to 13FH.
R11	D_8 to D_0	YMAXn	Sets the maximum value of the Y address in the window access mode. The Y address is incremented up to the address value set by this command, and then initialized to the minimum address value set by the MIN. ·Y address register (R10). Set 000H to 13FH.
R14	D_8 to D_0	SSLn	Scroll area start line register (000H to 13FH) When the screen is scrolled, the screen of the number of lines set by the scroll area line count register (R15) is scrolled up by the number of steps set by the scroll step count register (R16), starting from the line set by this command.
R15	D_8 to D_0	SAWn	Scroll area line count register (000H to 13FH) When the screen is scrolled, the screen of the number of lines set by this command is scrolled up by the number of steps set by the scroll step count register (R16), starting from the line set by the scroll area start line register (R14).
R16	D_8 to D_0	SSTn	Scroll step count register (000H to 13FH) When the screen is scrolled, the screen of the number of lines set by the scroll area line count register (R15) and the scroll step count register (R16) is scrolled up by the number of steps set by this command. Note that because this command is invalid in the partial display mode, the scroll function cannot be used.

(4/13)

Register	Bit	Symbol	Function
R17	D_3	PSEL	This bit selects whether the data specified the display color of partial non-displaying area in PGR, PGG and the PGB bit as color data, using MSB of a display data RAM is used as color data. 0: Use the data specified by PGR, PGG and PGB 1: Display data RAM, making it into color data for MSB of a use.
	D_2	PGR	Sets the color of the screen other than the partial display area during partial display (R0: DTY = 1). One of eight colors can be selected (RGB: 1 bit each) as the OFF color. The relationship between each color data and the bits of this register is as follows. This relationship is not dependent upon the value of ADC. PGR: R OFF= 0, ON = 1 PGG: G OFF= 0, ON = 1 PGB: B OFF= 0, ON = 1
	D_1	PGG	
	D_0	PGB	
R20	D_8 to D_0	P1SLn	Partial1 display area start line register (000H to 13FH) During partial display (R0: DTY = 1), the area starting from the line set by this command and ending as set by the partial 1 display area line count register (R22) is the partial 1 display area.
R21	D_8 to D_0	P2SLn	Partial2 display area start line register (000H to 13FH) During partial display (R0: DTY = 1), the area starting from the line set by this command and ending as set by the partial 2 display area line count register (R23) is the partial 2 display area.
R22	D_8 to D_0	P1AWn	Partial1 display area line count register (000H to 13FH) An area starting from the line set by the partial 1 display area start register (R20) and ending as set by this command is the partial 1 display area. If this register is 0, the values of the partial 2 display area start line register (R21) and the partial 2 display area line count register (R23) are not valid.
R23	D_8 to D_0	P2AWn	Partial 2 display area line count register (000H to 13FH) An area starting from the line set by the partial 2 display area start register (R21) and ending as set by this command is the partial 2 display area. If the partial 1 display area line count register is 0, the values of the partial 2 display area start line register (R21) and partial 2 display area line count register (R23) are not valid.
R25	D_2	NWRGB	This bit commands invalid of RGB interface input. 0: Invalid for RGB interface input 1: Valid for RGB interface input
	D_1	RGBS	This bit selects RGB interface mode. 0: Through mode 1: Capture mode
	D_0	DISPCK	This bit selects timing clock for display output in RGB interface mode. 0: Internal oscillator clock 1: HSYNC/VSYNC/DOTCLK
R26	D_7 to D_4	HBPn	This bit sets horizontal back porch period of RGB interface. Horizontal back porch period = set value x DOTCLK unit In addition, set up more than "1".
	D_3 to D_0	VBPn	This bit sets vertical back porch period of RGB interface. Vertical back porch period = set value x HSYNC unit In addition, set up more than "2".
R27	D_8 to D_0	RGBSTn	These bits set the start line of the display area to be displayed by the RGB interface. (000H ≤ R27 ≤ 0EEH) Be sure to observe the relationship “Set value of R27 register < Set value of R28 register“.
R28	D_8 to D_0	RGBEDn	These bits set the end line of the display area to be displayed by the RGB interface. (000H ≤ R28 ≤ 13FH) Be sure to observe the relationship “Set value of R27 register < Set value of R28 register“.

(5/13)

Register	Bit	Symbol	Function
R29	D_7 to D_0	CAPXMINn	Minimum of X address is set up at the time of window access at the time of selecting capture mode by the RGB interface.
R30	D_7 to D_0	CAPXMAXn	Maximum of X address is set up at the time of window access at the time of selecting capture mode by the RGB interface.
R31	D_8 to D_0	CAPYMINn	Minimum of Y address is set up at the time of window access at the time of selecting capture mode by the RGB interface.
R32	D_8 to D_0	CAPYMAXn	Maximum of Y address is set up at the time of window access at the time of selecting capture mode by the RGB interface.
R34	D_0	OC	This bit is used for calibration. The time from calibration start command execution until calibration stop command execution becomes the time for 1 line. 0: Calibration stop 1: Calibration start
R38	D_7 to D_0	PSD1n	The value set as PSD1n is outputted from the serial interface output for external IC control. For more details, refer to **5.1.8 Serial interface for power supply IC control**.
R39	D_7 to D_0	PSD2n	The value set as PSD2n is outputted from the serial interface output for external IC control. For more details, refer to **5.1.8 Serial interface for power supply IC control**.
R40	D_7 to D_0	PSD3n	The value set as PSD3n is outputted from the serial interface output for external IC control. For more details, refer to **5.1.8 Serial interface for power supply IC control**.
R41	D_7 to D_0	PSD4n	The value set as PSD4n is outputted from the serial interface output for external IC control. For more details, refer to **5.1.8 Serial interface for power supply IC control**.
R42	D_7 to D_0	PSD5n	The value set as PSD5n is outputted from the serial interface output for external IC control. For more details, refer to **5.1.8 Serial interface for power supply IC control**.
R43	D_4	GSEL	Sets the maximum/minimum output potential of the γ–correction register. If the internal γ-output adjustment circuit is selected, the maximum/minimum output potential of the γ-correction register is: 0: Sets power supply voltage (outputs V_S and V_{SS} potential). 1: Uses voltage of internal γ-output adjustment circuit (uses VPH, VNH, VPL, VNL output)
	D_0	GONSEL	About connection between γ-correction resistance and a power supply 0: Connect the both ends of positive-polarity γ-resistance with V_S and GND when in used γ-correction by positive-polarity. On the other hand, γ-resistance by negative-polarity does not connect with V_S and GND. Moreover, the both ends of negative-polarity γ-resistance are connected with V_S and GND when in used γ-correction by negative-polarity. In that case, γ-resistance by positive-polarity does not connect with V_S and GND. 1: Connect both V_S and GND on the side of positive and negative γ-correction regardless of output from positive- or negative-polarity.
R44	D_7 to D_0	GPHn	Sets the voltage value of γ-amplitude adjustment of positive polarity. For more detail, refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R45	D_7 to D_0	GNHn	Sets the voltage value of γ-amplitude adjustment of negative polarity. For more detail, refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R46	D_7 to D_0	GPLn	Sets the voltage value of γ-amplitude adjustment of positive polarity. For more detail, refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R47	D_7 to D_0	GNLn	Sets the voltage value of γ-amplitude adjustment of negative polarity. For more detail, refer to **5.5 γ- Curve Correction Power Supply Circuit**.

(6/13)

Register	Bit	Symbol	Function
R48	D_7 to D_4	VDRPn	Positive-polarity γ-amplitude adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_3 to D_0	VSRPn	Positive-polarity γ-amplitude adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R49	D_7 to D_4	VLRPn	Positive-polarity γ-inclination adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_3 to D_0	VHRPn	Positive-polarity γ-inclination adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R50	D_6 to D_4	VGR1Pn	Positive-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_2 to D_0	VGR0Pn	Positive-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R51	D_6 to D_4	VGR3Pn	Positive-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_2 to D_0	VGR2Pn	Positive-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R52	D_7 to D_4	VDRNn	Negative-polarity γ-amplitude adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_3 to D_0	VSRNn	Negative-polarity γ-amplitude adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R53	D_7 to D_4	VLRNn	Negative-polarity γ-inclination adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_3 to D_0	VHRNn	Negative-polarity γ-inclination adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R54	D_6 to D_4	VGR1Nn	Negative-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_2 to D_0	VGR0Nn	Negative-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R55	D_6 to D_4	VGR3Nn	Negative-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
	D_2 to D_0	VGR2Nn	Negative-polarity γ-fine tuning adjustment register Refer to **5.5 γ- Curve Correction Power Supply Circuit**.
R56	D_1, D_0	GV8S1	The voltage concerning a panel is set at the time of 8-color mode. 0 : Set power supply 1: Set amplifier output

<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td rowspan="5">R59</td><td>D7</td><td>WHP</td><td>Sets the output mode of the reference voltage generator amplifier for setting the white level of the positive-polarity and negative-polarity sides (when VPL and VNL are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
0: Normal mode
1: High-power mode (output circuit capacity: twice that of normal mode)</td></tr>
<tr><td>D6 to D4</td><td>WIn</td><td>Sets the output bias current of the reference voltage generator amplifier for setting the white level of the positive-polarity and negative-polarity sides (when VPL and VNL are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
<table>
<tr><th>WI2</th><th>WI1</th><th>WI0</th><th>Amplifier Bias Current</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.025 μA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0.050 μA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0.100 μA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0.200 μA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0.500 μA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1.000 μA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1.500 μA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>2.000 μA</td></tr>
</table></td></tr>
<tr><td>D3</td><td>BHP</td><td>Sets the output mode of the reference voltage generator amplifier for setting the black level of the positive-polarity and negative-polarity sides (when VPH and VNH are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
0: Normal mode
1: High-power mode (output circuit capacity: twice that of normal mode)</td></tr>
<tr><td>D2 to D0</td><td>BIn</td><td>Sets the output bias current of the reference voltage generator amplifier for setting the black level of the positive-polarity and negative-polarity sides (when VPH and VNH are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
<table>
<tr><th>BI2</th><th>BI1</th><th>BI0</th><th>Amplifier Bias Current</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.025 μA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0.050 μA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0.100 μA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0.200 μA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0.500 μA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1.000 μA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1.500 μA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>2.000 μA</td></tr>
</table></td></tr>
</table>

(8/13)

Register	Bit	Symbol	Function
R60	D_7 to D_0	PSD6n	The value set as PSD6n is outputted from the serial interface output for external IC control. For more details, refer to **5.1.8 Serial interface for power supply IC control**.
R61	D_7 to D_0	PSD7n	The value set as PSD7n is outputted from the serial interface output for external IC control. For more details, refer to **5.1.8 Serial interface for power supply IC control**.
R62	D_7 to D_0	PSD8n	The value set as PSD8n is outputted from the serial interface output for external IC control. For more details, refer to **5.1.8 Serial interface for power supply IC control**.
R63	D_7 to D_0	PSD9n	The value set as PSD9n is outputted from the serial interface output for external IC control. For more details, refer to **5.1.8 Serial interface for power supply IC control**.
R64	D_7 to D_0	PSDAn	The value set as PSDAn is outputted from the serial interface output for external IC control. For more details, refer to **5.1.8 Serial interface for power supply IC control**.
R65	D_7 to D_0	PSDBn	The value set as PSDBn is outputted from the serial interface output for external IC control. For more details, refer to **5.1.8 Serial interface for power supply IC control**.
R66	D_1	LMD1	The AMP drive method of a source output is selected. 0: Hi-Z period turns OFF AMP of a source output (default). 1: In the normal drive, turn ON AMP also for the Hi-Z period of a source output (except at the time of 8 color mode and at the time of stand-by)
R68	D_6 to D_4	REFMn	When partial display, the case where it is set as non-refreshing drive ([GSM = 0, PT1 = 1, PT0 = 1] and [GSM = 1, PT1 = 0, PT0 = 0]), non-refreshing frame (source output stop, gate scanning stop) and a refresh cycle (source white level output [the normally white panel], gate scan) are set up in the combination of the value set as this flag and the value set as the REFBn flag. For more details, refer to **5.6.2 Partial display, non-display area and normal partial driving**. The number of non-refreshing frames = REFB [4:0] x REFM [3:0]
	D_3 to D_0	REFBn	When partial display, the case where it is set as non-refreshing drive ([GSM = 0, PT1 = 1, PT0 = 1] and [GSM = 1, PT1 = 0, PT0 = 0]), non-refreshing frame (source output stop, gate scanning stop) and a refresh cycle (source white level output [the normally white panel], gate scan) are set up in the combination of the value set as this flag and the value set as the REFMn flag. For more details, refer to **5.6.2 Partial display, non-display area and normal partial driving**. The number of non-refreshing frames = REFB [4:0] x REFM [3:0]

REFM2	REFM1	REFM0	Setting Value
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

REFB3	REFB2	REFB1	REFB0	Setting Value
0	0	0	0	Only non-refresh drive
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15

(9/13)

<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td rowspan="2">R72</td><td>D7</td><td>DC4</td><td rowspan="2">The frequency of the clock outputted from the PCCLK pin used as clocks, such as a DC/DC converter circuit of a power supply IC, is set up. This clock is generated from oscillation frequency (fosc), is cycle ratio by the number of setting stages of this flag, and is outputted.

<table>
<tr><th>DC4</th><th>DC3</th><th>PCCLK Clock Frequency</th></tr>
<tr><td>0</td><td>0</td><td>fosc ÷ 4</td></tr>
<tr><td>0</td><td>1</td><td>fosc ÷ 8</td></tr>
<tr><td>1</td><td>0</td><td>fosc ÷ 16</td></tr>
<tr><td>1</td><td>1</td><td>fosc ÷ 32</td></tr>
</table>

Remark When outputs a clock signal from PCCLK pin, it is necessary to operate an oscillation circuit (OSC2OFF [R1] = 0).</td></tr>
<tr><td>D6</td><td>DC3</td></tr>
<tr><td></td><td>D4 to D0</td><td>DSCGn</td><td>To compensate for a XDON output H output (it outputs from the next frame of RXDON = H), the output of ASW3, ASW2 and ASW1 are considered as the line period H output fixation set up with this flag. The output of ASW3, ASW2, ASW1, STV, CKV, FR and OEV are carried out to L output fixation after setting period.
When DSCGn = 000H setup, the output of ASW3, ASW2, ASW1, STV, CKV, FR and OEV are carried out to L output fixation to a XDON output H output (it outputs from the next frame of RXDON = H) and this timing.
For more details, refer to 5.8 Power Supply Sequence.

<table>
<tr><th>DSCG4</th><th>DSCG3</th><th>DSCG2</th><th>DSCG1</th><th>DSCG0</th><th>Setting Line Count</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>31</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>32</td></tr>
</table></td></tr>
<tr><td>R75</td><td>D7 to D0</td><td>ADLNn</td><td>The number of lines set up by this register is set up as the number of lines of the FP [2 Line fixed] + BP period of a frame changing.
For more details, refer to 5.4.2 1-frame period timing.
ADLNn ≤ 2: Only BP period
ADLNn > 3: FP line count [2-line] + BP period line count = Setting line count = ADLNn setting value

<table>
<tr><th>ADLN7</th><th>ADLN6</th><th>ADLN5</th><th>ADLN4</th><th>ADLN3</th><th>ADLN2</th><th>ADLN1</th><th>ADLN0</th><th>Setting line count</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>BP1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>BP2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>FP2 + BP1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>FP2 + BP2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>FP2 + BP3</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>FP2 + BP252</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>FP2 + BP253</td></tr>
</table></td></tr>
</table>

(10/13)

<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R76</td><td>D4 to D0</td><td>ADCKn</td><td>The number of clocks set up by this register is inserted as a dummy clock within 1-line drive period.
For more details, refer to 5.4.1 1-line period timing.

<table>
<tr><th>ADCK4</th><th>ADCK3</th><th>ADCK2</th><th>ADCK1</th><th>ADCK0</th><th>Setting Clock Count</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>30</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31</td></tr>
</table></td></tr>
<tr><td rowspan="7">R77</td><td>D5</td><td>RSOUT</td><td>Operation of source output (Yn) is controlled.
0: OFF (VSS output fixed)
1: ON (Normal operation)
Setting by this flag becomes effective from the output timing of the following frame after inputted.
About the change timing of the frame, refer to 5.4.2 1-frame period timing.</td></tr>
<tr><td>D4</td><td>RGOE2</td><td>Operation of panel discharge is controlled.
0: GOE2 (H output), RSW, GSW and BSW (Normal operation)
1: GOE2 (L output), RSW, GSW and BSW (H fixed)
Setting by this flag becomes effective from the output timing of the following frame after inputted.
About the change timing of the frame, refer to 5.4.2 1-frame period timing.</td></tr>
<tr><td>D3</td><td>RGOE1</td><td>Operation of gate output enable signal is controlled.
0: OFF (VSS output fixed)
1: ON (Normal operation)
Setting by this flag becomes effective from the output timing of the following frame after inputted.
About the change timing of the frame, refer to 5.4.2 1-frame period timing.</td></tr>
<tr><td>D2</td><td>RXDON</td><td>Operation of panel discharge is controlled.
0: XDON (L output), ASW1, ASW2 and ASW3 (Normal operation)
1: XDON (H output), ASW1, ASW2 and ASW3 (H fixed)
Setting by this flag becomes effective from the output timing of the following frame after inputted.
About the change timing of the frame, refer to 5.4.2 1-frame period timing.</td></tr>
<tr><td>D1</td><td>ROEVE</td><td>OEVE output operation is controlled.
0: OEVE (L fixed)
1: OEVE (H fixed)
Setting by this flag becomes effective from the output timing of the following frame after inputted.
About the change timing of the frame, refer to 5.4.2 1-frame period timing.</td></tr>
<tr><td>D0</td><td>ROEV</td><td>Operation of output enable signal (OEV) is controlled.
0: OFF (L output fixed)
1: ON (Normal operation)
Setting by this flag becomes effective from the output timing of the following frame after inputted.
About the change timing of the frame, refer to 5.4.2 1-frame period timing.</td></tr>
</table>

(11/13)

<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td rowspan="4">R78</td><td>D6</td><td>RMMSK</td><td>The mask of the data of display RAM is carried out by "0" data.
0: All "0" data mask
1: RAM data enable (Normal operation)</td></tr>
<tr><td>D5</td><td>RMST1</td><td rowspan="2">It sets up about operation of power supply supplied to RAM circuit.

<table><tr><th>RMST1</th><th>RMST0</th><th>Display RAM Power Supply</th><th>Display RAM State</th></tr><tr><td>0</td><td>0</td><td>Power OFF</td><td>RAM data is abandoned</td></tr><tr><td>0</td><td>1</td><td>Low Power</td><td>RAM data maintenance Note1</td></tr><tr><td>1</td><td>0</td><td>Power ON</td><td>RAM writing operation is possible Note2</td></tr><tr><td>1</td><td>1</td><td colspan="2">Setting prohibited</td></tr></table>Notes 1. Sleep mode etc. can be used when low power consumption and RAM data need to be held. When normal operation, do not set up (Display ON, writing of display data).
2. When normal operation, use it in this mode (Display ON, writing of display data).</td></tr>
<tr><td>D4</td><td>RMST0</td></tr>
<tr><td>D3</td><td>PT1</td><td rowspan="2">When partial display, the drive of non-display area can be selected by setup of PT1, PT0 and GSM [R0] as shown in below.
For more details, refer to 5.6.1 Partial display, non-display area driving.

<table><tr><th>GSM [R0]</th><th>PT1</th><th>PT0</th><th>Partial Display Operation</th></tr><tr><td rowspan="4">0</td><td>0</td><td>0</td><td rowspan="3">Normal partial drive</td></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>Non-refresh drive 1</td></tr><tr><td rowspan="2">1</td><td>0</td><td>0</td><td>Non-refresh drive 2</td></tr><tr><td colspan="2">Other than above</td><td>Setting prohibited</td></tr></table></td></tr>
<tr><td>D2</td><td>PT0</td></tr>
<tr><td>D1</td><td>REV</td><td>The gray-scale level of source output is inverted.
0: Normal operation
1: Gray-scale inversion output</td></tr>
<tr><td>R79</td><td>D5 to D0</td><td>GOSTn</td><td>The start timing of the signal outputted from GOE1 (/GOE1) and OEV (/OEV) pin is set up.
Set up in the range 001H ≤ R79 ≤ 026H.
In addition, prohibited for setting up the same value as R79 and R80.</td></tr>
<tr><td>R80</td><td>D5 to D0</td><td>GOEDn</td><td>The end timing of the signal outputted from GOE1 (/GOE1) and OEV (/OEV) pin is set up.
Set up in the range 001H ≤ R80 ≤ 026H.
In addition, prohibited for setting up the same value as R79 and R80.</td></tr>
<tr><td>R81</td><td>D5 to D0</td><td>PCSTn</td><td>The start timing of the signal outputted from PCP (/PCP), PCN (/PCN) and PC (/PC) pin is set up.
Set up in the range 001H ≤ R81 ≤ 026H.
In addition, when unused output signal from these pins, set up the same value as R81 and R82.</td></tr>
<tr><td>R82</td><td>D5 to D0</td><td>PCEDn</td><td>The end timing of the signal outputted from PCP (/PCP), PCN (/PCN) and PC (/PC) pin is set up.
Set up in the range 001H ≤ R81 ≤ 026H.
In addition, when unused output signal from these pins, set up the same value as R81 and R82.</td></tr>
<tr><td>R83</td><td>D5 to D0</td><td>RSTn</td><td>The start timing of the signal outputted from RSW (/RSW) and ASW1 (/ASW1) pin is set up.
Set up in the range 002H ≤ R83 ≤ 025H.
In addition, prohibited for setting up the same value as R83 and R84.</td></tr>
</table>

(12/13)

Register	Bit	Symbol	Function
R84	D_5 to D_0	REDn	The end timing of the signal outputted from RSW (/RSW) and ASW1 (/ASW1) pin is set up. Set up in the range 002H ≤ R84 ≤ 025H. In addition, prohibited for setting up the same value as R83 and R84.
R85	D_5 to D_0	GSTn	The start timing of the signal outputted from GSW (/GSW) and ASW2 (/ASW2) pin is set up. Set up in the range 002H ≤ R85 ≤ 025H. In addition, prohibited for setting up the same value as R85 and R86.
R86	D_5 to D_0	GEDn	The end timing of the signal outputted from GSW (/GSW) and ASW2 (/ASW2) pin is set up. Set up in the range 002H ≤ R86 ≤ 025H. In addition, prohibited for setting up the same value as R85 and R86.
R87	D_5 to D_0	BSTn	The start timing of the signal outputted from BSW (/BSW) and ASW3 (/ASW3) pin is set up. Set up in the range 002H ≤ R87 ≤ 025H. In addition, prohibited for setting up the same value as R87 and R88.
R88	D_5 to D_0	BEDn	The end timing of the signal outputted from BSW (/BSW) and ASW3 (/ASW3) pin is set up. Set up in the range 002H ≤ R88 ≤ 025H. In addition, prohibited for setting up the same value as R87 and R88.
R89	D_5 to D_0	E1STn	The start timing of the signal outputted from EXT1 (/EXT1) pin is set up. Set up in the range 001H ≤ R89 ≤ 026H. In addition, when unused output signal from these pins, set up the same value as R89 and R90. In default, these bits are fixed to EXT1 = L, /EXT1 = H.
R90	D_5 to D_0	E1EDn	The end timing of the signal outputted from EXT1 (/EXT1) pin is set up. Set up in the range 001H ≤ R90 ≤ 026H. In addition, when unused output signal from these pins, set up the same value as R89 and R90.
R91	D_5 to D_0	E2STn	The start timing of the signal outputted from EXT2 (/EXT2) pin is set up. Set up in the range 001H ≤ R91 ≤ 026H. In addition, when unused output signal from these pins, set up the same value as R91 and R92. In default, these bits are fixed to EXT2 = L, /EXT2 = H.
R92	D_5 to D_0	E2EDn	The end timing of the signal outputted from EXT2 (/EXT2) pin is set up. Set up in the range 001H ≤ R92 ≤ 026H. In addition, when unused output signal from these pins, set up the same value as R91 and R92.

(13/13)

Register	Bit	Symbol	Function
R93	D_6	RVCOT	Operation of common timing signal (VCOUT) is controlled. 0: VCOUT signal and FR signal OFF (L output fixed) 1: VCOUT signal and FR signal ON (Normal operation) Setting by this flag becomes effective from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_5	RGBSW	Operation of panel multi-plexus signal (RSW, GSW, BSW) is controlled. 0: OFF (L output fixed) 1: ON (Normal operation) Setting by this flag becomes effective from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_4	RGSTB	Operation of the strobe signal for gate control (GSTB) is controlled. 0: OFF (H output fixed) 1: ON (Normal operation) Setting by this flag becomes effective from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_3	RGCLK	Operation of the clock signal for gate control (GCLK) is controlled. 0: OFF (L output fixed) 1: ON (Normal operation) Setting by this flag becomes effective from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_2	RASW	Operation of panel multi-plexus signal (ASW1, ASW2, ASW3) is controlled. 0: OFF (L output fixed) 1: ON (Normal operation) Setting by this flag becomes effective from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_1	RSTV	Operation of the start signal for gate control (STV) is controlled. 0: OFF (L output fixed) 1: ON (Normal operation) Setting by this flag becomes effective from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
	D_0	RCKV	Operation of the clock signal for gate control (CKV) is controlled. 0: OFF (L output fixed) 1: ON (Normal operation) Setting by this flag becomes effective from the output timing of the following frame after inputted. About the change timing of the frame, refer to **5.4.2 1-frame period timing**.
★ R98	D_5 to D_0	–	Be sure to use 005H as the value for this register.

8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_S	–0.5 to +6.0	V
Power supply voltage	V_{DD1}	–0.5 to +2.2	V
Power supply voltage	V_{DD2}	–0.5 to +2.2	V
Power supply voltage	V_{DDIO}	–0.5 to +4.6	V
Power supply voltage	V_{CC1}	–0.5 to +4.6	V
γ-correction power supply	V_1 to V_5	–0.5 to V_S + 0.5	V
Input voltage	V_{I1}	–0.5 to V_{DDIO} + 0.5	V
Input voltage	V_{I2}	–0.5 to V_{CC1} + 0.5	V
Input current	I_I	±10	mA
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_S	4.0	5.0	5.5	V
Power supply voltage	V_{DD1}	1.6		2.0	V
Power supply voltage	V_{DD2}	1.6		2.0	V
Power supply voltage	V_{DDIO}	1.8		3.3	V
Power supply voltage	V_{CC1}	2.5		3.3	V
Input voltage	V_{I1} **Note1**	0		V_{DDIO}	V
Input voltage	V_{I2} **Note2**	0		V_{CC1}	V

Notes 1. About pins of V_{DDIO} power supply system: /CS, /RD (E), /WR (R,/W), D_0 to D_{17}, RS, /RESET, etc.

2. About pins of V_{CC1} power supply system: PSX, C86, TOUT0 to TOUT19, GOE1, GOE2, GSTB, GCLK, TSTRTST, TSTVIHL, etc.

Electrical Specifications (Unless Otherwise Specified, T_A = –40 to +85°C, V_{DD1} = V_{DD2} = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V, V_{DDIO} = 1.8 to 3.3 V, V_S = 4.0 to 5.5 V)

Parameter	Symbol	Condition	MIN.	TYP.[Note1]	MAX.	Unit
High level input voltage	V_{IH1}	V_{DDIO}	0.8 V_{DDIO}			V
	V_{IH2}	V_{CC1}	0.8 V_{CC1}			V
Low level input voltage	V_{IL1}	V_{DDIO}			0.2 V_{DDIO}	V
	V_{IL2}	V_{CC1}			0.2 V_{CC1}	V
High level output voltage	V_{OH1}	V_{DDIO}, I_{OUT} = –1 mA	0.8 V_{DDIO}			V
	V_{OH2}	V_{CC1}, I_{OUT} = –1 mA	0.8 V_{CC1}			V
Low level output voltage	V_{OL1}	V_{DDIO}, I_{OUT} = 1 mA			0.2 V_{DDIO}	V
	V_{OL2}	V_{CC1}, I_{OUT} = 1 mA			0.2 V_{CC1}	V
High level input current	I_{IH1}	V_{DDIO}			1	μA
	I_{IH2}	V_{CC1}			1	μA
Low level input current	I_{IL1}	V_{DDIO}			–1	μA
	I_{IL2}	V_{CC1}			–1	μA
High level leakage current	I_{LIH}	D_0 to D_{17}			1	μA
Low level leakage current	I_{LIL}	D_0 to D_{17}			–1	μA
High level driver output current	I_{VOH}	V_X = 3.5 V, V_{OUT} = 3.0 V, V_S = 5.0 V			–25	μA
Low level driver output current	I_{VOL}	V_X = 1.5 V, V_{OUT} = 2.0 V, V_S = 5.0 V	25			μA
Current consumption	I_{DDIO}	V_{DDIO} (when non-access CPU)			5	μA
	I_{CC1}	V_{CC1} (when non-access CPU)			400	μA
	I_{STBY}	V_{DDIO}			1	μA
		V_{CC1} (STBY mode)			50	μA
		V_{CC1} (DEEP SLEEP)			200	μA
		V_{CC1} (SLEEP mode)			300	μA
	I_S	260,000-color mode[Note2]			1.5	μA
		8-color mode[Note2]			50	μA
		Stand-by mode			5	μA
Output voltage deviation	ΔV_O	V_S = 5.0 V, V_{OUT} = 1.65 V[Note3]			10	mV
		V_S = 5.0 V, V_{OUT} = 2.50 V[Note3]			10	mV

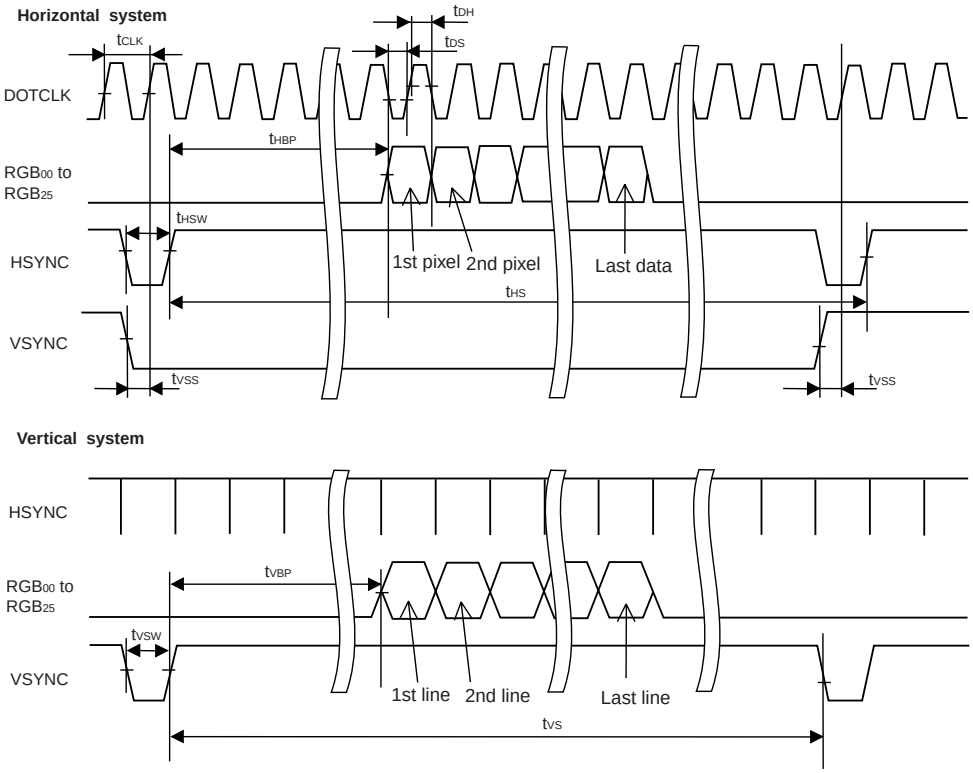
Notes 1. TYP. values are reference values when T_A = 25°C

2. Frame frequency: 60 Hz, line inversion mode selection, dot checkerboard input pattern, and no load.

3. V_X: The output voltage of analog output pins Y_1 to Y_{240}, V_{OUT}: The application voltage of analog output pins Y_1 to Y_{240}.

AC Characteristics (Unless Otherwise Specified, T_A = –40 to +85°C, V_{DD1} = V_{DD2} = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V, V_S = 4.0 to 5.5 V)

(a) RGB interface



Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Dot clock cycle time	t_{CLK}		150			ns
Dot clock high level pulse width	t_{CLKH}		75			ns
Dot clock low level pulse width	t_{CLKL}		75			ns
Data setup time	t_{DS}		60			ns
Data hold time	t_{DH}		60			ns
HSYNC pulse width	t_{HSW}		1			DOTCLK
Horizon period back porch time	t_{HBP}		1			DOTCLK
VSYNC pulse width	t_{VSW}		1			HS
VSYNC setup time	t_{VSS}		60			ns
Vertical period back porch time	t_{VBP}		2			HS

Note TYP. values are reference values when T_A = 25°C.

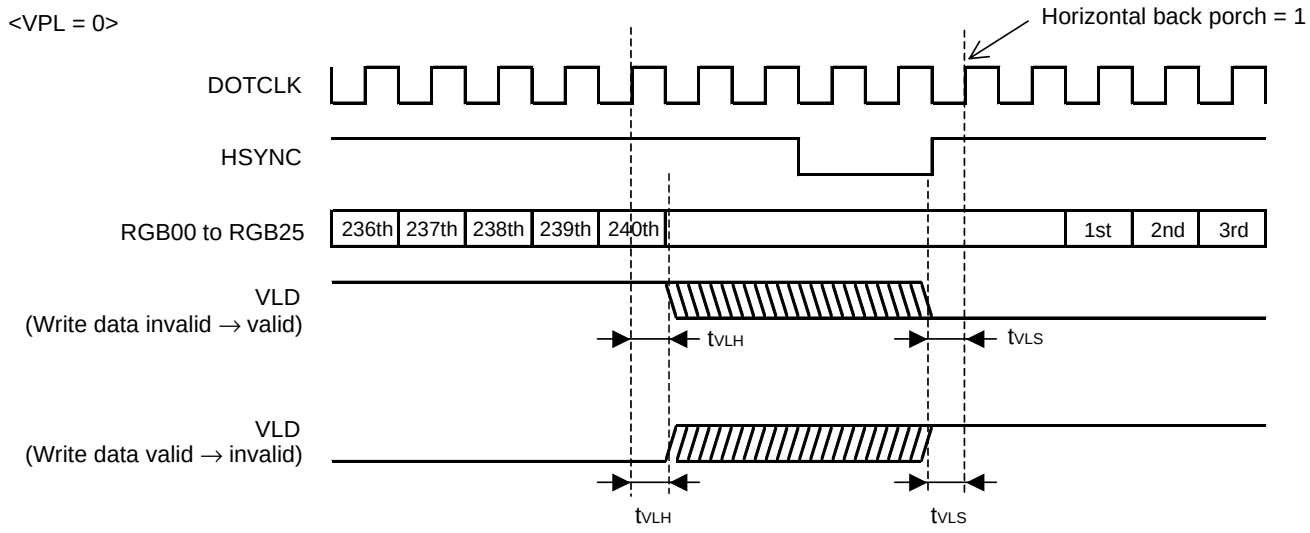
Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC1}.

3. One frame period ≥ VSYNC active period (1 HS) + VBP value (2 HS) + display line count (320 HS) = 323 line period (HS)

4. 1 line period HSYNC active period (1 DOTCLK) + HBP value (1 DOTCLK) + display pixel count (240 DOTCLK) = 242 clock period (DOTCLK)

(b) RGB interface capture mode VLD function



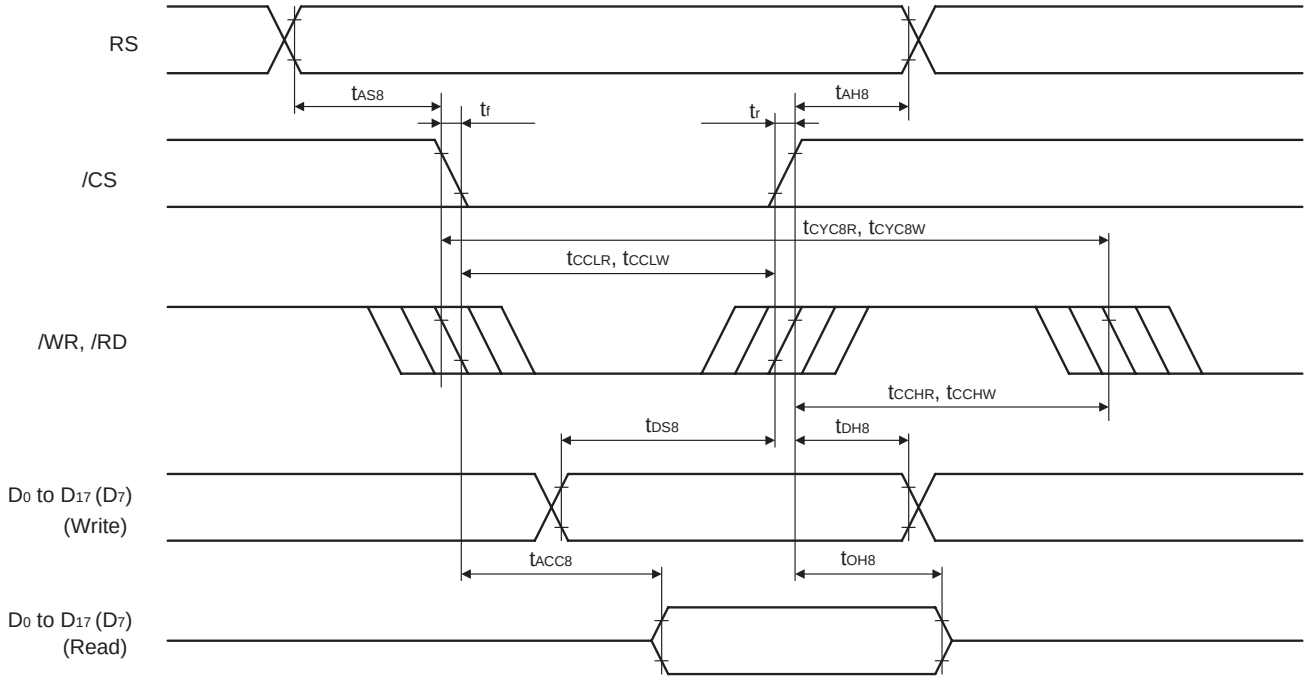
Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
VLD setup time	t_{VLS}		60			ns
VLD hold time	t_{VLH}		60			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC1}.

(c) i80 series CPU interface



When V_{DD1} = V_{DD2} = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V (normal write mode)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	10			ns
Address setup time	t_{AS8}	RS	10			ns
System cycle time (when write)	t_{CYC8W}	VSTBY = Low R98 = 005H	100			ns
		VSTBY = High V_{DD1} = V_{DD2} = 1.7 MIN. R98 = 005H	100			ns
System cycle time (when read)	t_{CYC8R}		250			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	25			ns
Control low-level pulse width (/RD)	t_{CCLR}	/RD	140			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	20			ns
Control high-level pulse width (/RD)	t_{CCHR}	/RD	80			ns
Data setup time	t_{DS8}	D_0 to D_{17}	25			ns
Data hold time	t_{DH8}	D_0 to D_{17}	10			ns
/RD access time	t_{ACC8}	D_0 to D_{17}, C_L = 100 pF			140	ns
Output disable time	t_{OH8}	D_0 to D_{17}, C_L = 100 pF	5		140	ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC1}.

When V_{DD1} = V_{DD2} = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V (high-speed RAM write mode, valid only for writing data)

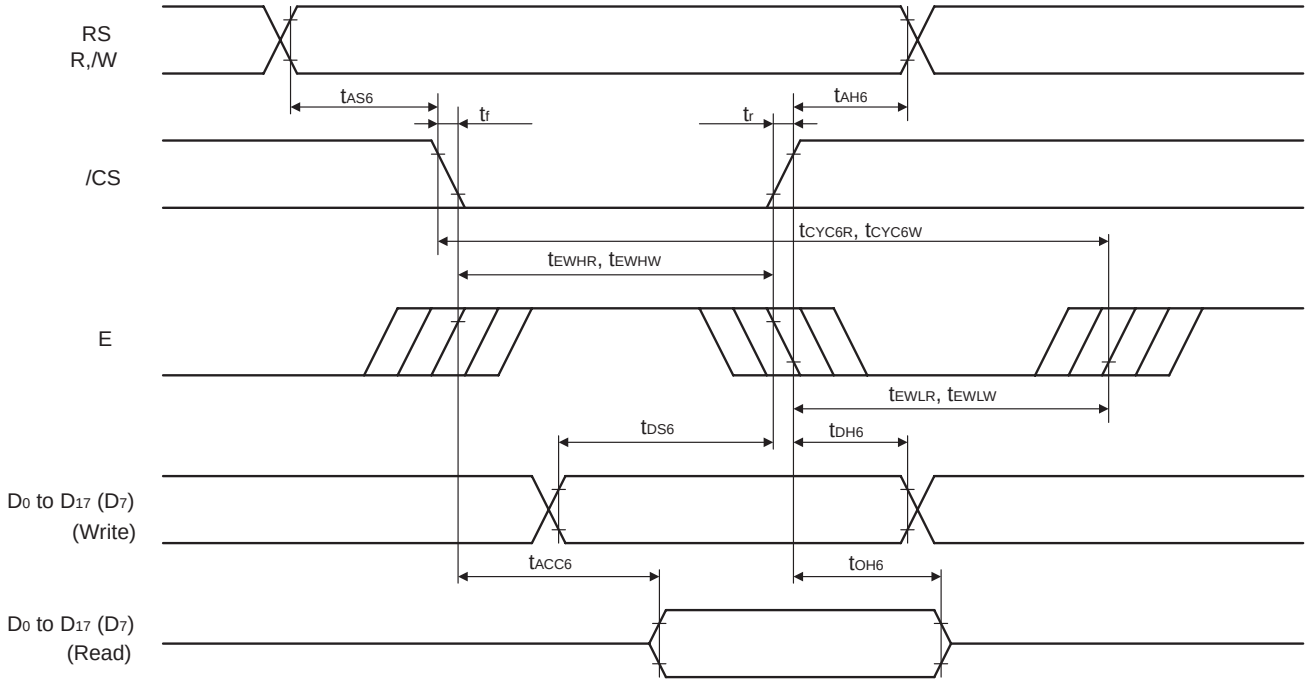
Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	10			ns
Address setup time	t_{AS8}	RS	10			ns
System cycle time (when write)	t_{CYC8W}		65			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	25			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	20			ns
Data setup time	t_{DS8}	D_0 to D_{17}	25			ns
Data hold time	t_{DH8}	D_0 to D_{17}	10			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC1}.

(d) M68 series CPU interface



When V_{DD1} = V_{DD2} = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V (normal write mode)

Parameter		Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time		t_{AH6}	RS	10			ns
Address setup time		t_{AS6}	RS	10			ns
System cycle time (when write)		t_{CYC6W}	VSTBY = Low R98 = 005H	100			ns
			VSTBY = High V_{DD1} = V_{DD2} = 1.7 MIN. R98 = 005H	100			ns
System cycle time (when read)		t_{CYC6R}		250			ns
Data setup time		t_{DS6}	D_0 to D_{17}	25			ns
Data hold time		t_{DH6}	D_0 to D_{17}	10			ns
Access time		t_{ACC6}	D_0 to D_{17}, C_L = 100 pF			140	ns
Output disable time		t_{OH6}	D_0 to D_{17}, C_L = 100 pF	5		140	ns
Enable high level pulse width	Read	t_{EWHR}	E	140			ns
	Write	t_{EWHW}	E	35			ns
Enable low level pulse width	Read	t_{EWLR}	E	80			ns
	Write	t_{EWLW}	E	30			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a high-speed system cycle time, the rated value range is either ($t_r + t_f$) < ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) or ($t_r + t_f$) < ($t_{CYC6} - t_{EWLW} - t_{EWHW}$).

2. All timing is rated based on 20 to 80% of V_{CC1}.

When V_{DD1} = V_{DD2} = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V (high-speed RAM write mode, valid only for writing data)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH6}	RS	10			ns
Address setup time	t_{AS6}	RS	10			ns
System cycle time	t_{CYC6W}		80			ns
Data setup time	t_{DS6}	D_0 to D_{17}	25			ns
Data hold time	t_{DH6}	D_0 to D_{17}	10			ns
Enable high level pulse width	t_{EWHW}	E	35			ns
Enable low level pulse width	t_{EWLW}	E	30			ns

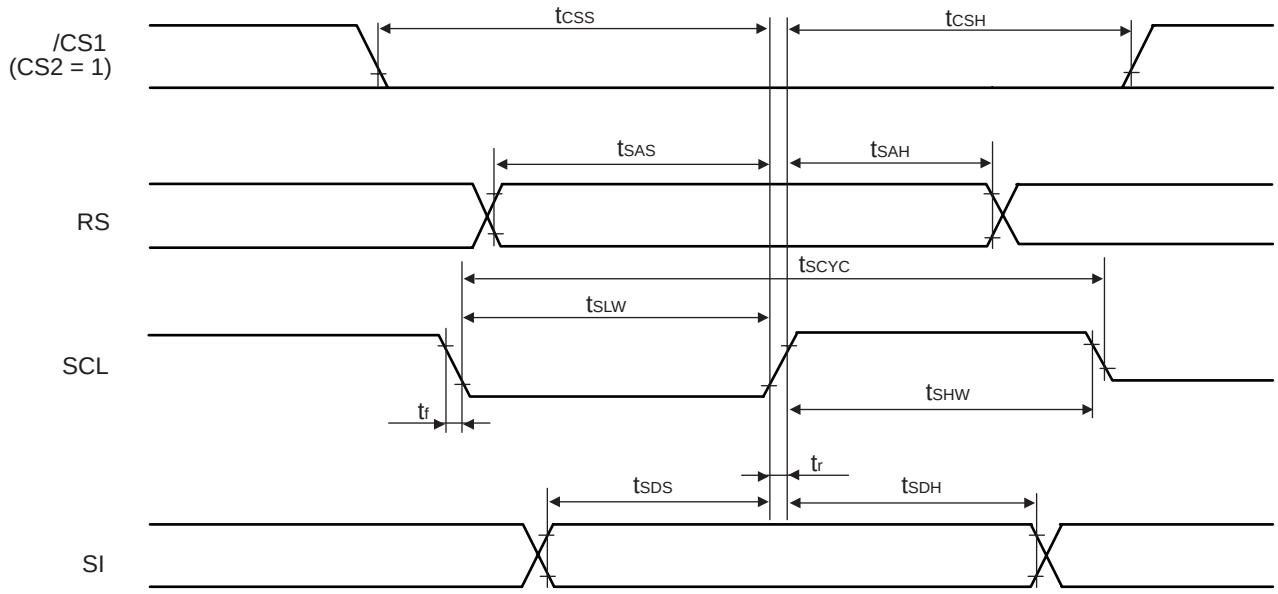
Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a high-speed system cycle time, the rated value range is either ($t_r + t_f$) < ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) or ($t_r + t_f$) < ($t_{CYC6} - t_{EWLW} - t_{EWHW}$).

2. All timing is rated based on 20 to 80% of V_{CC1}.

(e) Serial interface

<1> Serial interface between CPU and the μPD161801



When V_{DD1} = V_{DD2} = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V

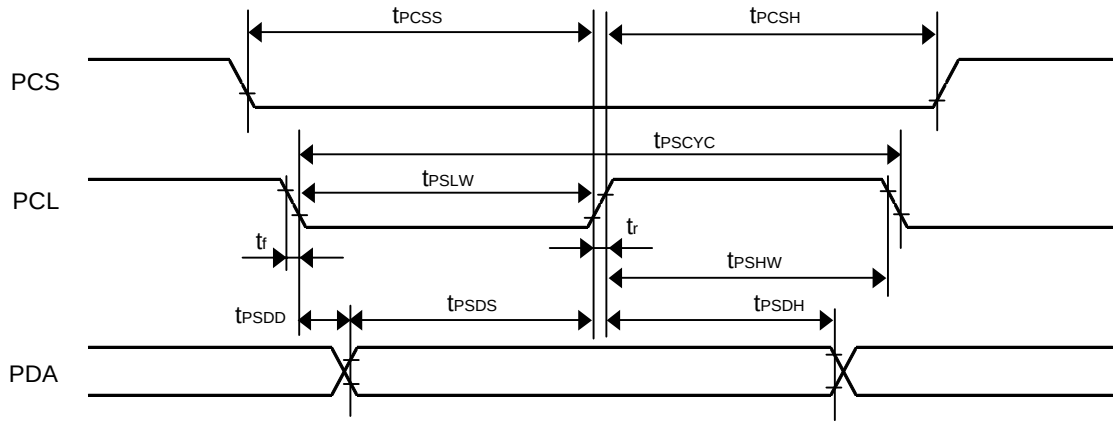
Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Serial clock cycle	t_{SCYC}	SCL	150			ns
SCL high level pulse width	t_{SHW}	SCL	60			ns
SCL low level pulse width	t_{SLW}	SCL	60			ns
Address hold time	t_{SAH}	RS	90			ns
Address set up time	t_{SAS}	RS	90			ns
Data set up time	t_{SDS}	SI	60			ns
Data hold time	t_{SDH}	SI	60			ns
CS - SCL time	t_{CSS}	/CS	90			ns
	t_{CSH}	/CS	90			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC1}.

<2> Serial interface between the μPD161801and the μPD161861



When $V_{DD1} = V_{DD2}$ = 1.6 to 2.0 V, V_{CC1} = 2.5 to 3.3 V

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Serial clock cycle	t_{PSCYC}		2			1/f_{OSC}
PCL high level pulse width	t_{PSHW}		1			1/f_{OSC}
PCL low level pulse width	t_{PSLW}		1			1/f_{OSC}
Data set up time	t_{PSDS}		1			1/f_{OSC}
Data hold time	t_{PSDH}		1			1/f_{OSC}
PCL↓ → PDA output delay time	t_{PSDD}		30			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC1}.

3. f_{OSC} is the internal oscillator's oscillation frequency.

(f) Common

Parameter	Symbol	Condition	MIN.	TYP.[Note1]	MAX.	Unit
Calibration setting time (frame frequency)	t_{cal} (f_{FRAME0})	**Note2**		51.9 (60)		μs (Hz)
Frame frequency	f_{FRAME2}	Calibrated [Note3]		60		Hz
	f_{FRAME3}	Calibrated [Note4]		60		Hz
Reset pulse width	t_{RW}		100			ns
Reset time	t_R	/RESET↑ to interface operation	100			ns

Notes 1. TYP. values are reference values when T_A = 25°C.

2. The relationship between the frame frequency and the calibration setting time is as follows.

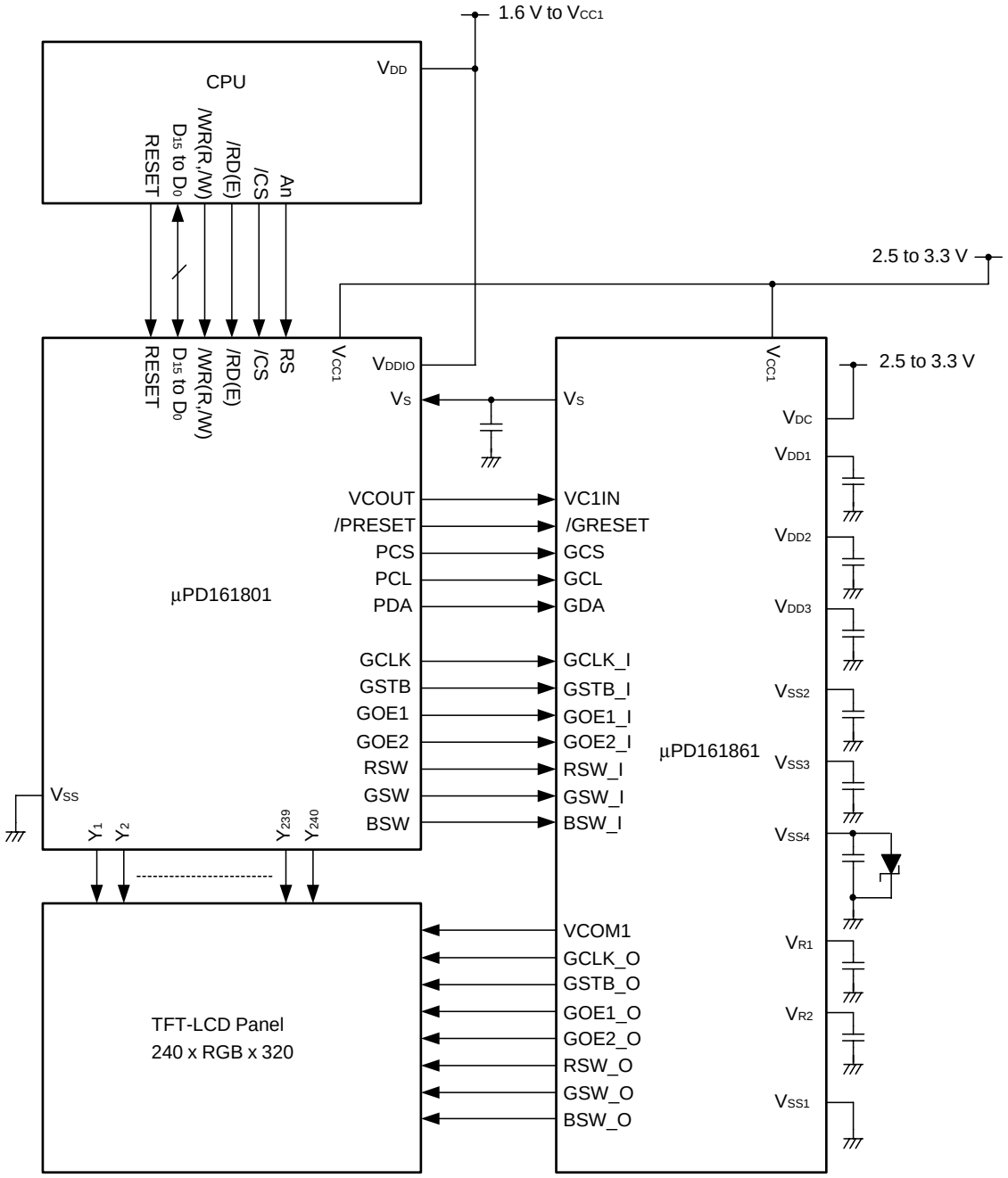
$f_{FRAME0} = 1/t_{cal} \times 321$

3. Measured at T_A = –40 to +85°C, after calibration at frame frequency = 60 Hz, T_A = 25°C exactly.

4. Measured at ±5°C, after calibration at frame frequency = 60 Hz exactly.

★ 9. THE μPD161801 AND THE μPD161861 CONNECTION

Connection diagram examples for the μPD161801 and the μPD161861 are show below.

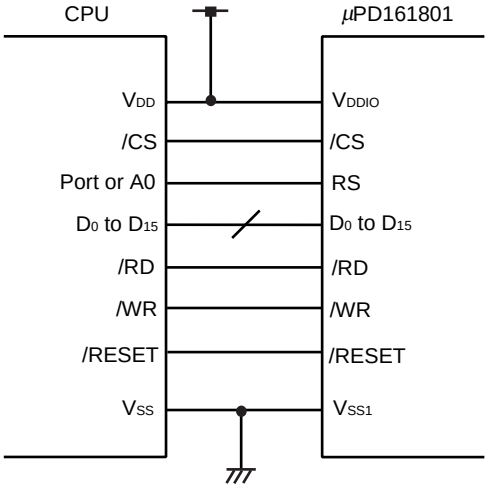


10. EXAMPLE OF THE μPD161801 AND CPU CONNECTION

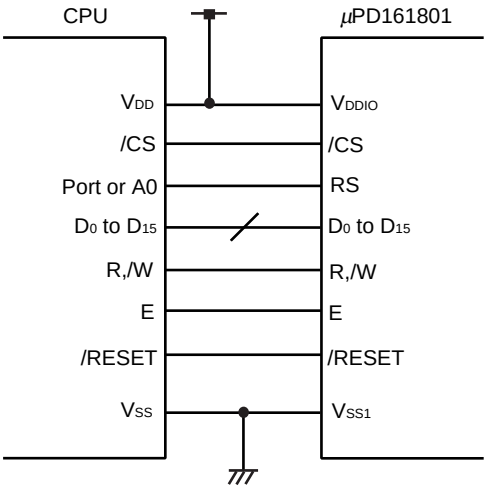
Examples of the μPD161801 and CPU connection are shown below.

In the example below, RS pin control in parallel interface mode is described for the case when the least significant bit of the address bus is being used.

(1) i80 series format



(2) M68 series format



NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

- **The information contained in this document is being issued in advance of the production cycle for the product. The parameters for the product may change before final production or NEC Electronics Corporation, at its own discretion, may withdraw the product prior to its production.**
- No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Electronics. NEC Electronics assumes no responsibility for any errors that may appear in this document.
- NEC Electronics does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC Electronics products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Electronics or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of a customer's equipment shall be done under the full responsibility of the customer. NEC Electronics assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC Electronics endeavors to enhance the quality, reliability and safety of NEC Electronics products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC Electronics products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.
- NEC Electronics products are classified into the following three quality grades: "Standard", "Special", and "Specific". The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of an NEC Electronics product depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics products before using it in a particular application.

  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.

  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC Electronics products is "Standard" unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact an NEC Electronics sales representative in advance to determine NEC Electronics' willingness to support a given application.

(Note)

(1) "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.

(2) "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).