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April 1st, 2010 Renesas Electronics Corporation

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BIPOLAR ANALOG INTEGRATED CIRCUIT $\mu PC8101GR$

150 MHz SILICON QUADRATURE MODULATOR IC FOR DIGITAL MOBILE COMMUNICATIONS

DESCRIPTION

 μ PC8101GR is a silicon monolithic integrated circuit designed as up-to-150 MHz quadrature modulator for digital mobile communications, mainly CT2. This modulator consists of digital 90° phase shifter, dual mixers and various buffer amplifiers which are packaged in 20 pin SSOP. Up/down converter IC (μ PC8100GR) is also available as for kit-use with this IC. So, these pair devices contribute to make RF block small, high-performance and low power-consumption.

This product is manufactured using NEC's 20 GHz f⊤ NESAT[™]III silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion and migration. Thus, this product has excellent performance, uniformity and reliability.

FEATURES

- Operating frequency: fir = 50 MHz to 150 MHz, Local input frequency: fLo = 100 MHz to 300 MHz, fi/Q = DC to 500 kHz
- Digital 90° phase shifter is incorporated. (Due to the flip flop phase shifter, $f_{IF} = f_{Lo}/2 + f_{I/Q}$.)
- 20 pin SSOP suitable for high-density surface mounting.
- Supply voltage Vcc = 2.7 to 5.5 V
- Equipped with Power Save Function.

APPLICATIONS

- Typical application Digital cordless phone CT2. (In the case of I/Q method)
- Further application Digital communication equipments.

ORDERING INFORMATION

PART NUMBER	PACKAGE	SUPPLYING FORM
μPC8101GR-E2	20 pin plastic SSOP (225 mil)	Embossed tape 12 mm wide. QTY 2.5 kp/Reel. Pin 1 indicates roll-in direction of tape.

Remark To order evaluation samples, please contact your local NEC sales office. (Order number: µPC8101GR)

Caution electro-static sensitive devices

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INTERNAL BLOCK DIAGRAM AND PIN CONNECTIONS



18 17 16 15 14 13 12 11 REG. 90° 270° LPF F/F 0° 180° LPF 3 4 5 6 7 8 9 10	1. LOCAL IN 2. LOCAL IN 3. GND 4. \overline{Q} – BIAS 5. Q – BIAS 6. GND 7. \overline{Q} – INPUT 8. Q – INPUT 9. GND 10. IF OUTPUT 11. Vcc 12. POWER SAVE 13. I – INPUT 14. \overline{I} – INPUT 15. GND 16. I – BIAS 17. \overline{I} – BIAS 18. GND 19. N.C. 20. GND	(Top View) 1 20 2 3 3 4 4 17 5 6 6 15 7 4 8 9 9 12 10 11

PIN EXPLANATION

PIN NO.	ASSIGNMENT	APPLIED VOLTAGE (V)	PIN VOLTAGE (V)	FUNCTION AND APPLICATION	EQUIVALENT CIRCUIT
1	LOCAL IN	_	_	Local input for phase shifter. This input impedance is 50 Ω matched internally.	
2	LOCAL IN	_	2.0	Bypass of local buffer amplifier input. Grounded through capacitor.	
3	GND	0	_	It must be connected to the system ground with minimum inductance. Ground pat- tern on the board should be formed as wide as possible. (Track length should be kept as short as possible.)	
4	Q-BIAS	_	0.175	These pins are to adjust local leakage level. These pins should be grounded through	
5	Q-BIAS	_	0.175	register 1 kΩ adjustable 30 mV offset.	
6	GND	0	-	Track length should be kept as short as possible.	
7	Q-INPUT	Vcc/2	-	Input for Q signal. This input impedance is larger than 500 kΩ. As Q signal, Vcc/ 2 bias DC signal should be input.	
8	Q-INPUT	Vcc/2		Input for Q signal. This input impedance is larger than 500 kΩ. As Q signal, Vcc/ 2 biased 1V _{P-P} signal should be input.	
9	GND	0	-	Track length should be kept as short as possible.	
10	IF OUTPUT	_	1.4	IF output from modulator. This output is emitter follower as 50 Ω impedance. IF output frequency is provided as fiF = fLo/ 2 + fl/Q.	
11	Vcc	2.7 to 5.5	-	Supply voltage pin.	

PIN NO.	ASSIGNMENT	APPLIED VOLTAGE (V)	PIN VOLTAGE (V)	FUNCTION AND APPLICATION	EQUIVALENT CIRCUIT
12	POWER SAVE	0 to 5.5	_	Power save control pin. This pin can control ON/OFF operation with bias as follows; $\boxed{ \begin{tabular}{c} \hline Bias: V & Operation \\ \hline V_{PS} & $\geq 1.8 & ON \\ \hline 0 & to 1.0 & OFF \\ \hline \end{tabular}$	
13	I-INPUT	Vcc/2	-	Input for I signal. This input imped- ance is larger than 500 kΩ. As I signal, Vcc/2 biased 1 VP-P MAX. signal should be input.	
14	Ī-INPUT	Vcc/2	_	Input for I signal. This input impedance is larger than 500 k Ω . As I signal, Vcc/2 bias DC signal should be input.	
15	GND	0	-	Track length should be kept as short as possible.	
16	I-BIAS	_	0.175	These pins are to adjust local leakage level. These pins should be grounded through	
17	ī-BIAS	_	0.175	register 1 kΩ adjustable 30 mV offset.	
18	GND	0	-	Track length should be kept as short as possible.	
19	N.C	C	_	Non connection	
20	GND	0	-	Track length should be kept as short as possible.	

* Pin voltage at Vcc = 2.7 V

NEC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	Vcc	T _A = +25 °C	6.0	V
Power Dissipation	PD	Mounted on $50 \times 50 \times 1.6$ mm double copper	530	mW
		clad epoxy glass board at T_A = +70 °C		
Operating Temperature	Topt		-20 to +70	°C
Storage Temperature	Tstg		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	Vcc	2.7	3.0	5.5	V
Operating Temperature	Topt	-20	+25	+70	°C

ELECTRICAL CHARACTERISTICS (T_A = +25 °C, UNLESS OTHERWISE SPECIFIED $V_{P/S} \ge 1.8 V$)

PARAMETER		SVMPOL	V	cc = 2.7	V	Vcc = 5.5 V				
		STNIBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Circuit current		Icc	10.0	15.0	22.0	17.0	24.5	32.0	mA	No input signal
Circuit current power-	save mode	Icc(P/S)		330	480		1050	1500	μA	$V_{P/S} \le 1.0 V$
IF output level		PIFout	-15	-11	-7.0	-12.5	-7.7	-4.5	dBm	50 Ω load, f = fLo/2 + fI/Q*1
Local leakage (carrie	r)	ISO(Lo)	26.0	35.0			30.6		dBc	$f = f_{Lo}/2^{*1}$
Local leak level at IF	out pin	Loif		-49	-37		-39.4	-28	dBm	I/Qinput : DC = Vcc/2
Image rejection (side	Image rejection (side band leak)		28.5	37.5		28.5	38.2		dBc	$f = f_{Lo}/2 - f_{I/Q}^{*1}$
I/Q input impedance		Zı/Q	500	1 000		500	700		kΩ	I/Qbias = 2.75 V
Power-save	rise time	TP/S(RISE)		1.0	5.0		1.0	5.0	μs	$V_{P/S}(OFF) \to V_{P/S}(ON)$
response time	fall time	TP/S(FALL)		1.0	3.0		1.0	3.0	μs	$V_{P/S}(ON) \to V_{P/S}(OFF)$
Power-save control voltage		VP/S(ON)	1.8		5.5	1.8		5.5	V	Normal operation
		VP/S(OFF)			1.0			1.0	V	Power-save mode
Local input level		PLoin	-17		-7	-17		-7	dBm	

STANDARD CHARACTERISTICS FOR REFERENCE (TA = +25 °C, UNLESS OTHERWISE SPECIFIED VP/s \ge 1.8 V)

DADAMETED	SYMBOL	Vcc = 2.7 V			Vcc = 5.5 V				
PARAMETER	STMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
3rd order distortion of I/Q	ΙΜ3ι/Q		-37.3			-56.5		dBc	$f = f_{Lo}/2 - 3f_{I/Q}^{*1}$
Local input VSWR	VSWRLoin		1.1			1.1		X : 1	
IF output VSWR	VSWRIFout		1.2			1.2		X : 1	

*1 : fLoin = 300.1 MHz PLoin = -10 dBm fl/Q = 36 kHz 1 VP-P DC = Vcc/2 **TEST CIRCUIT**



SYMBOL	Applied voltage (V)
Vcc = VP/s	2.7 to 5.5 V
$V_I = V_{Ib} = V_O = V_{Ob}$	0.5 imes Vcc



TYPICAL CHARACTERISTICS (Unless otherwise specified T_A = +25 °C)



NEC

TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD



IC MOUNTED SIDE

TYPICAL APPLICATION



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

SCORE

PACKAGE DIMENSIONS

* 20 PIN PLASTIC SSOP (225 mil) (UNIT: mm)



NOTE Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

NOTE ON CORRECT USE

- (1) Observe precautions for handling because of electrostatic sensitive devices.
- (2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired operation).
- $(3) \quad \text{Keep the track length of the ground pins as short as possible.}$
- (4) Connect a bypass capacitor (e.q. 1 000 pF) to the Vcc pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering method and conditions than the recommended conditions are to be consulted with our sales representatives.

μ PC8101GR

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 2, Exposure limit*: None	IR35–00-2
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 2, Exposure limit*: None	VP15-00-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below Number of flow process: 1, Exposure limit*: None	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

*: Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Note: Apply only a single process at once, except for "Partial heating method".

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).



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 a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device
 before using it in a particular application.
 - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
 - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
 - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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