UPC258, UPC4558

Low Noise Dual Operational Amplifiers

DESCRIPTION

The UPC258 and 4558 are dual operational amplifier with a built-in phase compensation circuit, feature high speed, wide band and low noise.

Therefore, applications such as active filters, audio amplifiers and VCOs can be realized with a simple circuit configuration.

Depending on the operating ambient temperature, UPC258 is suitable for communication application while UPC4558 is suitable for general-purpose usage.

In addition, special arrangement products with sorted DC items are available.

Along with this series of lineup, the quad type op-amp UPC458 and 4741 with same circuit configuration are also available

FEATURES

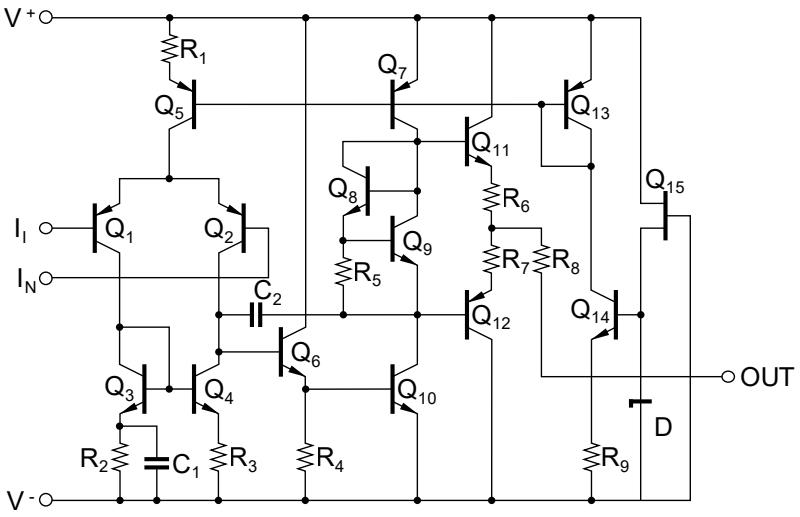
- Input Offset Voltage ±0.5 mV (TYP.)
- Input Offset Current ±5nA (TYP.)
- Input Bias Current 60nA (TYP.)
- Slew Rate 1.0 V/μs (TYP.)
- Input Equivalent Noise Voltage (RIAA) 1.0 $\mu V_{r.m.s.}$ (TYP.)
- Built-In Phase Compensation Circuit
- Built-In Output Short Circuit Protection
- Standard Dual Op-Amp terminal connection (pin compatible)

ORDERING INFORMATION

Part Number (1)	Selected Grade	Package
UPC258G2-AP	Standard	8-pin plastic SOP (5.72 mm (225))
UPC258G2(5)-AP	DC item sorted product	8-pin plastic SOP (5.72 mm (225))
UPC4558G2-AP	Standard	8-pin plastic SOP (5.72 mm (225))
UPC4558G2(5)-AP	DC item sorted product	8-pin plastic SOP (5.72 mm (225))

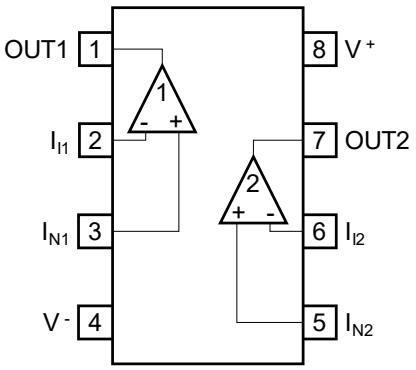
(1) Order names containing E1 or E2 indicate that the packaging format is embossed taping.
Pin 1 of E1 is on draw-out side, and pin 1 of E2 is at take-up side.

EQUIVALENT CIRCUIT (1/2 Circuit)



PIN CONFIGURATION (Top View)

UPC258G2, UPC4558G2



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	UPC258G2 UPC258G2(5)	UPC4558G2 UPC4558G2(5)	Unit
Power Supply Voltage Note 1	$V^+ - V^-$	-0.3 ~ +36		V
Differential Input Voltage	V_{ID}	±30		V
Input Voltage Note 2	V_I	V^- -0.3 ~ V^+ +0.3		V
Output Applied Voltage Note 3	V_O	V^- -0.3 ~ V^+ +0.3		V
Total Power Dissipation Note 4	P_T	440		mW
Output Short Circuit Duration Note 5		Indefinite		s
Operating Ambient Temperature	T_A	-40 ~ +85	-20 ~ +80	°C
Storage Temperature	T_{stg}	-55 ~ +125		°C

【Note】 **1.** Note that reverse connections of the power supply may damage the ICs.

2. The input terminal must be apply within the input voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp input voltage must operates within the electrical characteristics range of input common-mode voltage.

3. The output terminal must be apply within the output voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp output voltage must operates within the electrical characteristics range of maximum output voltage.

4. This is the value at $T_A \leq$ +25 °C. De-rate value at -4.4 mW/°C when T_A > 25 °C.

5. Please use the total loss and the de-rating value from Note 4.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage	$V^{\pm}$	±4		±16	V

ELECTRICAL CHARACTERISTICS

UPC258, UPC4558 (T_A = 25 °C, $V^{\pm}$ = ±15 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V_{IO}		±0.5	±6.0	mV	R_S ≤ 10 kΩ
Input Offset Current	I_{IO}		±5	±200	nA	
Input Bias Current Note 6	I_B		60	500	nA	
Large Signal Voltage Gain	A_V	20000	100000			R_L ≥ 2 kΩ, V_O = ±10 V
Power Consumption	P_d		90	170	mW	I_O = 0 A
Common Mode Rejection Ratio	CMR	70	90		dB	R_S ≤ 10 kΩ
Supply Voltage Rejection Ratio	SVR		30	150	μV/V	R_S ≤ 10 kΩ
Output Voltage Swing	V_{om}	±12	±14		V	R_L ≥ 10 kΩ
Output Voltage Swing	V_{om}	±10	±13		V	R_L ≥ 2 kΩ
Common Mode Input Voltage Range	V_{ICM}	±12	±14		V	
Slew Rate	SR		1.0		V/μs	A_V = 1
Input Equivalent Noise Voltage	V_n		6		μV_{p-p}	R_S = 1 kΩ, f = 1 Hz ~ 1 kHz (Fig 1)
Channel Separation			105		dB	f = 1 kHz (Fig 2)

UPC258(5), UPC4558(5) (T_A = 25 °C, $V^{\pm}$ = ±15 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V_{IO}		±0.5	±2.0	mV	R_S ≤ 10 kΩ
Input Offset Current	I_{IO}		±5	±50	nA	
Input Bias Current Note 6	I_B		60	100	nA	
Large Signal Voltage Gain	A_V	50000	100000			R_L ≥ 2 kΩ, V_O = ±10 V
Power Consumption	P_d		90	135	mW	I_O = 0 A
Common Mode Rejection Ratio	CMR	85	90		dB	R_S ≤ 10 kΩ
Supply Voltage Rejection Ratio	SVR		30	75	μV/V	R_S ≤ 10 kΩ
Output Voltage Swing	V_{om}	±12.5	±14		V	R_L ≥ 10 kΩ
Output Voltage Swing	V_{om}	±11	±13		V	R_L ≥ 2 kΩ
Common Mode Input Voltage Range	V_{ICM}	±13	±14		V	
Slew Rate	SR		1.0		V/μs	A_V = 1
Input Equivalent Noise Voltage	V_n		6		μV_{p-p}	R_S = 1 kΩ, f = 1 Hz ~ 1 kHz (Fig 1)
Channel Separation			105		dB	f = 1 kHz (Fig 2)

【Note】 **6.** The direction of the input bias current is the same direction that flows out from the IC because the first stage is composed of PNP transistor.

Fig 1 Noise Test Circuit

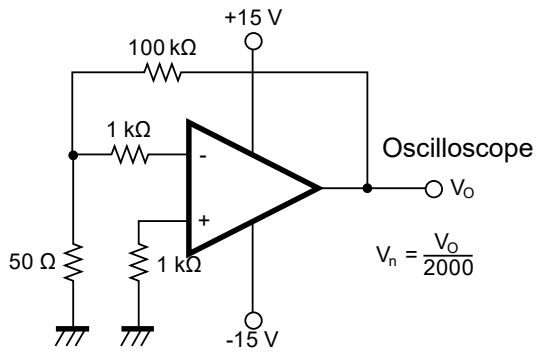
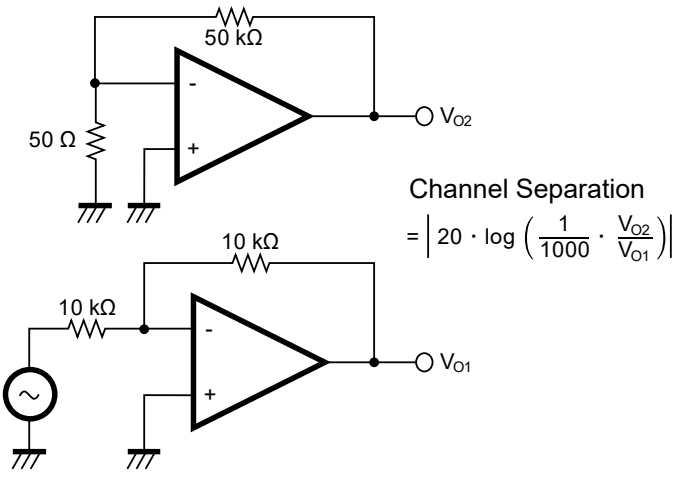
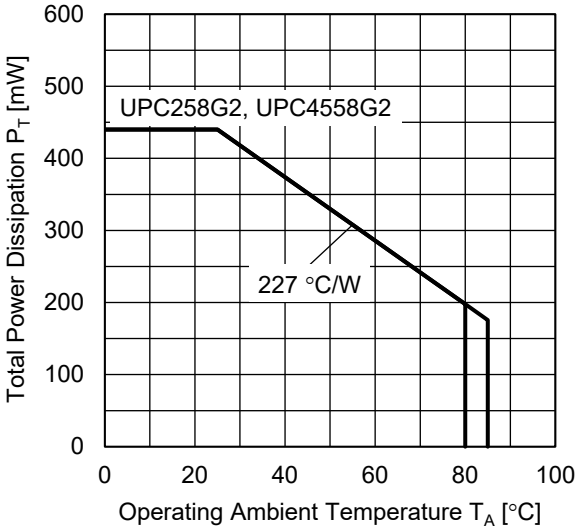


Fig 2 Channel Separation Test Circuit

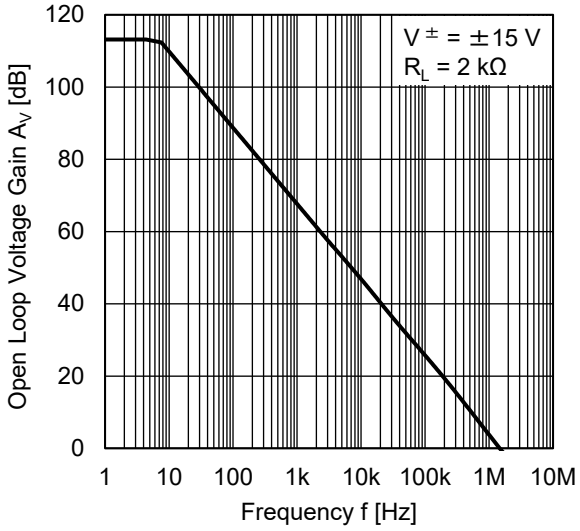


ELECTRICAL CHARACTERISTICS CURVE (T_A = 25 °C, TYP.) (REFERENCE VALUE)

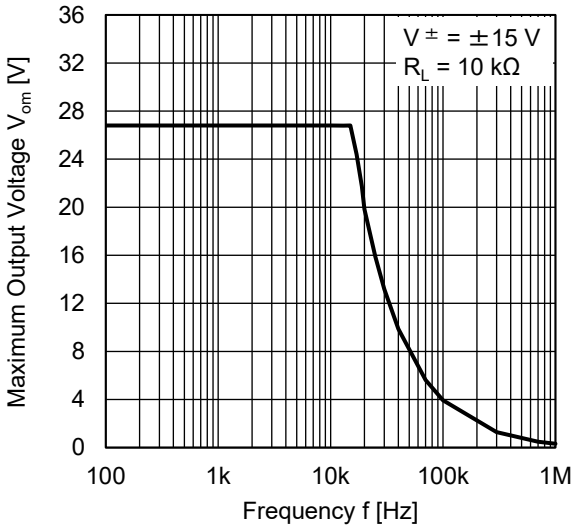
P_T vs. T_A (Absolute maximum rating)



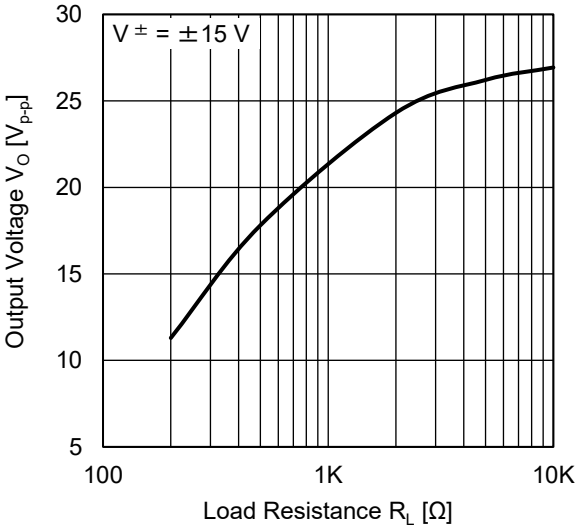
A_V vs. f



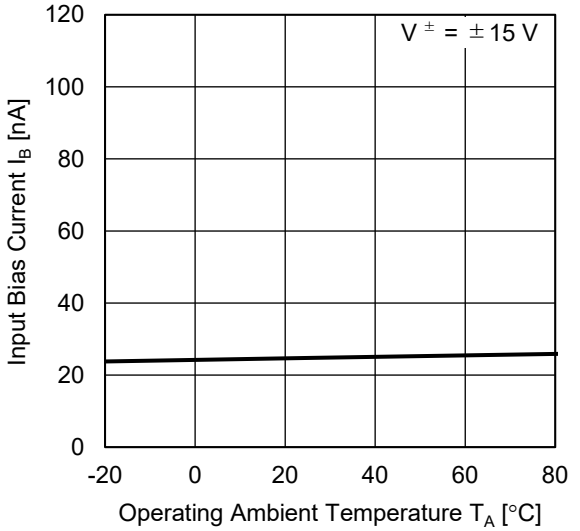
V_{om} vs. f



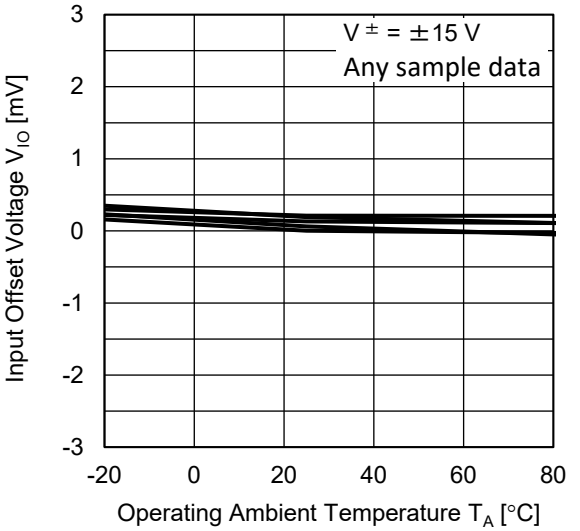
V_O vs. R_L



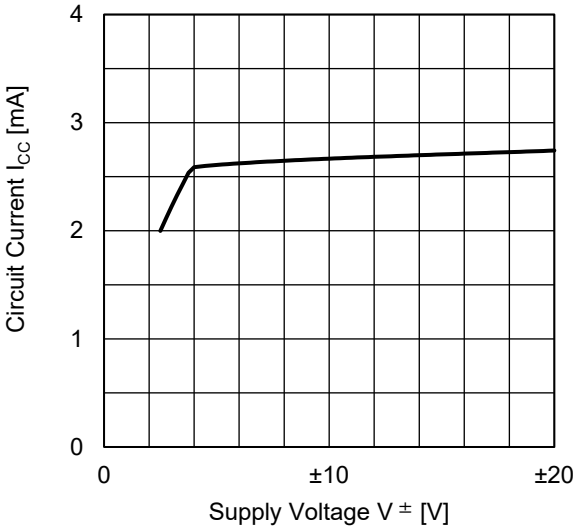
I_B vs. T_A



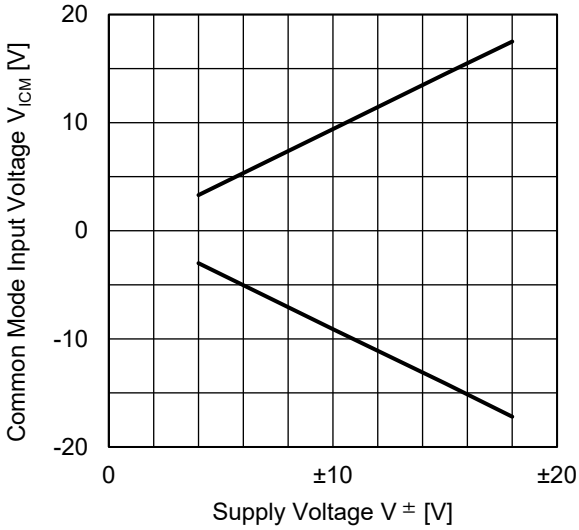
V_{IO} vs. T_A



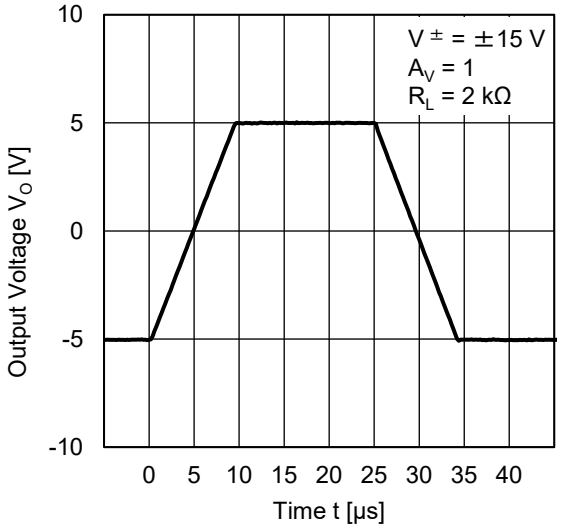
I_{CC} vs. V ±



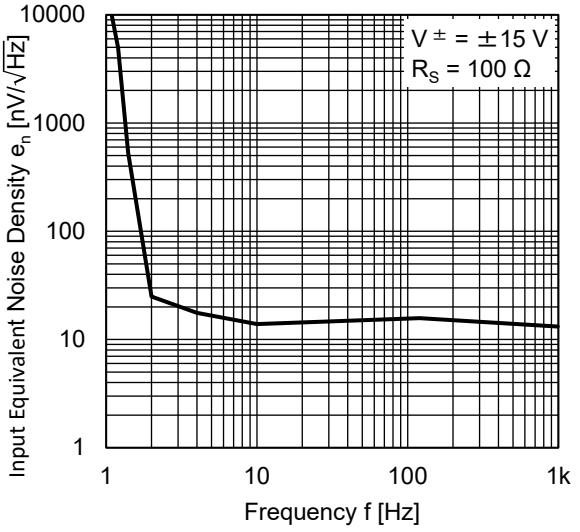
V_{ICM} vs. V ±



Output Response Characteristics

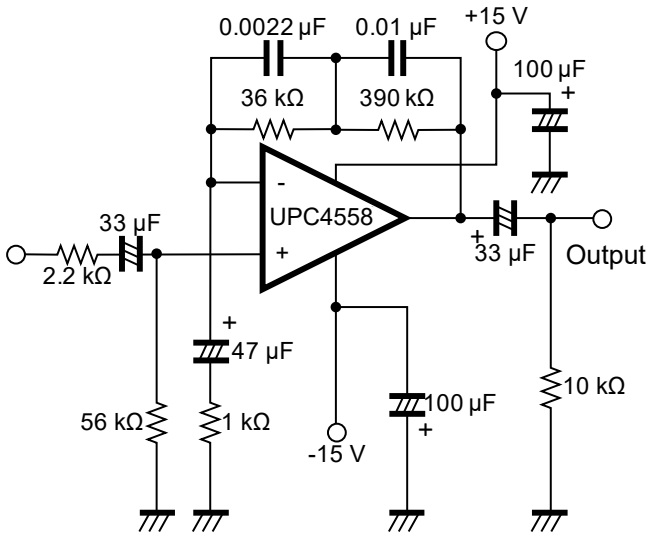


e_n vs. f



APPLICATION CIRCUIT

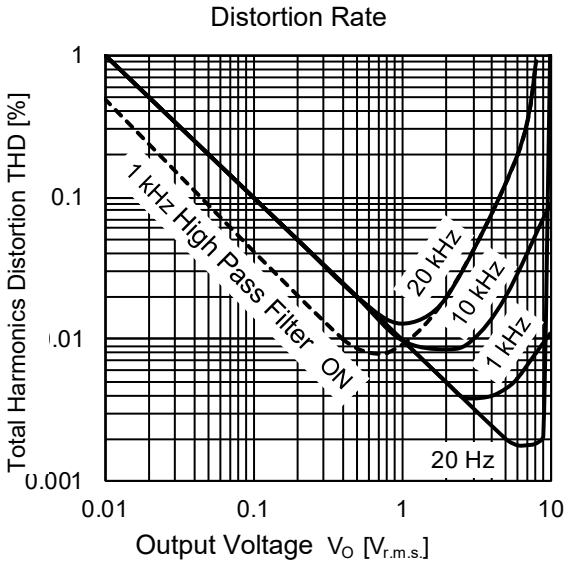
RIAA Pre-amplifier A_V = 32.5 dB



Standard Characteristics (Reference Value)

Distortion Rate 0.03 % (V_O = 1 $V_{r.m.s}$, f = 1 kHz)

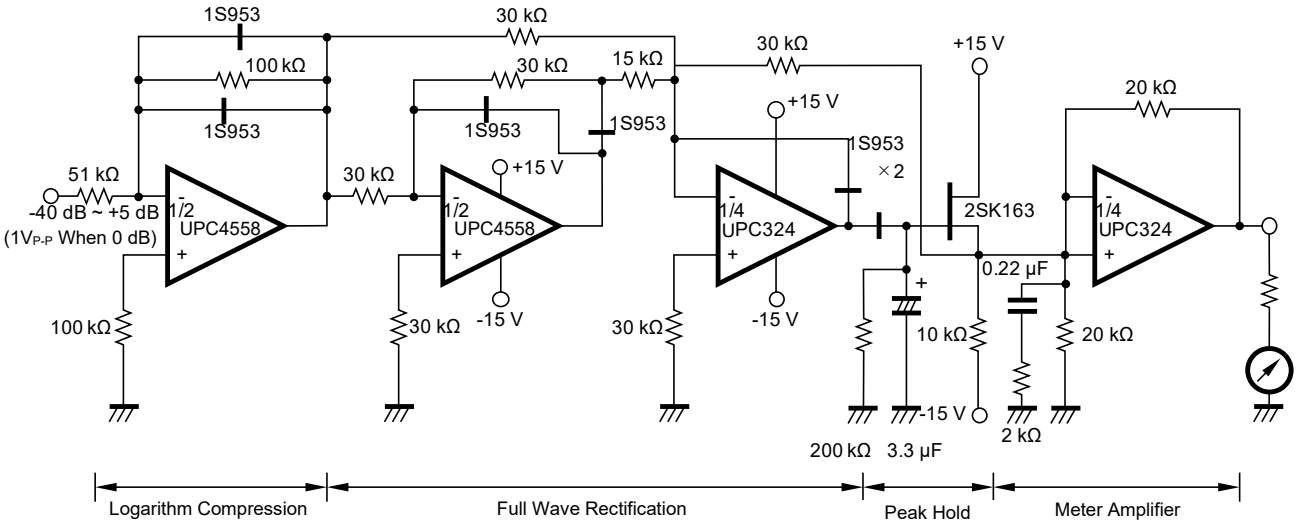
Noise 1.0 $\mu V_{r.m.s.}$ [Input referred, Input shorted, average peak voltage value]



Peak Level Meter

This circuit converts the peak voltage (about ± 10 mV ~ ± 10 V) of the input signal to a DC voltage (about 0.2V ~ 1.3 V) and drives the meter.

This output voltage is proportional to the logarithmic value of input peak voltage, thus providing a wider dynamic range indication compared to conventional linear indication methods.

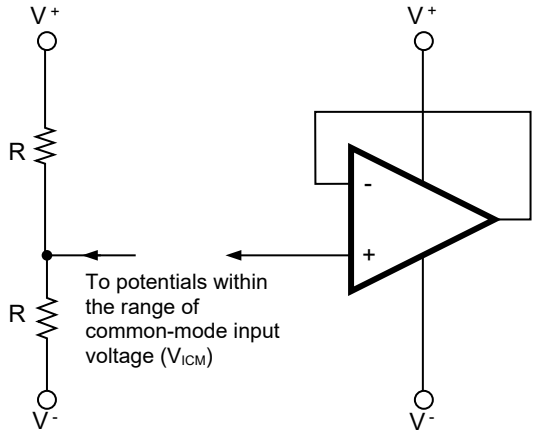


USE WITH PRECAUTIONS

- **Managing unused circuits**

  If there is an unused circuit, the following connection is recommended.

  Example of handling unused circuit



  Remark: In this example, an intermediate potential between V^+ and V^- is applied.

- **Power Supply (Dual Power Supply / Single Power Supply)**

  The op amp operates when a predetermine voltage is applied between V^+ - V^- . Therefore, while it operates from a single power supply (V^- = GND), it is not possible to operate the input and output near GND. So please be careful of the common-mode input voltage range and maximum output voltage

- **Ratings of input/output pin voltage**

  When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the input pin is lower than V^-, or the output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

- **Range of common-mode input voltage**

  When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

  V_{ICM} (TYP.): V^- +1 ~ V^+ -1 [V] (T_A = 25 °C).

  During designing, do include some margin by considering characteristics variation temperature characteristics etc.

- **Maximum output voltage**

  The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

  V_{om}^+ (TYP.) : V^+ -1 [V] (T_A = 25 °C), V_{om}^- (TYP.) : V^- +1 [V] (T_A = 25 °C)

  During designing, do include some tolerance by considering characteristics variation, temperature characteristics and so on. In addition, also note that the output voltage range ($V_{om}^+ - V_{om}^-$) will become narrow when the output current increases.

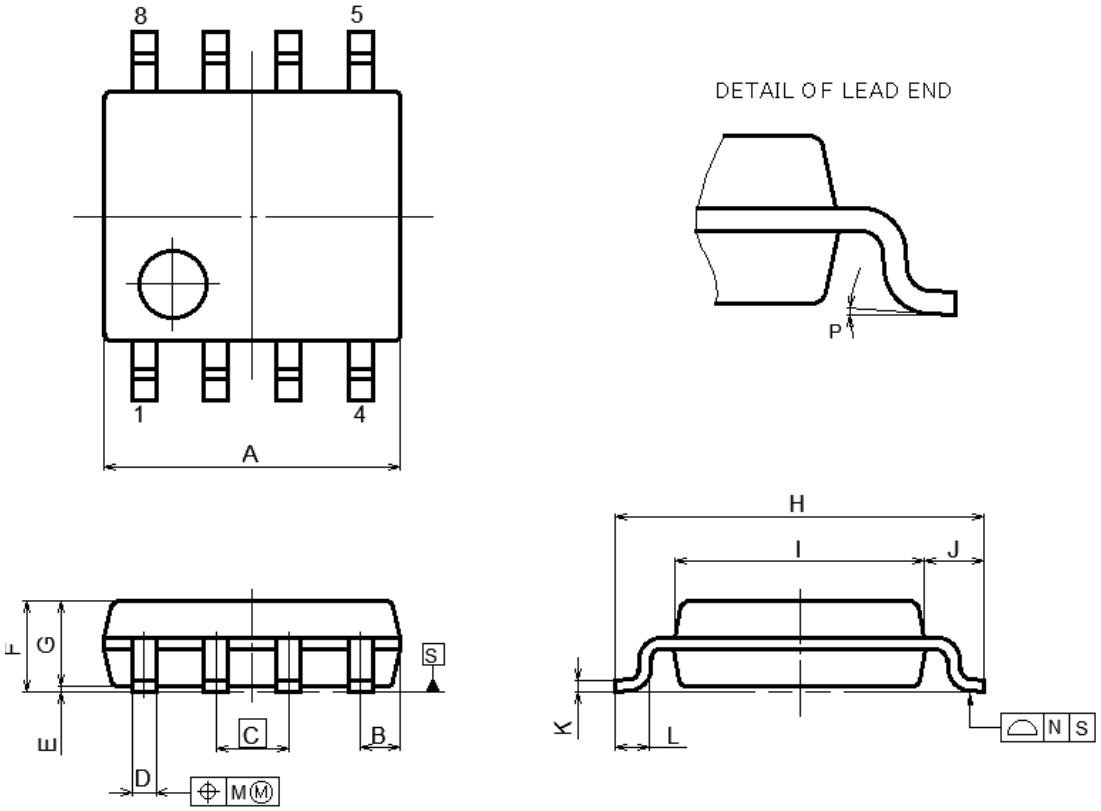
- **Handling of ICs**

  When stress is added to the ICs due to warpage or bending of a board, the characteristic may fluctuates due to piezoelectric (piezo) effect. Therefore, pay attention to warpage or bending of a board.

PACKAGE DRAWINGS

8-PIN PLASTIC SOP

JEITA Package code	RENESAS code	MASS (TYP.) [g]
P-LSOP8-4.4×5.2-1.27	PLSP0008DE-A	0.09[g]



NOTE
EACH LEAD CENTERLINE IS LOCATED WITHIN 0.12 MM OF
ITS TRUE POSITION(T.P.) AT MAXIMUM MATERIAL CONDITION.

(UNIT:mm)

ITEM	DIMENSIONS
A	5.2±0.17
B	0.78MAX
C	1.27(T.P)
D	0.40±0.05
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.1
J	1.05±0.15
K	0.2±0.07
L	0.6±0.20
M	0.1MAX
N	0.1MAX
P	4°±4°

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