

General Description

Renesas SLG7RN46452 is a low power and small form device. The SoC is housed in a 1mm x 1.2mm STQFN package which is optimal for using with small devices.

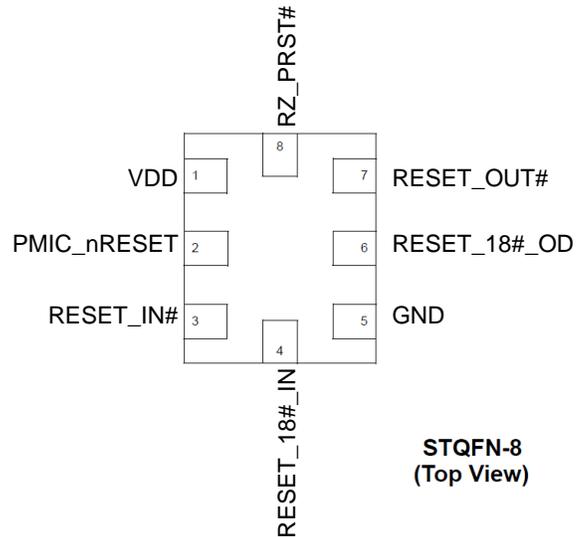
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 8 Package

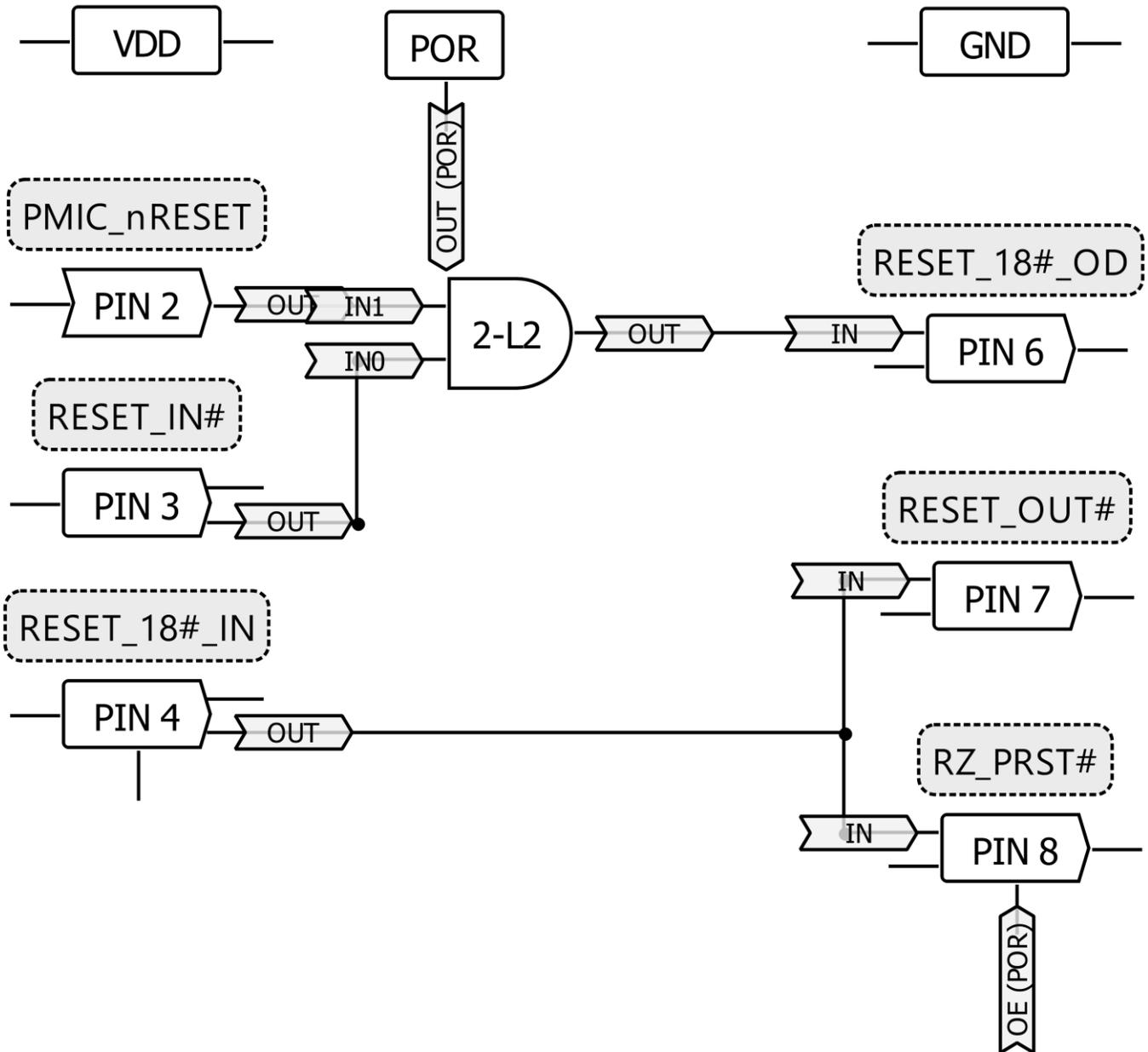
Output Summary

- 1 Output - Open Drain NMOS 2X
- 2 Outputs - Push Pull 1X

Pin Configuration



Block Diagram



Pin Configuration

| Pin # | Pin Name | Type | Pin Description | Internal Resistor |
|-------|--------------|----------------|---------------------------------------|-------------------|
| 1 | VDD | PWR | Supply Voltage | -- |
| 2 | PMIC_nRESET | Digital Input | Low Voltage Digital Input | floating |
| 3 | RESET_IN# | Digital Input | Digital Input with Schmitt trigger | floating |
| 4 | RESET_18#_IN | Digital Input | Digital Input without Schmitt trigger | 1MΩ pulldown |
| 5 | GND | GND | Ground | -- |
| 6 | RESET_18#_OD | Digital Output | Open Drain NMOS 2X | floating |
| 7 | RESET_OUT# | Digital Output | Push Pull 1X | floating |
| 8 | RZ_PRST# | Digital Output | Push Pull 1X | floating |

Ordering Information

| Part Number | Package Type |
|--------------|--|
| SLG7RN46452V | 8-pin STQFN |
| SLG7RN46452V | 8-pin STQFN - Tape and Reel (3k units) |

Absolute Maximum Conditions

| Parameter | | Min. | Max. | Unit |
|--|--------------|------------|------------|------|
| Supply Voltage on VDD relative to GND | | -0.5 | 7 | V |
| DC Input Voltage | | GND - 0.5V | VDD + 0.5V | V |
| Maximum Average or DC Current (Through pin) | Push-Pull 1x | -- | 8 | mA |
| | OD 2x | -- | 12 | |
| Current at Input Pin | | -1.0 | 1.0 | mA |
| Input leakage (Absolute Value) | | -- | 1000 | nA |
| Storage Temperature Range | | -65 | 150 | °C |
| Junction Temperature | | -- | 150 | °C |
| ESD Protection (Human Body Model) | | 2000 | -- | V |
| ESD Protection (Charged Device Model) | | 1300 | -- | V |
| Moisture Sensitivity Level | | 1 | | |

Electrical Characteristics

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|------------------|---|--|-------|------|-------|------|
| V _{DD} | Supply Voltage | | 1.71 | 3.3 | 5.5 | V |
| T _A | Operating Temperature | | -40 | 25 | 85 | °C |
| C _{VDD} | Capacitor Value at VDD | | -- | 0.1 | -- | μF |
| C _{IN} | Input Capacitance | | -- | 4 | -- | pF |
| I _Q | Quiescent Current | Static inputs and floating outputs | -- | 1 | -- | μA |
| V _O | Maximal Voltage Applied to any PIN in High-Impedance State | | -- | -- | VDD | V |
| I _{VDD} | Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2) | T _J = 85°C | -- | -- | 45 | mA |
| | | T _J = 110°C | -- | -- | 22 | mA |
| I _{GND} | Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2) | T _J = 85°C | -- | -- | 84 | mA |
| | | T _J = 110°C | -- | -- | 40 | mA |
| V _{IH} | HIGH-Level Input Voltage | Logic Input at VDD=1.8V | 1.071 | -- | VDD | V |
| | | Logic Input at VDD=3.3V | 1.84 | -- | VDD | V |
| | | Logic Input at VDD=5.0V | 2.744 | -- | VDD | V |
| | | Logic Input with Schmitt Trigger at VDD=1.8V | 1.276 | -- | VDD | V |
| | | Logic Input with Schmitt Trigger at VDD=3.3V | 2.17 | -- | VDD | V |
| | | Logic Input with Schmitt Trigger at VDD=5.0V | 3.19 | -- | VDD | V |
| | | Low-Level Logic Input at VDD=1.8V | 0.936 | -- | VDD | V |
| | | Low-Level Logic Input at VDD=3.3V | 1.086 | -- | VDD | V |
| | | Low-Level Logic Input at VDD=5.0V | 1.185 | -- | VDD | V |
| V _{IL} | LOW-Level Input Voltage | Logic Input at VDD=1.8V | 0 | -- | 0.73 | V |
| | | Logic Input at VDD=3.3V | 0 | -- | 1.255 | V |
| | | Logic Input at VDD=5.0V | 0 | -- | 1.877 | V |

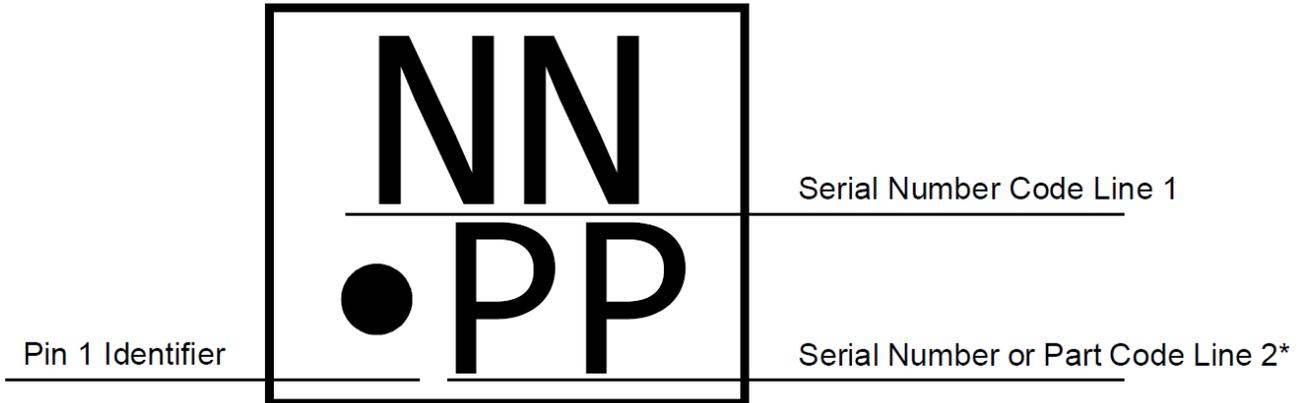
| | | | | | | |
|-----------------|--|--|--------|--------|-------|----|
| | | Logic Input with Schmitt Trigger at VDD=1.8V | 0 | -- | 0.475 | V |
| | | Logic Input with Schmitt Trigger at VDD=3.3V | 0 | -- | 0.934 | V |
| | | Logic Input with Schmitt Trigger at VDD=5.0V | 0 | -- | 1.488 | V |
| | | Low-Level Logic Input at VDD=1.8V | 0 | -- | 0.517 | V |
| | | Low-Level Logic Input at VDD=3.3V | 0 | -- | 0.669 | V |
| | | Low-Level Logic Input at VDD=5.0V | 0 | -- | 0.765 | V |
| V _{OH} | HIGH-Level Output Voltage | Push-Pull 1X, Open Drain PMOS 1X, I _{OH} =100μA, at VDD=1.8V | 1.692 | 1.788 | -- | V |
| | | Push-Pull 1X, Open Drain PMOS 1X, I _{OH} =3mA, at VDD=3.3V | 2.721 | 3.108 | -- | V |
| | | Push-Pull 1X, Open Drain PMOS 1X, I _{OH} =5mA, at VDD=5.0V | 4.171 | 4.761 | -- | V |
| V _{OL} | LOW-Level Output Voltage | Push-Pull 1X, I _{OL} =100μA, at VDD=1.8V | -- | 0.01 | 0.016 | V |
| | | Push-Pull 1X, I _{OL} =3mA, at VDD=3.3V | -- | 0.175 | 0.257 | V |
| | | Push-Pull 1X, I _{OL} =5mA, at VDD=5.0V | -- | 0.225 | 0.325 | V |
| | | Open Drain NMOS 2X, I _{OL} =100μA, at VDD=1.8V | -- | 0.003 | 0.003 | V |
| | | Open Drain NMOS 2X, I _{OL} =3mA, at VDD=3.3V | -- | 0.043 | 0.061 | V |
| | | Open Drain NMOS 2X, I _{OL} =5mA, at VDD=5.0V | -- | 0.057 | 0.08 | V |
| I _{OH} | HIGH-Level Output Current (see Note 1) | Push-Pull 1X, Open Drain PMOS 1X, V _{OH} =VDD-0.2V, at VDD=1.8V | 1.045 | 1.506 | -- | mA |
| | | Push-Pull 1X, Open Drain PMOS 1X, V _{OH} =2.4V, at VDD=3.3V | 5.774 | 11.066 | -- | mA |
| | | Push-Pull 1X, Open Drain PMOS 1X, V _{OH} =2.4V, at VDD=5.0V | 20.656 | 30.203 | -- | mA |
| I _{OL} | LOW-Level Output Current (see Note 1) | Push-Pull 1X, V _{OL} =0.15V, at VDD=1.8V | 0.984 | 1.363 | -- | mA |
| | | Push-Pull 1X, V _{OL} =0.4V, at VDD=3.3V | 4.491 | 6.438 | -- | mA |
| | | Push-Pull 1X, V _{OL} =0.4V, at VDD=5.0V | 6.087 | 8.611 | -- | mA |
| | | Open Drain NMOS 2X, V _{OL} =0.15V, at VDD=1.8V | 4.02 | 5.471 | -- | mA |
| | | Open Drain NMOS 2X, V _{OL} =0.4V, at VDD=3.3V | 17.995 | 25.459 | -- | mA |

| | | | | | | |
|------------------|-------------------------------|---|--------|--------|-------|-----------|
| | | Open Drain NMOS 2X, $V_{OL}=0.4V$, at $V_{DD}=5.0V$ | 24.032 | 33.581 | -- | mA |
| R_{PULL_DOWN} | Internal Pull Down Resistance | Pull down on PIN 4 | -- | 1 | -- | $M\Omega$ |
| T_{SU} | Startup Time | From V_{DD} rising past PON_{THR} | -- | 0.54 | -- | ms |
| PON_{THR} | Power On Threshold | V_{DD} Level Required to Start Up the Chip | 1.303 | 1.506 | 1.707 | V |
| $POFF_{THR}$ | Power Off Threshold | V_{DD} Level Required to Switch Off the Chip | 0.675 | 0.901 | 1.174 | V |

Note:

1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. Pins 2, 3 and 4 are connected to one side, pins 6, 7 and 8 to another.
3. Guaranteed by Design.

Package Top Marking



* PP may consist of the special characters +, -, and = for a total of 9 different combinations, or may consist of two character alphanumeric Part Code (A-Z and 0-9), depending on time of marking.

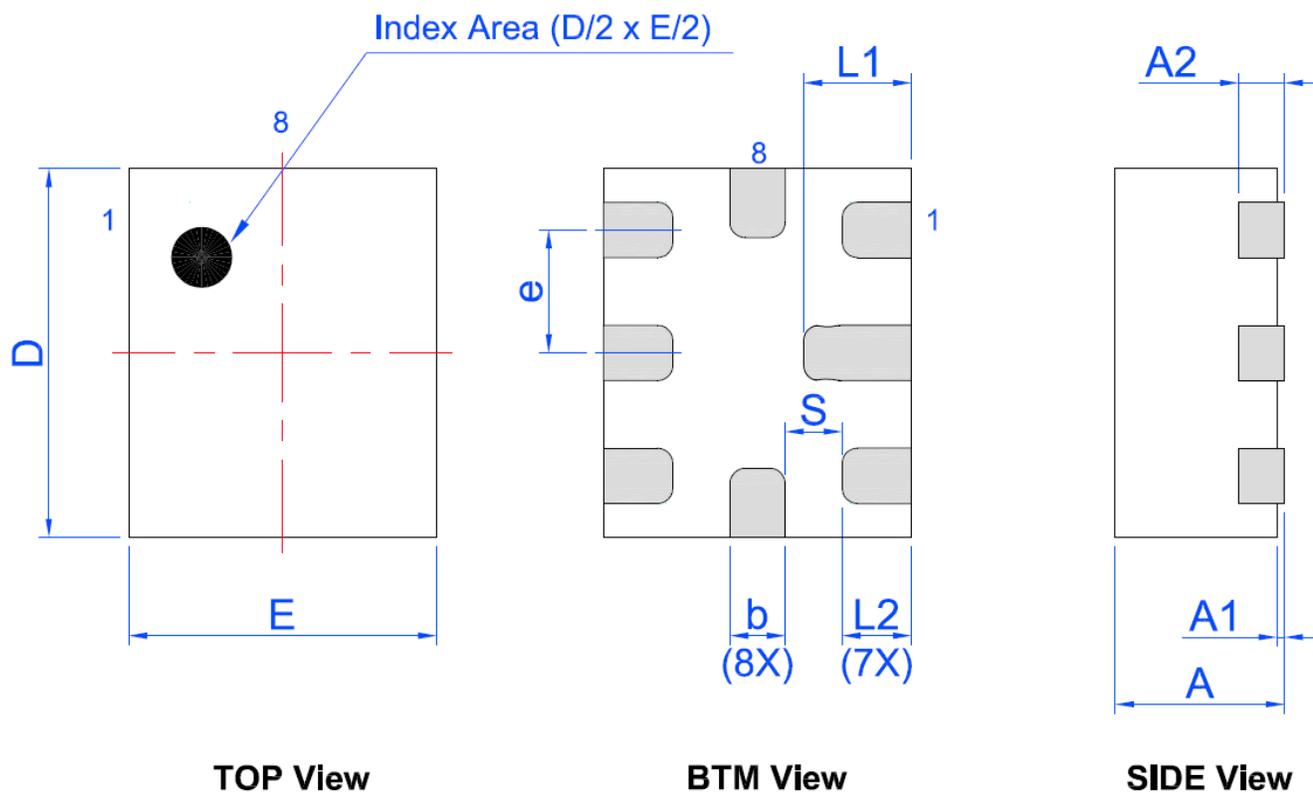
Note: The SN Code (Line 1 and Line 2) is generated during production, and encodes information including part number, programming code number, date code and lot code. This same information is provided in plain text form on a label placed on the reel. If you need assistance in decoding the SN Code, please contact Dialog Semiconductor.

| Datasheet Revision | Programming Code Number | Lock Status | Checksum | Part Code | Revision | Date |
|--------------------|-------------------------|-------------|------------|-----------|----------|------------|
| 0.10 | 001 | U | 0xA1436134 | | | 04/04/2023 |

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

8 Lead STQFN Package 1.0 x 1.2 mm



Unit: mm

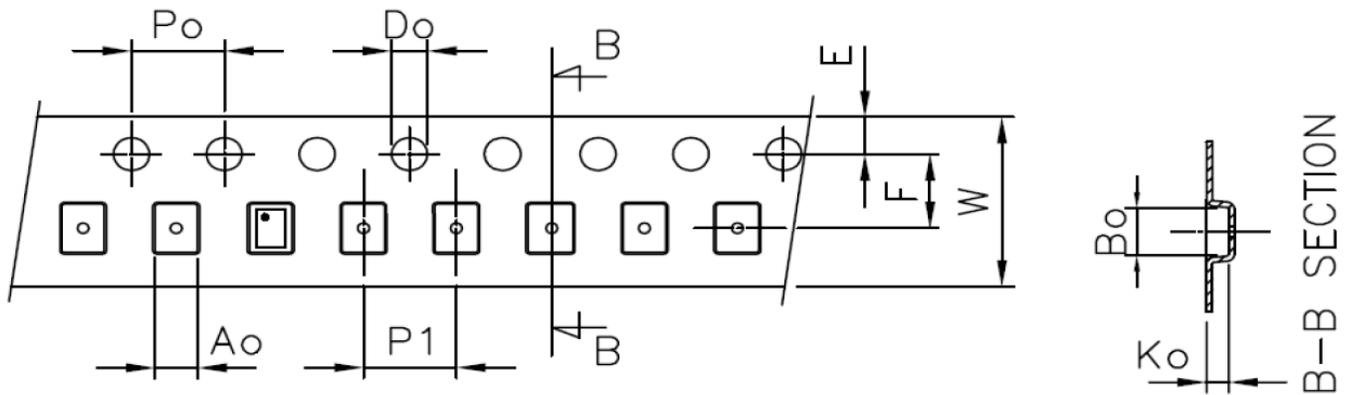
| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|--------|----------|------|-------|--------|-----------|-------|-------|
| A | 0.50 | 0.55 | 0.60 | D | 1.15 | 1.20 | 1.25 |
| A1 | 0.005 | - | 0.050 | E | 0.95 | 1.00 | 1.05 |
| A2 | 0.10 | 0.15 | 0.20 | L1 | 0.30 | 0.35 | 0.40 |
| b | 0.13 | 0.18 | 0.23 | L2 | 0.175 | 0.225 | 0.275 |
| e | 0.40 BSC | | | S | 0.185 REF | | |

Tape and Reel Specification

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|------------------------|-----------|---------------------------|-----------|---------|----------------------|--------------|-------------|---------------|-------------|-----------------|-----------------|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| STQFN 8L 0.4P FC Green | 8 | 1.0x1.2x0.55 | 3000 | 3000 | 178/60 | 100 | 400 | 100 | 400 | 8 | 4 |

Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|------------------------|-------------------|------------------|--------------|------------------|--------------|---------------------|-------------------------|-----------------------------|------------|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | |
| STQFN 8L 0.4P FC Green | 1.16 | 1.38 | 0.71 | 4 | 4 | 1.5 | 1.75 | 3.5 | 8 |



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.66 mm³ (nominal). More information can be found at www.jedec.org.

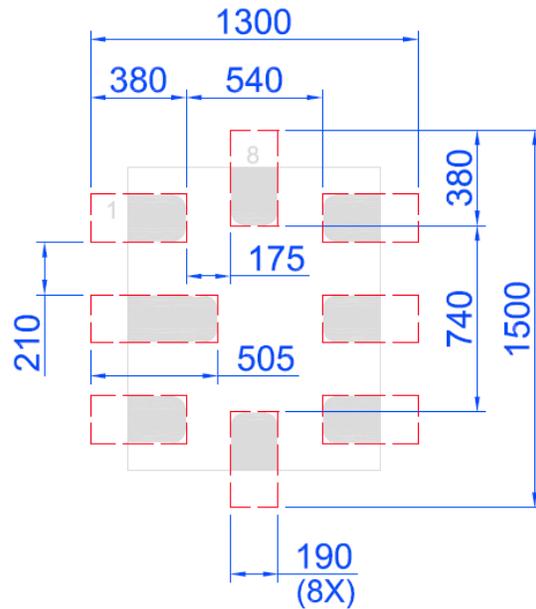
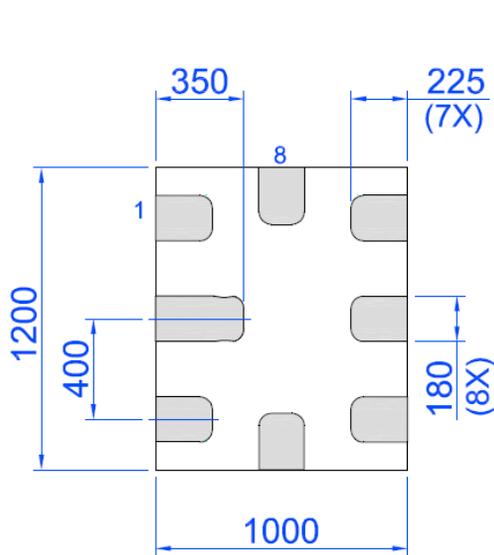
Recommended Land Pattern



**Exposed Pad
(PKG face down)**



**Recommended Landing Pattern
(PKG face down)**



Unit: um

Datasheet Revision History

| Date | Version | Change |
|------------|---------|------------------------------|
| 04/04/2023 | 0.10 | New design for SLG46108 chip |

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.