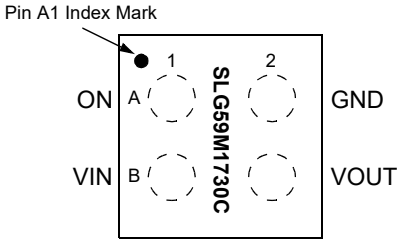
An Ultra-small 33 mΩ, 1.0 A pFET Load Switch with Controlled Inrush Current Profile

General Description

Operating from a 2.5 V to 5.5 V power supply, the SLG59M1730C is a self-powered, high-performance 33 mΩ, 1.0 A single-channel pFET load switch with a controlled V_{IN} inrush current profile. The SLG59M1730C's low supply current and controlled V_{IN} inrush current profile makes it an ideal pFET integrated load switch in small form-factor personal health monitor and watch applications.

Using a proprietary MOSFET design, the SLG59M1730C achieves a low RDS_{ON} across the entire input voltage range. Through the application of Renesas's proprietary CuFET technology, the SLG59M1730C's can be used in applications up to 1 A with a very-small 0.64 mm^2 WLCSP form factor.

Pin Configuration

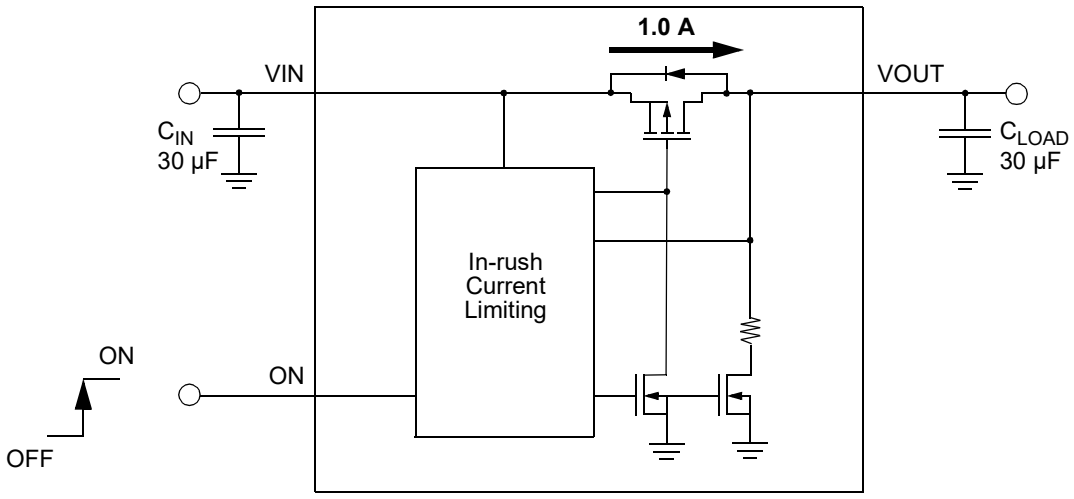


4L WLCSP
(Laser Marking View)

Features

- Integrated 1 A Continuous I_{DS} pFET Load Switch
- Low Typical RDS_{ON}:
  - 33 mΩ at V_{IN} = 5.5 V
  - 45.1 mΩ at V_{IN} = 3.3 V
  - 56.1 mΩ at V_{IN} = 2.5 V
- Input Voltage: 2.5 V to 5.5 V
- Low Typical No-load Supply Current: 0.004 µA
- Integrated VOUT Discharge Resistor
- Operating Temperature: -40 °C to 85 °C
- Low θ_{JA}, 4-pin 0.8 mm x 0.8 mm, 0.4 mm pitch 4L WLCSP Packaging
  - Pb-Free / Halogen-Free / RoHS compliant

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
A1	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59M1730C. ON is an asserted HIGH, level-sensitive CMOS input with V_{IL} < 0.3 V and V_{IH} > 0.85 V. As the ON pin input circuit does not have an internal pull-down resistor, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller – do not allow this pin to be open-circuited. In order to activate the SLG59M1730C's controlled inrush current control circuitry, ON shall be toggled HIGH only after V_{IN} is higher than the SLG59M1730C's $V_{SUCC(TH)}$ specification.
B1	VIN	MOSFET	Input terminal connection of the p-channel MOSFET. Connect a 10 µF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VIN should be rated at 10 V or higher.
B2	VOUT	MOSFET	Output terminal connection of the p-channel MOSFET. For optimal operation of the SLG59M1730C controlled inrush current profile, connect a 30 µF (or smaller) capacitor from this pin to ground. Capacitors used at VOUT should be rated at 10 V or higher.
A2	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59M1730C	WLCSP 4L	Industrial, -40 °C to 85 °C
SLG59M1730CTR	WLCSP 4L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Load Switch Input Voltage		--	--	6	V
V_{OUT} to GND	Load Switch Output Voltage to GND		-0.3	--	V_{IN}	V
ON to GND	ON Pin Voltage to GND		-0.3	--	V_{IN}	V
T_S	Storage Temperature		-65	--	140	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	1000	--	--	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Package Thermal Resistance, Junction-to-Ambient	0.8 x 0.8 mm 4L WLCSP; Determined using a 1 in^2, 2 oz .copper pad under each VIN and VOUT terminal and FR4 pcb material.	--	110	--	°C/W
W_{DIS}	Package Power Dissipation		--	--	0.5	W
MOSFET IDS_{PK}	Peak Current from VIN to VOUT	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	1.5	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Load Switch Input Voltage	-40 °C to 85 °C	2.5	--	5.5	V
I_{IN}	Load Switch Current (Pin B1) See Note 1	When OFF, V_{IN} = 5.5 V, No load	--	0.110	1.270	µA
		When OFF, V_{IN} = 5.0 V, No load	--	0.031	0.880	µA
		When OFF, V_{IN} = 3.8 V, No load	--	0.006	0.440	µA
		When OFF, V_{IN} = 3.3 V, No load	--	0.004	0.420	µA
		When OFF, V_{IN} = 2.5 V, No load	--	0.003	0.390	µA
		When ON, ON = V_{IN} = 5.5 V, No load	--	0.006	0.220	µA
		When ON, ON = V_{IN} =5.0 V, No load	--	0.004	0.190	µA
		When ON, ON = V_{IN} = 3.8V, No load	--	0.003	0.110	µA
		When ON, ON = V_{IN} = 3.3 V, No load	--	0.003	0.100	µA
		When ON, ON = V_{IN} = 2.5 V, No load	--	0.002	0.070	µA
		When ON, ON = 1.8 V, V_{IN} = 5.5 V, No load	--	0.900	1.100	µA
		When ON, ON = 1.8 V, V_{IN} = 5.0 V, No load	--	0.660	0.830	µA
		When ON, ON = 1.8 V, V_{IN} = 3.8 V, No load	--	0.210	0.330	µA
		When ON, ON = 1.8 V, V_{IN} = 3.3 V, No load	--	0.100	0.220	µA
		When ON, ON = 1.8 V, V_{IN} = 2.5 V, No load	--	0.005	0.110	µA
I_{ON_LKG}	ON Pin Input Leakage		--	--	0.1	µA

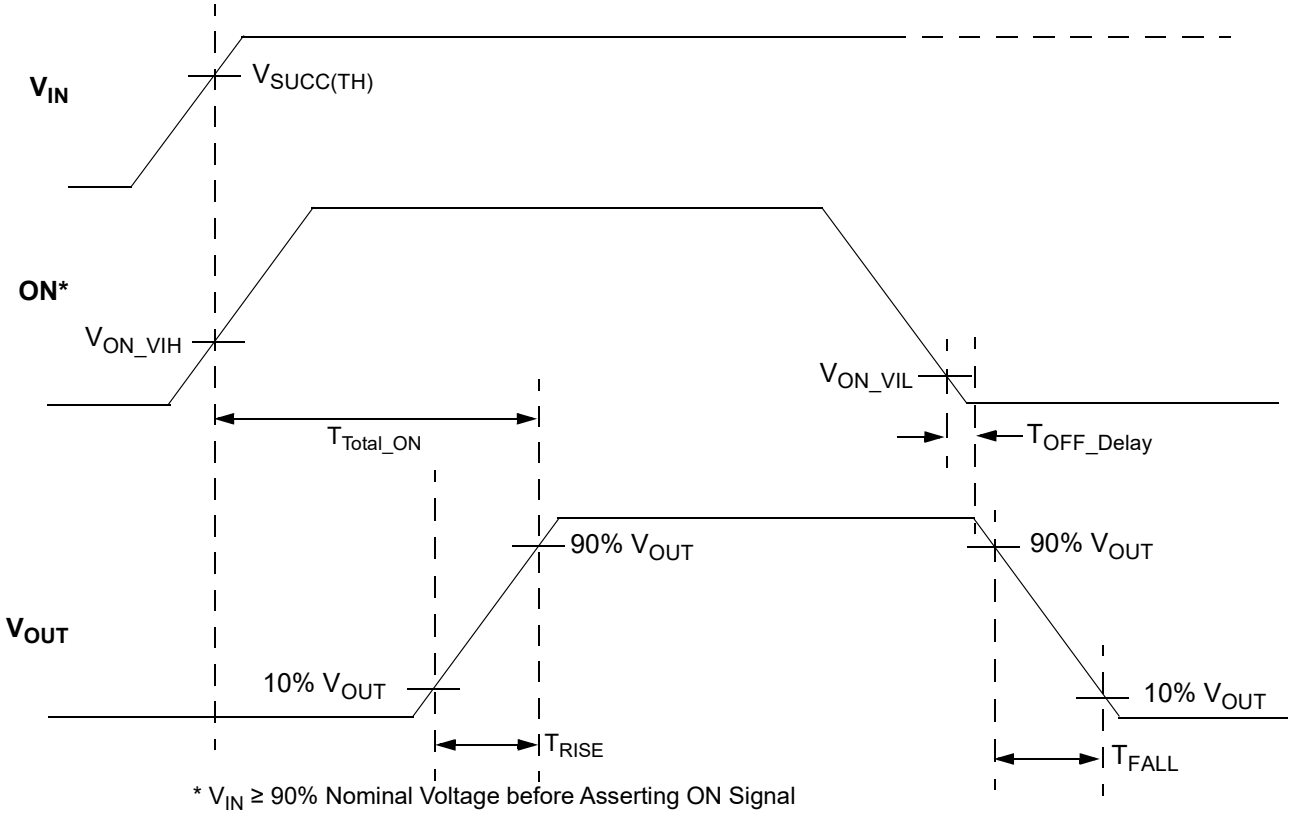
Electrical Characteristics (continued)

T_A = -40 °C to 85 °C (unless otherwise stated)

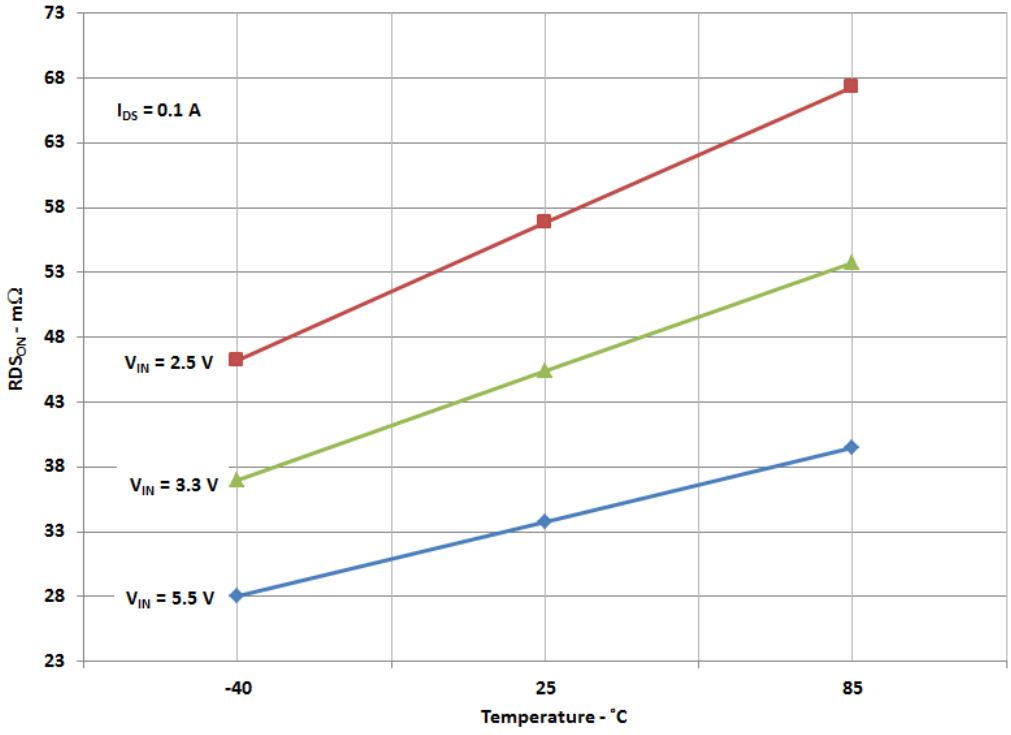
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
RDS_{ON}	ON Resistance @ T_A 25°C	@ 5.5 V, I_{DS} = 100 mA	--	33	41	mΩ
		@ 3.3 V, I_{DS} = 100 mA	--	45.1	55	mΩ
		@ 2.5 V, I_{DS} = 100 mA	--	56.1	69	mΩ
RDS_{ON}	ON Resistance @ T_A 85°C	@ 5.5 V, I_{DS} = 100 mA	--	40.2	49	mΩ
		@ 3.3 V, I_{DS} = 100 mA	--	54.5	66	mΩ
		@ 2.5 V, I_{DS} = 100 mA	--	68.2	82	mΩ
MOSFET IDS	Current from VIN to VOUT	Continuous	--	--	1.0	A
$V_{SUCC(TH)}$	V_{IN} Inrush Current Start-up Control Threshold Voltage	ON ≥ V_{ON_VIH}; See Timing Diagram on Page 5 and Note 1	--	0.9 x V_{IN}	--	V
I_{RISE}	Rise Time Charging Current	10% V_{OUT} to 90% V_{OUT} ↑; V_{IN} = 5.0 V, C_{LOAD} = 30 µF, See Note 1	11	16.5	25	mA
$V_{OUT(SR)}$	Slew Rate	10% V_{OUT} to 90% V_{OUT} ↑; V_{IN} = 5.0 V, C_{LOAD} = 30 µF	0.36	0.54	0.8	V/ms
T_{RISE}	Rise Time	10% V_{OUT} to 90% V_{OUT} ↑ V_{IN} = 5.0 V, C_{LOAD} = 30 µF, no R_{LOAD}	5	7.6	11	ms
		10% V_{OUT} to 90% V_{OUT} ↑ V_{IN} = 2.5 V, C_{LOAD} = 30 µF, no R_{LOAD}	2.5	3.8	5.5	ms
T_{Total_ON}	Total Turn On Time	V_{ON_VIH} to 90% V_{OUT} ↑ V_{IN} = 5 V, C_{LOAD} = 30 µF, No R_{LOAD}	6	8.6	12	ms
		V_{ON_VIH} to 90% V_{OUT} ↑ V_{IN} = 2.5 V, C_{LOAD} = 30 µF, No R_{LOAD}	3	4.3	6	ms
T_{OFF_Delay}	OFF Delay Time	V_{ON_VIL} to V_{OUT} Fall, V_{IN} = 5 V, R_{LOAD}=10 Ω, no C_{LOAD}	--	4.5	--	µs
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from VOUT to GND	--	--	30	µF
R_{DIS}	Discharge Resistance	V_{IN} = 2.5 V to 5.5 V, V_{OUT} = 0.4 V Input Bias	53	90	150	Ω
ON_V_{IH}	Initial Turn On Voltage		0.85	--	V_{IN}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V

Notes:
1. Rise of ON pin must only occur after V_{IN} reaches $V_{SUCC(TH)}$ in order to have proper in-rush current limiting and start-up.

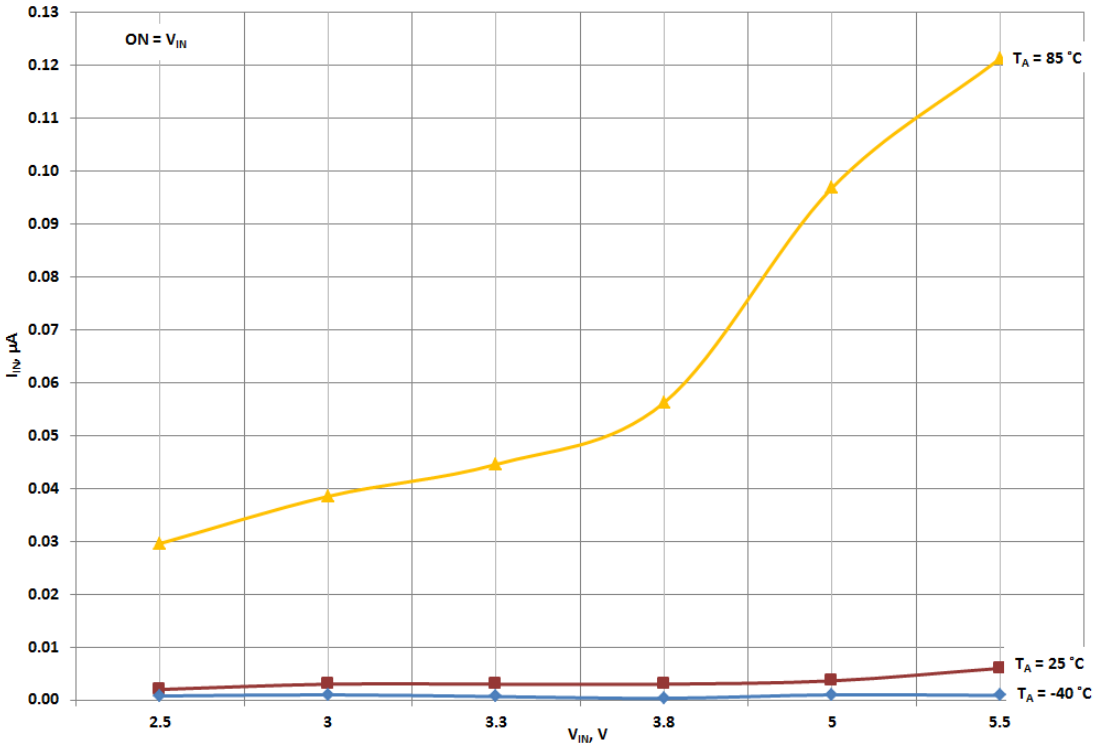
T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement



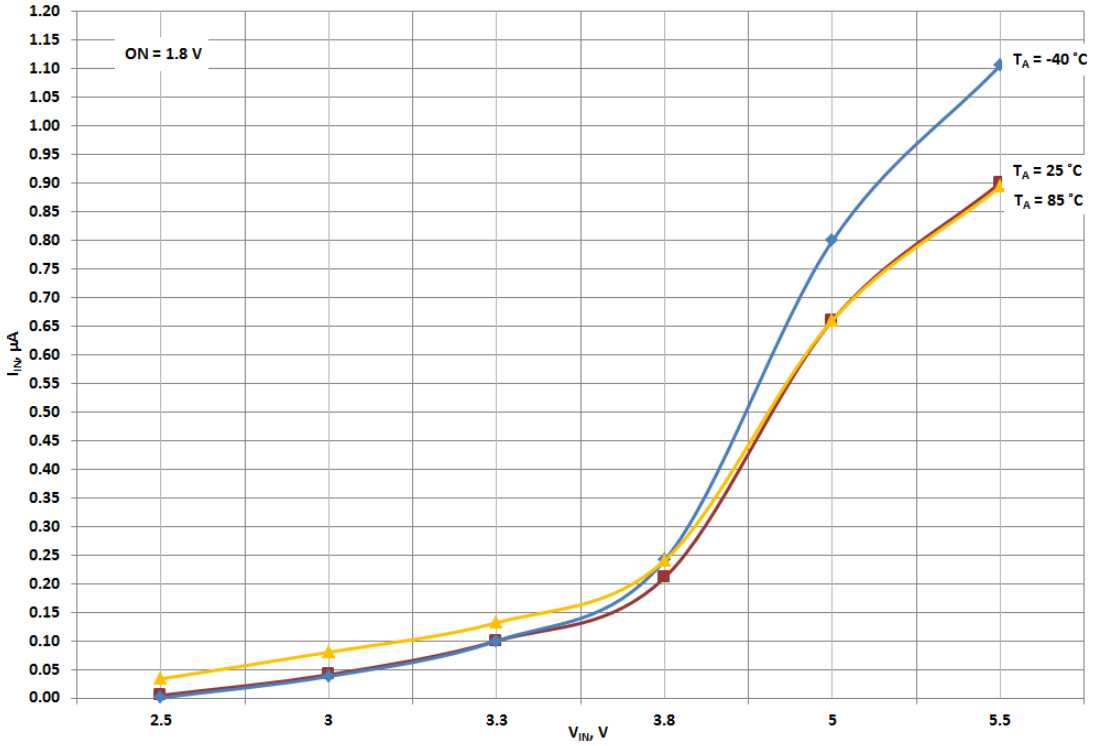
RDS_{ON} vs. Temperature and V_{IN}



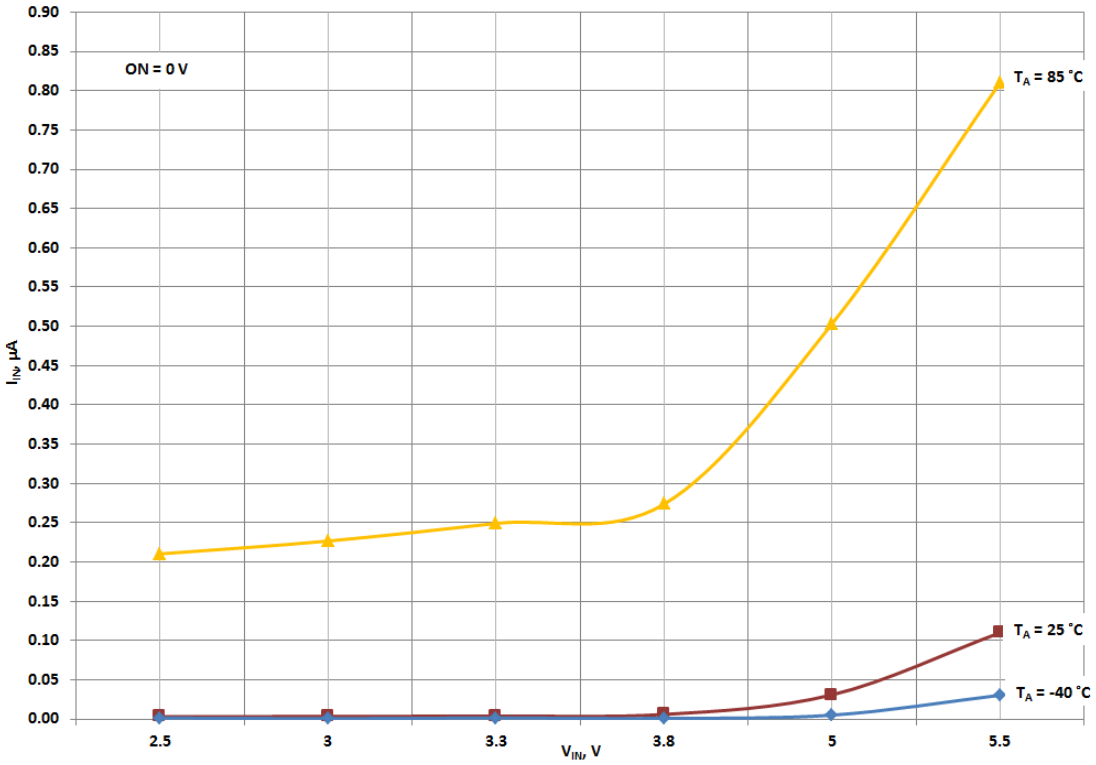
I_{IN} when ON vs. V_{IN} and Temperature



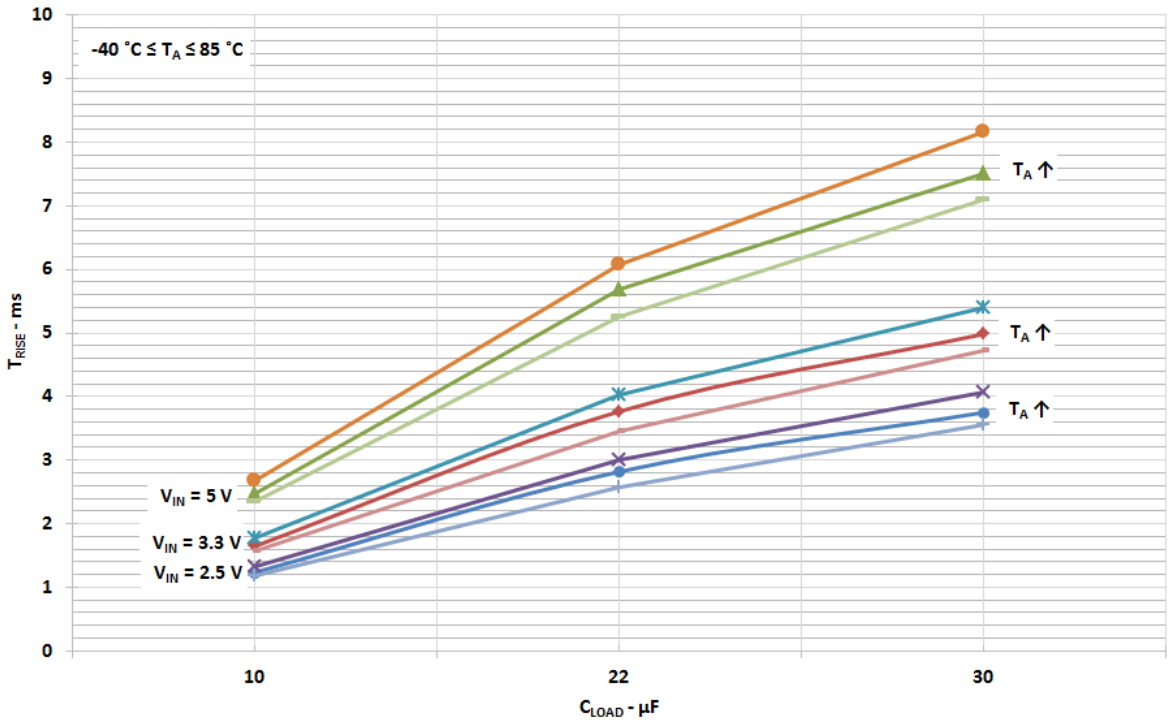
I_{IN} when ON = 1.8 V vs. V_{IN} and Temperature



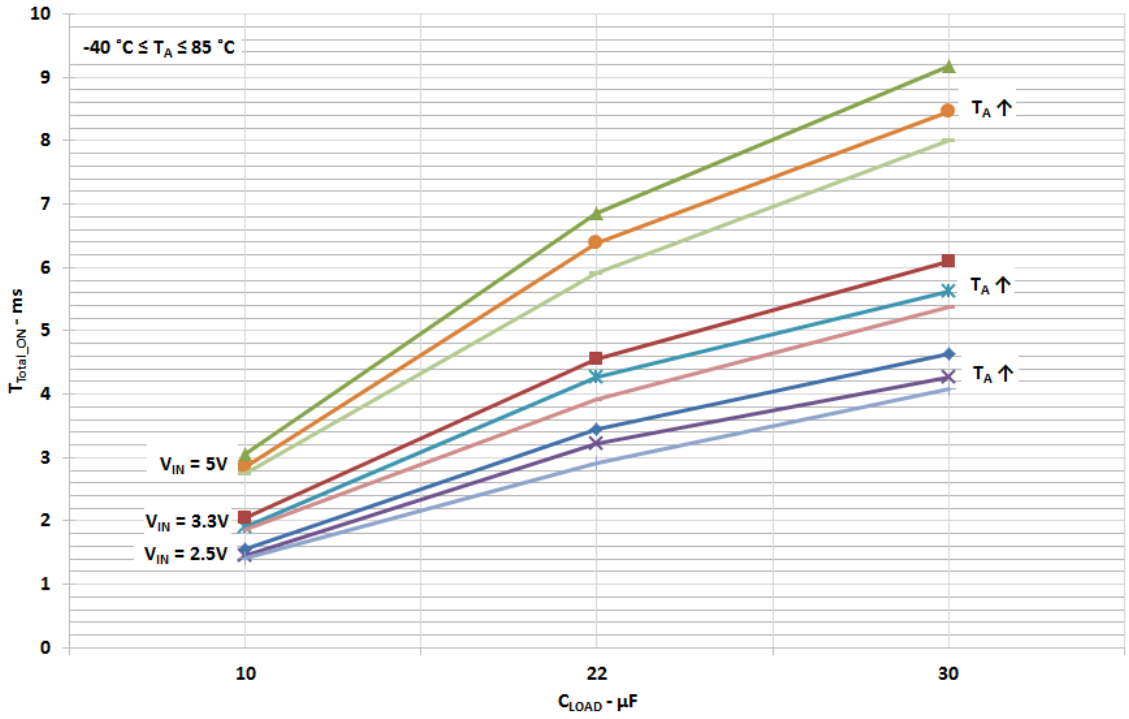
I_{IN} when OFF vs. V_{IN} and Temperature



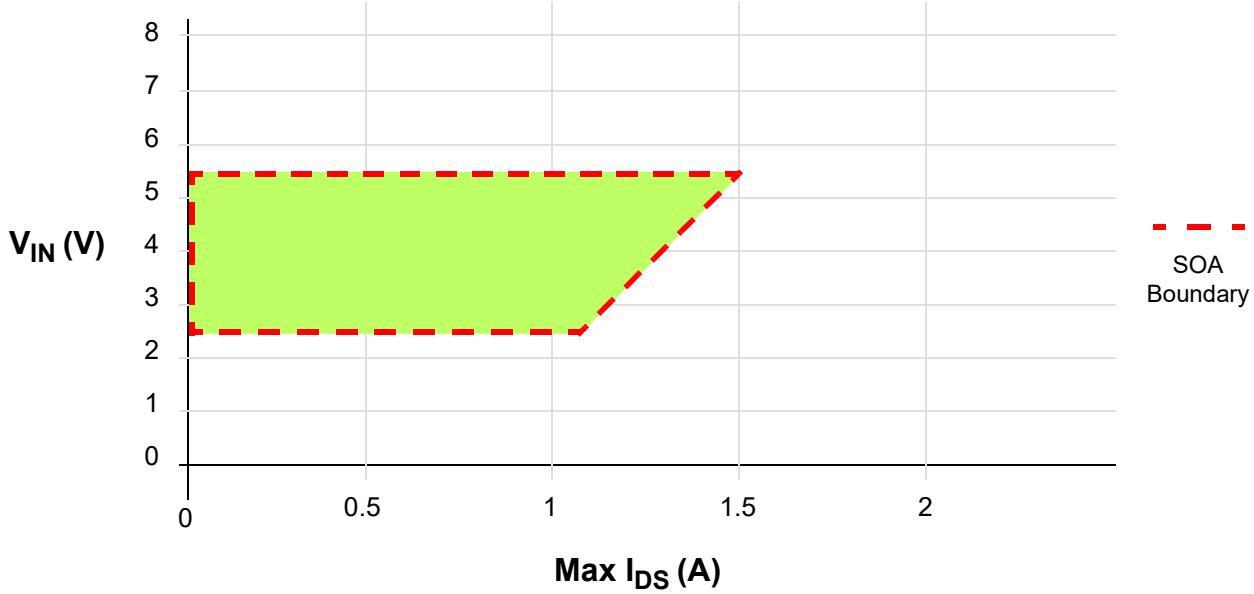
T_{RISE} vs. C_{LOAD}, Temperature, and V_{IN}



T_{Total_ON} vs. C_{LOAD}, Temperature, and V_{IN}



V_{IN} vs. Max I_{DS}, Safe Operation Area



Typical Turn-on Waveforms

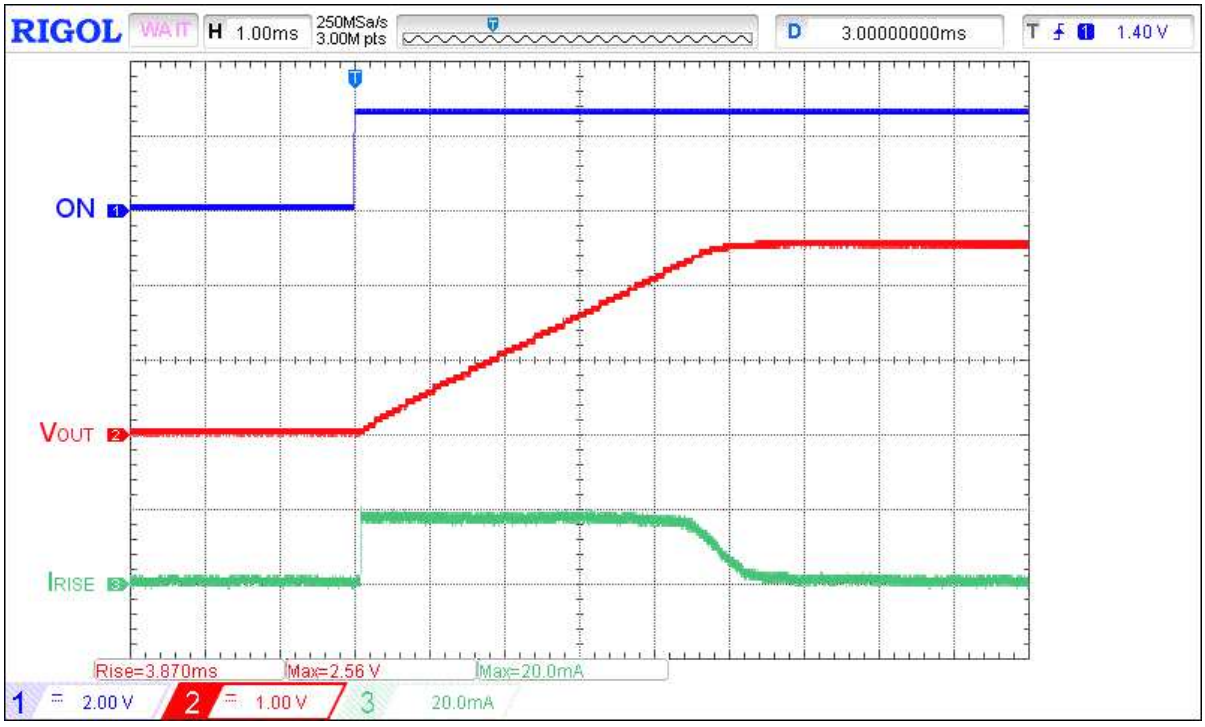


Figure 1. Typical Turn ON operation waveform for V_{IN} = 2.5 V, C_{LOAD} = 30 µF

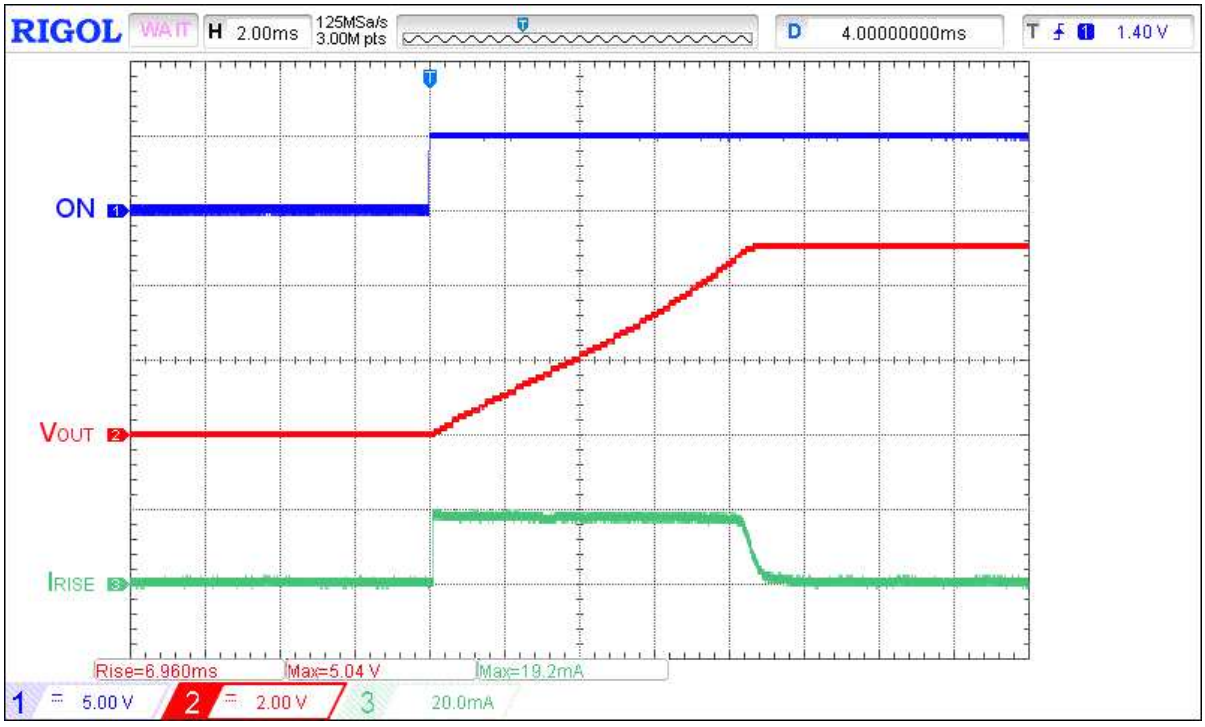


Figure 2. Typical Turn ON operation waveform for V_{IN} = 5 V, C_{LOAD} = 30 µF

Typical Turn-off Waveforms

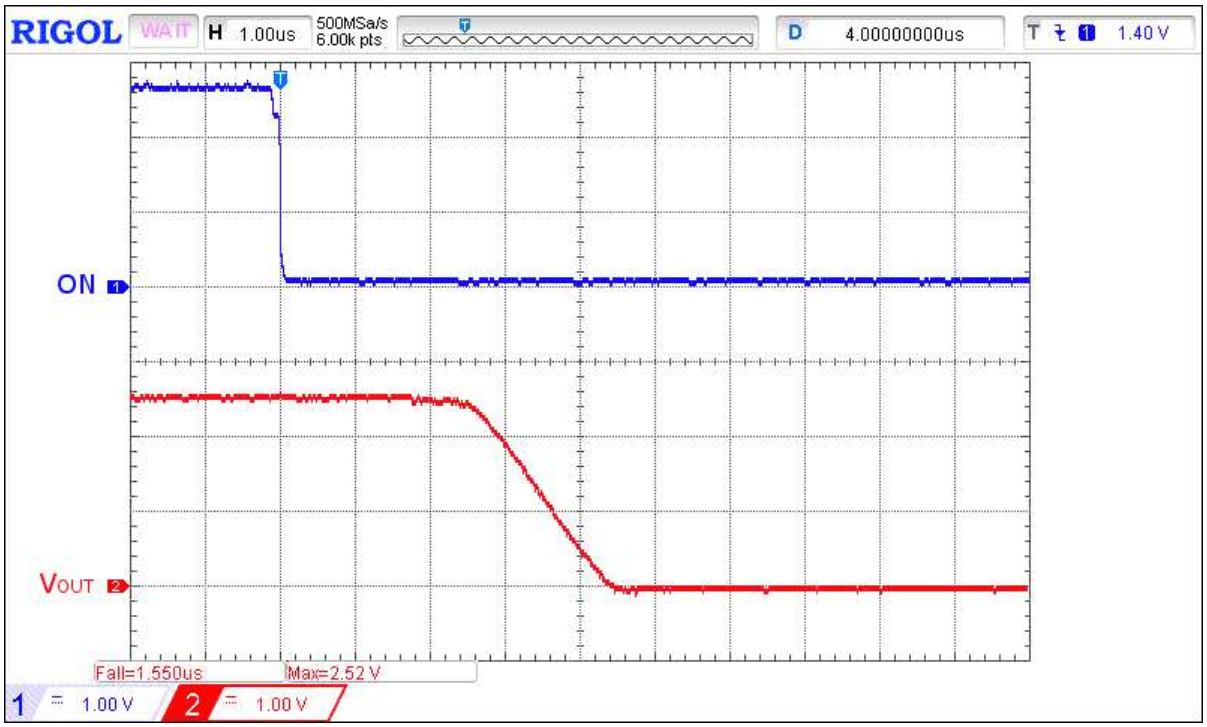


Figure 3. Typical Turn OFF operation waveform for V_{IN} = 2.5 V, no C_{LOAD} , R_{LOAD} = 10 Ω

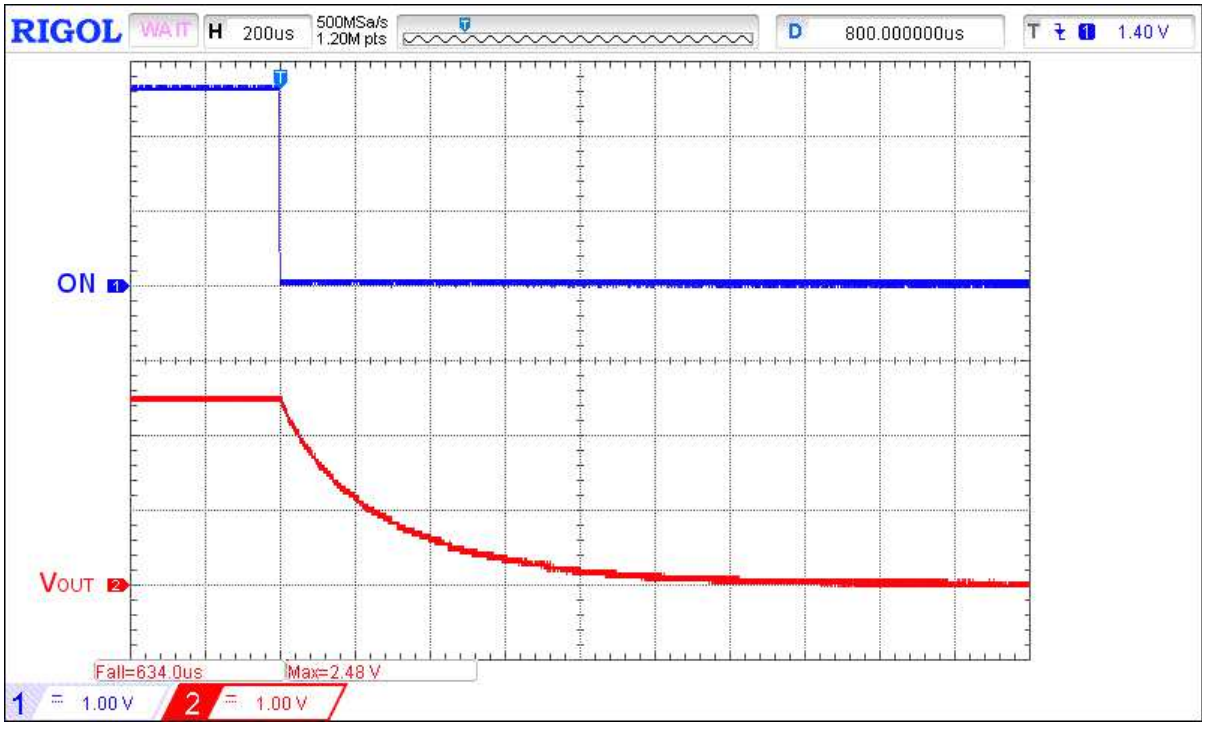


Figure 4. Typical Turn OFF operation waveform for V_{IN} = 2.5 V, C_{LOAD} = 30 µF, R_{LOAD} = 10 Ω

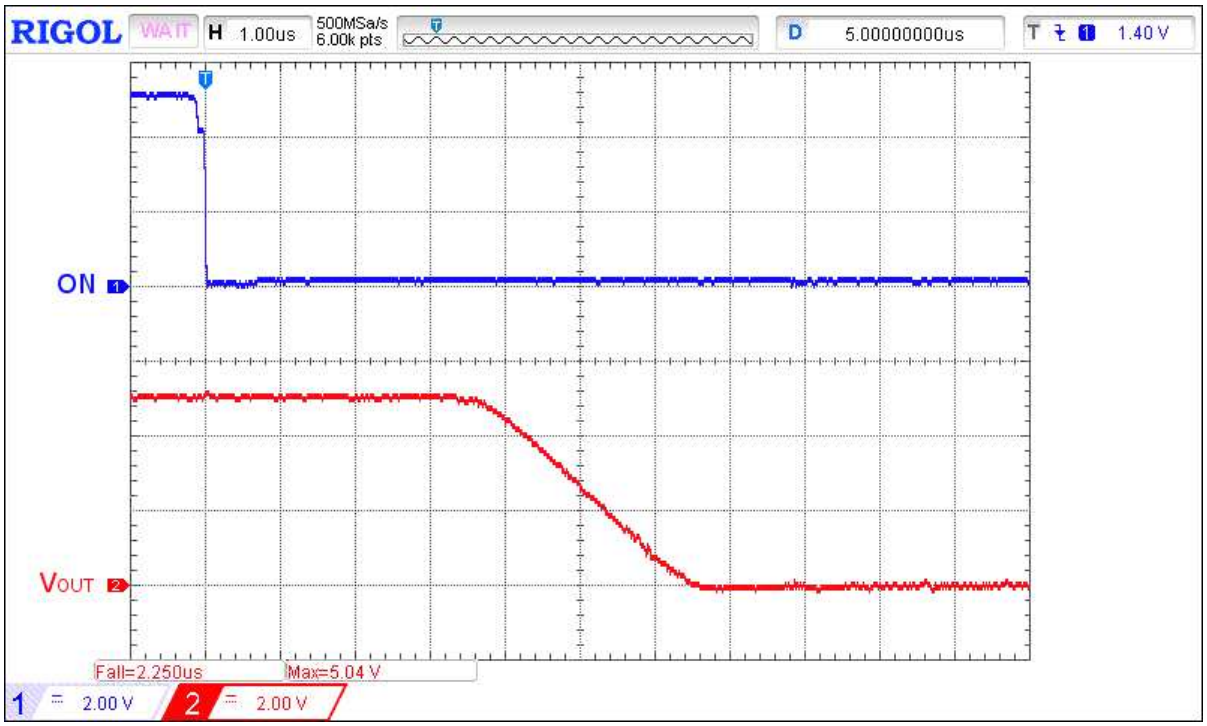


Figure 5. Typical Turn OFF operation waveform for V_{IN} = 5 V, no C_{LOAD} , R_{LOAD} = 10 Ω

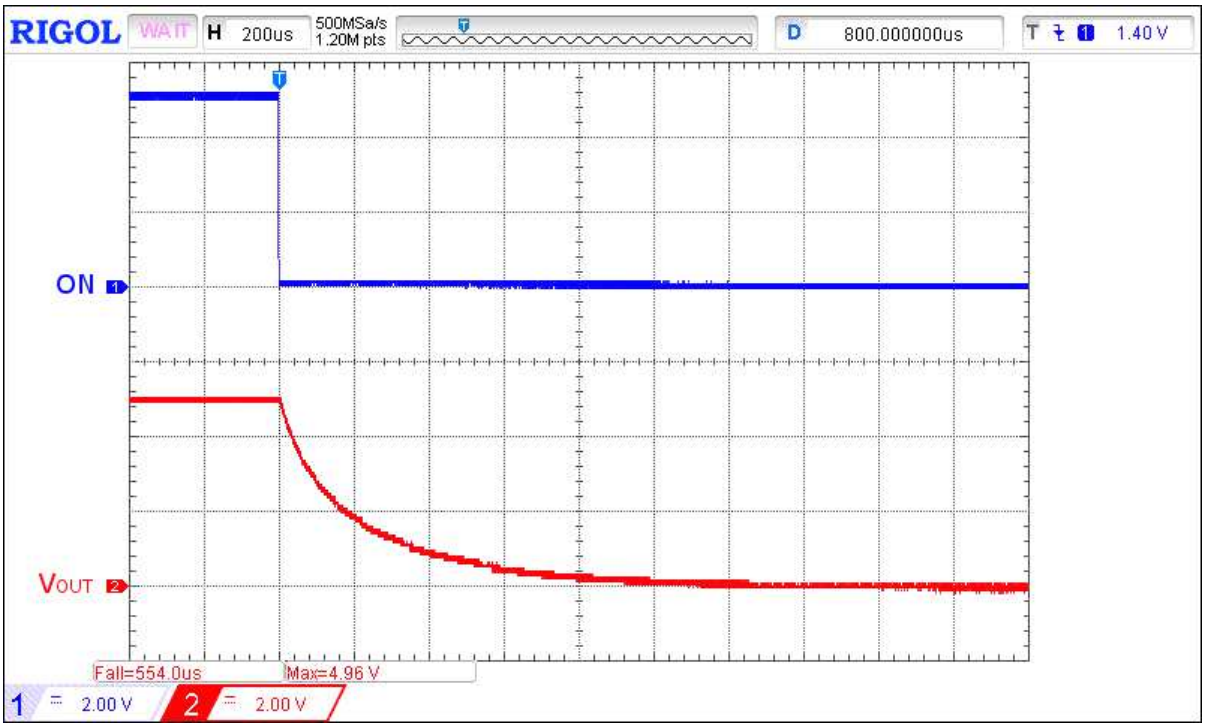


Figure 6. Typical Turn OFF operation waveform for V_{IN} = 5 V, C_{LOAD} = 30 µF, R_{LOAD} = 10 Ω

Applications Information

SLG59M1730C Nominal Operation

During V_{IN} power-up operation, the SLG59M1730C's internal inrush current Start-up Control circuit is activated once V_{IN} reaches 90% of its nominal voltage (Please see $V_{SUCC(TH)}$ specification). Once V_{IN} has reached this threshold (within the SLG59M1730C's nominal input range of 2.5 V to 5.5 V), the ON pin can be toggled LOW-to-HIGH to close the switch. Nominal power-off sequence is performed in reverse: that is, the ON pin is toggled HIGH-to-LOW to open the switch before V_{IN} is powered down/turned OFF.

SLG59M1730C VIN Inrush Current Limit on Startup

During startup, the current passing through the power FET is internally limited to a maximum specified by I_{RISE} in the EC table. To prevent incomplete start-up, the SLG59M1730C shall be powered up only with a capacitive load C_{LOAD} attached to the VOUT pin. After V_{OUT} ramps up to its nominal voltage, a resistive load (R_{LOAD}) can be applied to the integrated load SWITCH.

Slew Rate Calculation

During the rise of V_{OUT}, the SLG59M1730C limits the output current to I_{RISE}. With a capacitor C_{LOAD} attached to VOUT, the equation below provides the nominal value for the slew rate:

$$\text{Slew Rate} = \frac{I_{RISE}}{C_{LOAD}}$$

Power Dissipation Considerations

The junction temperature of the SLG59M1730C depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the RDS_{ON}-generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the SLG59M1730C is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = RDS_{ON} \times I_{DS}^2$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

RDS_{ON}= Power MOSFET ON resistance, in Ohms (Ω)

I_{DS} = Output current, in Amps (A)

and

$$T_J = PD_{TOTAL} \times \Theta_{JA} + T_A$$

where:

T_J = Die junction temperature, in Celsius degrees (°C)

Θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on pcb layout

T_A = Ambient temperature, in Celsius degrees (°C)

In nominal operating mode, the SLG59M1730C's power dissipation can also be calculated by taking into account the voltage drop across the switch (V_{IN} - V_{OUT}) and the magnitude of the switch's output current (I_{DS}):

$$PD_{TOTAL} = (V_{IN} - V_{OUT}) \times I_{DS} \text{ or}$$

$$PD_{TOTAL} = (V_{IN} – (R_{LOAD} \times I_{DS})) \times I_{DS}$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

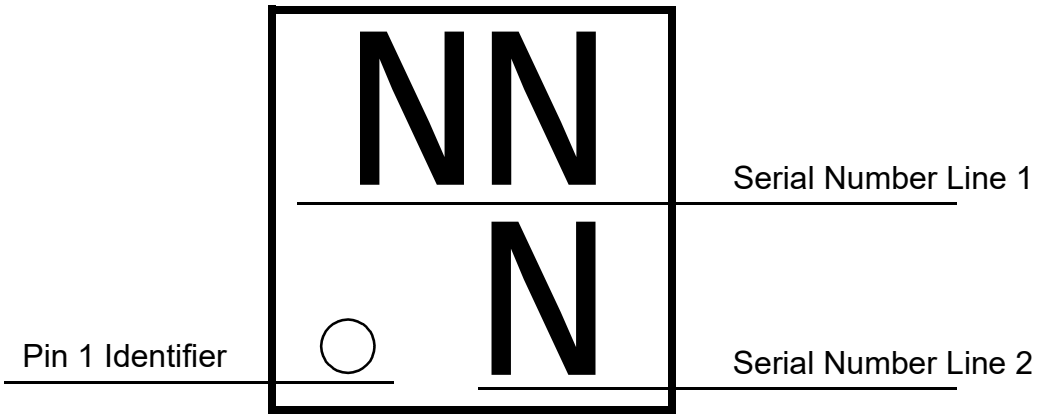
V_{IN} = Switch input Voltage, in Volts (V)

R_{LOAD} = Output Load Resistance, in Ohms (Ω)

I_{DS} = Switch output current, in Amps (A)

V_{OUT} = Switch output voltage, or $R_{LOAD} \times I_{DS}$

Package Top Marking System Definition



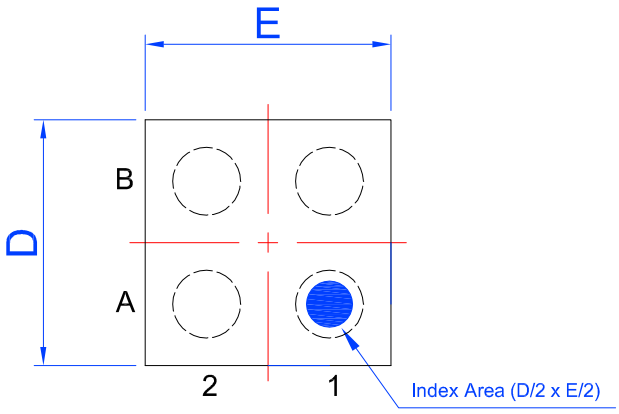
NN - Part Serial Number Field Line 1
where each “N” character can be A-Z and 0-9

N - Part Serial Number Field Line 2
where each “N” character can be A-Z and 0-9

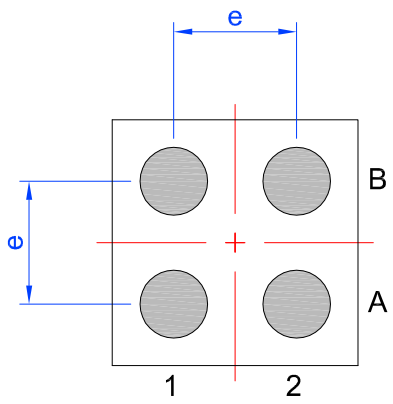
Package Drawing and Dimensions

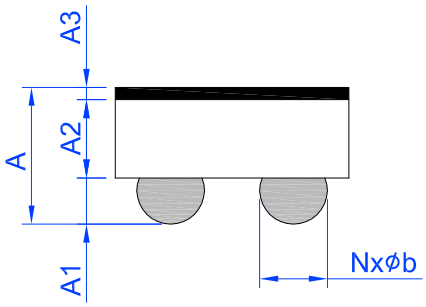
4 Pin WLCSP Green Package 0.8 x 0.8 mm

Laser Marking View



Bump View





SIDE View

TERMINALS ASSIGNMENTS		
B	VIN	VOUT
A	ON	GND
	1	2

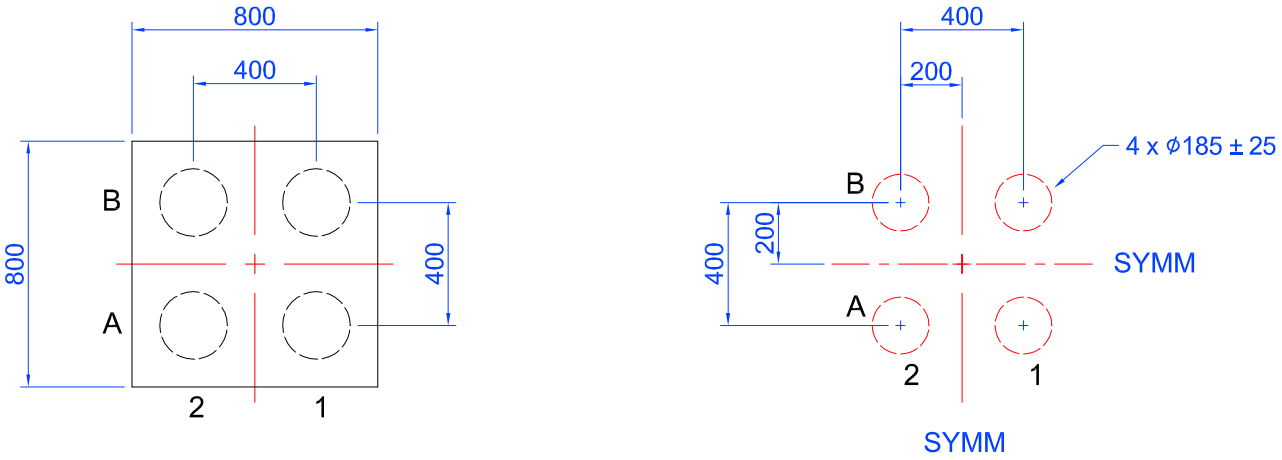
Unit: mm

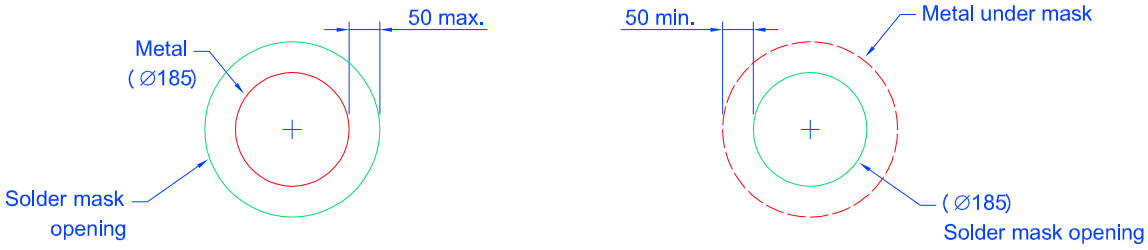
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.380	-	0.500	D	0.77	0.80	0.83
A1	0.125	0.150	0.175	E	0.77	0.80	0.83
A2	0.240	0.265	0.290	e	0.40 BSC		
A3	0.015	0.025	0.035	N	4 (Bump)		
b	0.195	0.220	0.245				

SLG59M1730C 4 Pin WLCSP PCB Landing Pattern

Exposed Bump
(Laser marking view)

Recommended
Land Pattern



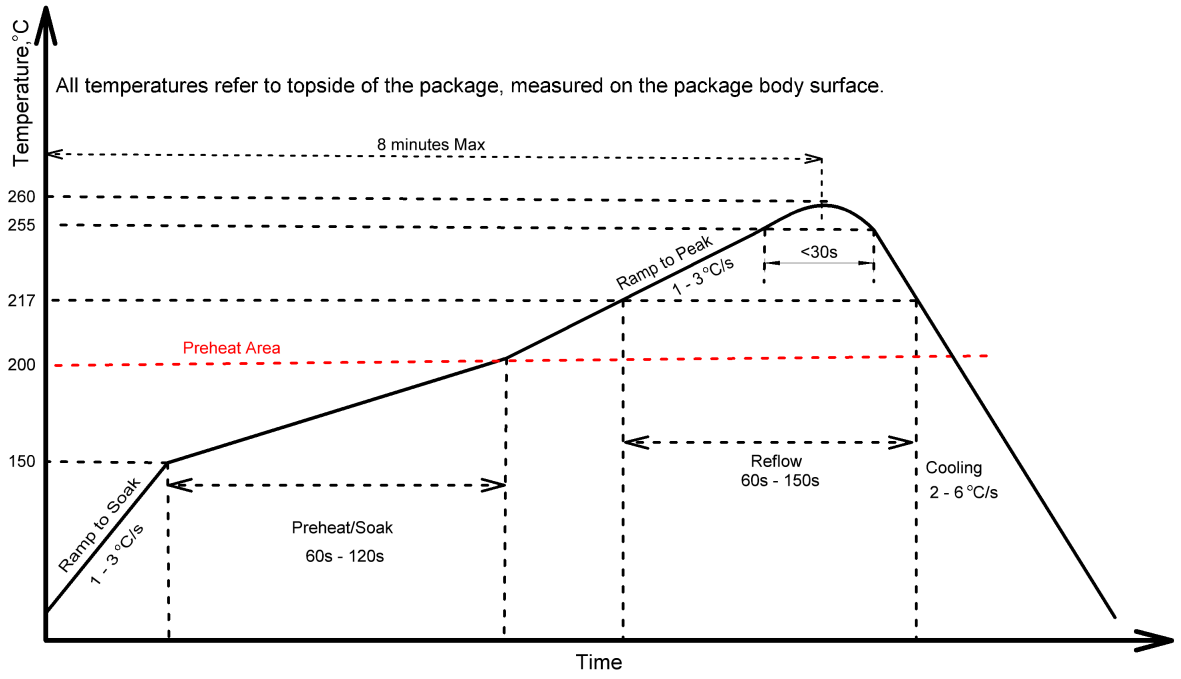


Solder mask detail (not to scale)

Unit: um

Recommended Reflow Soldering Profile

For successful reflow of the SLG59M1730C a recommended thermal profile is illustrated below:



Note: This reflow profile is for classification/preconditioning and are not meant to specify board assembly profile. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed parameters depicted on figure above.

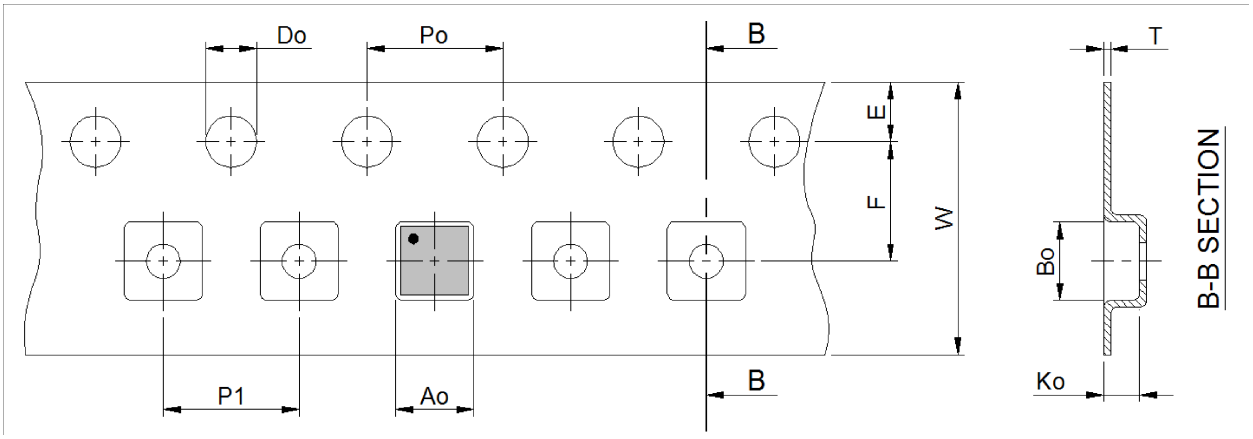
Please see more information on IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.352 mm^3 (nominal).

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
WLCSP 4L 0.8 x 0.8 mm 0.4P Green	4	0.8 x 0.8 x 0.44	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width	Tape Thickness
	A0	B0	K0	P0	P1	D0	E	F	W	T
WLCSP 4L 0.8 x 0.8 mm 0.4P Green	0.87	0.87	0.56	4	2	1.5	1.75	3.5	8	0.2



Note: 1.Orientation in carrier: Pin1 is at upper left corner (Quadrant 1). **Refer to EIA-481 specification**

Revision History

Date	Version	Change
2/14/2022	1.05	Renesas rebranding Fixed typos
10/24/2017	1.04	Updated I_{IN} specifications Updated Charts
7/24/2017	1.03	Updated Tape and Reel Specification
5/5/2 017	1.02	Updated EC Table
3/28/2017	1.01	Fixed typos Updated PCB Landing Pattern
3/1/2017	1.00	Production Release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.