

SLG59M1657V

An Ultra-small 3 mm², 8.4 mΩ, 4 A, 125 °C-Rated Internally-protected Load Switch

General Description

The SLG59M1657V is a high performance 8.4 mΩ, 4 A single-channel nFET load switch which can operate with a 2.5 V to 5.5 V V_{DD} supply to switch power rails from as low as 0.9 V up to the supply voltage. The SLG59M1657V incorporates two-level overload current protection, thermal shutdown protection, and inrush current control which can easily be adjusted by a small external capacitor.

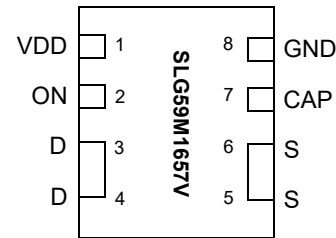
Using a proprietary MOSFET design, the SLG59M1657V achieves a stable 8.4 mΩ RDS_{ON} across a wide input voltage range. In addition, the SLG59M1657V's package also exhibits low thermal resistance for high-current operation using Renesas's proprietary CuFET technology.

Fully specified over the -40 °C to 125 °C temperature range, the SLG59M1657V is packaged in a space-efficient, low thermal resistance, RoHS-compliant 1.5 mm x 2.0 mm STDFN package.

Features

- 1.5 x 2.0 mm TDFN package (2 fused pins for drain and 2 fused pins for source)
- Logic level ON pin capable of supporting 0.85 V CMOS Logic
- User selectable ramp rate with external capacitor
- 8.4 mΩ RDS_{ON} while supporting 4 A
- Two Over Current Protection Modes
 - Short Circuit Current Limit
 - Active Current Limit
- Over Temperature Protection
- Pb-Free / Halogen-Free / RoHS compliant
- Operating Temperature: -40 °C to 125°C
- Operating Voltage: 2.5 V to 5.5 V

Pin Configuration

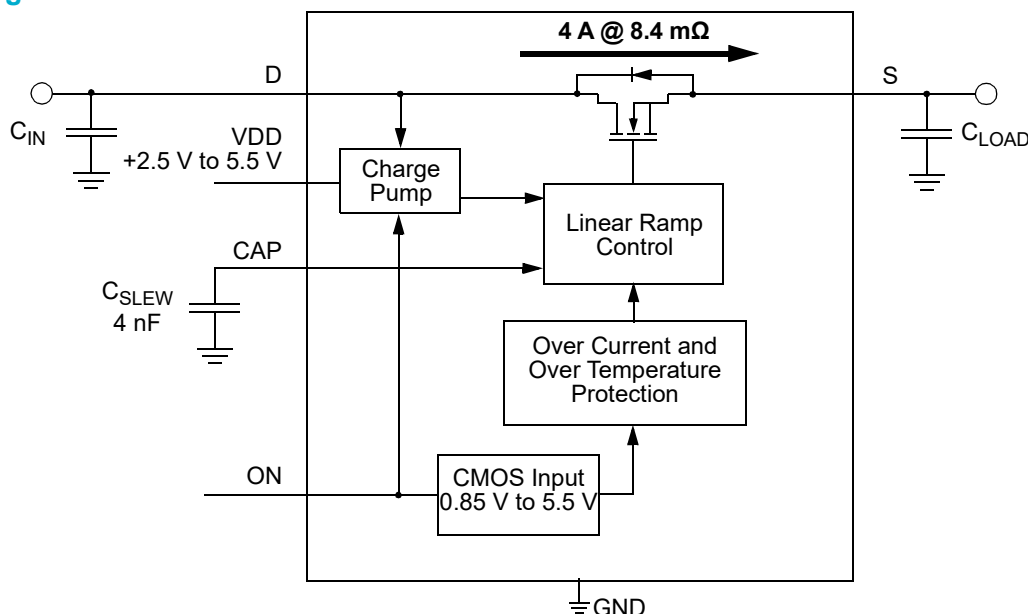


8-pin FC-TDFN
(Top View)

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

Block Diagram



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Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	With an internal 1.8 V $V_{DD(UVLO)}$, VDD supplies the power for the operation of the load switch and internal control circuitry. Bypass the VDD pin to GND with a 0.1 μF (or larger) capacitor.
2	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59M1657V's state machine. ON is a CMOS input with $ON_{V_{IL}} < 0.3$ V and $ON_{V_{IH}} > 0.85$ V thresholds. While there is an internal pull-down circuit to GND (~4 MΩ), connect this pin directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller.
3, 4	D	MOSFET	Drain terminal connection of the n-channel MOSFET (2 pins fused for D). Connect at least a low-ESR 0.1 μF capacitor from this pin to ground. Capacitors used at D should be rated at 10 V or higher.
5, 6	S	MOSFET	Source terminal connection of the n-channel MOSFET (2 pins fused for S). Connect a low-ESR capacitor from this pin to ground and consult the Electrical Characteristics table for recommended C_{LOAD} range. Capacitors used at S should be rated at 10 V or higher.
7	CAP	Input	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the V_S slew rate and overall turn-on time of the SLG59M1657V. For best performance C_{SLEW} value should be ≥ 1.5 nF and voltage level should be rated at 10 V or higher.
8	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59M1657V	FC-TDFN 8L	Extended Industrial, -40 °C to 125 °C
SLG59M1657VTR	FC-TDFN 8L (Tape and Reel)	Extended Industrial, -40 °C to 125 °C

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Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Power Supply		--	--	7	V
V _D to GND	Load Switch Input Voltage to GND		-0.3	--	7	V
V _S to GND	Load Switch Output Voltage to GND		-0.3	--	V _D	V
ON and CAP to GND	ON and CAP Pin Voltages to GND		-0.3	--	7	V
T _O	Operating Temperature		-40	--	125	°C
T _S	Storage Temperature		-65	--	150	°C
T _A	Rated Operating Temperature		-40	--	125	°C
ESD _{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD _{CDM}	ESD Protection	Charged Device Model	1000	--	--	V
MSL	Moisture Sensitivity Level		1			
θ _{JA}	Thermal Resistance	1.5 x 2 mm, 8L TDFN; Determined using 1 in ² , 1 oz. copper pads under each D and S terminals and FR4 pcb material	--	69	--	°C/W
W _{DIS}	Package Power Dissipation		--	--	1	W
MOSFET I _{DS} CONT	Max Continuous Switch Current		--	--	4	A
MOSFET I _{DS} PK	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	--	--	4.5	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 to 125 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Power Supply Voltage	-40 to 125°C	2.5	--	5.5	V
V _{DD(UVLO)}	V _{DD} Undervoltage Lockout Threshold	V _{DD} ↑	--	1.8	--	V
I _{DD}	Power Supply Current	when OFF; T _A = 70 °C; V _S = 0 V; V _D = V _{DD} = 5.5 V	--	--	1	μA
		when OFF; T _A = 85 °C; V _S = 0 V; V _D = V _{DD} = 5.5 V	--	--	1	μA
		when OFF; T _A = 125 °C; V _S = 0 V; V _D = V _{DD} = 5.5 V	--	--	1.5	μA
		when ON, no Load	--	70	120	μA
R _{DS} ON	ON Resistance	T _A = 25 °C; I _{DS} = 100 mA	--	8.4	10	mΩ
		T _A = 85 °C; I _{DS} = 100 mA	--	10	12	mΩ
		T _A = 125 °C; I _{DS} = 100 mA	--	12	14.4	mΩ
V _D	Drain Voltage		0.9	--	V _{DD}	V
MOSFET I _{DS}	Current from D to S	Continuous	--	--	4	A

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Electrical Characteristics (continued)

T_A = -40 to 125 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I _{FET_OFF}	MOSFET OFF Leakage Current	V _D = V _{DD} = 5.5 V; V _S = 0 V; ON = 0 V; T _A = 70 °C	--	--	1	μA
		V _D = V _{DD} = 5.5 V; V _S = 0 V; ON = 0 V; T _A = 85 °C	--	--	1	μA
		V _D = V _{DD} = 5.5 V; V _S = 0 V; ON = 0 V; T _A = 125 °C	--	--	20	μA
V _{S(SR)}	Slew Rate	10% V _S to 90% V _S	Set by External C _{SLEW} ¹			ms
		Example: C _{SLEW} = 4 nF, V _{DD} = V _D = 5 V, C _{LOAD} = 10 μF, R _{LOAD} = 20 Ω	--	3	--	V/ms
T _{ON_Delay}	ON Delay Time	50% ON to V _S Ramp Start	--	200	--	μs
T _{OFF_Delay}	OFF Delay Time	50% ON to V _S Fall Start, V _{DD} = V _D = 5 V, no C _{LOAD} , R _{LOAD} = 20 Ω	--	22	--	μs
T _{FALL}	V _S Fall Time	90% V _S to 10% V _S , V _{DD} = V _D = 5 V, no C _{LOAD} , R _{LOAD} = 20 Ω	--	10	--	μs
C _{LOAD}	Output Capacitive Load to GND	C _{LOAD} connected from S to GND	--	--	500	μF
ON_V _{IH}	High Input Voltage on ON pin		0.85	--	V _{DD}	V
ON_V _{IL}	Low Input Voltage on ON pin		-0.3	0	0.25	V
I _{LIMIT}	Active Current Limit, I _{ACL}	MOSFET will automatically limit current when V _S > 250 mV	--	6.0	--	A
	Short Circuit Current Limit, I _{SCL}	MOSFET will automatically limit current when V _S < 250 mV	--	0.5	--	A
THERM _{ON}	Thermal shutoff turn-on temperature		--	150	--	°C
THERM _{OFF}	Thermal shutoff turn-off temperature		--	130	--	°C
THERM _{TIME}	Thermal shutoff time		--	--	1	ms

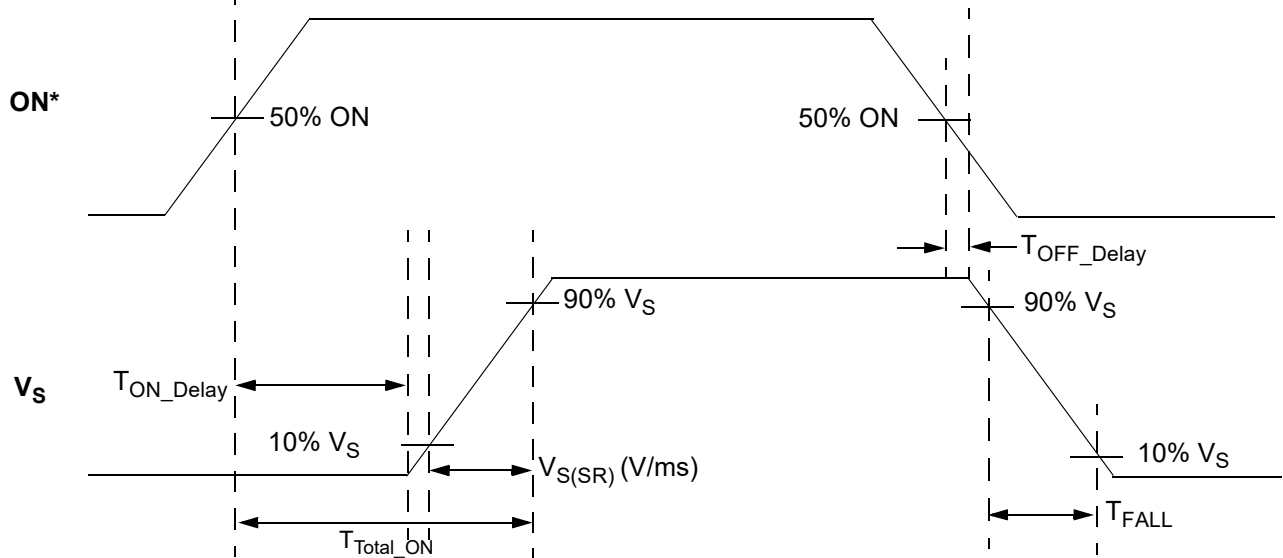
Notes:

1. Refer to typical timing parameter vs. C_{SLEW} performance charts for additional information when available.

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T_{ON_Delay} , $V_{S(SR)}$, and T_{Total_ON} Timing Details



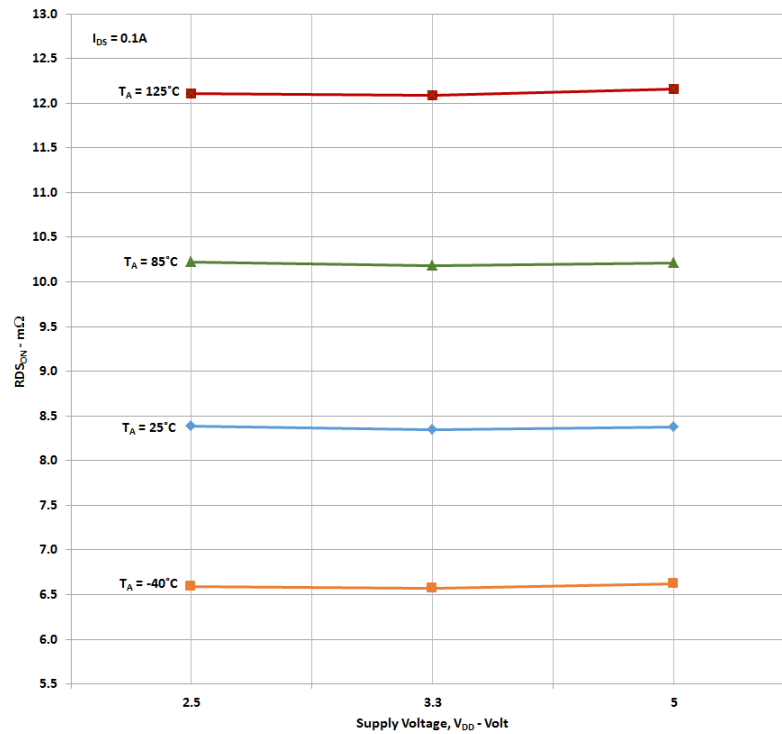
Note: * Rise and Fall times of the ON signal are 100 ns

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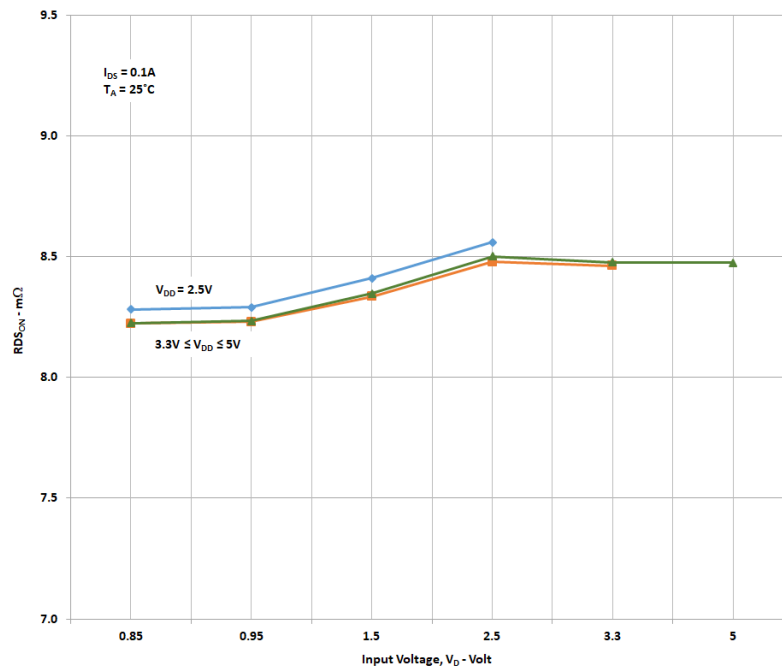
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Typical Performance Characteristics

RDS_{ON} vs. V_{DD}, and Temperature



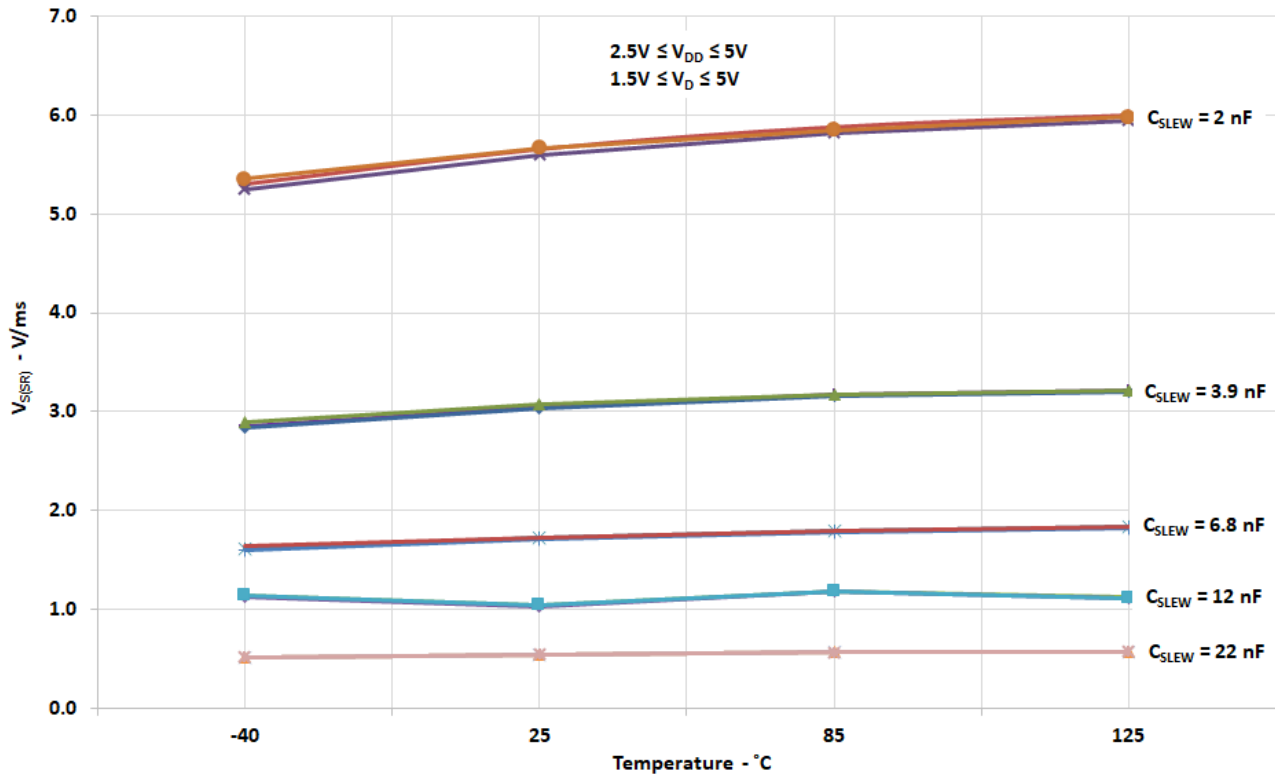
RDS_{ON} vs. V_D and V_{DD}



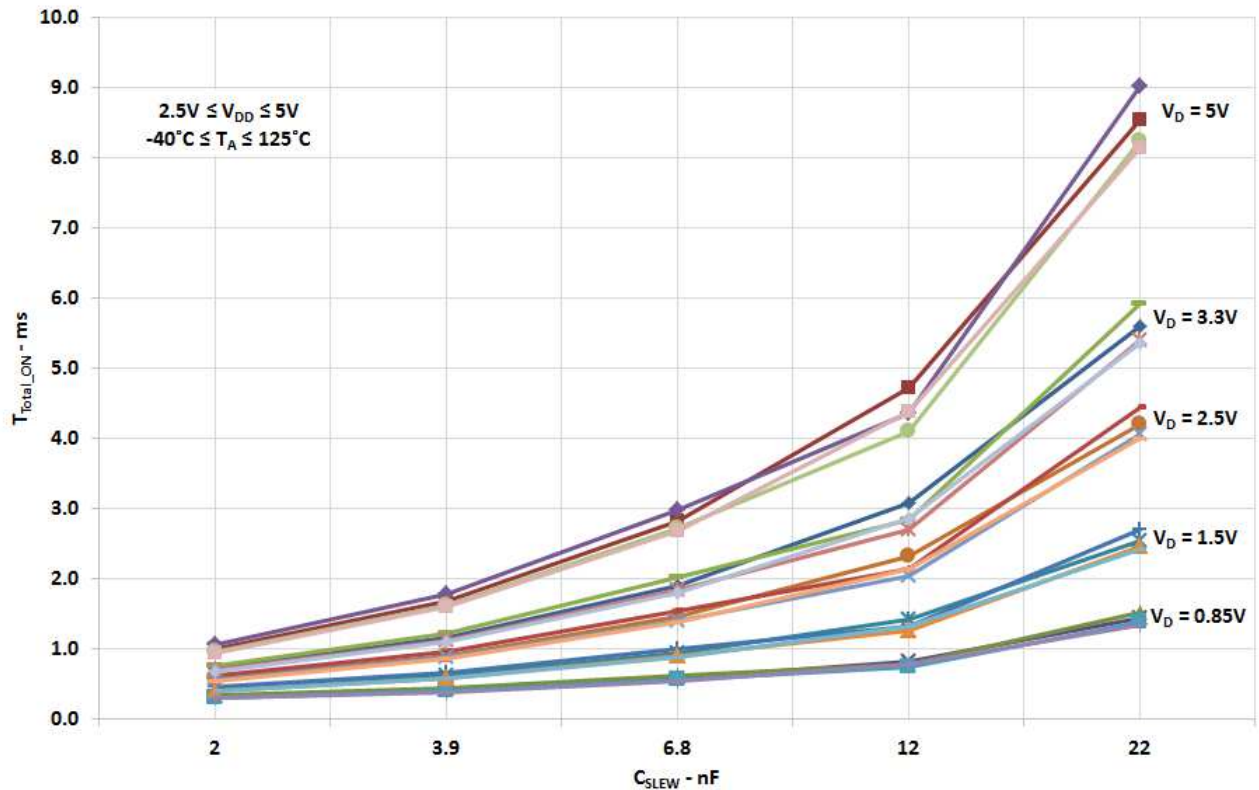
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$V_{S(SR)}$ vs. Temperature, V_D , V_{DD} , and C_{SLEW}



T_{Total_ON} vs. C_{SLEW} , V_D , V_{DD} , and Temperature



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Typical Operation Waveforms

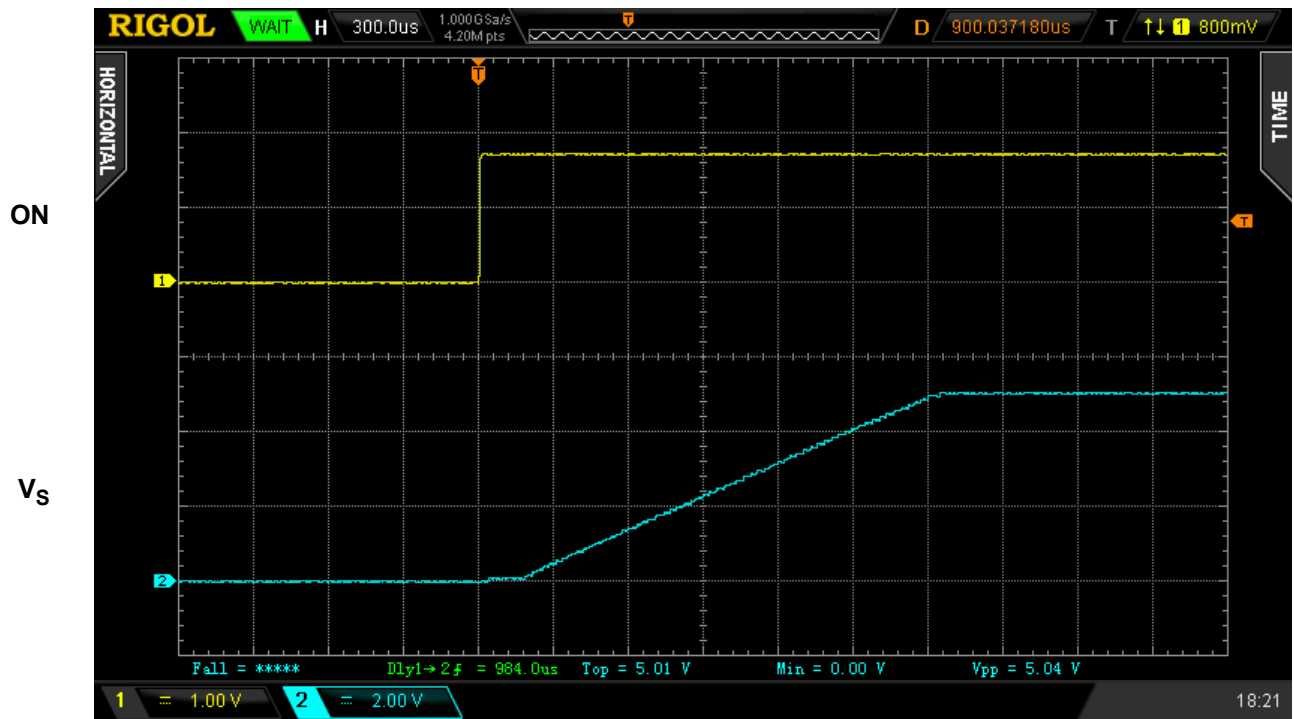


Figure 1. Typical Turn ON operation waveform for $V_{DD} = V_D = 5\text{ V}$, $C_{SLEW} = 4\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 20\text{ }\Omega$

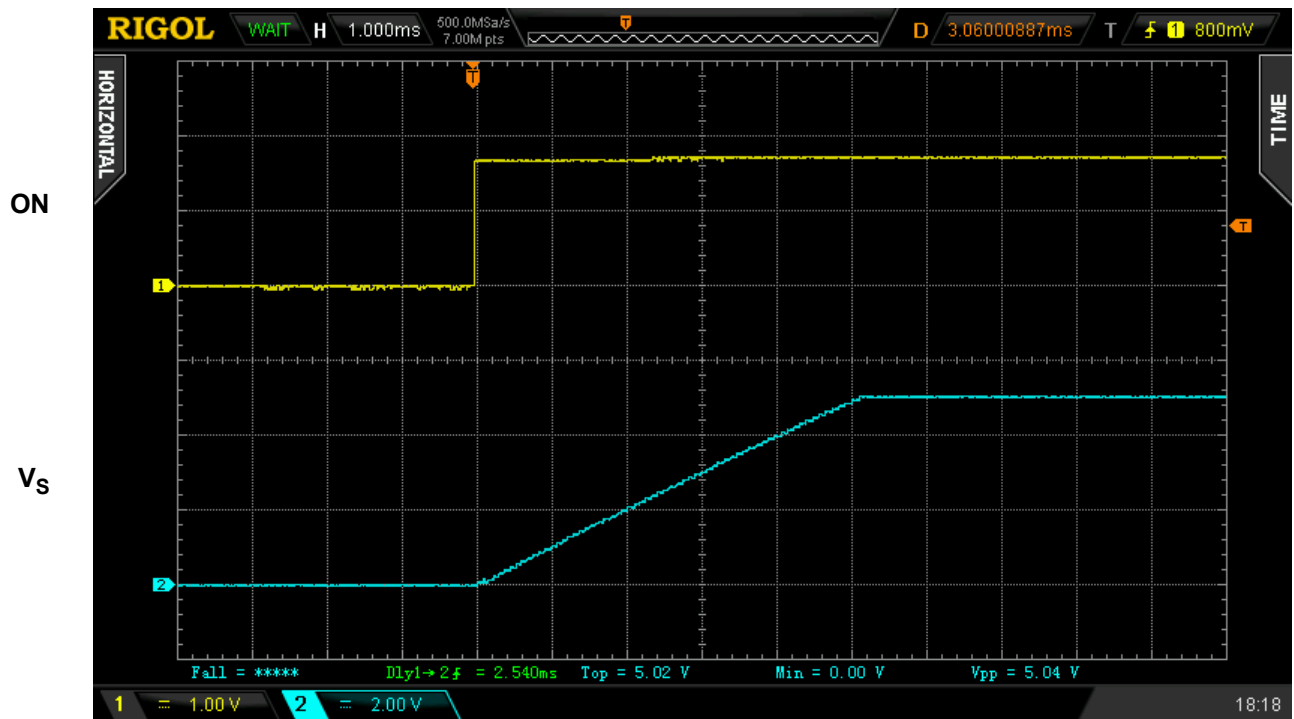


Figure 2. Typical Turn ON operation waveform for $V_{DD} = V_D = 5\text{ V}$, $C_{SLEW} = 12\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 20\text{ }\Omega$

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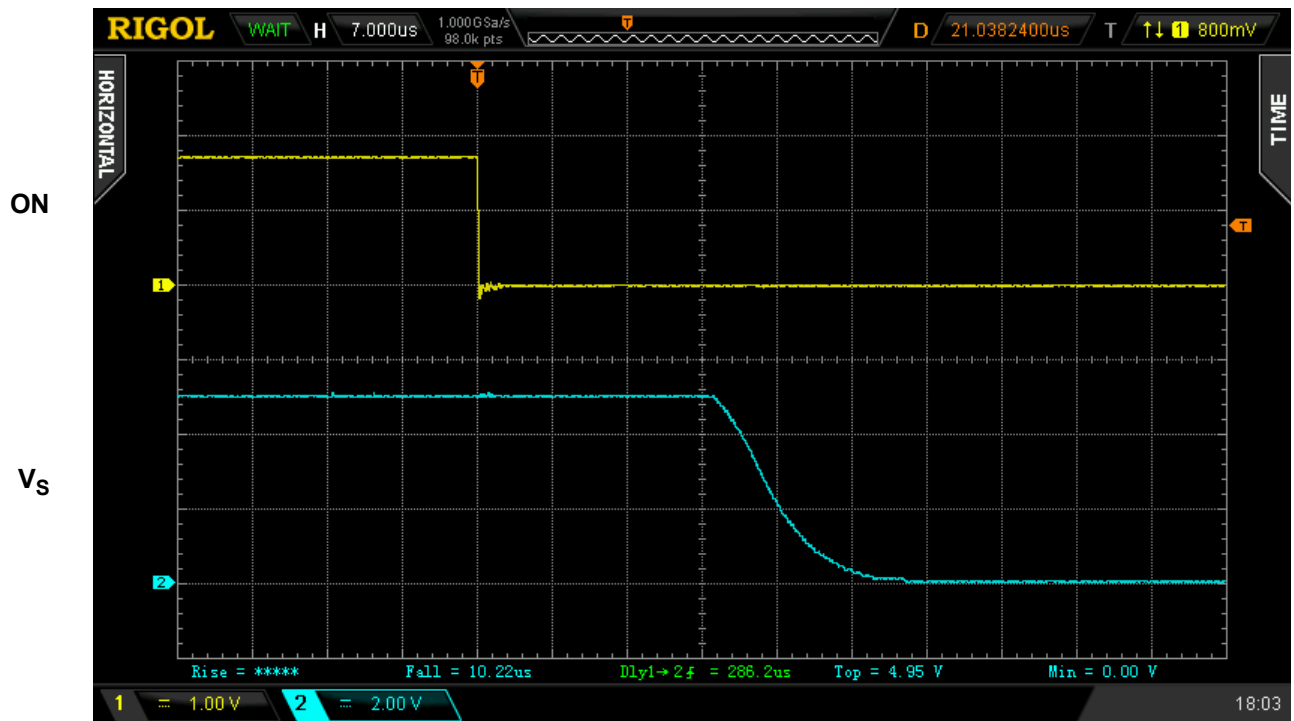


Figure 3. Typical Turn OFF operation waveform for $V_{DD} = V_D = 5 \text{ V}$, $C_{SLEW} = 4 \text{ nF}$, no C_{LOAD} , $R_{LOAD} = 20 \text{ } \Omega$

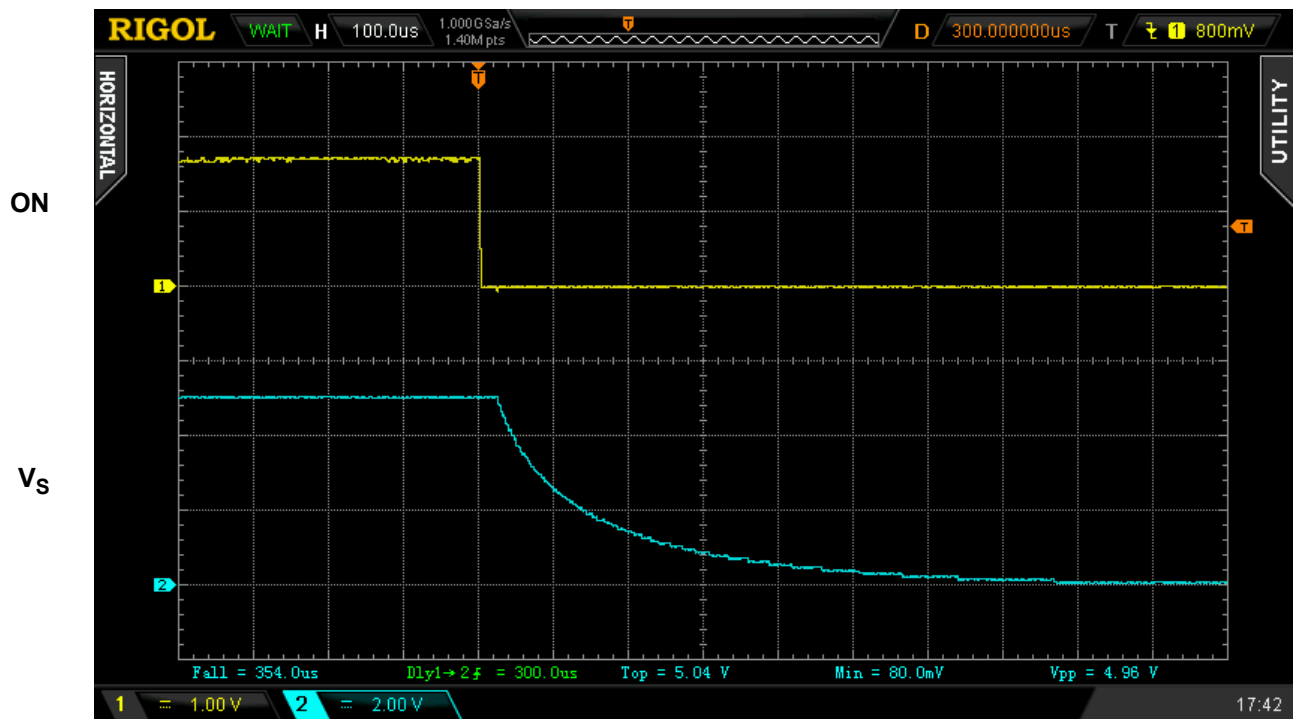


Figure 4. Typical Turn OFF operation waveform for $V_{DD} = V_D = 5 \text{ V}$, $C_{SLEW} = 4 \text{ nF}$, $C_{LOAD} = 10 \text{ } \mu\text{F}$, $R_{LOAD} = 20 \text{ } \Omega$

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SLG59M1657V Power-Up/Power-Down Sequence Considerations

To ensure glitch-free power-up under all conditions, apply V_{DD} first, followed by V_D after V_{DD} exceeds 1 V. Then allow V_D to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If V_{DD} and V_D need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10 μF C_{LOAD} will prevent glitches for rise times of V_{DD} and V_D higher than 2 ms.

If the ON pin is toggled HIGH before V_{DD} and V_D have reached their steady-state values, the load switch timing parameters may differ from datasheet specifications.

The slew rate of output V_S follows a linear ramp set by a capacitor connected to the CAP pin. A larger capacitor value at the CAP pin produces a slower ramp, reducing inrush current from capacitive loads.

SLG59M1657V Current Limiting Operation

The SLG59M1657V has two types of current limiting triggered by the output S pin voltage.

1. Standard Current Limiting Mode (with Thermal Shutdown Protection)

When the V_S voltage > 250 mV, the output current is initially limited to the Active Current Limit (I_{ACL}) specification listed in the Electrical Characteristics table. The ACL monitor's response time is very fast and is triggered within a few microseconds to sudden (transient) changes in load current. When a load current overload is detected, the ACL monitor increases the FET resistance to keep the current from exceeding the load switch's I_{ACL} threshold.

However, if a load-current overload condition persists where the die temperature rises because of the increased FET resistance, the load switch's internal Thermal Shutdown Protection circuit can be activated. If the die temperature exceeds the listed $THERM_{ON}$ specification, the FET is shut OFF completely, thereby allowing the die to cool. When the die cools to the listed $THERM_{OFF}$ temperature threshold, the FET is allowed to turn back on. This process may repeat as long as the output current overload condition persists.

2. Short Circuit Current Limiting Mode (with Thermal Shutdown Protection)

When the V_S voltage < 250 mV (which is the case with a hard short, such as a solder bridge on the power rail), the load switch's internal Short-circuit Current Limit (SCL) monitor limits the FET current to approximately 500 mA (the I_{SCL} threshold). While the internal Thermal Shutdown Protection circuit remains enabled and since the I_{SCL} threshold is much lower than the I_{ACL} threshold, thermal shutdown protection may become activated only at higher ambient temperatures.

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Power Dissipation

The junction temperature of the SLG59M1657V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59M1657V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = R_{DS(ON)} \times I_{DS}^2$$

where:

PD = Power dissipation, in Watts (W)

$R_{DS(ON)}$ = Power MOSFET ON resistance, in Ohms (Ω)

I_{DS} = Output current, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:

T_J = Junction temperature, in Celsius degrees (°C)

θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W)

T_A = Ambient temperature, in Celsius degrees (°C)

During active current-limit operation, the SLG59M1657V's power dissipation can be calculated by taking into account the voltage drop across the load switch ($V_D - V_S$) and the magnitude of the output current in active current-limit operation (I_{ACL}):

$$PD = (V_D - V_S) \times I_{ACL} \text{ or}$$

$$PD = (V_D - (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:

PD = Power dissipation, in Watts (W)

V_D = Input Voltage, in Volts (V)

R_{LOAD} = Load Resistance, in Ohms (Ω)

I_{ACL} = Output limited current, in Amps (A)

$V_S = R_{LOAD} \times I_{ACL}$

For more information on GreenFET load switch features, please visit our website and see App Note "AN-1068 GreenFET and High Voltage GreenFET Load Switch Basics".

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Layout Guidelines:

1. The VDD pin needs a 0.1 μF and 10 μF external capacitors to smooth pulses from the power supply. Locate these capacitors as close as possible to the SLG59M1657V's PIN1.
2. Since the D and S pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with an absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in [Figure 5](#), illustrates proper techniques for heat to transfer as efficiently as possible out of the device;
3. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59M1657V's D and S pins;
4. The GND pin should be connected to system analog or power ground plane.
5. 2 oz. copper is recommended for high current operation.

SLG59M1657V Evaluation Board:

A GreenFET Evaluation Board for SLG59M1657V is designed according to the statements above and is illustrated on [Figure 5](#). Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

Please solder your SLG59M1657V here

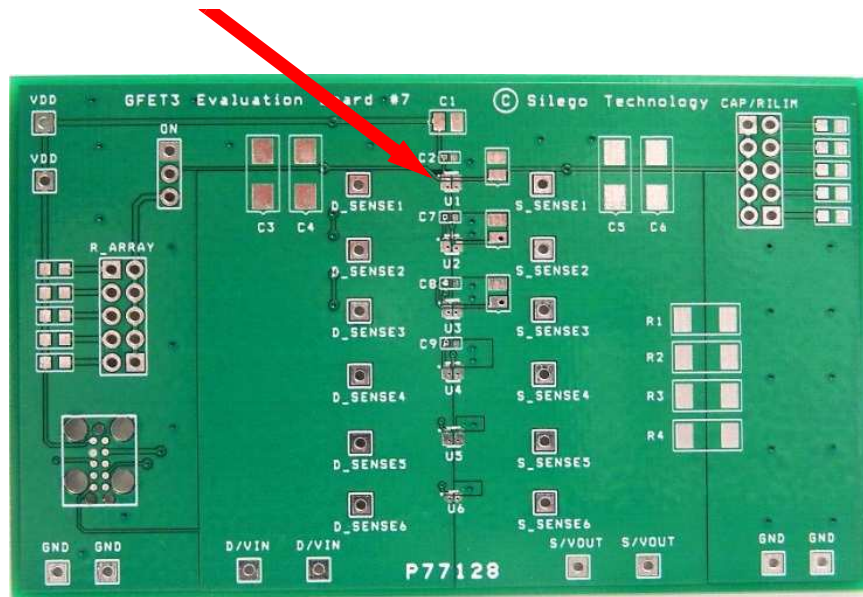


Figure 5. SLG59M1657V Evaluation Board

Datasheet

3-Feb-2022



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Basic Test Setup and Connections

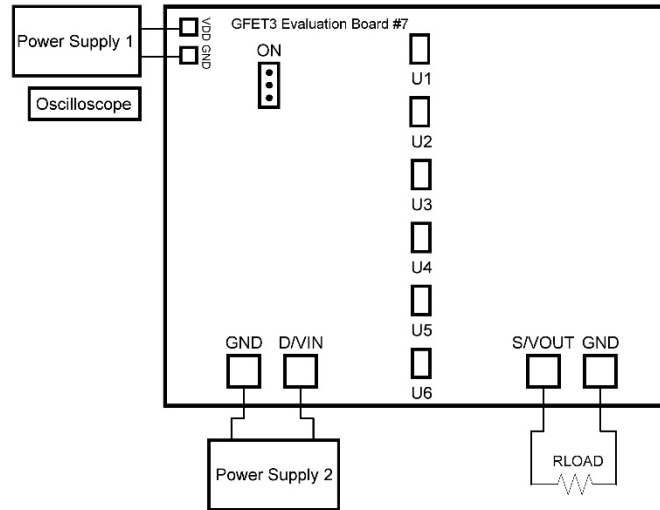


Figure 7. Typical connections for GreenFET Evaluation

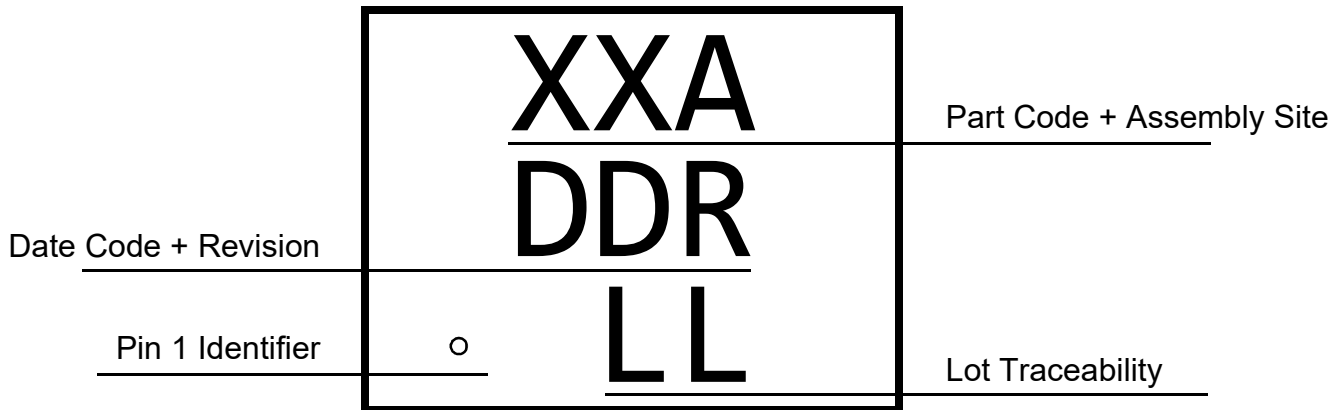
EVB Configuration

1. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;
2. Turn on Power Supply 1 and set desired V_{DD} from 2.5 V...5.5 V range;
3. Turn on Power Supply 2 and set desired V_D from 0.85 V...5.5 V range;
4. Toggle the ON signal High or Low to observe SLG59M1657V operation.

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Package Top Marking System Definition



XX - Part Code Field¹
A - Assembly Site Code Field²
DD - Date Code Field¹
R - Part Revision Code Field²
LL - Lot Traceability Field¹

Note 1: Each character in code field can be alphanumeric A-Z and 0-9

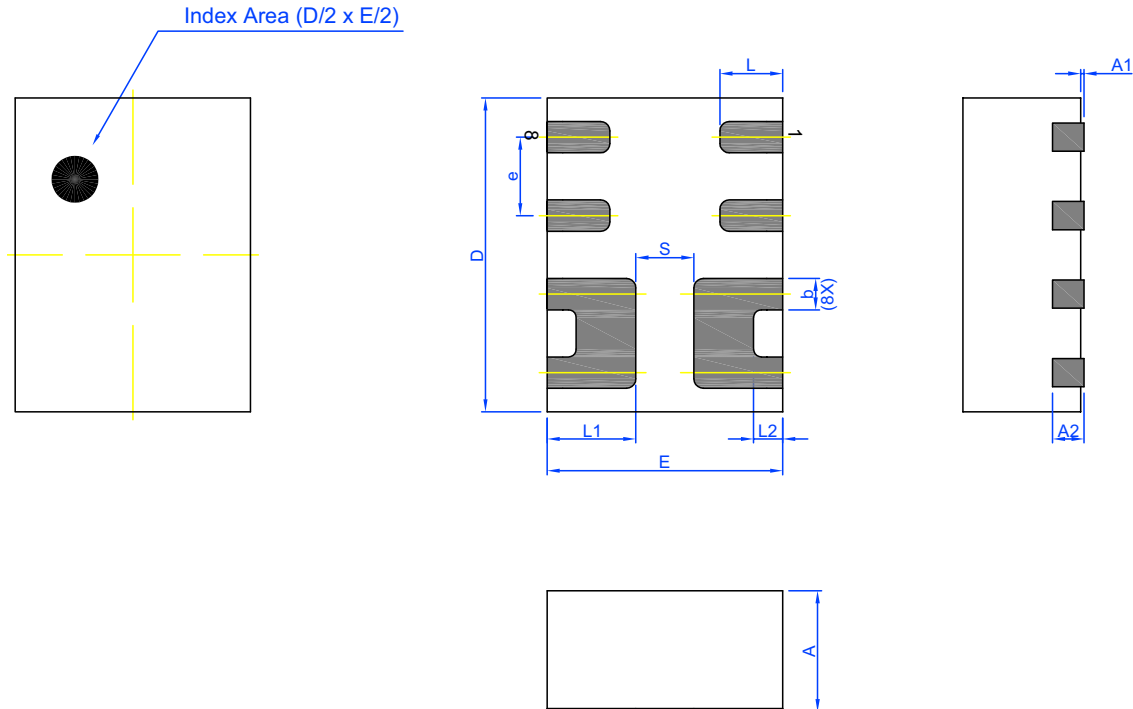
Note 2: Character in code field can be alphabetic A-Z

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Package Drawing and Dimensions

8 Lead TDFN Package 1.5 x 2.0 mm (Fused Lead)
JEDEC MO-252



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.70	0.75	0.80	L	0.35	0.40	0.45
A1	0.005	-	0.060	L1	0.515	0.565	0.615
A2	0.15	0.20	0.25	L2	0.135	0.185	0.235
b	0.15	0.20	0.25	e	0.50 BSC		
D	1.95	2.00	2.05	S	0.37 REF		
E	1.45	1.50	1.55				

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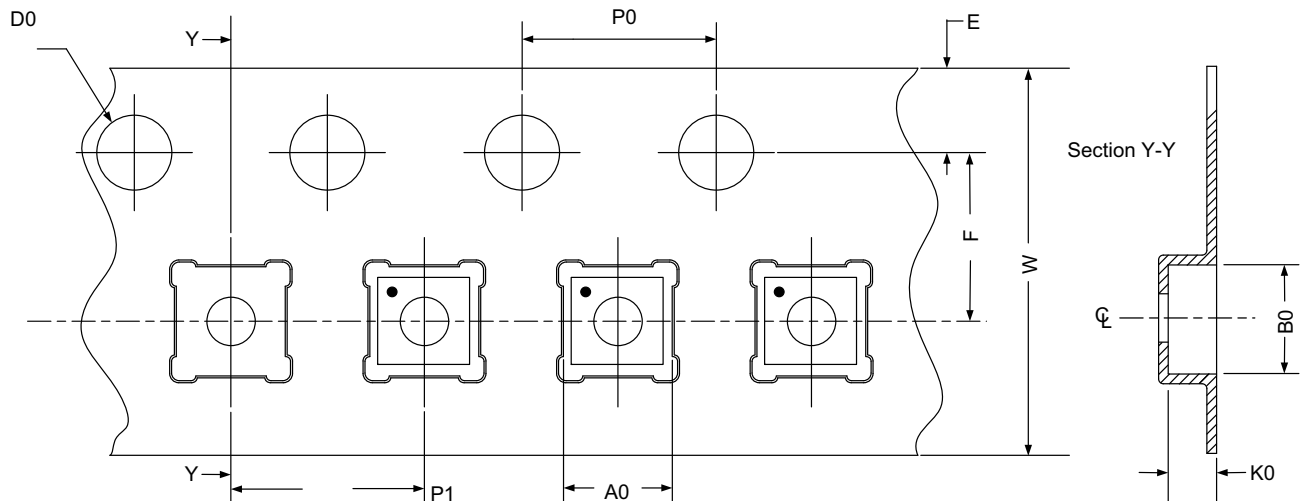
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Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TDFN 8L FC Green	8	1.5 x 2.0 x 0.75	3000	3000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 8L FC Green	1.68	2.18	0.9	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.25 mm³ (nominal). More information can be found at www.jedec.org.

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Revision History

Date	Version	Change
2/3/2022	1.02	Updated Company name and logo Fixed typos
4/15/2017	1.01	Updated Style and Formatting Updated Charts Added Layout Guidelines Fixed typos
2/23/2017	1.00	Production Release

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