The SLG59H1017V is a high-performance 13.3 mΩ NMOS load switch designed to control 12 V or 24 V power rails up to 4 A. Using a proprietary MOSFET design, the SLG59H1017V achieves a stable 13.3 mΩ RDS\(_{\text{ON}}\) across a wide input voltage range. In combining novel FET design and copper pillar interconnects, the SLG59H1017V package also exhibits a low thermal resistance for high-current operation.

Designed to operate over a -40 °C to 85 °C range, the SLG59H1017V is available in a low thermal resistance, RoHS-compliant, 1.6 x 3.0 mm STQFN package.

### Features
- Wide Operating Input Voltage: 12 V or 24 V
- Maximum Continuous Current: 4 A
- Automatic nFET SOA Protection
- 10 W SOA Protection Threshold
- High-performance MOSFET Switch
  - Low RDS\(_{\text{ON}}\): 13.3 mΩ at V\(_{\text{IN}}\) = 24 V
  - Low ΔRDS\(_{\text{ON}}\)/ΔV\(_{\text{IN}}\): < 0.05 mΩ/V
  - Low ΔRDS\(_{\text{ON}}\)/ΔT: < 0.06 mΩ/°C
- Pin-selectable 12V/24V Input Overvoltage and Undervoltage Lockout
- Capacitor-adjustable Inrush Current Control
- Two stage Current Limit Protection:
  - Resistor-adjustable Active Current Limit
  - Internal Short-circuit Current limit
- Open Drain FAULT Signaling
- Analog MOSFET Current Monitor Output: 10 µA/A
- Fast 4 kΩ Output Discharge
- Pb-Free / Halogen-Free / RoHS Compliant Packaging

### Applications
- Power-Rail Switching
- Multifunction Printers
- Large-format Copiers
- Telecommunications Equipment
- High-performance Computing
- 12 V and 24 V Point-of-Load Power Distribution
- Motor Drives
### Pin Description

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Pin Name</th>
<th>Type</th>
<th>Pin Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ON</td>
<td>Input</td>
<td>A low-to-high transition on this pin initiates the operation of the SLG59H1017V’s state machine. ON is an asserted HIGH, level-sensitive CMOS input with ( \text{ON}<em>\text{VIL} &lt; 0.3 \text{ V} ) and ( \text{ON}</em>\text{VIH} &gt; 0.9 \text{ V} ). As the ON pin input circuit does not have an internal pull-down resistor, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller, do not allow this pin to be open-circuited.</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>GND</td>
<td>Pin 2 is a low-current GND terminal for the SLG59H1017V. Connect directly to Pin 3.</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>GND</td>
<td>Pin 3 is the main ground connection for the SLG59H1017V’s internal charge pump, its gate driver and current-limit circuits as well as its internal state machine. Therefore, use a short, stout connection from Pin 3 to the system’s analog or power plane.</td>
</tr>
<tr>
<td>4-8</td>
<td>VIN</td>
<td>MOSFET</td>
<td>VIN supplies the power for the operation of the SLG59H1017V, its internal control circuitry, and the drain terminal of the nFET load switch. With 5 pins fused together at VIN, connect a 47 ( \mu \text{F} ) (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VIN should be rated at 50 V or higher.</td>
</tr>
<tr>
<td>9-13</td>
<td>VOUT</td>
<td>MOSFET</td>
<td>Source terminal of n-channel MOSFET (5 pins fused for VOUT). Connect a 47 ( \mu \text{F} ) (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VOUT should be rated at 50 V or higher.</td>
</tr>
<tr>
<td>14</td>
<td>SEL</td>
<td>Input</td>
<td>As a low logic-level CMOS input with ( \text{SEL}<em>\text{VIL} &lt; 0.3 \text{ V} ) and ( \text{SEL}</em>\text{VIH} &gt; 1.65 \text{ V} ), SEL selects one of two undervoltage/overvoltage lockout windows. When SEL = LOW, the ( \text{VIN} ) undervoltage/overvoltage lockout window is set for 12 V ±10% applications. When SEL = HIGH, the ( \text{VIN} ) undervoltage/overvoltage lockout window is set for 24 V ± 5% applications. See the Electrical Characteristics table for additional information.</td>
</tr>
<tr>
<td>15</td>
<td>FAULT</td>
<td>Output</td>
<td>An open drain output, FAULT is asserted within ( T_{\text{FAULT,LOW}} ) when a ( \text{VIN} ) undervoltage, ( \text{VIN} ) overvoltage, a current-limit, or an over-temperature condition is detected. FAULT is deasserted within ( T_{\text{FAULT,HIGH}} ) when the fault condition is removed. Connect an 100 kΩ external resistor from the FAULT pin to local system logic supply.</td>
</tr>
<tr>
<td>16</td>
<td>CAP</td>
<td>Output</td>
<td>A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the ( V_{\text{OUT}} ) slew rate and overall turn-on time of the SLG59H1017V. For best performance, the range for ( C_{\text{SLEW}} ) values are ( 10 \text{ nF} \leq C_{\text{SLEW}} \leq 20 \text{ nF} ). Please see typical characteristics for additional information. Capacitors used at the CAP pin should be rated at 10 V or higher. Please consult Applications Section on how to select ( C_{\text{SLEW}} ) based on ( V_{\text{OUT}} ) slew rate and loading conditions.</td>
</tr>
<tr>
<td>17</td>
<td>IOUT</td>
<td>Output</td>
<td>IOUT is the SLG59H1017V’s power MOSFET load current monitor output. As an analog current output, this signal when applied to a ground-reference resistor generates a voltage proportional to the current through the n-channel MOSFET. The ( I_{\text{OUT}} ) transfer characteristic is typically 10 ( \mu \text{A} / \text{A} ) with a voltage compliance range of 0.5 V ( \leq V_{\text{OUT}} \leq 4 \text{ V} ). Optimal ( I_{\text{OUT}} ) linearity is exhibited for 0.5 A ( \leq I_{\text{DS}} \leq 4 \text{ A} ). In addition, it is recommended to bypass the IOUT pin to GND with a 0.18 nF capacitor.</td>
</tr>
<tr>
<td>18</td>
<td>RSET</td>
<td>Input</td>
<td>A 1%-tolerance, metal-film resistor between 20 kΩ and 91 kΩ sets the SLG59H1017V’s active current limit. A 91 kΩ resistor sets the SLG59H1017V’s active current limit to 1 A and a 20 kΩ resistor sets the active current limit to 4.5 A.</td>
</tr>
</tbody>
</table>

### Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Type</th>
<th>Production Flow</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLG59H1017V</td>
<td>STQFN 18L FC</td>
<td>Industrial, -40 °C to 85 °C</td>
</tr>
<tr>
<td>SLG59H1017VTR</td>
<td>STQFN 18L FC (Tape and Reel)</td>
<td>Industrial, -40 °C to 85 °C</td>
</tr>
</tbody>
</table>
### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$ to GND</td>
<td>Load Switch Input Voltage to GND</td>
<td>Continuous</td>
<td>-0.3</td>
<td>--</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Maximum pulsed $V_{IN}$, pulse width &lt;0.1s</td>
<td>--</td>
<td>--</td>
<td>32</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OUT}$ to GND</td>
<td>Load Switch Output Voltage to GND</td>
<td></td>
<td>-0.3</td>
<td>--</td>
<td>$V_{IN}$</td>
<td>V</td>
</tr>
<tr>
<td>ON, SEL, CAP, RSET, IOUT, and FAULT to GND</td>
<td>ON, SEL, CAP, RSET, IOUT, and FAULT Pin Voltages to GND</td>
<td></td>
<td>-0.3</td>
<td>--</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>$T_S$</td>
<td>Storage Temperature</td>
<td></td>
<td>-65</td>
<td>--</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>ESD$_{HBM}$</td>
<td>ESD Protection</td>
<td>Human Body Model</td>
<td>2000</td>
<td>--</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>ESD$_{CDM}$</td>
<td>ESD Protection</td>
<td>Charged Device Model</td>
<td>500</td>
<td>--</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>MSL</td>
<td>Moisture Sensitivity Level</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>$\theta_{JA}$</td>
<td>Package Thermal Resistance, Junction-to-Ambient</td>
<td>1.6 x 3.0 mm 18L STQFN; Determined with the device mounted onto a 1 in$^2$, 1 oz. copper pad of FR-4 material</td>
<td>--</td>
<td>40</td>
<td>--</td>
<td>°C/W</td>
</tr>
<tr>
<td>MOSFET IDS$_{CONT}$</td>
<td>Continuous Current from VIN to VOUT</td>
<td>$T_J &lt; 150$ °C</td>
<td>--</td>
<td>--</td>
<td>4</td>
<td>A</td>
</tr>
<tr>
<td>MOSFET IDS$_{PEAK}$</td>
<td>Peak Current from VIN to VOUT</td>
<td>Maximum pulsed switch current, pulse width &lt; 1 ms</td>
<td>--</td>
<td>--</td>
<td>6</td>
<td>A</td>
</tr>
</tbody>
</table>

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Electrical Characteristics

12 V ≤ $V_{IN}$ ≤ 24 V; $C_{IN} = 47$ μF, $T_A = -40$ °C to 85 °C, unless otherwise noted. Typical values are at $T_A = 25$ °C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Operating Input Voltage</td>
<td></td>
<td>10.8</td>
<td>--</td>
<td>25.2</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IN(OVLO)}$</td>
<td>$V_{IN}$ Overvoltage Lockout Threshold</td>
<td>$V_{IN} \uparrow; SEL = HIGH$</td>
<td>25.3</td>
<td>27</td>
<td>28.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} \uparrow; SEL = LOW$</td>
<td>13.3</td>
<td>13.7</td>
<td>14.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IN(UVLO)}$</td>
<td>$V_{IN}$ Undervoltage Lockout Threshold</td>
<td>$V_{IN} \downarrow; SEL = HIGH$</td>
<td>19.5</td>
<td>20.5</td>
<td>21.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} \downarrow; SEL = LOW$</td>
<td>9.7</td>
<td>10.2</td>
<td>10.7</td>
<td>V</td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Quiescent Supply Current</td>
<td>ON = HIGH; $I_{DS} = 0$ A</td>
<td>--</td>
<td>0.5</td>
<td>0.6</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{SHDN}$</td>
<td>OFF Mode Supply Current</td>
<td>ON = LOW; $I_{DS} = 0$ A</td>
<td>--</td>
<td>1</td>
<td>3</td>
<td>μA</td>
</tr>
<tr>
<td>RDS$_{ON}$</td>
<td>ON Resistance</td>
<td>$T_A = 25$ °C; $I_{DS} = 0.1$ A</td>
<td>--</td>
<td>13.3</td>
<td>14</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = 85$ °C; $I_{DS} = 0.1$ A</td>
<td>--</td>
<td>16.8</td>
<td>19</td>
<td>mΩ</td>
</tr>
<tr>
<td>MOSFET IDS</td>
<td>Current from VIN to VOUT</td>
<td>Continuous</td>
<td></td>
<td>--</td>
<td>--</td>
<td>4</td>
</tr>
<tr>
<td>$I_{LIMIT}$</td>
<td>Active Current Limit, $I_{ACL}$</td>
<td>$V_{OUT} &gt; 0.5$ V; $R_{SET} = 30.1$ kΩ</td>
<td>3.0</td>
<td>3.19</td>
<td>3.5</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Short-circuit Current Limit, $I_{SCL}$</td>
<td>$V_{OUT} &lt; 0.5$ V</td>
<td>--</td>
<td>0.5</td>
<td>--</td>
</tr>
<tr>
<td>$T_{ACL}$</td>
<td>Active Current Limit Response Time</td>
<td>$V_{IN} = 12$ V; $R_{SET} = 91$ kΩ; $C_{LOAD} = 10$ μF; switch in 10 Ω load</td>
<td>117</td>
<td>150</td>
<td>220</td>
<td>μs</td>
</tr>
<tr>
<td>R$\text{DISCHRG}$</td>
<td>Output Discharge Resistance</td>
<td>$V_{OUT} = 0.4$ V Input Bias; ON = LOW</td>
<td>3.5</td>
<td>4.4</td>
<td>5.3</td>
<td>kΩ</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Analog MOSFET Current Monitor Output</td>
<td>$I_{DS} = 1$ A</td>
<td>9.3</td>
<td>10</td>
<td>10.7</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{DS} = 3$ A</td>
<td>28.5</td>
<td>30</td>
<td>31.5</td>
<td>μA</td>
</tr>
</tbody>
</table>
**SLG59H1017V**

A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V

**V<sub>IN</sub>** Lockout Select and MOSFET Current Monitor Output

### Electrical Characteristics (continued)

12 V ≤ V<sub>IN</sub> ≤ 24 V; C<sub>IN</sub> = 47 µF, T<sub>A</sub> = -40 °C to 85 °C, unless otherwise noted. Typical values are at T<sub>A</sub> = 25 °C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>T&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>Response Time to Change Current in Main MOSFET</td>
<td>C&lt;sub&gt;OUT&lt;/sub&gt; = 180 pF; Step load 0 to 2.4 A; 0% to 90% I&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>--</td>
<td>45</td>
<td>--</td>
<td>µs</td>
</tr>
<tr>
<td>C&lt;sub&gt;LOAD&lt;/sub&gt;</td>
<td>Output Load Capacitance</td>
<td>C&lt;sub&gt;LOAD&lt;/sub&gt; connected from VOUT to GND</td>
<td>--</td>
<td>47</td>
<td>--</td>
<td>µF</td>
</tr>
<tr>
<td>T&lt;sub&gt;ON_Delay&lt;/sub&gt;</td>
<td>ON Delay Time</td>
<td>50% ON to 10% V&lt;sub&gt;OUT&lt;/sub&gt;↑; V&lt;sub&gt;IN&lt;/sub&gt; = 12 V; C&lt;sub&gt;SLEW&lt;/sub&gt; = 10 nF; R&lt;sub&gt;LOAD&lt;/sub&gt; = 100 Ω, C&lt;sub&gt;LOAD&lt;/sub&gt; = 10 µF</td>
<td>480</td>
<td>600</td>
<td>720</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>50% ON to 10% V&lt;sub&gt;OUT&lt;/sub&gt;↑; V&lt;sub&gt;IN&lt;/sub&gt; = 24 V; C&lt;sub&gt;SLEW&lt;/sub&gt; = 10 nF; R&lt;sub&gt;LOAD&lt;/sub&gt; = 100 Ω, C&lt;sub&gt;LOAD&lt;/sub&gt; = 10 µF</td>
<td>0.8</td>
<td>1.0</td>
<td>1.2</td>
<td>ms</td>
</tr>
<tr>
<td>T&lt;sub&gt;Total_ON&lt;/sub&gt;</td>
<td>Total Turn ON Time</td>
<td>50% ON to 90% V&lt;sub&gt;OUT&lt;/sub&gt;↑</td>
<td>Set by External C&lt;sub&gt;SLEW&lt;/sub&gt;↑</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>50% ON to 90% V&lt;sub&gt;OUT&lt;/sub&gt;↑; V&lt;sub&gt;IN&lt;/sub&gt; = 12 V; C&lt;sub&gt;SLEW&lt;/sub&gt; = 10 nF; R&lt;sub&gt;LOAD&lt;/sub&gt; = 100 Ω, C&lt;sub&gt;LOAD&lt;/sub&gt; = 10 µF</td>
<td>2.9</td>
<td>3.6</td>
<td>4.3</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>50% ON to 90% V&lt;sub&gt;OUT&lt;/sub&gt;↑; V&lt;sub&gt;IN&lt;/sub&gt; = 24 V; C&lt;sub&gt;SLEW&lt;/sub&gt; = 10 nF; R&lt;sub&gt;LOAD&lt;/sub&gt; = 100 Ω, C&lt;sub&gt;LOAD&lt;/sub&gt; = 10 µF</td>
<td>5.7</td>
<td>7.1</td>
<td>8.5</td>
<td>ms</td>
</tr>
<tr>
<td>V&lt;sub&gt;OUT(SR)&lt;/sub&gt;</td>
<td>V&lt;sub&gt;OUT&lt;/sub&gt; Slew rate</td>
<td>10% V&lt;sub&gt;OUT&lt;/sub&gt; to 90% V&lt;sub&gt;OUT&lt;/sub&gt;↑</td>
<td>Set by External C&lt;sub&gt;SLEW&lt;/sub&gt;↑</td>
<td>V/ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10% V&lt;sub&gt;OUT&lt;/sub&gt; to 90% V&lt;sub&gt;OUT&lt;/sub&gt;↑; V&lt;sub&gt;IN&lt;/sub&gt; = 12 V or 24 V; C&lt;sub&gt;SLEW&lt;/sub&gt; = 10 nF; R&lt;sub&gt;LOAD&lt;/sub&gt; = 100 Ω, No C&lt;sub&gt;LOAD&lt;/sub&gt;</td>
<td>2.7</td>
<td>3.2</td>
<td>3.9</td>
<td>V/ms</td>
</tr>
<tr>
<td>T&lt;sub&gt;OFF_Delay&lt;/sub&gt;</td>
<td>OFF Delay Time</td>
<td>50% ON to V&lt;sub&gt;OUT&lt;/sub&gt; Fall Start ↓; V&lt;sub&gt;IN&lt;/sub&gt; = 12 V or 24 V; R&lt;sub&gt;LOAD&lt;/sub&gt; = 100 Ω, No C&lt;sub&gt;LOAD&lt;/sub&gt;</td>
<td>--</td>
<td>15</td>
<td>--</td>
<td>µs</td>
</tr>
<tr>
<td>T&lt;sub&gt;FALL&lt;/sub&gt;</td>
<td>V&lt;sub&gt;OUT&lt;/sub&gt; Fall Time</td>
<td>90% V&lt;sub&gt;OUT&lt;/sub&gt; to 10% V&lt;sub&gt;OUT&lt;/sub&gt;↑; ON = HIGH-to-LOW; V&lt;sub&gt;IN&lt;/sub&gt; = 12 V or 24 V; R&lt;sub&gt;LOAD&lt;/sub&gt; = 100 Ω, No C&lt;sub&gt;LOAD&lt;/sub&gt;</td>
<td>10.4</td>
<td>12.7</td>
<td>14.3</td>
<td>µs</td>
</tr>
<tr>
<td>T&lt;sub&gt;FAULT_LOW&lt;/sub&gt;</td>
<td>FAULT Assertion Time</td>
<td>Abnormal Step Load Current event to FAULT↑; I&lt;sub&gt;ACL&lt;/sub&gt; = 1 A; V&lt;sub&gt;IN&lt;/sub&gt; = 24 V; R&lt;sub&gt;SET&lt;/sub&gt; = 91 kΩ; switch in 20 Ω load</td>
<td>--</td>
<td>80</td>
<td>--</td>
<td>µs</td>
</tr>
<tr>
<td>T&lt;sub&gt;FAULT_HIGH&lt;/sub&gt;</td>
<td>FAULT De-assertion Time</td>
<td>Delay to FAULT↑ after fault condition is removed; I&lt;sub&gt;ACL&lt;/sub&gt; = 1 A; V&lt;sub&gt;IN&lt;/sub&gt; = 24 V; R&lt;sub&gt;SET&lt;/sub&gt; = 91 kΩ; switch out 20 Ω load</td>
<td>--</td>
<td>180</td>
<td>--</td>
<td>µs</td>
</tr>
<tr>
<td>FAULT&lt;sub&gt;VOL&lt;/sub&gt;</td>
<td>FAULT Output Low Voltage</td>
<td>I&lt;sub&gt;FAULT&lt;/sub&gt; = 1 mA</td>
<td>--</td>
<td>0.2</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>ON_V&lt;sub&gt;H&lt;/sub&gt;</td>
<td>ON Pin Input High Voltage</td>
<td>0.9</td>
<td>--</td>
<td>5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>ON_V&lt;sub&gt;L&lt;/sub&gt;</td>
<td>ON Pin Input Low Voltage</td>
<td>-0.3</td>
<td>0</td>
<td>0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>SEL_V&lt;sub&gt;H&lt;/sub&gt;</td>
<td>SEL pin Input High Voltage</td>
<td>1.65</td>
<td>--</td>
<td>4.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>SEL_V&lt;sub&gt;L&lt;/sub&gt;</td>
<td>SEL pin Input Low Voltage</td>
<td>-0.3</td>
<td>--</td>
<td>0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;ON(Leakage)&lt;/sub&gt;</td>
<td>ON Pin Leakage Current</td>
<td>1 V ≤ ON ≤ 5 V or ON = GND</td>
<td>--</td>
<td>--</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td>THERM&lt;sub&gt;ON&lt;/sub&gt;</td>
<td>Thermal Protection Shutdown Threshold</td>
<td>--</td>
<td>145</td>
<td>--</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>THERM&lt;sub&gt;OFF&lt;/sub&gt;</td>
<td>Thermal Protection Restart Threshold</td>
<td>--</td>
<td>125</td>
<td>--</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

1. Refer to typical Timing Parameter vs. C<sub>SLEW</sub> performance charts for additional information.
SLG59H1017V
A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
V_IN Lockout Select and MOSFET Current Monitor Output

$T_{\text{Total\_ON}}, T_{\text{ON\_Delay}}$, and Slew Rate Measurement

*V_{OUT}* $T_{\text{ON\_Delay}}$

50% ON

90% $V_{OUT}$

$V_{\text{OUT\_SR}}$ (V/ms)

$T_{\text{Total\_ON}}$

10% $V_{OUT}$

$T_{OFF\_Delay}$

50% ON

90% $V_{OUT}$

10% $V_{OUT}$

$T_{FALL}$

*Rise and Fall Times of the ON Signal are 100 ns*
Typical Performance Characteristics

**RDS\(_{\text{ON}}\) vs. Temperature and V\(_\text{IN}\)**

![Graph showing RDS\(_{\text{ON}}\) vs. Temperature and V\(_\text{IN}\)](image)

**I\(_\text{ACL}\) vs. Temperature and R\(_\text{SET}\)**

![Graph showing I\(_\text{ACL}\) vs. Temperature and R\(_\text{SET}\)](image)
SLG59H1017V
A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
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I_{ACL} vs. R_{SET} and V_{IN}

I_{OUT} vs. MOSFET IDS and V_{IN}
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A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
V_IN Lockout Select and MOSFET Current Monitor Output

I_OUT vs. Temperature and MOSFET IDS

V_OUT Slew Rate vs. Temperature, V_IN, and C_SLEW
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A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
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\[ T_{\text{Total\_ON}} \text{ vs. } C_{\text{SLEW}} \text{ and } V_{\text{IN}} \]

\[-40^\circ C \leq T_A \leq 85^\circ C\]

\[ V_{\text{IN}} = 24V \]
\[ V_{\text{IN}} = 12V \]
SLG59H1017V

A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
$V_{IN}$ Lockout Select and MOSFET Current Monitor Output

Timing Diagram - Basic Operation including Active Current Limit Protection

- **$V_{IN}$**:
  - HIGH
  - LOW

- **$V_{OUT}$**:
  - HIGH
  - $T_{ON\_Delay}$
  - $I_{ACL}$
  - $I_{DS}$
  - $I_{SCL}$

- **$I_{ACL}$**:
  - Abnormal Step Load Current Event
  - Active Current Limit Operation

- **$T_{FAULT\_LOW}$**:
  - ACL Threshold Triggered

- **$T_{FAULT\_HIGH}$**:
  - Nominal Steady State Operation Resumes
Timing Diagram - Active Current Limit & Thermal Protection Operation

- **V\textsubscript{IN}**
  - HIGH
  - LOW
- **V\textsubscript{OUT}**
  - Abnormal Step Load Current Event
  - Total\textsubscript{ON} Delay
  - Active Current Limit Operation
  - Die temp > T\textsubscript{HERM\textsubscript{ON}}
- **I\textsubscript{DS}**
  - Die temp < T\textsubscript{HERM\textsubscript{OFF}}
- **I\textsubscript{ACL}**
  - Thermal Protection Operation
  - Die temp > T\textsubscript{HERM\textsubscript{ON}}
  - Die temp < T\textsubscript{HERM\textsubscript{OFF}}
  - Nominal Steady State Operation Resumes
- **I\textsubscript{SCL}**
SLG59H1017V

A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
V_IN Lockout Select and MOSFET Current Monitor Output

Timing Diagram - Basic Operation including Active Current + Internal FET SOA Protection

[Diagram showing the timing diagram with various parameters and thresholds, including V_IN, V_OUT, I_DS, I_SCL, FAULT, T_FAULT_LOW, T_FAULT_HIGH, T_ON_DELAY, T_RISE, and SOA threshold.]
SLG59H1017V

A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
VIN Lockout Select and MOSFET Current Monitor Output

SLG59H1017V Application Diagram

Figure 1. Test setup Application Diagram

Typical Turn-on Waveforms

Figure 2. Typical Turn ON operation waveform for \( V_{\text{IN}} = 12 \, \text{V} \), \( C_{\text{SLEW}} = 10 \, \text{nF} \), \( C_{\text{LOAD}} = 10 \, \mu\text{F} \), \( R_{\text{LOAD}} = 100 \, \Omega \)
SLG59H1017V

A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
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Figure 3. Typical Turn ON operation waveform for V_IN = 12 V, C_{SLEW} = 18 nF, C_{LOAD} = 10 μF, R_{LOAD} = 100 Ω

Figure 4. Typical Turn ON operation waveform for V_IN = 24 V, C_{SLEW} = 10 nF, C_{LOAD} = 10 μF, R_{LOAD} = 100 Ω
SLG59H1017V

A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V

$V_{IN}$ Lockout Select and MOSFET Current Monitor Output

**Typical Turn-on Waveforms**

![Figure 5. Typical Turn ON operation waveform for $V_{IN} = 24$ V, $C_{SLEW} = 18$ nF, $C_{LOAD} = 10$ μF, $R_{LOAD} = 100$ Ω](image)

**Typical Turn-off Waveforms**

![Figure 6. Typical Turn OFF operation waveform for $V_{IN} = 12$ V, $C_{SLEW} = 10$ nF, no $C_{LOAD}$, $R_{LOAD} = 100$ Ω](image)
SLG59H1017V
A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
$V_{IN}$ Lockout Select and MOSFET Current Monitor Output

Figure 7. Typical Turn OFF operation waveform for $V_{IN} = 12$ V, $C_{SLEW} = 10$ nF, $C_{LOAD} = 10$ μF, $R_{LOAD} = 100$ Ω

Figure 8. Typical Turn OFF operation waveform for $V_{IN} = 24$ V, $C_{SLEW} = 10$ nF, no $C_{LOAD}$, $R_{LOAD} = 100$ Ω
SLG59H1017V

A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
V_IN Lockout Select and MOSFET Current Monitor Output

Typical ACL Operation Waveforms

Figure 9. Typical Turn OFF operation waveform for V_IN = 24 V, C_SLEW = 10 nF, C_LOAD = 10 μF, R_LOAD = 100 Ω

Figure 10. Typical ACL operation waveform for V_IN = 12 V, C_LOAD = 10 μF, I_ACL = 1 A, R_SET = 91 kΩ
Figure 11. Typical ACL operation waveform for $V_{IN} = 24$ V, $C_{LOAD} = 10 \mu$F, $I_{ACL} = 1$ A, $R_{SET} = 91$ kΩ

Figure 12. Thermally induced SOA shutdown for $V_{IN} = 24$ V, $C_{LOAD} = 10 \mu$F, $R_{SET} = 91$ kΩ, $I_{ACL} = 1$ A, $R_{LOAD} = 20$ Ω,
A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
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Typical FAULT Operation Waveforms

Figure 13. Typical FAULT assertion waveform for $V_{IN} = 12$ V, $C_{LOAD} = 10$ μF, $I_{ACL} = 1$ A, $R_{SET} = 91$ kΩ, switch on 9 Ω load

Figure 14. Typical FAULT de-assertion waveform for $V_{IN} = 12$ V, $C_{LOAD} = 10$ μF, $I_{ACL} = 1$ A, $R_{SET} = 91$ kΩ, switch out 9 Ω load
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A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
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Figure 15. Typical FAULT assertion waveform for V_IN = 24 V, C_LOAD = 10 μF, I_ACL = 1 A, R_SET = 91 kΩ, switch on 18.5 Ω load

Figure 16. Typical FAULT de-assertion waveform for V_IN = 24 V, C_LOAD = 10 μF, I_ACL = 1 A, R_SET = 91 kΩ, switch out 18.5 Ω load
Typical $I_{OUT}$ Response Time Waveforms

Figure 17. Typical $I_{OUT}$ response time waveform for $V_{IN} = 12$ V, $C_{LOAD} = 10$ μF, $R_{LOAD} = 12$ Ω, $C_{IOUT} = 0.18$ nF, $R_{IOUT} = 84.5$ kΩ, Load step 0 A to 1 A

Figure 18. Typical $I_{OUT}$ response time waveform for $V_{IN} = 12$ V, $C_{LOAD} = 10$ μF, $R_{LOAD} = 12$ Ω, $C_{IOUT} = 0.18$ nF, $R_{IOUT} = 84.5$ kΩ, Load step 1 A to 0 A
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A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
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Figure 19. Typical I\textsubscript{OUT} response time waveform for V\textsubscript{IN} = 24 V, C\textsubscript{LOAD} = 10 μF, R\textsubscript{LOAD} = 24 Ω
C\textsubscript{IOUT} = 0.18 nF, R\textsubscript{IOUT} = 84.5 kΩ, Load step 0 A to 1 A

Figure 20. Typical I\textsubscript{OUT} response time waveform for V\textsubscript{IN} = 24 V, C\textsubscript{LOAD} = 10 μF, R\textsubscript{LOAD} = 24 Ω
C\textsubscript{IOUT} = 0.18 nF, R\textsubscript{IOUT} = 84.5 kΩ, Load step 1 A to 0 A
SLG59H1017V

A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
VIN Lockout Select and MOSFET Current Monitor Output

Typical SOA Waveforms

Figure 21. Typical SOA waveform during power up on heavy load for VIN = 12 V, CLOAD = 10 μF, RSET = 30.1 kΩ, RLOAD = 3.5 Ω

Figure 22. Extended typical SOA waveform during power up under heavy load for VIN = 12 V, CLOAD = 10 μF, RSET = 30.1 kΩ, RLOAD = 3.5 Ω
SLG59H1017V

A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
V_IN Lockout Select and MOSFET Current Monitor Output

Figure 23. Typical SOA waveform during power up under heavy load for V_IN = 24 V, C_LOAD = 10 μF, R_SET = 30.1 kΩ, R_LOAD = 12 Ω

Figure 24. Extended typical SOA waveform during power up under heavy load for V_IN = 24 V, C_LOAD = 10 μF, R_SET = 30.1 kΩ, R_LOAD = 12 Ω
A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
$V_{IN}$ Lockout Select and MOSFET Current Monitor Output

Figure 25. Typical non-monotonic $V_{OUT}$ ramping waveform during power up on heavy load for $V_{IN} = 24$ V, $C_{LOAD} = 470 \mu F$, $R_{SET} = 91$ kΩ, $R_{LOAD} = 40$ Ω
Applications Information

High Voltage GreenFET Safe Operating Area Explained

Renesas’s High Voltage GreenFET load switches incorporate a number of internal protection features that prevents them from damaging themselves or any other circuit or subcircuit downstream of them. One particular protection feature is their Safe Operation Area (SOA) protection. SOA protection is automatically activated under overpower and, in some cases, under overcurrent conditions. Overpower SOA is activated if package power dissipation exceeds an internal 10 W threshold and High Voltage GreenFET devices will quickly switch off (open circuit) upon overpower detection and automatically resume (close) nominal operation once overpower condition no longer exists.

One of the possible ways to have an overpower condition trigger SOA protection is when High Voltage GreenFET products are enabled into heavy output resistive loads and/or into large load capacitors. It is under these conditions to follow carefully the “Safe Start-up Loading” guidance in the Applications section of the datasheet. During an overcurrent condition, High Voltage GreenFET devices will try to limit the output current to the level set by the external R\text{SET} resistor. Limiting the output current, however, causes an increased voltage drop across the FET’s channel because the FET’s R\text{DS}_{\text{ON}} increased as well. Since the FET’s R\text{DS}_{\text{ON}} is larger, package power dissipation also increases. If the resultant increase in package power dissipation is greater than or equal to 10 W, internal SOA protection will be triggered and the FET will open circuit (switch off). Every time SOA protection is triggered, all High Voltage GreenFET devices will automatically attempt to resume nominal operation after 160 ms. The automatic retry attempt only allows power-up with SOA at 5 W. This SOA fold back power ensures that the FET survives a short circuit condition. To clear the 5 W SOA fold back, switch the ON pin to “LOW” to power reset SOA to 10 W.

Safe Start-up Condition

SLG59H1017V has built-in protection to prevent over-heating during start-up into a heavy load. Overloading the VOUT pin with a capacitor and a resistor may result in non-monotonic \( V_{\text{OUT}} \) ramping (Figure 25) or repeated restarts (Figure 21 to Figure 24). In general, under light loading on VOUT, \( V_{\text{OUT}} \) ramping can be controlled with \( C_{\text{SLEW}} \) value. The following equation serves as a guide:

\[
C_{\text{SLEW}} = \frac{T_{\text{RISE}}}{V_{\text{IN}}} \times 4.9 \mu\text{A} \times \frac{20}{3}
\]

where

- \( T_{\text{RISE}} \) = Total rise time from 10% \( V_{\text{OUT}} \) to 90% \( V_{\text{OUT}} \)
- \( V_{\text{IN}} \) = Input Voltage
- \( C_{\text{SLEW}} \) = Capacitor value for CAP pin

When capacitor and resistor loading on VOUT during start up, the following tables will ensure \( V_{\text{OUT}} \) ramping is monotonic without triggering internal protection:

<table>
<thead>
<tr>
<th>Slew Rate (V/ms)</th>
<th>( C_{\text{SLEW}} ) (nF(^2))</th>
<th>( C_{\text{LOAD}} ) (µF)</th>
<th>( R_{\text{LOAD}} ) (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>33.3</td>
<td>500</td>
<td>8</td>
</tr>
<tr>
<td>2</td>
<td>16.7</td>
<td>250</td>
<td>8</td>
</tr>
<tr>
<td>3</td>
<td>11.1</td>
<td>160</td>
<td>8</td>
</tr>
<tr>
<td>4</td>
<td>8.3</td>
<td>120</td>
<td>8</td>
</tr>
<tr>
<td>5</td>
<td>6.7</td>
<td>100</td>
<td>8</td>
</tr>
</tbody>
</table>
SLG59H1017V

A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
V_IN Lockout Select and MOSFET Current Monitor Output

<table>
<thead>
<tr>
<th>Safe Start-up Loading for V_IN = 24 V (Monotonic Ramp)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slew Rate (V/ms)</td>
</tr>
<tr>
<td>------------------</td>
</tr>
<tr>
<td>0.5</td>
</tr>
<tr>
<td>1.0</td>
</tr>
<tr>
<td>1.5</td>
</tr>
<tr>
<td>2.0</td>
</tr>
<tr>
<td>2.5</td>
</tr>
</tbody>
</table>

Note 2: Select the closest value tolerance capacitor.

Setting the SLG59H1017V’s Active Current Limit

<table>
<thead>
<tr>
<th>R_{SET} (kΩ)</th>
<th>Active Current Limit (A)^3</th>
</tr>
</thead>
<tbody>
<tr>
<td>91</td>
<td>1</td>
</tr>
<tr>
<td>45</td>
<td>2</td>
</tr>
<tr>
<td>30</td>
<td>3</td>
</tr>
<tr>
<td>20</td>
<td>4.5</td>
</tr>
</tbody>
</table>

Note 3: Active Current Limit accuracy is ±15% over voltage range and over temperature range.

Configuring the SLG59H1017V for 12 V V_IN Lockout Applications

To configure the SLG59H1017V for conditioned 12 V ±10% V_IN applications is simply a matter of connecting the SEL pin to GND as shown in Figure A. For other V_IN lockout window applications, please consult Renesas for additional information.

Figure A.
SLG59H1017V
A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
V_IN Lockout Select and MOSFET Current Monitor Output

24 V V_IN and 12 V V_IN Lockout Window Thresholds

Shown in Figure B and Figure C are the two sets of V_IN overvoltage/undervoltage lockout windows – one for conditioned 24 V ±5% V_IN systems and the second for conditioned 12 V ±10% V_IN systems. To avoid lockout threshold collision with nominal operation, the SLG59H1017V's V_IN(OVLO) min and V_IN(UVLO) max thresholds were set 0.1 V correspondingly higher than the system's nominal V_IN max or lower than the system's V_IN min range.

Figure B.

24 V V_IN ±5%

25.2 V (max) → 28.5 V (max)
27 V (typ)
25.3 V (min)

24 V (nom) → 24 V V_IN

21.6 V (min) → 21.5 V (max)
20.5 V (typ)
19.5 V (min)

24 V V_IN UVLO Band

Figure C.

12 V V_IN ±10%

13.2 V (max) → 14.5 V (max)
13.7 V (typ)
13.3 V (min)

12 V (nom) → 12 V V_IN

10.8 V (min) → 10.7 V (max)
10.2 V (typ)
9.7 V (min)

12 V V_IN UVLO Band

Power Dissipation

The junction temperature of the SLG59H1017V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59H1017V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

\[ PD = R_{DS\, ON} \times I_{DS}^2 \]

where:

- PD = Power dissipation, in Watts (W)
- R_{DS\, ON} = Power MOSFET ON resistance, in Ohms (Ω)
- I_{DS} = Output current, in Amps (A)

and

\[ T_J = PD \times \theta_{JA} + T_A \]

where:

- T_J = Junction temperature, in Celsius degrees (°C)
- \theta_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W)
- T_A = Ambient temperature, in Celsius degrees (°C)
Power Dissipation (continued)

In current-limit mode, the SLG59H1017V’s power dissipation can be calculated by taking into account the voltage drop across the load switch ($V_{IN} - V_{OUT}$) and the magnitude of the output current in current-limit mode ($I_{ACL}$):

\[
PD = (V_{IN} - V_{OUT}) \times I_{ACL} \quad \text{or} \quad PD = (V_{IN} - (R_{LOAD} \times I_{ACL})) \times I_{ACL}
\]

where:

- $PD$ = Power dissipation, in Watts (W)
- $V_{IN}$ = Input Voltage, in Volts (V)
- $R_{LOAD}$ = Load Resistance, in Ohms (Ω)
- $I_{ACL}$ = Output limited current, in Amps (A)
- $V_{OUT} = R_{LOAD} \times I_{ACL}$
SLG59H1017V

A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
VIN Lockout Select and MOSFET Current Monitor Output

Layout Guidelines:

1. Since the VIN and VOUT pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 26, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

2. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_IN and output C_LOAD low-ESR capacitors as close as possible to the SLG59H1017V’s VIN and VOUT pins;

3. The GND pin should be connected to system analog or power ground plane.

4. 2 oz. copper is recommended for high current operation.

SLG59H1017V Evaluation Board:

A High Voltage GreenFET Evaluation Board for SLG59H1017V is designed according to the statements above and is illustrated on Figure 26. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_ON evaluation.

Figure 26. SLG59H1017V Evaluation Board
Basic Test Setup and Connections

1. Set SEL0 to GND;
2. Based on $V_{IN}$ voltage, set SEL1 to GND or 5 V to configure OVLO;
3. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;
4. Turn on Power Supply and set $V_{IN}$ to 12 V or 24 V;
5. Toggle the ON signal High or Low to observe SLG59H1017V operation.

EVB Configuration

1. Set SEL0 to GND;
2. Based on $V_{IN}$ voltage, set SEL1 to GND or 5 V to configure OVLO;
3. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;
4. Turn on Power Supply and set $V_{IN}$ to 12 V or 24 V;
5. Toggle the ON signal High or Low to observe SLG59H1017V operation.
## Package Top Marking System Definition

<table>
<thead>
<tr>
<th>Part Code</th>
<th>Date Code + LOT Code</th>
<th>Assembly + Rev. Code</th>
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</thead>
<tbody>
<tr>
<td>1017V</td>
<td>WWNNN</td>
<td>ARR</td>
</tr>
</tbody>
</table>

1017V - Part ID Field  
WW - Date Code Field\(^1\)  
NNN - Lot Traceability Code Field\(^1\)  
A - Assembly Site Code Field\(^2\)  
RR - Part Revision Code Field\(^2\)

**Note 1:** Each character in code field can be alphanumeric A-Z and 0-9  
**Note 2:** Character in code field can be alphabetic A-Z
SLG59H1017V

A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
V_IN Lockout Select and MOSFET Current Monitor Output

Package Drawing and Dimensions

18 Lead TQFN Package 1.6 x 3 mm (Fused Lead)
JEDEC MO-220, Variation WCEE

Unit: mm

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Min</th>
<th>Nom.</th>
<th>Max</th>
<th>Symbol</th>
<th>Min</th>
<th>Nom.</th>
<th>Max</th>
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<tbody>
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<td>0.55</td>
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<td>b</td>
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<td>0.18</td>
<td>0.23</td>
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<td>2.44</td>
<td>L4</td>
<td>0.13</td>
<td>0.18</td>
<td>0.23</td>
</tr>
</tbody>
</table>
SLG59H1017V
A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V
$V_{\text{IN}}$ Lockout Select and MOSFET Current Monitor Output

SLG59H1017V 18-pin STQFN PCB Landing Pattern

Note: All dimensions shown in micrometers ($\mu$m)
SLG59H1017V

A 13.3 mΩ, 4 A Load Switch with 12 V / 24 V

V_{\text{IN}} Lockout Select and MOSFET Current Monitor Output

Tape and Reel Specifications

<table>
<thead>
<tr>
<th>Package Type</th>
<th># of Pins</th>
<th>Nominal Package Size [mm]</th>
<th>Max Units</th>
<th>Reel &amp; Hub Size [mm]</th>
<th>Leader (min)</th>
<th>Trailer (min)</th>
<th>Tape Width [mm]</th>
<th>Part Pitch [mm]</th>
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</thead>
<tbody>
<tr>
<td>STQFN 18L 1.6x3mm 0.4P FC Green</td>
<td>18</td>
<td>1.6 x 3 x 0.55</td>
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<td>3,000</td>
<td>178 / 60</td>
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</table>

Carrier Tape Drawing and Dimensions

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<thead>
<tr>
<th>Package Type</th>
<th>Pocket BTM Length</th>
<th>Pocket BTM Width</th>
<th>Pocket Depth</th>
<th>Index Hole Pitch</th>
<th>Pocket Pitch</th>
<th>Index Hole Diameter</th>
<th>Index Hole to Tape Edge</th>
<th>Index Hole to Pocket Center</th>
<th>Tape Width</th>
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</thead>
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Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm³ (nominal). More information can be found at www.jedec.org.
### Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Change</th>
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<tr>
<td>2/2/2022</td>
<td>1.04</td>
<td>Updated Company name and logo</td>
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<td>Added SOA Protection Threshold to Features</td>
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<td>Fixed typos</td>
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<td>10/17/2019</td>
<td>1.03</td>
<td>Updated Applications Info SOA Description</td>
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<td>Updated HFET Evaluation Board image</td>
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<td>12/18/2018</td>
<td>1.02</td>
<td>Updated style and formatting</td>
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<td>Updated Charts</td>
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<td>Added Scopeshots</td>
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<td>Added Layout Guidelines</td>
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<td>11/2/2017</td>
<td>1.01</td>
<td>Updated $V_{IN}$ Max and $V_{IN(OVLO)}$ Min</td>
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<td>5/13/2016</td>
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