SLG47115

GreenPAK Programmable Mixed-Signal Matrix with High Voltage Features

The SLG47115 provides a small, low power component for commonly used Mixed-Signal and Full Bridge functions. The user creates their circuit design by programming the one time programmable (OTP) Non-Volatile Memory (NVM) to configure the interconnect logic, the IO Pins, the High Voltage Pins, and the macrocells of the SLG47115.

Configurable PWM macrocells in combination with Special High Voltage outputs will be useful for a motor drive or load drive applications. High Voltage pins allow to design smart level translators or to drive the high voltage high current load.

Features

- Two Power Supply Inputs:
  - 2.5 V (±8 %) to 5.0 V (±10 %) V_{DD}
  - 5.0 V (±10 %) to 24.0 V (±10 %) V_{DD2}
- Two High Voltage High Current Drive GPOs
  - Full Bridge Driver Option
  - Dual/Single Half Bridge Driver Option
  - Slew Rate Modes:
    - Motor Driver Mode
    - Pre-Driver (MOSFET Driver) Mode
  - High Drive GPOs with Sleep Function
  - Low $R_{DS(ON)}$ High-side + Low-side resistance = 0.5 Ω typical
  - 3 A Peak, 1.5 A RMS per Full Bridge[1]
  - Current up to 3 A Peak, 1.5 A RMS per GPO/Half Bridge and up to 6 A Peak, 3 A RMS for two HV GPOs Connected in Parallel[1]
  - Integrated Over Current/Short Circuit/Undervoltage-Lockout Protections
  - SENSE Input that is connected to the Current Comparator for Current Control
  - Fault Signal Indicator (OCP/UVLO/TSD/)
- Differential Amplifier with Integrator and Comparator for Motor Speed Control Function
- Current Sense Comparator with Dynamical Vref Mode
- Two High-Speed General Purpose ACMPs
  - Modes: UVLO, OCP, TSD, Voltage Monitor, Current Monitor
- One Voltage Reference (Vref) Output
- Five Multi-Function Macrocells
  - Four Selectable DFF/LATCH/3-bit LUTs + 8-bit Delay/Counters
  - One Selectable DFF/LATCH/4-bit LUT + 16-bit Delay/Counter
- Twelve Combination Function Macrocells
  - Three Selectable DFF/LATCH or 2-bit LUTs
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Six Selectable DFF/LATCH or 3-bit LUTs
  - One Selectable Pipe Delay or Ripple Counter or 3-bit LUT
  - One Selectable DFF/LATCH or 4-bit LUT
- Two PWM Macrocells
  - Flexible 8-bit/7-bit PWM Mode with the Duty Cycle Control
  - 16 Preset Duty Cycle Registers Switching Mode for PWM Sine or Other Waveforms[2]
- Serial Communications
  - I^2C Protocol Interface
- Programmable Delay with Edge Detector Output
- Additional Logic Function – One Deglitch Filter with Edge Detectors
- Two Oscillators (OSC)
  - 2.048 kHz Oscillator
  - 25 MHz Oscillator
- Analog Temperature Sensor with ACMP Connected Output
- POR
- One Time Programmable Memory
- Operating Temperature Range: -40 °C to 85 °C
- RoHS Compliant/Halogen-Free
- 20-pin STQFN: 2 mm x 3 mm x 0.55 mm, 0.4 mm pitch

Applications

- Smart Locks
- Personal Computers and Servers
- Consumer Electronics
- Motor Drivers
- Toys
- HV MOSFET Drivers
- Video Security Cameras
- LED Matrix Dimmers

Note 1: Power dissipation and thermal limits must be observed. See Section 3.3 Recommended Operating Conditions.
Note 2: For all PWM features see Section 13. Pulse Width Modulation Macrocell.

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1. Block Diagram

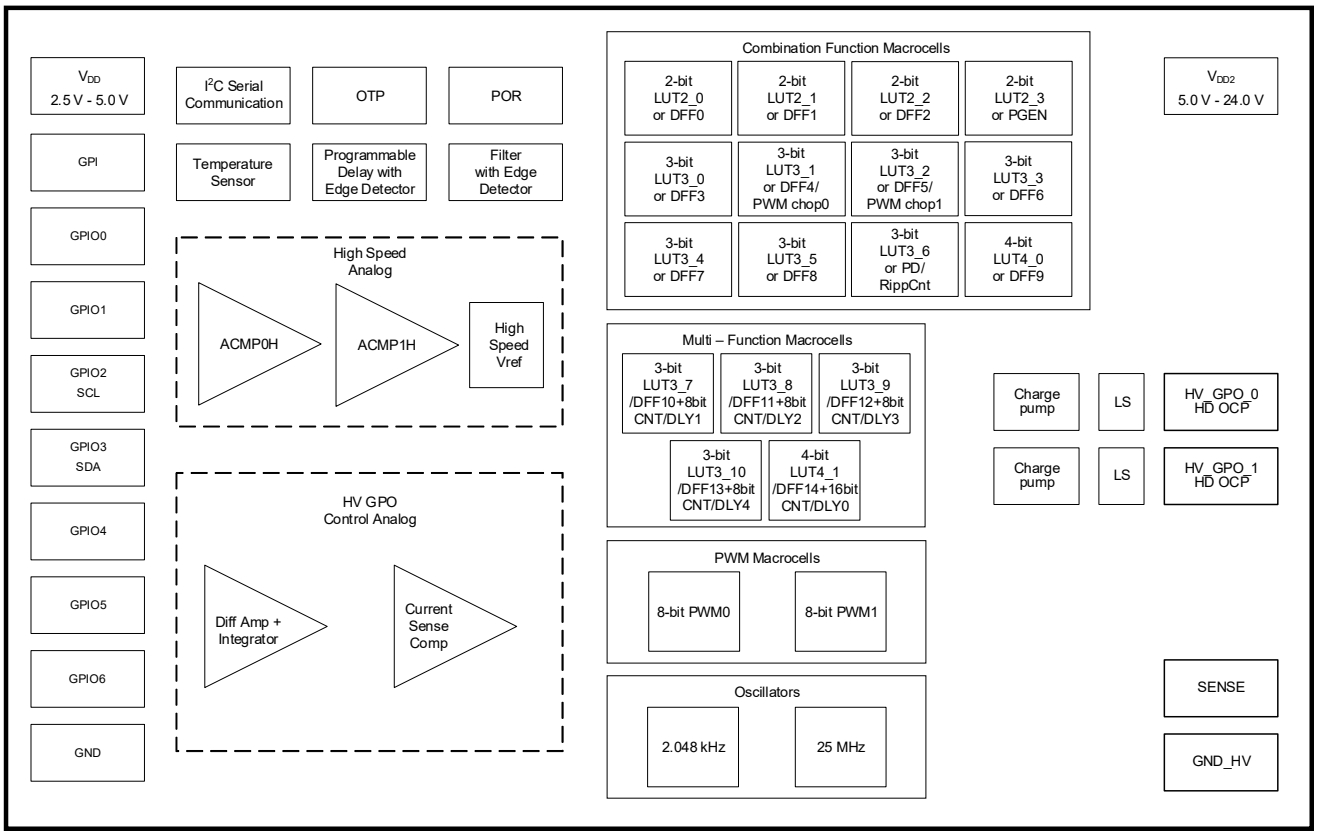


Figure 1. Block Diagram

2. Pin Information

2.1 Pin Assignments

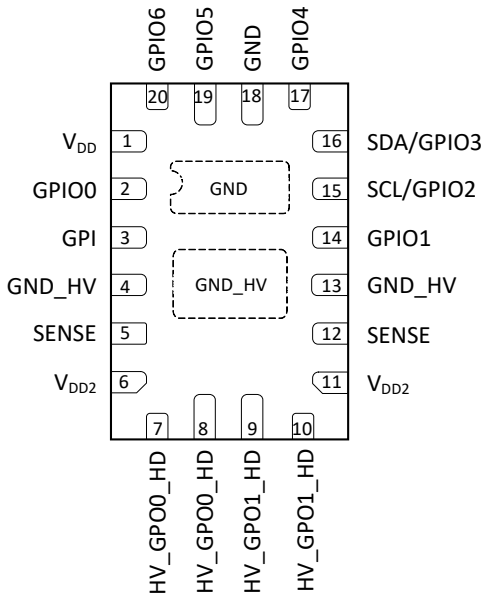


Figure 2. Pin Assignments - STQFN - 20L

2.2 Pin Descriptions

Table 1. Pin Description

Pin Number	Pin Name	Description
1	V_{DD}	Power Supply 2.5 V – 5.0 V
2	GPIO0	Matrix OE GPIO, Vref OUT, Diff Amp Vset Input, TS _OUT
3	GPI	GPI, EXT_Vref0, SLA_0
4	GND_HV	Analog Ground
5	SENSE	Winding Sense, relate to HV_GPO0_HD, HV_GPO1_HD
6	V_{DD2}	High Voltage Power Supply 5.0 V - 24.0 V
7	HV_GPO0_HD	HV_GPO_HD
8	HV_GPO0_HD	HV_GPO_HD
9	HV_GPO1_HD	HV_GP1_HD
10	HV_GPO1_HD	HV_GP1_HD
11	V_{DD2}	High Voltage Power Supply 5.0 V - 24.0 V
12	SENSE	Winding Sense, relate to HV_GPO0_HD/HV_GPO1_HD
13	GND_HV	Analog Ground
14	GPIO1	Matrix OE GPIO, SLA_1, EXT_CLK for OSC0 or Current Sense CMP EXT_Vref
15	SCL/GPIO2	SCL, GPIO
16	SDA/GPIO3	SDA, GPIO

Table 1. Pin Description (Cont.)

Pin Number	Pin Name	Description
17	GPIO4	Matrix OE GPIO, EXT_Vref1, SLA_2, EXT_CLK for OSC1
18	GND	General Ground
19	GPIO5	Matrix OE GPIO, ACMP0_H
20	GPIO6	Matrix OE GPIO, SLA_3, ACMP1_H

Table 2. Pin Type Definitions

Pin type	Definition
V_{DD}	Power Supply
GPIO	General Purpose Input/Output
GPI	General Purpose Input
HV_GPO_HD	High Voltage General Purpose Output High Current Drive
SCL	I^2C Serial Clock Input
SDA	I^2C Serial Data Input/Output
GND	General Ground
GND_HV	Analog Ground
SENSE	Current Sense Pin
V_{DD2}	High Voltage Power Supply

3. Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter		Description	Condition	Min	Max	Unit
Supply voltage on V_{DD} relative to GND		--	--	-0.3	7.0	V
Supply voltage on V_{DD2} relative to GND		--	--	-0.3	32	V
DC input voltage		--	--	GND - 0.5 V	V_{DD} + 0.5 V	V
Maximum V_{DD} average or DC current		(Through V_{DD} or GND pin) for V_{DD} group	--	--	120	mA
Maximum V_{DD2} or sense average or DC current		(Through V_{DD2} or SENSE pin)	--	--	2000	mA
Maximum average or DC current (V_{DD} power supply)	push-pull 1x	Through V_{DD} group pins	T_J = -40 °C to 85 °C	--	11	mA
	push-pull 2x			--	16	
	OD 1x			--	11	
	OD 2x			--	21	
Maximum average or DC current (V_{DD} power supply)	push-pull 1x	Through V_{DD} group pins	T_J = -40 °C to 150 °C	--	3.8	mA
	push-pull 2x			--	7.6	
	OD 1x			--	3.8	
	OD 2x			--	7.6	
Maximum average or DC current (V_{DD2} power supply)	push-pull/ half bridge	Through V_{DD2} High Current group pins	--	--	1500	mA
Maximum pulsed current sink/sourced per HV HD pin		Pulse width ≤ 0.5 ms; duty cycle ≤ 2 %	--	--	Internally limited by OCP	mA
Current at input pin		Through V_{DD} group pin	--	-0.1	1.0	mA
Input leakage current (absolute value)		--	--	--	1000	nA
Storage temperature range		--	--	-65	150	°C
Junction temperature		--	--	--	150	°C
Moisture sensitivity level		--	--	1		

3.2 Electrostatic Discharge Ratings

Table 4. Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD protection (human body model)	4000	--	V
ESD protection (charged device model)	1300	--	V

3.3 Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage	--	2.3	5.0	5.5	V
V_{DD2}	High supply voltage	--	4.5	24.0	26.4	V
T_A	Operating ambient temperature	--	-40	25	85	°C
T_J	Junction temperature range	--	-40	--	150	°C
C_{VDD}	Capacitor value at V_{DD}	--	--	0.1	--	µF
V_{AIH}	Analog input common mode range	Allowable input voltage at analog pins	0	--	V_{DD} or V_{DD2}[1]	V

[1] V_{DD} for GPI, GPIO3, IO13 and V_{DD2} for HV GPO0 and HV GPO1.

3.4 Thermal Information

Table 6. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
θ_{JA}	Thermal resistance	4L JEDEC PCB	--	--	65	°C/W
θ_{JA}	Thermal resistance	4L JEDEC PCB with a thermal vias that connect thermal pad through all layers of the PCB	--	--	56	°C/W
$\theta_{JC(top)}$	Junction-to-case (top) thermal resistance	--	--	38.40	--	°C/W
θ_{JB}	Junction-to-board thermal resistance	--	--	34.88	--	°C/W
$\Psi_{JC(top)}$	Junction-to-case (top) characterization parameter	--	--	13.46	--	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	--	--	27.24	--	°C/W

3.5 Electrical Specifications

Table 7. ES at T_A = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	High-level input voltage for V_{DD} group[3]	Logic input[1]	0.7x V_{DD}	--	V_{DD}+ 0.3	V
		Logic input with Schmitt trigger	0.8x V_{DD}	--	V_{DD}+ 0.3	V
		Low-level logic input[1]	1.3	--	V_{DD}+ 0.3	V
V_{IL}	Low-level input voltage for V_{DD} group[3]	Logic input[1]	GND- 0.3	--	0.3x V_{DD}	V
		Logic Input with Schmitt trigger	GND- 0.3	--	0.2x V_{DD}	V
		Low-level logic input[1]	GND- 0.3	--	0.5	V
V_O	Maximal voltage applied to any pin in High impedance state	for V_{DD} group	--	--	V_{DD}+ 0.3	V
V_{O2}		for V_{DD2} group	--	--	V_{DD2}+ 0.3	V
V_{OH}	High-level output voltage for V_{DD} group T_J = -40 °C to 85 °C	push-pull, 1x Drive, V_{DD} = 2.5 V ± 8 %, I_{OH} = 1 mA	2.1	--	--	V
		push-pull, 1x Drive, V_{DD} = 3.3 V ± 10 %, I_{OH} = 3 mA	2.5	--	--	V
		push-pull, 1x Drive, V_{DD} = 5 V ± 10 %, I_{OH} = 5 mA	4.0	--	--	V
		push-pull, 2x Drive, V_{DD} = 2.5 V ± 8 %, I_{OH} = 1 mA	2.1	--	--	V
		push-pull, 2x Drive, V_{DD} = 3.3 V ± 10 %, I_{OH} = 3 mA	2.7	--	--	V
		push-pull, 2x Drive, V_{DD} = 5 V ± 10 %, I_{OH} = 5 mA	4.1	--	--	V
	High-level output voltage for V_{DD} group T_J = -40 °C to 150 °C	push-pull, 1x Drive, V_{DD} = 2.5 V ± 8 %, I_{OH} = 1 mA	2.1	--	--	V
		push-pull, 1x Drive, V_{DD} = 3.3 V ± 10 %, I_{OH} = 3 mA	2.5	--	--	V
		push-pull, 1x Drive, V_{DD} = 5 V ± 10 %, I_{OH} = 5 mA	3.9	--	--	V
		push-pull, 2x Drive, V_{DD} = 2.5 V ± 8 %, I_{OH} = 1 mA	2.1	--	--	V
		push-pull, 2x Drive, V_{DD} = 3.3 V ± 10 %, I_{OH} = 3 mA	2.7	--	--	V
		push-pull, 2x Drive, V_{DD} = 5 V ± 10 %, I_{OH} = 5 mA	4.1	--	--	V

Table 7. ES at T_A = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Cont.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage for V_{DD} group T_J = -40 °C to 85 °C	push-pull, 1x Drive, V_{DD} = 2.5 V ± 8 %, I_{OL}= 1 mA	--	--	0.1	V
		push-pull, 1x Drive, V_{DD} = 3.3 V ± 10 %, I_{OL} = 3 mA	--	--	0.2	V
		push-pull, 1x Drive, V_{DD} = 5 V ± 10 %, I_{OL}= 5 mA	--	--	0.2	V
		push-pull, 2x Drive, V_{DD} = 2.5 V ± 8 %, I_{OL} = 1 mA	--	--	0.0	V
		push-pull, 2x Drive, V_{DD} = 3.3 V ± 10 %, I_{OL}= 3 mA	--	--	0.1	V
		push-pull, 2x Drive, V_{DD} = 5 V ± 10 %, I_{OL} = 5 mA	--	--	0.1	V
		NMOS OD, 1x Drive, V_{DD} = 2.5 V ± 8 %, I_{OL} = 1 mA	--	--	0.030	V
		NMOS OD, 1x Drive, V_{DD} = 3.3 V ± 10 %, I_{OL} = 3 mA	--	--	0.068	V
		NMOS OD, 1x Drive, V_{DD} = 5 V ± 10 %, I_{OL} = 5 mA	--	--	0.083	V
		NMOS OD, 2x Drive, V_{DD} = 2.5 V ± 8 %, I_{OL} = 1 mA	--	--	0.014	V
		NMOS OD, 2x Drive, V_{DD} = 3.3 V ± 10 %, I_{OL} = 3 mA	--	--	0.035	V
		NMOS OD, 2x Drive, V_{DD} = 5 V ± 10 %, I_{OL} = 5 mA	--	--	0.083	V

Table 7. ES at T_A = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Cont.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage for V_{DD} group T_J = -40 °C to 150 °C	push-pull, 1x Drive, V_{DD} = 2.5 V ± 8 %, I_{OL}= 1 mA	--	--	0.1	V
		push-pull, 1x Drive, V_{DD} = 3.3 V ± 10 %, I_{OL} = 3 mA	--	--	0.2	V
		push-pull, 1x Drive, V_{DD} = 5 V ± 10 %, I_{OL}= 5 mA	--	--	0.3	V
		push-pull, 2x Drive, V_{DD} = 2.5 V ± 8 %, I_{OL} = 1 mA	--	--	0.0	V
		push-pull, 2x Drive, V_{DD} = 3.3 V ± 10 %, I_{OL}= 3 mA	--	--	0.1	V
		push-pull, 2x Drive, V_{DD} = 5 V ± 10 %, I_{OL} = 5 mA	--	--	0.1	V
		NMOS OD, 1x Drive, V_{DD} = 2.5 V ± 8 %, I_{OL} = 1 mA	--	--	0.035	V
		NMOS OD, 1x Drive, V_{DD} = 3.3 V ± 10 %, I_{OL} = 3 mA	--	--	0.082	V
		NMOS OD, 1x Drive, V_{DD} = 5 V ± 10 %, I_{OL} = 5 mA	--	--	0.100	V
		NMOS OD, 2x Drive, V_{DD} = 2.5 V ± 8 %, I_{OL} = 1 mA	--	--	0.017	V
		NMOS OD, 2x Drive, V_{DD} = 3.3 V ± 10 %, I_{OL} = 3 mA	--	--	0.042	V
		NMOS OD, 2x Drive, V_{DD} = 5 V ± 10 %, I_{OL} = 5 mA	--	--	0.052	V
V_{OH2}	High-level output voltage for V_{DD2} High current group	push-pull, V_{DD2} = 5 V ± 10 %, I_{OH2} = 10 mA	4.5	--	--	V
		push-pull, V_{DD2} = 9 V ± 10 %, I_{OH2} = 10 mA	8.1	--	--	V
		push-pull, V_{DD2} = 12 V ± 10 %, I_{OH2} = 10 mA	10.8	--	--	V
		push-pull, V_{DD2} = 18V ± 10 %, I_{OH2} = 10 mA	16.2	--	--	V
		push-pull, V_{DD2} = 24 V ± 10 %, I_{OH2} = 10 mA	21.6	--	--	V

Table 7. ES at T_A = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Cont.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OL2}	Low-level output voltage for V_{DD2} High current group	push-pull, V_{DD2} = 5 V ± 10 %, I_{OL2} = 10 mA	--	--	0.004	V
		push-pull, V_{DD2} = 9 V ± 10 %, I_{OL2} = 10 mA	--	--	0.004	V
		push-pull, V_{DD2} = 12 V ± 10 %, I_{OL2} = 10 mA	--	--	0.004	V
		push-pull, V_{DD2} = 18V ± 10 %, I_{OH2} = 10 mA	--	--	0.004	V
		push-pull, V_{DD2} = 24 V ± 10 %, I_{OH2} = 10 mA	--	--	0.004	V
I_{OH}	High-level output pulse current[2] Voltage for V_{DD} group, T_J = -40 °C to 85 °C	push-pull, 1x Drive, V_{DD} = 2.5 V ± 8 %, V_{OH} = V_{DD} - 0.2	1.4	--	--	mA
		push-pull, 1x Drive, V_{DD} = 3.3 V ± 10 %, V_{OH} = 2.4 V	4.8	--	--	mA
		push-pull, 1x Drive, V_{DD} = 5 V ± 10 %, V_{OH} = 2.4 V	18.6	--	--	mA
		push-pull, 2x Drive, V_{DD} = 2.5 V ± 8 %, V_{OH} = V_{DD} - 0.2	2.9	--	--	mA
		push-pull, 2x Drive, V_{DD} = 3.3 V ± 10 %, V_{OH} = 2.4 V	9.6	--	--	mA
		push-pull, 2x Drive, V_{DD} = 5 V ± 10 %, V_{OH} = 2.4 V	36.8	--	--	mA
	High-level output pulse current[2] Voltage for V_{DD} group, T_J = -40 °C to 150 °C	push-pull, 1x Drive, V_{DD} = 2.5 V ± 8 %, V_{OH} = V_{DD} - 0.2	1.3	--	--	mA
		push-pull, 1x Drive, V_{DD} = 3.3 V ± 10 %, V_{OH} = 2.4 V	4.4	--	--	mA
		push-pull, 1x Drive, V_{DD} = 5 V ± 10 %, V_{OH} = 2.4 V	16.7	--	--	mA
		push-pull, 2x Drive, V_{DD} = 2.5 V ± 8 %, V_{OH} = V_{DD} - 0.2	2.5	--	--	mA
		push-pull, 2x Drive, V_{DD} = 3.3 V ± 10 %, V_{OH} = 2.4 V	8.6	--	--	mA
		push-pull, 2x Drive, V_{DD} = 5 V ± 10 %, V_{OH} = 2.4 V	33.0	--	--	mA

Table 7. ES at T_A = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Cont.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OL}	Low-level output pulse current[2] Voltage for V_{DD} group, T_J = -40 °C to 85 °C	push-pull, 1x Drive, V_{DD} = 2.5 V ± 8 %, V_{OL} = 0.15 V	1.9	--	--	mA
		push-pull, 1x Drive, V_{DD} = 3.3 V ± 10 %, V_{OL} = 0.4 V	6.2	--	--	mA
		push-pull, 1x Drive, V_{DD} = 5.0 V ± 10 %, V_{OL} = 0.4 V	9.0	--	--	mA
		push-pull, 2x Drive, V_{DD} = 2.5 V ± 8 %, V_{OL} = 0.15 V	3.8	--	--	mA
		push-pull, 2x Drive, V_{DD} = 3.3 V ± 10 %, V_{OL} = 0.4 V	12.3	--	--	mA
		push-pull, 2x Drive, V_{DD} = 5.0 V ± 10 %, V_{OL} = 0.4 V	17.7	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 2.5 V ± 8 %, V_{OL} = 0.15 V	4.7	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 3.3 V ± 10%, V_{OL} = 0.4 V	15.2	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 5.0 V ± 10%, V_{OL} = 0.4 V	21.8	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 2.5 V ± 8 %, V_{OL} = 0.15 V	9.2	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 3.3 V ± 10%, V_{OL} = 0.4 V	29.5	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 5.0 V ± 10%, V_{OL} = 0.4 V	41.9	--	--	mA

Table 7. ES at T_A = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Cont.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OL}	Low-level output pulse current[2] Voltage for V_{DD} group, T_J = -40 °C to 150 °C	push-pull, 1x Drive, V_{DD} = 2.5 V ± 8 %, V_{OL} = 0.15 V	1.6	--	--	mA
		push-pull, 1x Drive, V_{DD} = 3.3 V ± 10%, V_{OL} = 0.4 V	5.2	--	--	mA
		push-pull, 1x Drive, V_{DD} = 5.0 V ± 10%, V_{OL} = 0.4 V	7.5	--	--	mA
		push-pull, 2x Drive, V_{DD} = 2.5 V ± 8 %, V_{OL} = 0.15 V	3.2	--	--	mA
		push-pull, 2x Drive, V_{DD} = 3.3 V ± 10%, V_{OL} = 0.4 V	10.3	--	--	mA
		push-pull, 2x Drive, V_{DD} = 5.0 V ± 10%, V_{OL} = 0.4 V	14.8	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 2.5 V ± 8 %, V_{OL} = 0.15 V	4.0	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 3.3 V ± 10%, V_{OL} = 0.4 V	12.8	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 5.0 V ± 10%, V_{OL} = 0.4 V	18.3	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 2.5 V ± 8 %, V_{OL} = 0.15 V	7.8	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 3.3 V ± 10%, V_{OL} = 0.4 V	24.9	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 5.0 V ± 10%, V_{OL} = 0.4 V	35.0	--	--	mA
I_{sleep}	All macrocells are in Sleep mode including charge pumps	For V_{DD2} <= 5.0V UVLO disabled	--	--	117	nA
PON_{THR}	Power-on threshold	V_{DD} level required to start up the chip, T_J = -40 °C to 150 °C	1.80	1.98	2.20	V
$POFF_{THR}$	Power-off threshold	V_{DD} level required to switch off the chip, T_J = -40 °C to 150 °C	1.30	1.55	1.80	V
R_{PULL}	Pull-up or pull-down resistance T_J = -40 °C to 85°C	1 M for pull-up: V_{IN} = GND; for pull-down: V_{IN} = DV_{DD}	--	1	--	MΩ
		100 k for pull-up: V_{IN} = GND; for pull-down: V_{IN} = DV_{DD}	--	100	--	kΩ
		10 k for pull-up: V_{IN} = GND; for pull-down: V_{IN} = DV_{DD}	--	10	--	kΩ
	Pull-up or pull-down resistance T_J = -40 °C to 150 °C	1 M for pull-up: V_{IN} = GND; for pull-down: V_{IN} = DV_{DD}	--	1	--	MΩ
		100 k for pull-up: V_{IN} = GND; for pull-down: V_{IN} = DV_{DD}	--	100	--	kΩ
		10 k for pull-up: V_{IN} = GND; for pull-down: V_{IN} = DV_{DD}	--	10	--	kΩ

Table 7. ES at T_A = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Cont.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_{IN}	Input capacitance	--	--	2.46	--	pF

[1] No hysteresis.
[2] DC or average current through any pin should not exceed value given in Absolute maximum conditions.
[3] ESD resistor should be taken into consideration when using pull-up/pull-down resistors. It may affect V_{IH} and V_{IL}. See sections 6.6 ESD Protection to 6.9 Matrix OE IO Structure (VDD Group).

3.6 I²C Pins Electrical Specifications

Table 8. ES of the I²C Pins for Digital Input Mode at T_A = -40 °C to +150 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Condition	Fast-mode		Fast-mode plus		Unit
			Min	Max	Min	Max	
V_{IL}	Low-level input voltage	--	-0.5	0.3xV_{DD}	-0.5	0.3xV_{DD}	V
V_{IH}	High-level input voltage	--	0.7xV_{DD}	5.5	0.7xV_{DD}	5.5	V
V_{HYS}	Hysteresis of Schmitt trigger inputs	--	0.05xV_{DD}	--	0.05xV_{DD}	--	V
V_{OL1}	Low-level output voltage 1	(Open-drain) at 3 mA sink current V_{DD} > 2 V	0	0.4	0	0.4	V
V_{OL2}	Low-level output voltage 2	(Open-drain) at 2 mA sink current V_{DD} ≤ 2 V	0	0.2xV_{DD}	0	0.2xV_{DD}	V
I_{OL}	Low-level output current	V_{OL} = 0.4 V	3	--	20	--	mA
		V_{OL} = 0.6 V	6	--	--	--	mA
t_{of}	Output fall time from V_{IHmin} to V_{ILmax} [1]	--	14x (V_{DD}/5.5 V)	250	14x (V_{DD}/5.5 V)	120	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	--	0	50	0	50	ns
I_i	Input current each IO pin	0.1xV_{DD} < V_I < 0.9xV_{DDmax}	-10	+10	-10	+10	µA
C_i	Capacitance for each IO pin	--	--	10	--	10	pF

[1] Does not meet standard I²C specifications: t_{of} = 20x(V_{DD}/5.5 V) (min).
[2] For Fast-mode Plus SDA pin must be configured as 3.2x open-drain, see register [837] in Section 23. Register Definitions.

Table 9. ES of the I²C Pins for Low-Level Input Mode at T_A = -40°C to +150°C, V_{DD} = 2.3V to 5.5V Unless Otherwise Noted

Symbol	Parameter	Condition	Fast-mode		Unit
			Min	Max	
V_{IL}	Low-level input voltage	--	-0.5	0.5	V
V_{IH}	High-level input voltage	--	1.2	5.5	V
V_{HYS}	Hysteresis of Schmitt trigger inputs	--	0.05xV_{DD}	--	V
V_{OL1}	Low-level output voltage 1	(open-drain) at 3 mA sink current V_{DD} > 2 V	0	0.4	V
V_{OL2}	Low-level output voltage 2	(open-drain) at 2 mA sink current V_{DD} ≤ 2 V	0	0.2xV_{DD}	V
I_{OL}	Low-level output current	V_{OL} = 0.4 V	3	--	mA
		V_{OL} = 0.6 V	6	--	mA
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}[1]	--	14x (V_{DD}/5.5 V)	250	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	--	0	50	ns
I_i	Input current each IO pin	0.1xV_{DD} < V_I < 0.9xV_{DDmax}	-10	+10	µA
C_i	Capacitance for each IO pin	--	--	10	pF

[1] Does not meet standard I²C specifications: t_{of} = 20x(V_{DD}/5.5 V) (min).

Table 10. I²C Pins Timing Specifications, DI Mode, T_A = -40 °C to +150 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Condition	Speed						Unit
			400 kHz			1 MHz			
			Min	Typ	Max	Min	Typ	Max	
F_{SCL}	Clock frequency, SCL	--	--	--	400	--	--	1000	kHz
t_{LOW}	Clock pulse width Low	--	1300	--	--	500	--	--	ns
t_{HIGH}	Clock pulse width High	--	600	--	--	260	--	--	ns
t_I	Input filter spike suppression (SCL, SDA)	--	--	--	50	--	--	50	ns
t_{AA}	Clock Low to Data OUT Valid	--	--	--	900	--	--	450	ns
t_{BUF}	Bus free time between stop and start	--	1300	--	--	500	--	--	ns
t_{HD_STA}	Start hold time	--	600	--	--	260	--	--	ns
t_{SU_STA}	Start set-up time	--	600	--	--	260	--	--	ns
t_{HD_DAT}	Data hold time	--	0	--	--	0	--	--	ns
t_{SU_DAT}	Data set-up time	--	100	--	--	50	--	--	ns
t_R	Inputs rise time	--	--	--	300	--	--	120	ns
t_F	Inputs fall time	--	--	--	300	--	--	120	ns

Table 10. I²C Pins Timing Specifications, DI Mode, T_A = -40 °C to +150 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Condition	Speed						Unit
			400 kHz			1 MHz			
			Min	Typ	Max	Min	Typ	Max	
t_{SU_STO}	Stop set-up time	--	600	--	--	260	--	--	ns
t_{DH}	Data OUT hold time	--	50	--	--	50	--	--	ns
[1] Please follow official I²C spec UM10204.									

Table 11. I²C Pins Timing Specifications, DILV Mode, T_A = -40 °C to +150 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Condition	Speed			Unit
			400 kHz			
			Min	Typ	Max	
F_{SCL}	Clock frequency, SCL	--	--	--	400	kHz
t_{LOW}	Clock pulse width Low	--	1300	--	--	ns
t_{HIGH}	Clock pulse width High	--	600	--	--	ns
t_I	Input filter spike suppression (SCL, SDA)	--	--	--	50	ns
t_{AA}	Clock Low to Data OUT Valid	--	--	--	900	ns
t_{BUF}	Bus free time between stop and start	--	1300	--	--	ns
t_{HD_STA}	Start hold time	--	600	--	--	ns
t_{SU_STA}	Start set-up time	--	600	--	--	ns
t_{HD_DAT}	Data hold time[1]	--	327	--	--	ns
t_{SU_DAT}	Data set-up time[1]	--	443	--	--	ns
t_R	Inputs rise time	--	--	--	300	ns
t_F	Inputs fall time	--	--	--	300	ns
t_{SU_STO}	Stop set-up time	--	600	--	--	ns
t_{DH}	Data OUT hold time	--	50	--	--	ns
[1] Does not meet standard I²C specifications: t_{HD_DAT} = 0 ns (min), t_{SU_DAT} = 100 ns (min) for Fast-mode. **[2]** Please follow official I²C spec UM10204. **[3]** When SCL Input is in Low-level Logic mode max frequency is 400 kHz.									

3.7 Macrocells Current Consumption

Table 12. Typical Current Estimated for Each Macrocell at T_A = 25 °C

Symbol	Parameter	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
I_{DD}	Current	Chip quiescent (Pdet + OTP st-by) [1]	0.038	0.040	0.047	µA
		Chip quiescent and LPBG (LPBG + Pdet + OTP st-by + I^2C en + leakages) [1]	0.57	0.59	0.59	µA
		Vref (LPBG + Vref_mux + Vref_OUT_BUF)	21.57	21.65	22.08	µA
		OSC1 25 MHz, pre-divider = 1	62.37	79.34	126.74	µA
		OSC1 25 MHz, pre-divider = 2	47.41	59.26	94.93	µA
		OSC1 25 MHz, pre-divider = 4	40.14	49.41	79.02	µA
		OSC1 25 MHz, pre-divider = 8	36.28	44.22	70.81	µA
		OSC1 25 MHz, pre-divider = 12	35.21	42.76	68.41	µA
		OSC0 2.048 kHz, pre-divider = 1	0.35	0.35	0.37	µA
		OSC0 2.048 kHz, pre-divider = 4	0.34	0.35	0.37	µA
		OSC0 2.048 kHz, pre-divider = 8	0.34	0.35	0.37	µA
		IO with 1x push-pull + 4 pF (2.048 kHz)	0.13	0.16	0.22	µA
		Temperature sensor (LPBG + Vref_mux + Vref_OUT_BUF + I_TS)	23.0	22.0	23.0	µA
		One ACMPxH (includes internal Vref)[2]	36.1	36.5	37.8	µA
		One ACMPxH (includes external Vref)[2]	21.5	21.9	23.2	µA
		Two ACMPxH (includes internal Vref)[2]	56.8	57.6	59.9	µA
		Two ACMPxH (includes external Vref)[2]	38.1	39.2	42.5	µA
		Any Half Bridge, V_{DD2} = 5 V	156.4	184.0	257.5	µA
		Both Half Bridges, V_{DD2} = 5 V	214.9	243.6	320.1	µA
		Both Half Bridges + Integrator + PWM + OSC1, V_{DD2} = 5 V	497.7	615.5	904.1	µA
		One Half Bridge + CCMP (any Vref, any gain), V_{DD2} = 5 V	196.1	223.9	297.9	µA
		Both Half Bridges + CCMP (any Vref, any gain), V_{DD2} = 5 V	254.6	283.4	360.5	µA

Table 12. Typical Current Estimated for Each Macrocell at T_A = 25 °C (Cont.)

Symbol	Parameter	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
I_{DD2}	Current	Any Half Bridge, V_{DD2} = 5 V	113.9	88.7	75.5	µA
		Both Half Bridges, V_{DD2} = 5 V	151.3	126.4	114.0	µA
		Both Half Bridges + Integrator + PWM + OSC1, V_{DD2} = 5 V	191.2	192.1	195.6	µA
		One Half Bridge + CCMP (any Vref, any gain), V_{DD2} = 5 V	74.2	74.5	75.5	µA
		Both Half Bridges +CCMP (any Vref, any gain), V_{DD2} = 5 V	111.3	112.0	114.0	µA

[1] Chip Quiescent current values in the table represent the typical value, contact your sales representative if your application requires more detailed information.
[2] Numbers in this table for ACMPx are averaged from different Vref since different Vref has different current.

3.8 HV Output Electrical Specification

Table 13. HV Output Electrical Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Rise time HV OUT in Motor Driver Mode	V_{DD2} = 5 V, 16 Ω to GND, 10 % to 90 % V_{DD2}, T_J = -40 °C to 150 °C	56	107	168	ns
	Rise time HV OUT in Pre-Driver Mode	V_{DD2} = 5 V, 16 Ω to GND, 10 % to 90 % V_{DD2}, T_J = -40 °C to 150 °C	9	16	23	ns
t_F	Fall time HV OUT in Motor Driver Mode	V_{DD2} = 5 V, 16 Ω to GND, 90 % to 10 % V_{DD2}, T_J = -40 °C to 150 °C	57	129	216	ns
	Fall time HV OUT in Pre-Driver Mode	V_{DD2} = 5 V, 16 Ω to GND, 90 % to 10 % V_{DD2}, T_J = -40 °C to 150 °C	11	15	20	ns
t_{DEAD}	Dead band time of HV_GPOx_HD in Motor Driver Mode	V_{DD2} = 4.5 V, T_J = -40 °C to 150 °C	--	91	--	ns
		V_{DD2} = 12 V, T_J = -40 °C to 150 °C	--	85	--	ns
		V_{DD2} = 26.4 V, T_J = -40 °C to 150 °C	--	121	--	ns
t_{DEAD}	Dead band time of HV_GPOx_HD in Pre-Driver Mode	V_{DD2} = 4.5 V, T_J = -40 °C to 150 °C	--	39	--	ns
		V_{DD2} = 12 V, T_J = -40 °C to 150 °C	--	29	--	ns
		V_{DD2} = 26.4 V, T_J = -40 °C to 150 °C	--	34	--	ns
PWM_t_{DEAD}	Dead band time, generated by PWM block	Configured in PWM block	0; 1·T_{clk}; 2·T_{clk}; 3·T_{clk};			Clk time

Table 13. HV Output Electrical Specification (Cont.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$R_{DS(ON)}$	HS FET on resistance (SENSE, GND_HV and GND Pins are connected together)	V_{DD2} = 4.5 V to 5.5 V, I_o = 500 mA, T_J = 25 ºC	--	240	--	mΩ
		V_{DD2} = 4.5 V to 5.5 V, I_o = 500 mA, T_J = 150 ºC	--	276	336	mΩ
		V_{DD2} = 5.5 V to 26.4 V, I_o = 500 mA, T_J = 25 ºC	--	239	--	mΩ
		V_{DD2} = 5.5 V to 26.4 V, I_o = 500 mA, T_J = 150 ºC	--	276	336	mΩ
	LS FET on resistance (SENSE, GND_HV and GND Pins are connected together, $R_{DS(ON)}$ with Sense Pin = GND, If Sense Pin V_{DD} = 0.5 V additional 100 mΩ at worst case)	V_{DD2} = 4.5 V to 5.5 V, I_o = 500 mA, T_J = 25 ºC	--	239	--	mΩ
		V_{DD2} = 4.5 V to 5.5 V, I_o = 500 mA, T_J = 150 ºC	--	274	338	mΩ
		V_{DD2} = 5.5 V to 26.4 V, I_o = 500 mA, T_J = 25 ºC	--	235	--	mΩ
		V_{DD2} = 5.5 V to 26.4 V, I_o = 500 mA, T_J = 150 ºC	--	270	327	mΩ
I_{OFF}	Off-state leakage current	GPO0_HD, GPO1_HD[1], V_{DD2} = 5.0 V, T_J = -40 °C to 85 °C PWM is off, including the charge pump OSC	0	--	9.3	µA
		GPO0_HD, GPO1_HD[1], V_{DD2} = 5.0 V, T_J = -40 °C to 150 °C PWM is off, including the charge pump OSC	0	--	10.2	µA
I_{DD2}	Single HV Driver Current Consumption (including support circuits), without output load	V_{DD2} = 5.0 V, T_J = -40 °C to 150 °C, Static (PWM is off), including the charge pump OSC	--	--	115.9	µA
		V_{DD2} = 5.0 V, T_J = -40 °C to 150 °C, Switching (PWM = 250 kHz)	--	0.7	1.4	mA
t_{WAKE}	Wake-up time	HV Sleep OUT High to output transition, BG is always on, Another pins SLEEP - disable	--	80	130	µs

[1] There is a resistive voltage divider in front of Diff Amplifier that is connected to GPO0_HD and GPO1_HD.

3.9 Protection Circuits Electrical Specifications

Table 14. Protection Circuits

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OCP}	Overcurrent protection threshold	Per any HS or LS FET	--	3.0	--	A
t_{OCP1}	OCP deglitch time[1]	V_{DD} = 5 V, V_{DD2} = 5 V, T = 25 ºC, deglitch = enable, High-side	--	3.0	--	µs
		V_{DD} = 5 V, V_{DD2} = 5 V, T = 25 ºC, deglitch = enable, Low-side	--	1.7	--	µs
t_{OCP2}	OCP retry time[2]	Delay = 492 µs	--	490	--	µs
		Delay = 656 µs	--	654	--	µs
		Delay = 824 µs	--	817	--	µs
		Delay = 988 µs	--	981	--	µs
		Delay = 1152 µs	--	1144	--	µs
		Delay = 1316 µs	--	1308	--	µs
		Delay = 1480 µs	--	1471	--	µs
		Delay = 1640µs	--	1635	--	µs
V_{UVLO}[3]	Undervoltage lockout	At falling edge of V_{DD2}	3.97	4.03	4.08	V
	Recover from Undervoltage lockout	At rising edge of V_{DD2}	4.16	4.22	4.27	V
T_{TSD}	Thermal shutdown temperature	Junction temperature T_J	135.0	147.4	159.2	°C
T_{HYST}	Thermal shutdown hysteresis		--	16.2	--	°C

[1] CP deglitch time option can be enabled by register [873] for Full Bridge. The High-side FETs doesn't have OCP deglitch time if the current through the FET is higher than I_{OCP} level during enable time.This is done to avoid huge currents during retry when the short is persist on the output.
[2] OCP retry time can be selected separately for each HV OUT: HV GPO0 - registers[780:778], HV GPO1 - registers[788:786]. For more information check the Section 7.4.3 Over-Current Protection.
[3] UVLO function can be enabled separately for V_{DD2} by register [864]. For more information see Section 7.4.5 Under-Voltage Lockout.

3.10 Timing Specifications

Table 15. Typical Startup Estimated for Chip

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{SU}	Chip startup time	From V_{DD} rising past PON_{THR}	--	0.91	1.20	ms

Table 16. Typical Delay Estimated for Each Macrocell at T_A = 25 °C

Symbol	Parameter	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Digital input to PP 1x	25	25	16	18	12	13	ns
tpd	Delay	Digital input with Schmitt trigger to PP 1x	25	26	17	19	14	14	ns
tpd	Delay	Low voltage digital input to PP 1x	25	247	17	157	13	83	ns
tpd	Delay	Digital input to PP 2x	22	24	15	17	11	13	ns
tpd	Delay	Digital input to NMOS 1x	--	23	--	17	--	13	ns
tpd	Delay	Digital input to NMOS 2x	--	23	--	16	--	12	ns
tpd	Delay	1x3-State Hi-Z to 0	--	23	--	17	--	12	ns
tpd	Delay	1x3-State Hi-Z to 1	24	--	17	--	12	--	ns
tpd	Delay	2x3-State Hi-Z to 0	--	23	--	16	--	11	ns
tpd	Delay	2x3-State Hi-Z to 1	23	--	16	--	12	--	ns
tpd	Delay	OE Hi-Z to 0	--	23	--	17	--	12	ns
tpd	Delay	OE Hi-Z to 1	24	--	17	--	12	--	ns
tpd	Delay	DFF	22	24	15	17	10	11	ns
tpd	Delay	LATCH	24	25	15	17	10	11	ns
tpd	Delay	CTN/DLY	72	71	51	50	35	34	ns
tpd	Delay	2-bit LUT	17	17	11	12	8	8	ns
tpd	Delay	3-bit LUT	19	19	13	13	8	9	ns
tpd	Delay	4-bit LUT	20	19	13	12	9	9	ns
tpd	Delay	Pipe delay nRESET OUT Q, nQ	24	24	17	17	12	12	ns
tpd	Delay	Pipe delay OUT0 Q, nQ	24	26	18	15	10	11	ns
tpd	Delay	PGEN CLK	18	18	12	13	8	9	ns
tpd	Delay	PGEN nRESET Zto0	--	20	--	14	--	10	ns
tpd	Delay	PGEN nRESET Zto1	21	--	13	--	9	--	ns
tw	Width	Edge detect	256	255	180	179	125	125	ns
tpd	Delay	Edge detect	18	19	12	12	8	8	ns
tpd	Delay	Edge detect delayed	275	274	190	191	132	133	ns
tpd	Delay	Filter nQ	180	209	118	137	75	82	ns
tpd	Delay	Filter nQ first spark	--	191	--	123	--	73	ns
tpd	Delay	Filter Q	209	180	136	119	81	75	ns
tpd	Delay	Filter Q first spark	191	--	123	--	73	--	ns
tpd	Delay	Inverter filter nQ first spark	--	165	--	107	--	68	ns
tpd	Delay	Inverter filter Q first spark	164	--	107	--	68	--	ns
tpd	Delay	Ripple CNT CLK UP Q1	25	23	17	16	11	11	ns
tpd	Delay	Ripple CNT CLK UP Q2	29	22	29	16	13	11	ns
tpd	Delay	Ripple CNT CLK UP Q3	33	22	23	16	15	11	ns
tpd	Delay	Ripple CNT CLK DOWN Q1	25	24	17	17	11	11	ns
tpd	Delay	Ripple CNT CLK DOWN Q2	25	29	17	20	11	13	ns
tpd	Delay	Ripple CNT CLK DOWN Q3	25	36	16	25	11	16	ns
tpd	Delay	Ripple CNT nSET UP Q1	25	41	16	29	11	19	ns
tpd	Delay	Ripple CNT nSET UP Q2	23	42	15	29	11	19	ns

Table 16. Typical Delay Estimated for Each Macrocell at T_A = 25 °C (Cont.)

tpd	Delay	Ripple CNT nSET UP Q3	22	46	14	31	10	21	ns
tpd	Delay	Ripple CNT nSET DOWN Q1	25	41	16	28	11	19	ns
tpd	Delay	Ripple CNT nSET DOWN Q2	23	40	15	27	10	18	ns
tpd	Delay	Ripple CNT nSET DOWN Q3	22	40	14	27	10	18	ns
tpd	Delay	PWM CHOPPER BLANK	--	37	--	25	--	17	ns
tpd	Delay	PWM OUT- nQ1	--	25	--	17	--	11	ns
tpd	Delay	PWM0 OUT- Q1	24	--	16	--	11	--	ns
tpd	Delay	PWM0 OUT+ nQ1	21	--	14	--	9	--	ns
tpd	Delay	PWM0 OUT+ Q1	--	22	--	15	--	10	ns

Table 17. Programmable Delay Expected Typical Delays and Widths at T_A = 25 °C

Symbol	Parameter	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
tw	Pulse width, 1 cell	mode: (any) edge detect, edge detect output	234	162	113	ns
tw	Pulse width, 2 cell	mode: (any) edge detect, edge detect output	464	321	222	ns
tw	Pulse width, 3 cell	mode: (any) edge detect, edge detect output	695	481	334	ns
tw	Pulse width, 4 cell	mode: (any) edge detect, edge detect output	926	641	445	ns
time1	Delay, 1 cell	mode: (any) edge detect, edge detect output	18	12	8	ns
time1	Delay, 2 cell	mode: (any) edge detect, edge detect output	18	12	8	ns
time1	Delay, 3 cell	mode: (any) edge detect, edge detect output	18	12	8	ns
time1	Delay, 4 cell	mode: (any) edge detect, edge detect output	18	12	8	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	249	173	120	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	476	329	229	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	704	488	339	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	933	647	450	ns

Table 18. Typical Filter Rejection Pulse Width at T_A = 25 °C

Parameter	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Filtered pulse width	< 180	< 117	< 71	ns

Table 19. LP_BG Specifications at T_A = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V

Parameter	Conditions	Min	Typ	Max	Unit
LP_BG start-up time	--	--	--	2.0	ms
LP_BG I_{cc}	--	--	555	--	nA

3.11 Counter/Delay Specifications

Table 20. Typical Counter/Delay Offset at T_A = 25 C

Parameter	OSC freq	OSC Power-on	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Power-on time	25 MHz	auto	134	127	125	ns
Power-on time	2.048 kHz	auto	496	443	398	µs
Frequency settling time	25 MHz	auto	850	1100	1200	ns
Frequency settling time	2.048 kHz	auto	900	950	900	µs
Variable (CLK period)	25 MHz	forced	39-42	39-42	39-42	ns
Variable (CLK period)	2.048 kHz	forced	476-495	476-495	476-495	µs
Typical Propagation Delay (non-delayed edge)	25 MHz	either	39	26	17	ns

3.12 Oscillator Specifications

Table 21. OSC0 Frequency Limits, V_{DD} = 2.3 V to 5.5 V

OSC	Junction Temperature Range								
	+25 °C			-40 °C to +85 °C			-40 °C to +150 °C		
	Min. value	Max. value	Error, %	Min. value	Max. value	Error, %	Min. value	Max. value	Error, %
2.048 kHz OSC0	2.012 kHz	2.061 kHz	+0.6	1.898 kHz	2.126 kHz	+3.8	1.717 kHz	2.126 kHz	+3.8
			-1.8			-7.3			-16.2

Table 22. OSC1 Frequency Limits, V_{DD} = 2.3 V to 5.5 V

OSC	Junction Temperature Range								
	+25 °C			-40 °C to +85 °C			-40 °C to +150 °C		
	Minimum value	Maximum value	Error, %	Minimum value	Maximum value	Error, %	Minimum value	Maximum value	Error, %
25 MHz OSC1	24.547 MHz	25.125 MHz	+0.5	24.021 MHz	25.769 MHz	+3.1	23.497 MHz	25.769 MHz	+3.1
			-1.8			-3.9			-6.0

3.12.1 OSC Power-On Delay

Table 23. Oscillators Power-On Delay at T_A = 25 °C, OSC Power Setting: "Auto Power-On"

Power Supply Range (V_{DD}) V	OSC0 2.048 kHz		OSC1 25 MHz		OSC1 25 MHz start with delay	
	Typical value, µs	Maximum value, µs	Typical value, ns	Maximum value, ns	Typical value, ns	Maximum value, ns
2.30	516	693	53	64	138	150
2.50	496	622	44	50	134	143
3.30	443	539	29	34	127	137
5.00	392	486	16	40	125	137
5.50	380	466	17	31	125	137

3.13 Current Sense Comparator Specifications

Table 24. Current Sense Comparator Specifications at T_A = -40 °C to +85 °C, V_{DD} = 2.3 to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Note	Conditions	Min	Typ	Max	Unit
$R_{CurrCMP}$	Current limit input range	Per Full Bridge Sense pin (LS FET only)	$I_{FET}*R_{SENSE}$	50	--	500	mV
I_{accur}	Current sense accuracy	T_J = 25 °C	120 mV input	-3.1	--	+3.9	%
			504 mV input	-0.9	--	+1.0	%
		T_J = -40 °C to 85 °C	120 mV input	-4.5	--	+4.7	%
			504 mV input	-1.2	--	+1.2	%
		T_J = -40 °C to 150 °C	120 mV input	-4.5	--	+5.6	%
			504 mV input	-1.2	--	+1.4	%
		T_J = 25 °C	60 mV input	-5.1	--	+7.7	%
			252 mV input	-1.6	--	+1.8	%
I_{accur}	Current sense accuracy	T_J = -40 °C to 85 °C	60 mV input	-7.5	--	+8.8	%
			252 mV input	-2.0	--	+2.1	%
		T_J = -40 °C to 150 °C	60 mV input	-7.5	--	+10.4	%
			252 mV input	-2.2	--	+2.5	%
t_{start}	Current sense CMP startup time	Current sense CMP power-on delay	T_J = -40 °C to 85 °C	--	6.7	12.1	µs

Table 24. Current Sense Comparator Specifications at T_A = -40 °C to +85 °C, V_{DD} = 2.3 to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Note	Conditions	Min	Typ	Max	Unit
PROP	Propagation Delay, Response time Normal speed		LOW to HIGH, T_J = -40 °C to 85 °C, Vref = 1024 mV, Overdrive = 100 mV	--	0.56	0.9	µs
			LOW to HIGH, T_J = -40 °C to 85 °C, Vref = 1024 mV, Overdrive = 10 mV	--	0.67	1.3	µs
			LOW to HIGH, T_J = -40 °C to 85 °C, Vref = 480 mV to 2016 mV, Overdrive = 100 mV	--	0.59	1.3	µs
			LOW to HIGH, T_J = -40 °C to 85 °C, Vref = 480 mV to 2016 mV, Overdrive = 10 mV	--	0.69	1.8	µs
			HIGH to LOW, T_J = -40 °C to 85 °C, Vref = 1024 mV, Overdrive = 100 mV	--	0.57	0.9	µs
			HIGH to LOW, T_J = -40 °C to 85 °C, Vref = 1024 mV, Overdrive = 10 mV	--	0.71	1.4	µs
			HIGH to LOW, T_J = -40 °C to 85 °C, Vref = 480 mV to 2016 mV, Overdrive = 100 mV	--	0.63	1.6	µs
			HIGH to LOW, T_J = -40 °C to 85 °C, Vref = 480 mV to 2016 mV, Overdrive = 10 mV	--	0.80	3.4	µs
			LOW to HIGH, T_J = -40 °C to 150 °C, Vref = 1024 mV, Overdrive = 100 mV	--	0.57	0.9	µs
			LOW to HIGH, T_J = -40 °C to 150 °C, Vref = 1024 mV, Overdrive = 10 mV	--	0.71	1.4	µs
			LOW to HIGH, T_J = -40 °C to 150 °C, Vref = 480 mV to 2016 mV, Overdrive = 100 mV	--	0.60	1.3	µs
			LOW to HIGH, T_J = -40 °C to 150 °C, Vref = 480 mV to 2016 mV, Overdrive = 10 mV	--	0.72	1.9	µs

Table 24. Current Sense Comparator Specifications at T_A = -40 °C to +85 °C, V_{DD} = 2.3 to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Note	Conditions	Min	Typ	Max	Unit
PROP	Propagation Delay, Response time Normal speed		HIGH to LOW, T_J = -40 °C to 150 °C, Vref = 1024 mV, Overdrive = 100 mV	--	0.58	0.9	µs
			HIGH to LOW, T_J = -40 °C to 150 °C, Vref = 1024 mV, Overdrive = 10 mV	--	0.74	1.5	µs
			HIGH to LOW, T_J = -40 °C to 150 °C, Vref = 480 mV to 2016 mV, Overdrive = 100 mV	--	0.64	1.7	µs
			HIGH to LOW, T_J = -40 °C to 150 °C, Vref = 480 mV to 2016 mV, Overdrive = 10 mV	--	0.85	3.9	µs
PROP	Propagation Delay, Response time Fast speed		LOW to HIGH, T_J = -40 °C to 85 °C, Vref = 1024 mV, Overdrive = 100 mV	--	0.35	0.6	µs
			LOW to HIGH, T_J = -40 °C to 85 °C, Vref = 1024 mV, Overdrive = 10 mV	--	0.40	0.7	µs
			LOW to HIGH, T_J = -40 °C to 85 °C, Vref = 480 mV to 2016 mV, Overdrive = 100 mV	--	0.37	0.8	µs
			LOW to HIGH, T_J = -40 °C to 85 °C, Vref = 480 mV to 2016 mV, Overdrive = 10 mV	--	0.41	0.9	µs
			HIGH to LOW, T_J = -40 °C to 85 °C, Vref = 1024 mV, Overdrive = 100 mV	--	0.38	0.6	µs
			HIGH to LOW, T_J = -40 °C to 85 °C, Vref = 1024 mV, Overdrive = 10 mV	--	0.43	0.7	µs
			HIGH to LOW, T_J = -40 °C to 85 °C, Vref = 480 mV to 2016 mV, Overdrive = 100 mV	--	0.42	0.9	µs
			HIGH to LOW, T_J = -40 °C to 85 °C, Vref = 480 mV to 2016 mV, Overdrive = 10 mV	--	0.48	1.8	µs

Table 24. Current Sense Comparator Specifications at T_A = -40 °C to +85 °C, V_{DD} = 2.3 to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Note	Conditions	Min	Typ	Max	Unit
PROP	Propagation Delay, Response time Fast speed		LOW to HIGH, T_J = -40 °C to 150 °C, Vref = 1024 mV, Overdrive = 100 mV	--	0.36	0.6	µs
			LOW to HIGH, T_J = -40 °C to 150 °C, Vref = 1024 mV, Overdrive = 10 mV	--	0.42	0.8	µs
			LOW to HIGH, T_J = -40 °C to 150 °C, Vref = 480 mV to 2016 mV, Overdrive = 100 mV	--	0.37	0.8	µs
			LOW to HIGH, T_J = -40 °C to 150 °C, Vref = 480 mV to 2016 mV, Overdrive = 10 mV	--	0.42	0.9	µs
			HIGH to LOW, T_J = -40 °C to 150 °C, Vref = 1024 mV, Overdrive = 100 mV	--	0.39	0.6	µs
			HIGH to LOW, T_J = -40 °C to 150 °C, Vref = 1024 mV, Overdrive = 10 mV	--	0.44	0.8	µs
			HIGH to LOW, T_J = -40 °C to 150 °C, Vref = 480 mV to 2016 mV, Overdrive = 100 mV	--	0.43	1.0	µs
			HIGH to LOW, T_J = -40 °C to 150 °C, Vref = 480 mV to 2016 mV, Overdrive = 10 mV	--	0.50	2.1	µs

3.14 Differential Amplifier with Integrator and Comparator Specifications

Table 25. Differential Amplifier Specifications at T_A = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔV_{LINe}	Line regulation	V_{DD2} = 5 V to 11.1 V, V_{OUT} = 4.096 V, I_{Load} = 0.5 A, T_J = -40 °C to 85 °C	--	±0.8	--	%
		V_{DD2} = 14.8 V to 26.4 V, V_{OUT} = 8.192 V, I_{Load} = 0.5 A, T_J = -40 °C to 85 °C	--	±2.1	--	%
		V_{DD2} = 5 V to 11.1 V, V_{OUT} = 4.096 V, I_{Load} = 0.5 A, T_J = -40 °C to 150 °C	--	±0.7	--	%
		V_{DD2} = 14.8 V to 26.4 V, V_{OUT} = 8.192 V, I_{Load} = 0.5 A, T_J = -40 °C to 150 °C	--	±2.0	--	%
ΔV_{LOAD}	Load regulation	V_{DD2} = 5 V, V_{OUT} = 4.096 V, I_{LOAD} = 200 mA to 500 mA, T_J = 25 °C	--	±1.0	--	%
		V_{DD2} = 14.8 V, V_{OUT} = 8.192 V, I_{LOAD} = 200 mA to 500 mA, T_J = 25 °C	--	±1.4	--	%
		V_{DD2} = 26.4 V, V_{OUT} = 16.128 V, I_{LOAD} = 200 mA to 500 mA, T_J = 25°C	--	±1.8	--	%
		V_{DD2} = 5 V, V_{OUT} = 4.096 V, I_{LOAD} = 200 mA to 500 mA, T_J = -40 °C to 85 °C	--	±1.0	--	%
		V_{DD2} = 14.8 V, V_{OUT} = 8.192 V, I_{LOAD} = 200 mA to 500 mA, T_J = -40 °C to 85 °C	--	±1.4	--	%
		V_{DD2} = 26.4 V, V_{OUT} = 16.128 V, I_{LOAD} = 200 mA to 500 mA, T_J = -40 °C to 85 °C	--	±1.9	--	%
		V_{DD2} = 5 V, V_{OUT} = 4.096 V, I_{LOAD} = 200 mA to 500 mA, T_J = -40 °C to 150 °C	--	±1.0	--	%
		V_{DD2} = 14.8 V, V_{OUT} = 8.192 V, I_{LOAD} = 200 mA to 500 mA, T_J = -40 °C to 150 °C	--	±1.3	--	%
		V_{DD2} = 26.4 V, V_{OUT} = 16.128 V, I_{LOAD} = 200 mA to 500 mA, T_J = -40 °C to 150 °C	--	±1.7	--	%
f_{INT}	Integrated frequency	--	49	--	--	kHz

3.15 ACMP Specifications

Table 26. ACMP Specifications at T_A = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Note	Condition	Min	Typ	Max	Unit
V_{ACMP}	ACMP input voltage range	Positive input	--	0	--	V_{DD}	V
		Negative input		0	--	V_{DD}	V
V_{offset}	ACMP input offset[2]	ACMPxH Vhys = 0 mV, Gain = 1, Vref = 32 mV to 2016 mV	T_J = -40 °C to 85 °C	-8.0	--	6.5	mV
			T_J = -40 °C to 150 °C	-9.8	--	7.2	mV
t_{start}	ACMP startup time	ACMPxH power-on delay, Minimal required wake time for the "Wake and Sleep function"	T_J = -40 °C to 85 °C	--	--	32.0	µs
			T_J = -40 °C to 150 °C	--	--	32.7	µs
V_{HYS}	ACMPxH Built-in hysteresis[1][2]	V_{HYS} = 32 mV	T_J = -40 °C to 85 °C	30.0	--	35.0	mV
		V_{HYS} = 64 mV		61.5	--	66.0	mV
		V_{HYS} = 192 mV		187.0	--	197.0	mV
		V_{HYS} = 32 mV	T_J = -40 °C to 150 °C	29.0	--	36.0	mV
		V_{HYS} = 64 mV		60.5	--	67.0	mV
		V_{HYS} = 192 mV		186.0	--	198.0	mV
R_{sin}	Series input resistance	Gain = 1x	--	--	10	--	GΩ
		Gain = 0.5x		1.7	--	2.4	MΩ
		Gain = 0.33x		1.7	--	2.4	MΩ
		Gain = 0.25x		1.7	--	2.4	MΩ
PROP	Propagation Delay, Response time	ACMPxH, Vref =1.024 V, Gain = 1, Overdrive = 100 mV	LOW to HIGH, T_J = -40 °C to 85 °C	--	0.51	1.50	µs
			HIGH to LOW, T_J = -40 °C to 85 °C	--	0.51	0.80	µs
		ACMPxH, Vref = 0.032 V to 2.016 V, Gain = 1, Overdrive = 100 mV	LOW to HIGH, T_J = -40 °C to 85 °C	--	0.53	1.50	µs
			HIGH to LOW, T_J = -40 °C to 85 °C	--	0.52	1.10	µs
		ACMPxH, Vref = 1.024 V, Gain = 1, Overdrive = 100 mV	LOW to HIGH, T_J = -40 °C to 150 °C	--	0.51	1.50	µs
			HIGH to LOW, T_J = -40 °C to 150 °C	--	0.51	0.80	µs
PROP	Propagation Delay, Response time	ACMPxH, Vref = 0.032 V to 2.016 V, Gain = 1, Overdrive = 100 mV	LOW to HIGH, T_J = -40 °C to 150 °C	--	0.53	1.50	µs
			HIGH to LOW, T_J = -40 °C to 150 °C	--	0.52	1.20	µs

Table 26. ACMP Specifications at T_A = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Cont.)

Symbol	Parameter	Note	Condition	Min	Typ	Max	Unit
G	Gain error (including threshold and internal Vref error)	G = 1	T_J = -40 °C to 85 °C	1	1	1	
		G = 0.5		0.50	0.50	0.50	
		G = 0.33		0.30	0.33	0.30	
		G = 0.25		0.20	0.25	0.30	
		G = 1	T_J = -40 °C to 150 °C	1	1	1	
		G = 0.5		0.50	0.50	0.50	
		G = 0.33		0.30	0.33	0.30	
		G = 0.25		0.20	0.25	0.30	
$Vref_{accuracy}$	Internal Vref accuracy	Vref ≥ 1.216 V	T_J = 25 °C	-0.42	--	0.17	%
			T_J = -40 °C to 150 °C	-0.43	--	0.18	%
$Vref_{buf\_offset}$	Vref output buffer offset (when connected to the output pin)	Vref = 32 mV to 2016 mV	T_J = 25 °C	-17.1	--	9.6	mV
			T_J = -40 °C to 150 °C	-18.0	--	11.1	mV
C_{VREF}	Vref output buffer capacitance loading	Resistance load in condition cell	1 MΩ	--	--	5	pF
			560 kΩ	--	--	10	pF
			100 kΩ	--	--	40	pF
			10 kΩ	--	--	80	pF
			2 kΩ	--	--	120	pF
			1 kΩ, Vref: 32 mV to 1024 mV	--	--	150	pF

[1] V_{IL} = Vin - V_{HYS}, V_{IH} = Vin.
[2] ESD resistor should be taken into consideration when using pull-up/pull-down resistors. It may affect V_{IH} and V_{IL}. See sections 6.6 ESD Protection to 6.9 Matrix OE IO Structure (VDD Group).

3.16 Analog Temperature Sensor Specifications

Table 27. TS Output vs Temperature (Output Range 1)

T, °C	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 4.5 V to 5.5 V	
	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %
-40	998.9	±1.7	998.8	±1.7	998.9	±1.6
-30	976.9	±1.5	976.8	±1.5	976.9	±1.5
-20	954.3	±1.4	954.2	±1.4	954.4	±1.3
-10	931.7	±1.2	931.6	±1.2	931.8	±1.2
0	908.9	±1.2	908.7	±1.1	909.0	±1.1
10	908.9	±1.1	885.7	±1.1	886.0	±1.1
20	862.9	±1.3	862.8	±1.2	863.0	±1.2
25	851.0	±1.3	850.9	±1.2	851.2	±1.2
30	839.4	±1.4	839.3	±1.3	839.6	±1.3
40	816.2	±1.5	816.1	±1.4	816.4	±1.4
50	792.8	±1.6	792.6	±1.5	793.0	±1.5
60	769.1	±1.6	768.9	±1.5	769.3	±1.6
70	745.1	±1.7	744.9	±1.6	745.3	±1.6
80	721.1	±1.7	721.0	±1.6	721.4	±1.6
85	708.8	±1.7	708.7	±1.6	709.1	±1.6
90	696.8	±1.7	696.6	±1.6	697.1	±1.7
100	672.4	±1.7	672.3	±1.6	672.8	±1.7
110	648.0	±1.7	647.9	±1.6	648.4	±1.7
120	623.5	±1.7	623.3	±1.6	623.9	±1.7
125	611.0	±1.6	610.8	±1.5	611.4	±1.6
130	598.5	±1.6	598.3	±1.5	598.9	±1.6
140	573.5	±1.6	573.4	±1.5	574.0	±1.5
150	549.1	±2.0	548.9	±1.9	549.6	±1.8

Table 28. TS Output vs Temperature (Output Range 2)

T, °C	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5 V	
	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %
-40	1206.1	±1.7	1206.1	±1.7	1206.0	±1.6
-30	1179.5	±1.5	1179.5	±1.5	1179.5	±1.5
-20	1152.2	±1.4	1152.2	±1.4	1152.2	±1.3
-10	1124.9	±1.2	1124.9	±1.2	1124.9	±1.2
0	1097.3	±1.2	1097.3	±1.1	1097.4	±1.1
10	1069.6	±1.1	1069.6	±1.1	1069.7	±1.1
20	1041.8	±1.2	1041.8	±1.2	1041.9	±1.2

Table 28. TS Output vs Temperature (Output Range 2) (Cont.)

T, °C	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5 V	
	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %
25	1027.5	±1.3	1027.5	±1.2	1027.7	±1.2
30	1013.5	±1.3	1013.5	±1.3	1013.7	±1.3
40	985.4	±1.5	985.4	±1.4	985.6	±1.4
50	957.1	±1.5	957.1	±1.5	957.3	±1.5
60	928.5	±1.6	928.5	±1.5	928.7	±1.6
70	899.5	±1.6	899.5	±1.6	899.7	±1.6
80	870.6	±1.7	870.6	±1.6	870.9	±1.6
85	855.7	±1.7	855.7	±1.6	856.1	±1.6
90	841.2	±1.7	841.2	±1.6	841.5	±1.7
100	811.8	±1.7	811.8	±1.6	812.2	±1.7
110	782.3	±1.7	782.1	±1.6	782.7	±1.7
120	752.7	±1.7	752.7	±1.6	753.2	±1.7
125	737.6	±1.6	737.6	±1.5	738.1	±1.6
130	722.5	±1.6	722.5	±1.5	723.0	±1.6
140	692.5	±1.5	692.5	±1.5	693.0	±1.5
150	663.0	±1.9	663.0	±1.9	663.5	±1.8

4. User Programmability

The SLG47115 is a user programmable device with one time programmable (OTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.hvp file) is forwarded to Renesas Electronics Corporation to integrate into a production process.

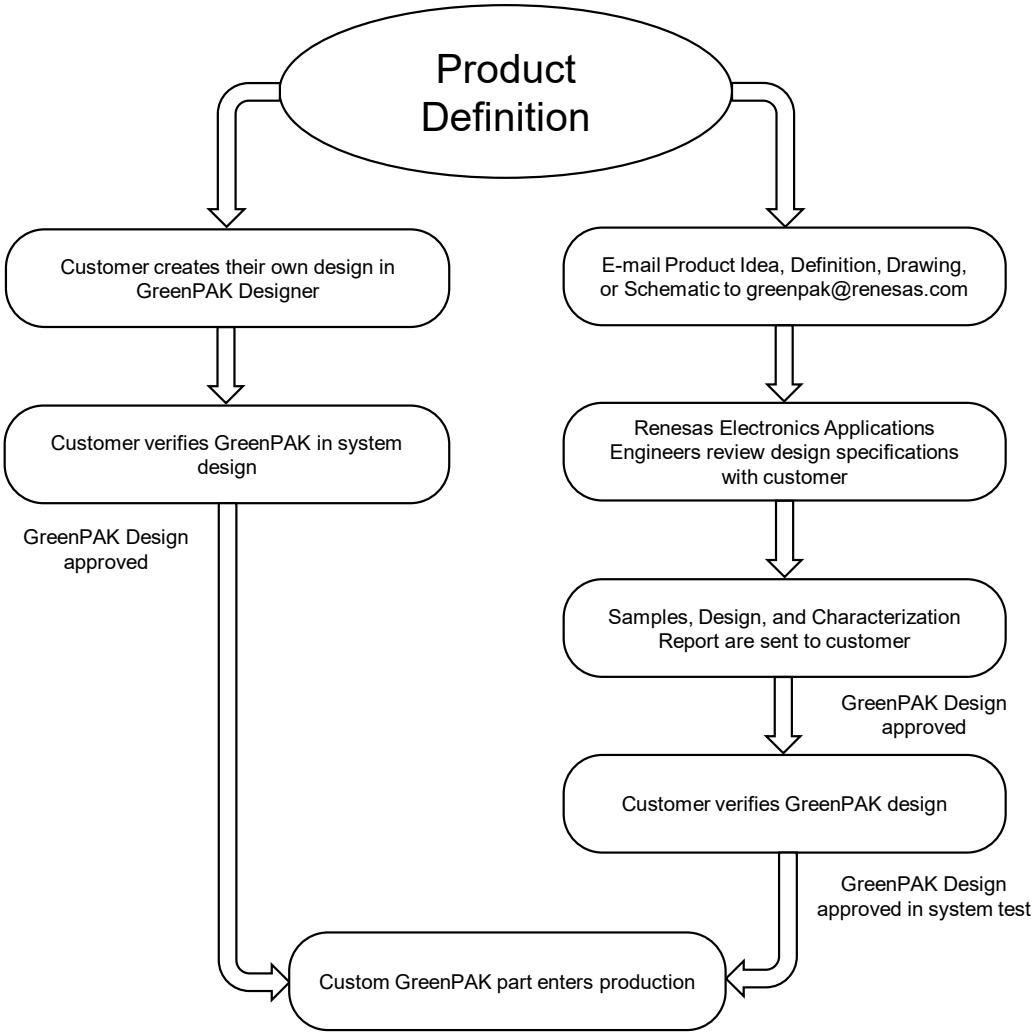


Figure 3. Steps to Create a Custom GreenPAK Device

5. System Overview

5.1 General Purpose IO Pins

- Digital input (low voltage or normal voltage, with or without Schmitt trigger)
- NMOS open-drain outputs
- Push-pull outputs
- Analog IOs
- 10 kΩ/100 kΩ/1 MΩ pull-up/pull-down resistors
- GPIOs with OE can be configured as bidirectional IOs or three-state outputs

5.2 High Voltage Output Pins

- High voltage digital output in push-pull, open-drain configurations or Full Bridge logic
- Build-in thermal shut down, overcurrent and short circuit protection
- Configurable dead band time
- Sleep mode to save energy
- Advanced voltage control and current control

5.3 Connection Matrix

- Digital matrix for circuit connections based on user design

5.4 Current Sense Comparator

- SENSE pin that is connected to a positive input of sense comparator for advanced current control
- Selectable Vref: 6-bit selection
- Static or dynamic Vref selection
- Configurable gain: 4x or 8x

5.5 Differential Amplifier with Integrator and Comparator

- Low quiescent current
- Provide constant motor speed for variable V_{DD2}
- Connected to HV GPO0 and HV GPO1

5.6 Two General Purpose Analog Comparators

- Wide Vref selector: 32 mV to 2016 mV, with 32 mV step
- Selectable hysteresis: 2-bit selection
- Configurable gain (resistor divider) 1x; 0.5x; 0.33x; 0.25x
- Different input sources: PINs, V_{DD}, V_{DD2} or temp sense

5.7 Voltage Reference

- Used for references on analog comparators
- Can be driven to external pin

5.8 Twelve Combination Function Macrocells

- Three selectable DFF/LATCH or 2-bit LUTs
- One selectable Programmable Pattern Generator or 2-bit LUT
- Six selectable DFF/LATCH with Set/Reset input or 3-bit LUTs
- One selectable pipe delay or ripple counter or 3-bit LUT
- One selectable DFF/LATCH with Set/Reset input or 4-bit LUT

5.9 Five Multi-Function Macrocells

- Four selectable DFF/LATCH/3-bit LUTs + 8-bit Delay/Counters
- One selectable DFF/LATCH/4-bit LUT + 16-bit Delay/Counter

5.10 Two PWM Macrocells

- Flexible 8-bit or 7-bit PWM mode with the duty cycle control
- True 0 % and 100 % duty cycle
- Regular or 16 preset registers mode
- Autostop mode
- Phase correct mode
- Selectable separate dead band time
- Glitch safety

5.11 Serial Communication

- I^2C interface

5.12 Programmable Delay

- 125 ns/250 ns/375 ns/500 ns @ 3.3 V
- Includes edge detection function

5.13 Additional Logic Function

- One deglitch filter macrocell
- Includes edge detection function

5.14 Two Oscillators

- 2.048 kHz
- 25 MHz

5.15 Dual V_{DD}

- General power supply V_{DD} in range 2.5 V to 5.0 V
- Second power supply V_{DD2} in range 5.0 V to 24.0 V
- Two GPIOs groups: V_{DD} GPIOs group, V_{DD2} GPOs group

6. Input/Output Pins

The SLG47115 has a total of 7 GPIO, 1 GPI, and 2 HV GPO pins, which can function as either a user-defined input or output, as well as serving as a special function (such as outputting the voltage reference).

6.1 GPIO Pins

GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6 serve as general purpose IO pins of V_{DD} group.

6.2 GPI Pin

GPI serves as general purpose input pin of V_{DD} group.

6.3 HV GPO Pins

HV GPO0, HV GPO1 serve as high voltage general purpose output pins of V_{DD2} group.

6.4 Pull-Up/Down Resistors

All IO pins of V_{DD} group have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ. The internal resistors can be configured as either pull-up or pull-downs.

6.5 Fast Pull-Up/Down During Power-Up

During power-up, IO pull-up/down resistance will switch to 2.6 kΩ initially and then it will switch to the normal setting value. This function is enabled by register [754].

6.6 ESD Protection

Every pin has the ESD protection circuit built-in, see Figure 4, Figure 5, Figure 6. In addition to the ESD diodes, when configured as inputs, all pins have a series resistor which decreases the exceeding input current to a safe level. For the value of the resistors refer to Table 29. It should be noted, this additional input resistance will affect the input thresholds (V_{IH} and V_{IL}) when using pull-up/pull-down resistors.

Table 29. ESD Resistors Value

Pin	Value, Ω
GPIO0	200
GPI	200
GPIO1	1060
GPIO2	200
GPIO3	200
GPIO4	1060
GPIO5	1060
GPIO6	1060

6.7 GPI IO Structure (V_{DD} Group)

6.7.1 GPI IO Structure

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en = 1
01: Digital In with Schmitt Trigger, smt_en = 1
10: Low Voltage Digital In mode, lv_en = 1
11: Analog IO mode

Note 1: Can be varied over PVT, for reference only.
Note 2: Should be taken into consideration when using pull-up/pull-down resistors. May affect V_{IH} and V_{IL}.

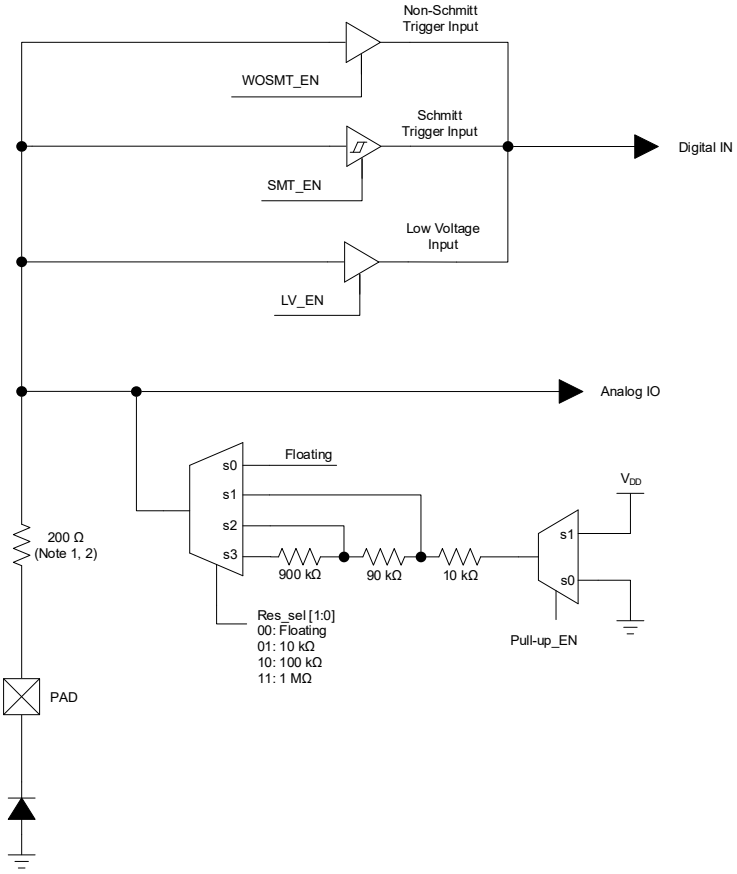


Figure 4. GPI Structure Diagram

6.8 I²C Mode IO Structure (for V_{DD} Group)

6.8.1 I²C Mode IO Structure (for SCL/GPIO2 and SDA/GPIO3, Register OE)

Input mode [1:0]
00: Digital input without Schmitt trigger, WOSMT_EN = 1
01: Digital input with Schmitt trigger, SMT_EN = 1
10: Low voltage, digital input, LV_EN = 1
11: Reserved

[1] It is possible to apply an input voltage higher than V_{DD} to GPIO2 and GPIO3. However, this voltage should not exceed 5.5 V
[2] GPIO2 and GPIO3 don't support push-pull and PMOS open-drain modes
[3] When an internal pull-up/down is used, the input voltage can't be higher than V_{DD}
[4] OE goes HIGH only when I²C_EN signal = 0 and register [831] = 1 (for GPIO2)/register[837] = 1 (for GPIO3)
[5] When OE is HIGH, Input mode[1:0] = 11 must be selected
[6] When I²C_EN signal = 1, fast+ mode (3.2x OD for SDA) can be selected by register [830] = 0 and standard/fast mode (0.8x OD for SDA) can be selected by register [830] = 1
[7] When OE is HIGH, only OD 3.2x option is active
[8] When I²C_EN signal = 1, internal pull-up/down resistors would be always floating
[9] Can be varied over PVT, for reference only.
[10] Should be taken into consideration when using pull-up/pull-down resistors. May affect V_{IH} and V_{IL}.

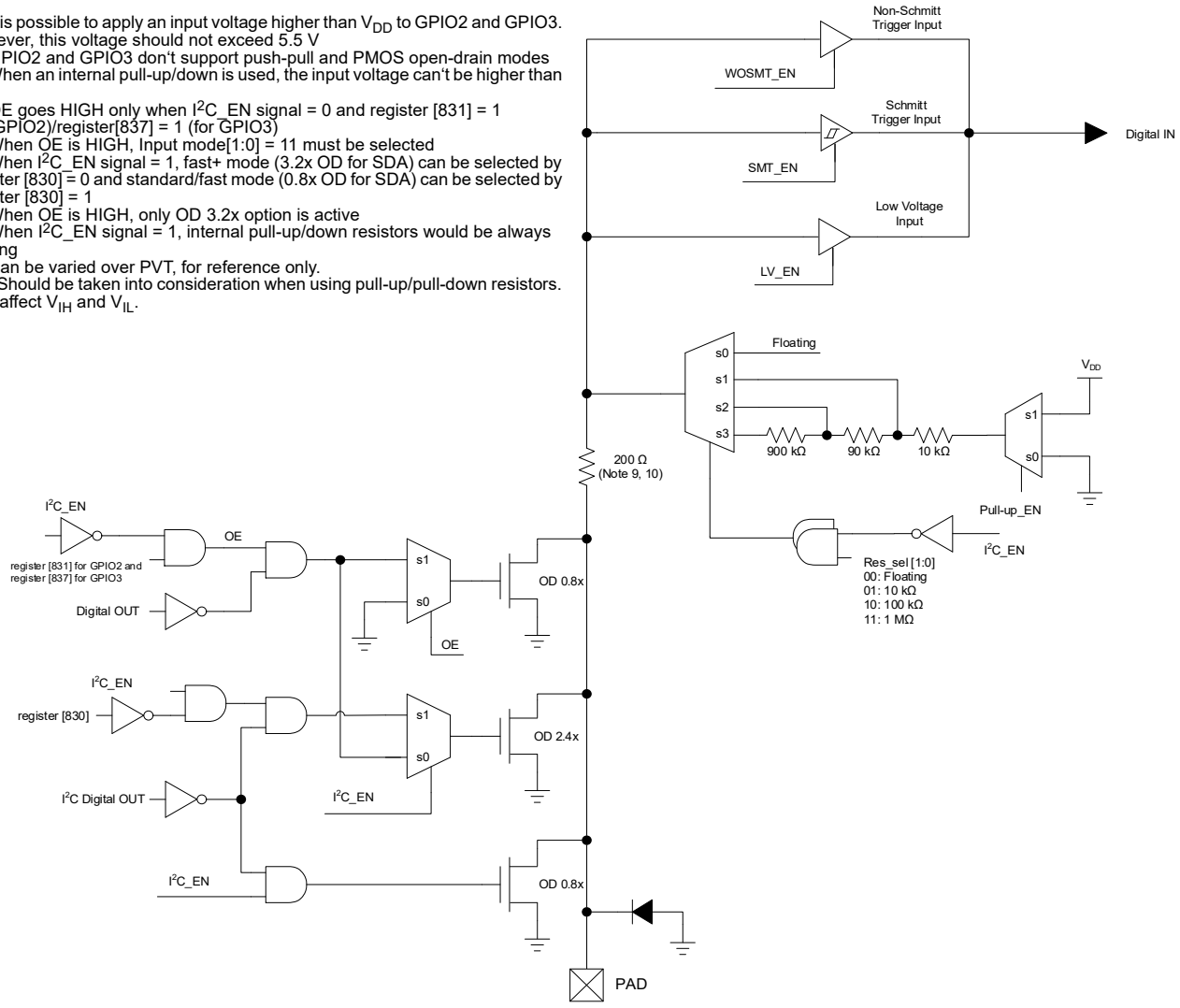


Figure 5. GPIO with I²C Mode Structure Diagram

Table 30. GPIO2 Mode Selection

Register [2032]	Register [831]	Register [830]	GPIO2 Mode
0	x	x	I^2C SCL
1	0	x	GPI, depends on registers[826:825]
1	1	x	GPO, 3.4x OD only

Table 31. GPIO3 Mode Selection

Register [2032]	Register [837]	Register [830]	GPIO3 Mode
0	x	0	I^2C SDA, fast+
0	x	1	I^2C SDA, standard/fast
1	0	x	GPI, depends on registers[833:832]
1	1	x	GPO, 3.4x OD only

6.9 Matrix OE IO Structure (V_{DD} Group)

6.9.1 Matrix OE IO Structure (for GPIOs 0, 1, 4, 5, 6)

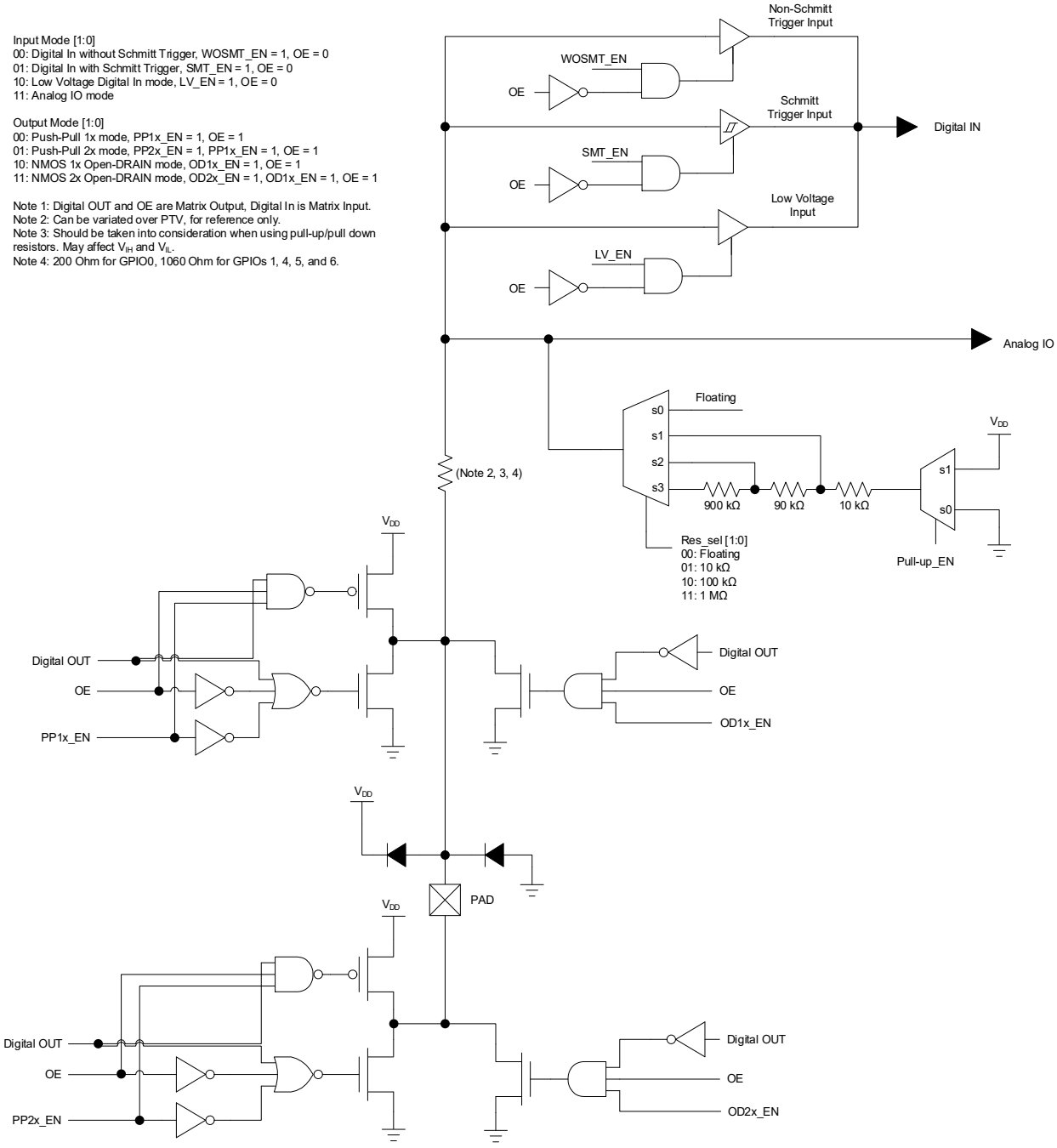


Figure 6. GPIO Matrix OE IO Structure Diagram

6.10 GPO Matrix OE Structure (V_{DD2} Group)

Using Sleep mode to minimize supply current should be sufficient under normal operation.

Outputs HV GPO0, HV GPO1 have individual HV_SLEEP input signal. If Sleep input is active, charge pumps are disabled, and Full Bridge FETs are set to Hi-Z state.

6.10.1 GPO with Matrix OE Structure (for HV GPOs 0 and 1)

Output Mode registers [777:776] for HV_GPO_0, registers [785:784] for HV_GPO_1:
00: Hi-Z mode (High Impedance)
01: NMOS 1x LOW SIDE Open-DRAIN mode (Open-DRAIN LOW side On)
10: NMOS 1x HIGH SIDE Open-DRAIN mode (Open-DRAIN HIGH side On)
11: Push-Pull 1x mode (Open-DRAIN HIGH and LOW sides On)

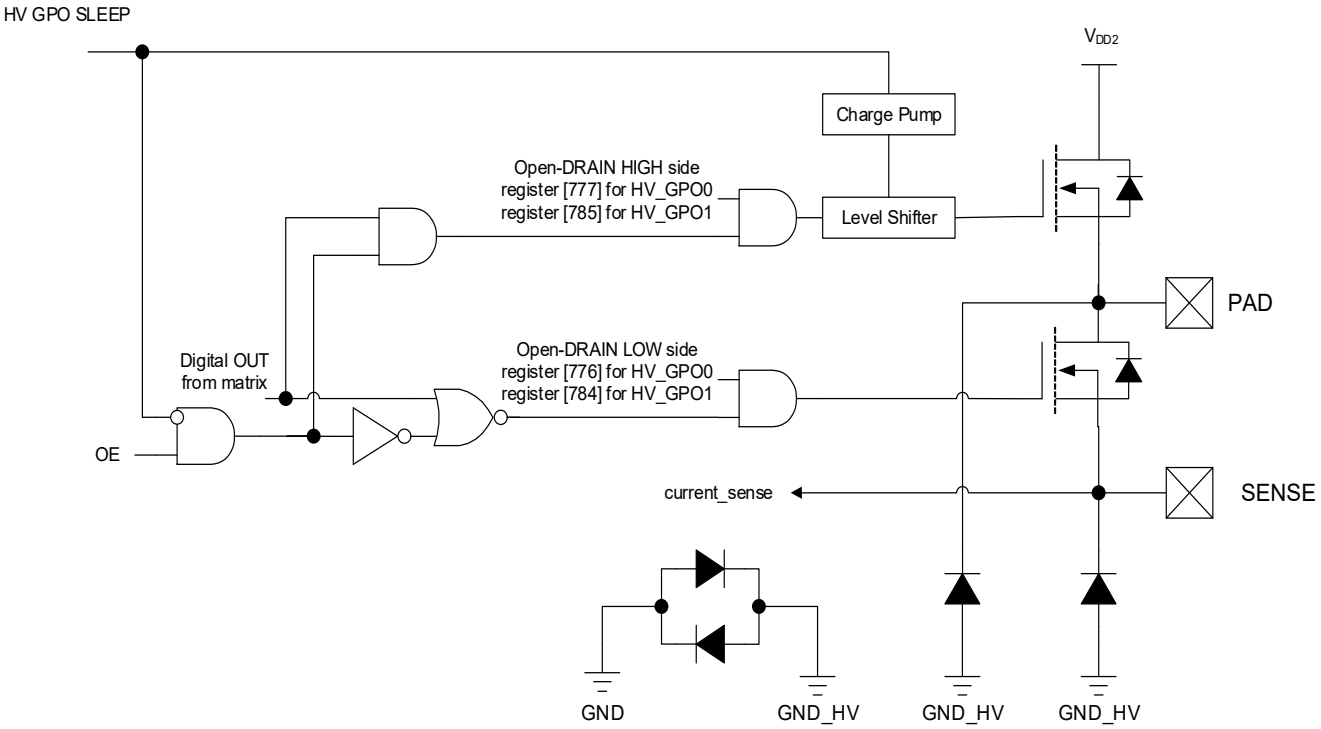


Figure 7. HV GPO Matrix OE IO Structure Diagram (for HV GPOs 0 and 1)

6.11 IO Typical Performance

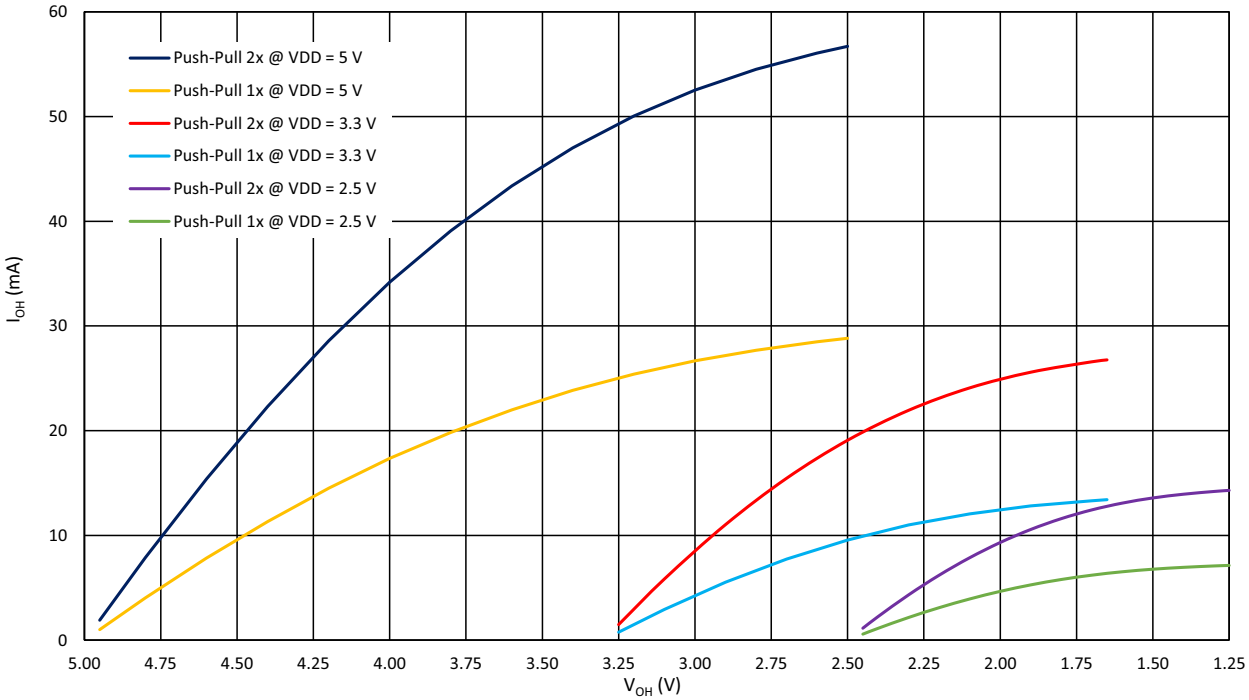


Figure 8. Typical High Level Output Current vs. High Level Output Voltage at T_A = 25 °C

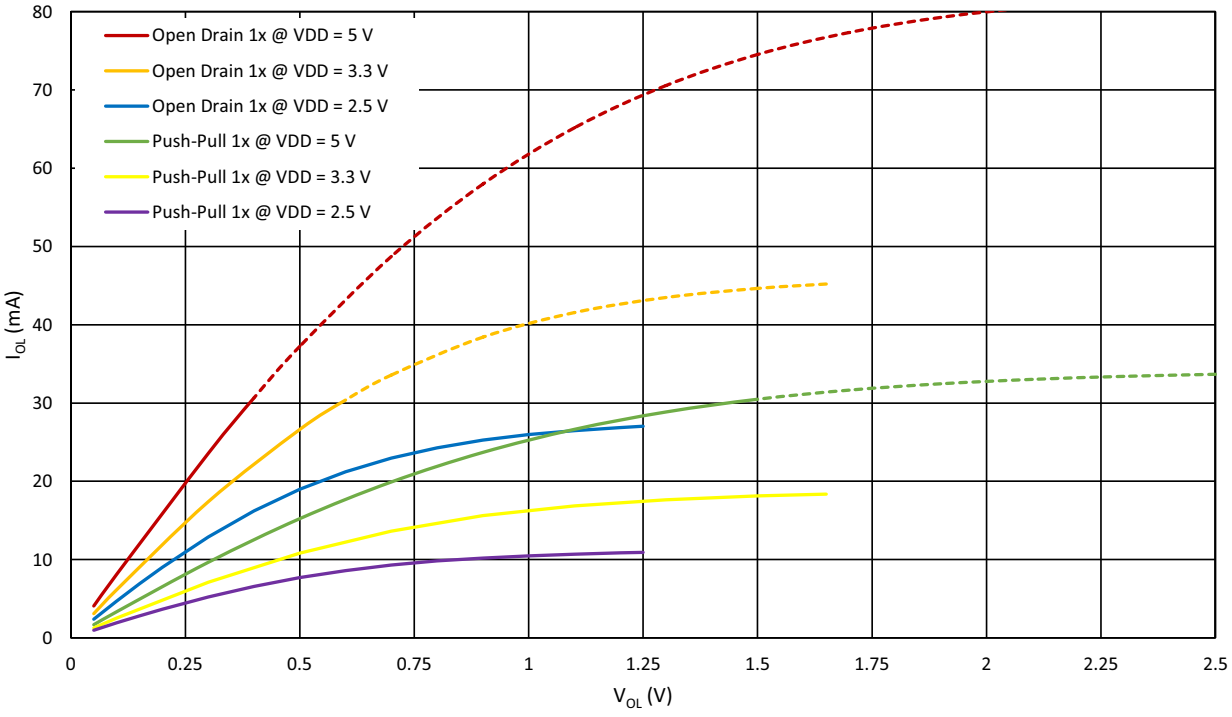


Figure 9. Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T_A = 25 °C, Full Range

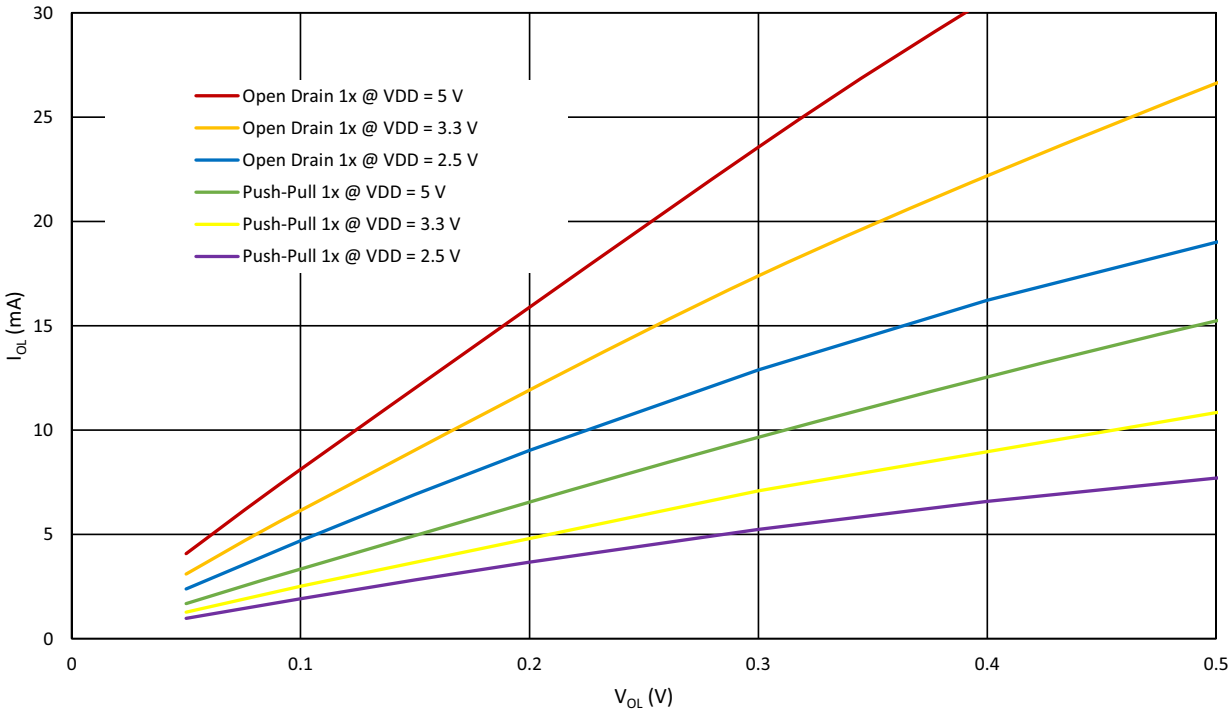


Figure 10. Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T_A = 25 °C

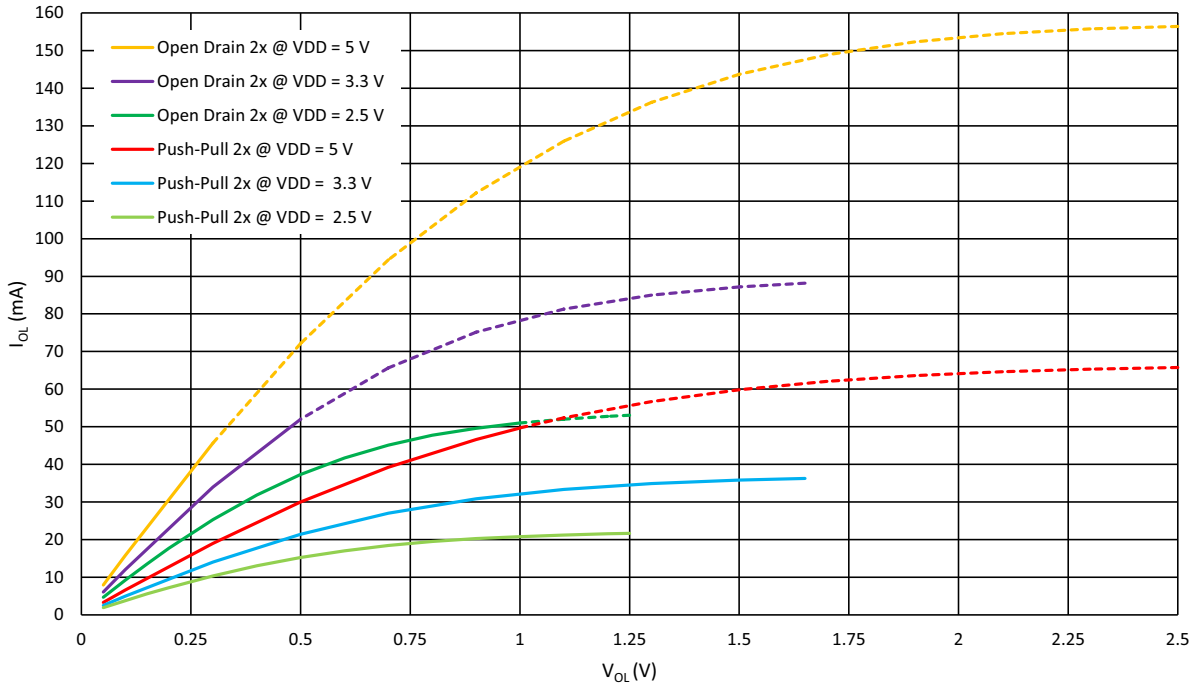


Figure 11. Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T_A = 25 °C, Full Range

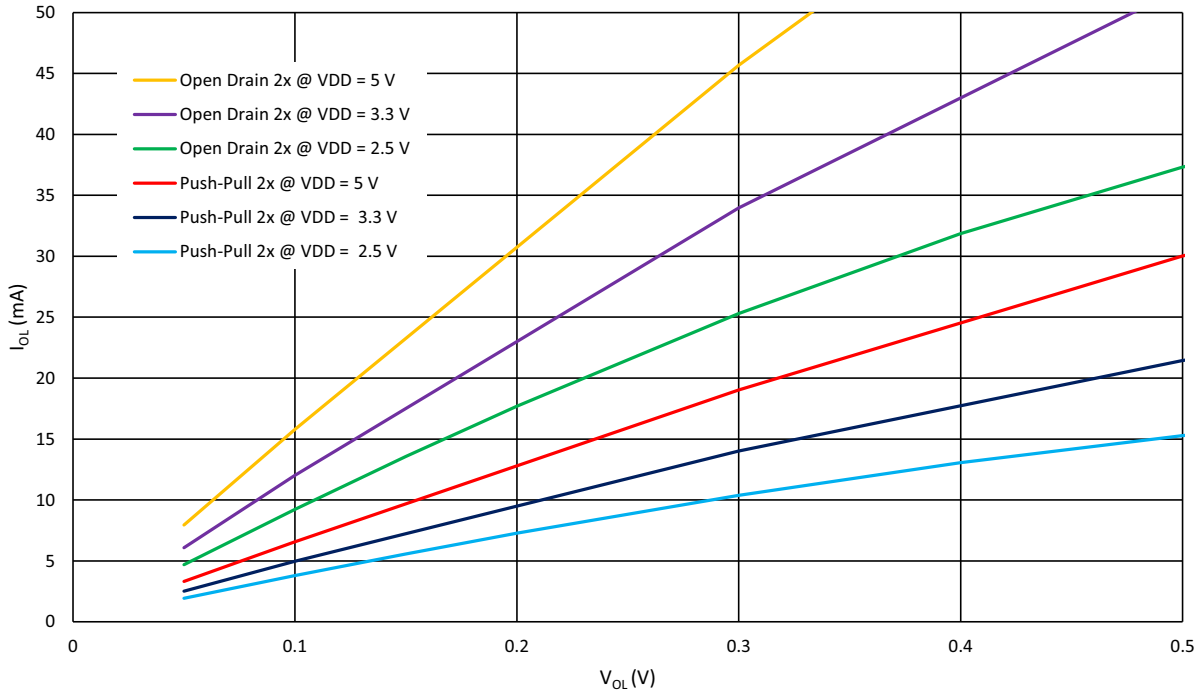


Figure 12. Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T_A = 25 °C

7. High Voltage Output Modes

The device integrates two High Drive Half Bridges, PWM voltage regulation method, current regulation circuitry, and protection circuits, including dead band circuit.

HV GPOs work as power pins, so if two bridges open simultaneously for any reason, for example, timing desynchronization, it will result in cross-conduction (shoot-through) between the two bridges and damage the chip. To avoid this, t_{DEAD} is entered between switching on upper and lower power transistors. During output state transition from LOW to HIGH, the lower NMOS turns off and only after t_{DEAD} the upper NMOS turns on. While t_{DEAD} the pin is in Hi-Z state. The same process is applied when transiting from HIGH to LOW. t_{DEAD} is different for Driver and Pre-Driver modes.

The user can select the Modes of HV outputs:

- Full Bridge Mode;
- Half Bridge Mode.

Additionally, the user can select Slew Rate Modes:

- Slow Slew Rate Motor Driver Mode;
- Fast Slew Rate Pre-Driver Mode.

PWM voltage regulation is useful for designs where there is a need to maintain constant motor speed with changeable power supply level. When the High V_{DD2} is decreasing (battery discharging), it's possible to increase PWM duty cycle, and when the High V_{DD2} is increasing (battery charging) it's possible to decrease PWM duty cycle. It's possible to turn off the PWM and HV GPO for battery saving when the motor is idle, and others.

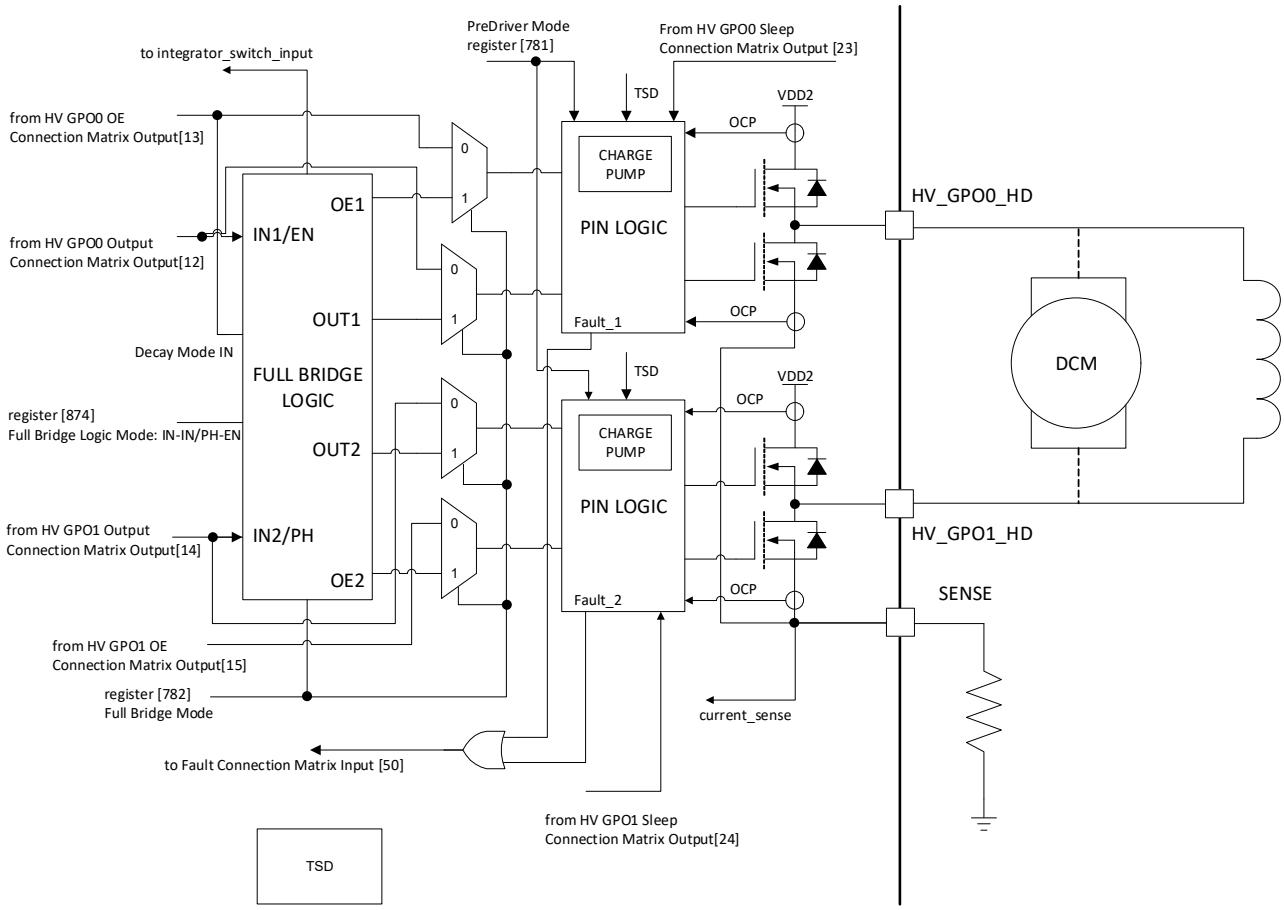


Figure 13. HV OUT Block Diagram

7.1 HV Output Modes

7.1.1 Full Bridge Mode

Full Bridge mode is selected by setting register [782] to 1. In this mode, HV GPO0 functions in couple with HV GPO1. This mode is useful for driving DC motor with the ability to change the motors rotation direction. Also, this mode can be used to drive one winding of stepper motor as shown in the figure below.

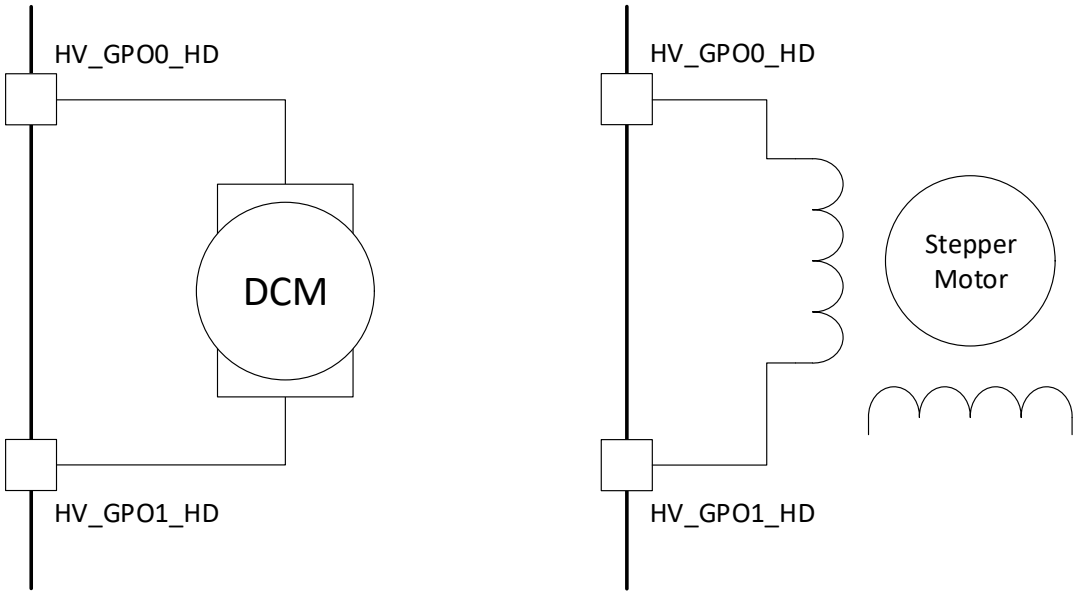


Figure 14. Full Bridge Mode Operation

OE inputs of high voltage pins aren't used in Full Bridge mode except HV GPO0 OE input in PH-EN sub-mode, where these inputs are used to select decay mode for Full Bridge. Other inputs and outputs operate depending on Control Selection register [874] as shown below:

Table 32. HV OUT CTRL Full Bridge Logic for IN-IN Mode

Sleep_x	IN0	IN1	HV_GPO0_HD (pins 7, 8)	HV_GPO1_HD (pins 9, 10)	Function
1	X	X	Hi-Z	Hi-Z	Off (coast)
0	0	0	Hi-Z	Hi-Z	Coast
0	0	1	L	H	Reverse
0	1	0	H	L	Forward
0	1	1	L	L	Brake

Note: Sleep 0 and Sleep 1 should be connected together in Full Bridge mode for each HV OUT CTRL block.

Table 33. HV OUT CTRL Full Bridge Logic for PH-EN Mode

Sleep_x	Decay	EN	PH	HV_GPO0_HD (pins 7, 8)	HV_GPO1_HD (pins 9, 10)	Function
1	X	X	X	Hi-Z	Hi-Z	Off (coast)
0	0 (Fast decay)	0	X	Hi-Z	Hi-Z	Coast
0	1 (Slow decay)	0	X	L	L	Brake

Table 33. HV OUT CTRL Full Bridge Logic for PH-EN Mode (Cont.)

Sleep_x	Decay	EN	PH	HV_GPO0_HD (pins 7, 8)	HV_GPO1_HD (pins 9, 10)	Function
0	X	1	0	H	L	Forward
0	X	1	1	L	H	Reverse

HV GPO0 and HV GPO1 are tri-state pins, which can't be pulled up/down internally.

The HV GPOs can be used to control the motor speed with the help of PWM technique. Fast Decay mode causes a rapid reduction in inductive current and allows the motor to coast toward zero velocity. Slow Decay mode leads to a slower reduction in inductive current, but produces rapid deceleration.

In IN-IN mode, to drive DC motor in fast-decay mode, the PWM signal should be applied to one of IN0 or IN1 inputs, while the other is held in the logic LOW state. To use Slow Decay mode, one of IN0 or IN1 inputs should be sourced by PWM signal, while the opposite pin is held in the logic HIGH state.

Table 34. PWM Control of Motor Speed (IN-IN Mode)

IN0	IN1	Function
PWM	0	Forward PWM, fast decay
1	PWM	Forward PWM, slow decay
0	PWM	Reverse PWM, fast decay
PWM	1	Reverse PWM, slow decay

PH-EN mode is convenient for Full Bridge control by internal PWM macrocell, because PWM signal is connected to EN input only. In this case there is no need to use an additional MUXs. Rotation direction is changed by PH input.

Table 35. PWM Control of Motor Speed (PH-EN Mode)

Decay	EN	PH	Function
0	PWM	0	Forward PWM, fast decay
0	PWM	1	Reverse PWM, fast decay
1	PWM	0	Forward PWM, slow decay
1	PWM	1	Reverse PWM, slow decay

Figure 15 shows the current paths in a different drive and decay modes.

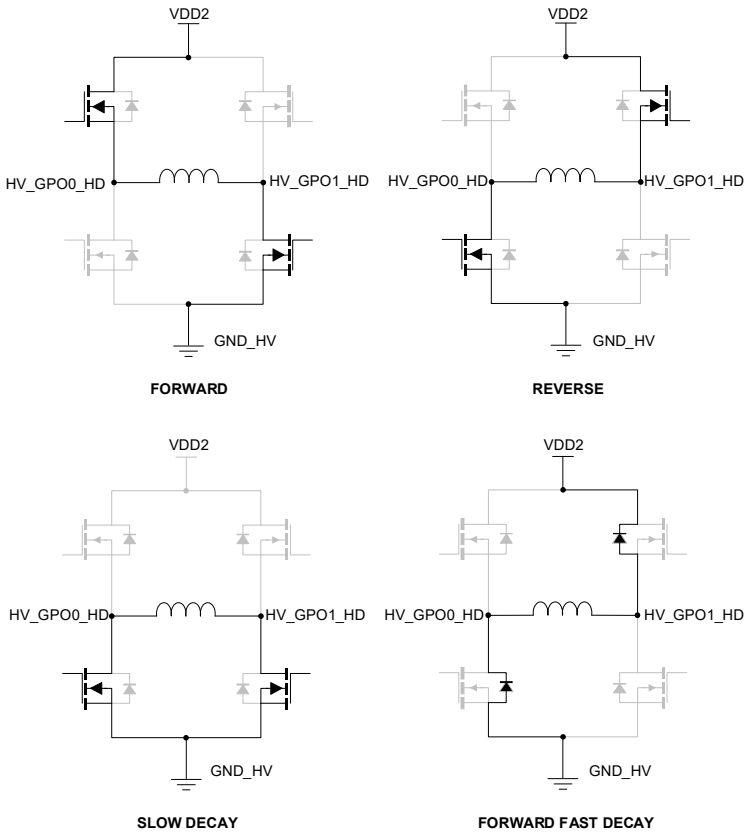


Figure 15. Drive and Decay Modes

7.1.2 Half Bridge Mode

Half Bridge mode is selected by setting register [782] to 0. This mode is the default mode for HV GPO pins. In this mode, there is a possibility to drive up to two motors spinning in one direction.

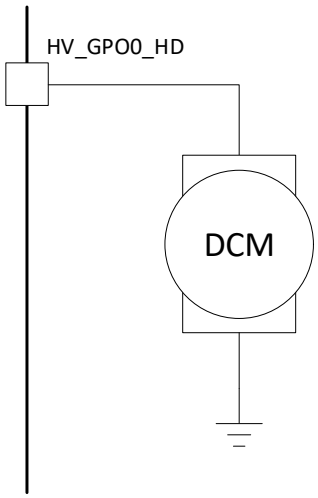


Figure 16. Half Bridge Mode Operation

In Half Bridge mode HV GPO will work as shown in Table 36 to Table 37.

Table 36. HV_GPO0_HD Half Bridge Logic

Function	Sleep0	OE0	IN0	HV_GPO0_HD (pins 7, 8)
Off	1	X	X	Hi-Z
Off (coast)	0	0	X	Hi-Z
Brake	0	1	0	L
Forward	0	1	1	H

Table 37. HV_GPO1_HD Half Bridge Logic

Function	Sleep1	OE1	IN1	HV_GPO1_HD (pins 9, 10)
Off	1	X	X	Hi-Z
Off (coast)	0	0	X	Hi-Z
Brake	0	1	0	L
Forward	0	1	1	H

7.2 Fast Slew Rate Pre-Driver Mode

This mode is activated by setting register [781] to 1. The difference of this mode is that the rise time t_R and fall time t_F of High Drive HV GPO MOSFETs are much smaller, than in regular mode. This allows using SLG47115 as a driver for external transistors.

When this mode is active, user can configure HV GPO to work in Full Bridge or Half Bridge modes, as well as in regular mode (Pre-Driver mode is disabled, register [781] = 0).

7.3 Parallel Connection of HV GPO

The user can connect outputs in parallel to increase current rating. Note that this mode has no special register for activation.

Note that user can configure HV GPO outputs in Half Bridge mode and connect them in parallel. In this case, user must take care of HV GPO control to prevent short circuit.

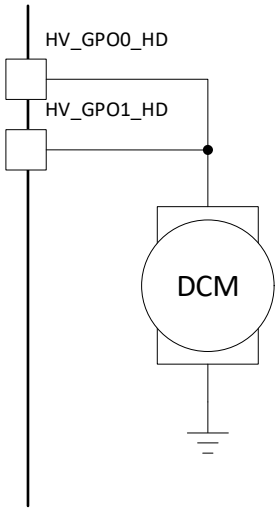


Figure 17. Parallel Connection of HV GPOs for Half Bridge Mode

7.4 Protection Circuits

7.4.1 General FAULT Signals

The SLG47115 has three types of FAULT signals. One of them is FAULT signal. It is the general signal which consists of all available FAULT signals for V_{DD2}.

FAULT:

- Over-Current Protection (OCP)
- Thermal Shutdown (TSD)
- Under-Voltage Lockout (UVLO)

For more information on each of FAULT signals see Section 7.4.3 Over-Current Protection, Section 7.4.4 Thermal Shutdown and Thermal Considerations, and Section 7.4.5 Under-Voltage Lockout.

7.4.2 Advanced Current Control

A current control circuit is provided to regulate the system in the event of an overcurrent condition, for example, an abnormal mechanical load of DC motor. This circuit can be used for implementing constant current closed loop systems or for current limitation.

The current is sensed by external sense resistor connected to Sense pin. Current comparator is used to convert these current to logic level. Using a current comparator with PWM block, output current can be dynamically changed. For example, for a stepper motor in micro stepping it is possible to set 16 values for sinusoidal current limit form.

7.4.3 Over-Current Protection

Each of FETs has an analog current limit circuit for turning off FETs when the current exceeds the threshold. When the overcurrent (I_{OCP}) persists for longer than the t_{OCP1} time, the FETs in the Half Bridge are disabled, and FAULT signal to matrix driven high. t_{OCP1} time is optional. It can be enabled by register [873] for HV GPO0/1. When this option is disabled, OCP circuit reacts immediately without deglitch time. The FETs will be disabled along t_{OCP2} time when the current decreases to a normal value. t_{OCP2} could be changed by setting the registers (HV GPO0 - registers[780:778], HV GPO1 - registers[788:786]). Overcurrent conditions are detected for both High-side and Low-side FETs. There is a special type of matrix input FAULT [60] for OCP_FAULT.

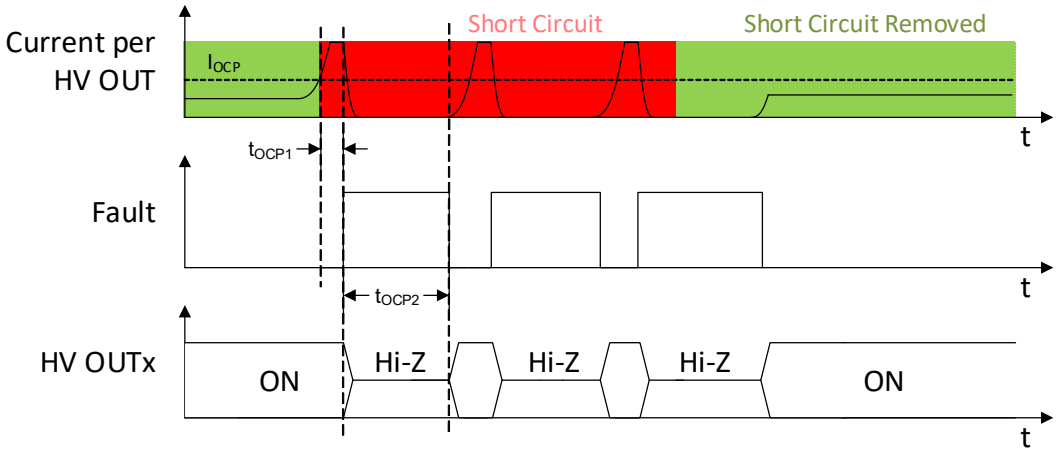


Figure 18. Overcurrent Protection Operation

7.4.4 Thermal Shutdown and Thermal Considerations

If the die temperature exceeds safe limits thermal shutdown (TSD), all output FETs in any Full or Half Bridge are disabled. After the die temperature has fallen to a safe level, operation automatically resumes. Note that TSD is active only during HV GPOs are wake. When all HV GPOs are in power-down, TSD function is inactive. The SLG47115 has a special package optimized for better heat dissipation. All HV output pins and central plates should be thermally connected to copper traces or pads on the PCB for better heat dissipation. It is recommended to use thermal vias under the Ground and V_{DD} plates for the better thermal characteristic.

TSD_FAULT signal is connected to matrix input [62]. TSD_FAULT signal is also present in FAULT signal.

7.4.5 Under-Voltage Lockout

When the voltage on the V_{DD2} pin goes less than the V_{UVLO} at falling edge, then the HV_GPOx outputs are disabled, the Fault output is driven HIGH. When the voltage rises to the V_{UVLO} at rising edge, then the Fault output is driven LOW and operating is restored.

UVLO can be enabled for V_{DD2} by register [864].

7.5 PWM Voltage Control

The SLG47115 provides the ability to control the voltage applied to the motor winding. This feature allows achieving constant motor speed during supply voltage variations.

The best way to use this function is to enable Full Bridge mode and use the integrator on Full Bridge. The integrator output is connected to the positive input of a separate analog comparator. Also, the Vref value on the negative comparator input must be selected. The integrator monitors the voltage difference between HV_GPO0_HD and HV_GPO1_HD pins of Full Bridge and integrates it to get an average voltage value.

The outputs of the comparator should be connected to the PWM block with or without an additional logic circuit. If the average output voltage is lower than the Vref, the duty cycle of the PWM output needs to increase; if the average output value is higher than Vref, the duty cycle needs to decrease; when the average output value is equal to comparator threshold, PWM duty cycle is kept by the EQUAL output of integrator macrocell.

Note that if the desired output voltage (reference of the ACMP) is greater than the supply voltage, the device will operate at 100% duty cycle and the voltage regulation feature will be disabled. In this mode, the device behaves as a conventional Full Bridge driver.

7.6 High Voltage Outputs Typical Performance

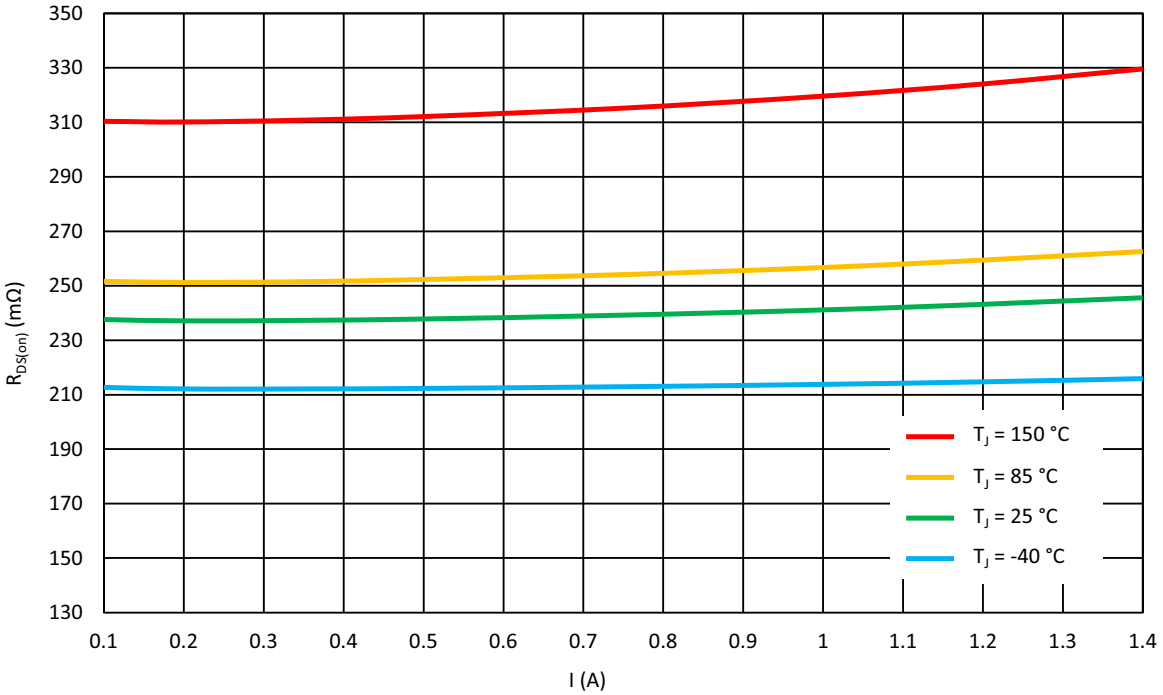


Figure 19. Full Bridge High-Side Typical Drain-Source On-Resistance vs. Load Current at V_{DD} = 5.5 V, V_{DD2} = 5 V

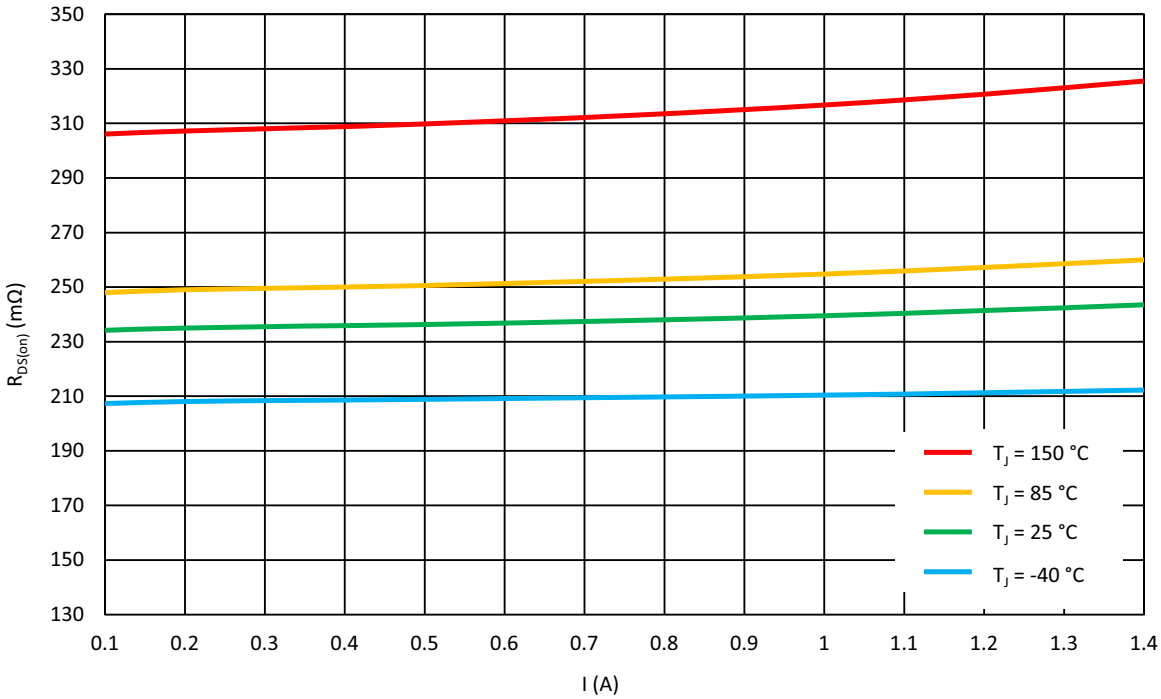


Figure 20. Full Bridge Low-Side Typical Drain-Source On-Resistance vs. Load Current at V_{DD} = 5.5 V, V_{DD2} = 5 V

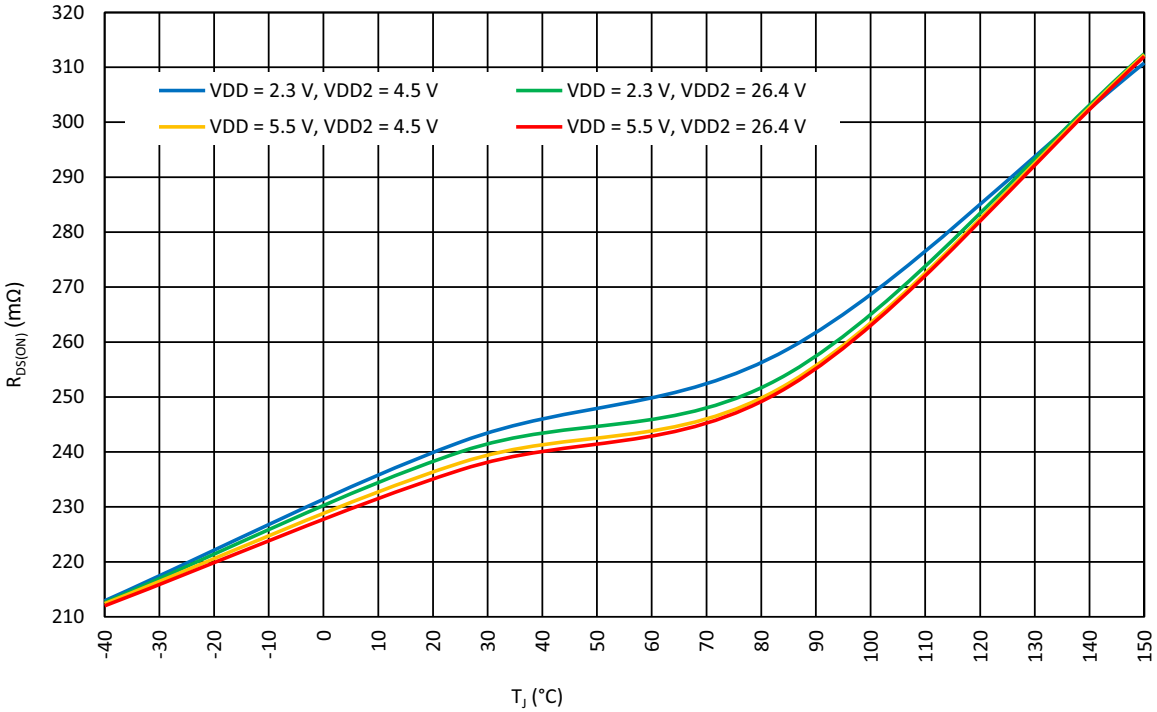


Figure 21. Full Bridge High Side Typical Drain-Source On-Resistance vs. Temperature at I_{LOAD} = 0.5 A

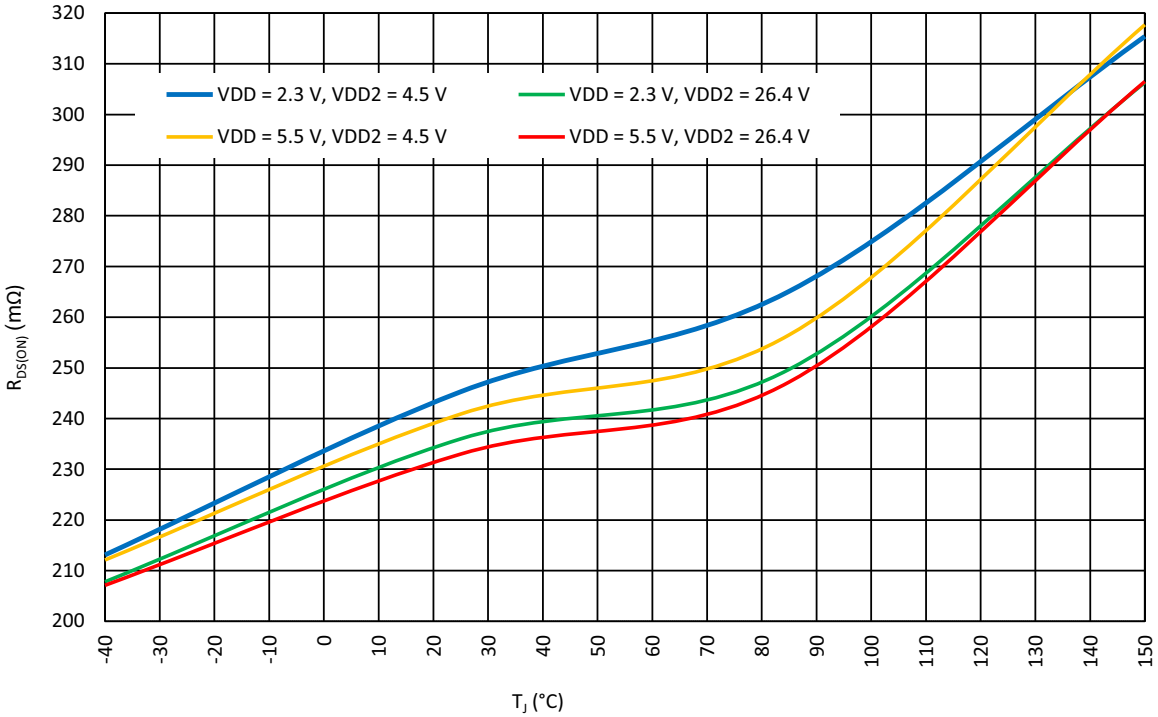


Figure 22. Full Bridge Low-Side Typical Drain-Source On-Resistance vs. Temperature at I_{LOAD} = 0.5 A

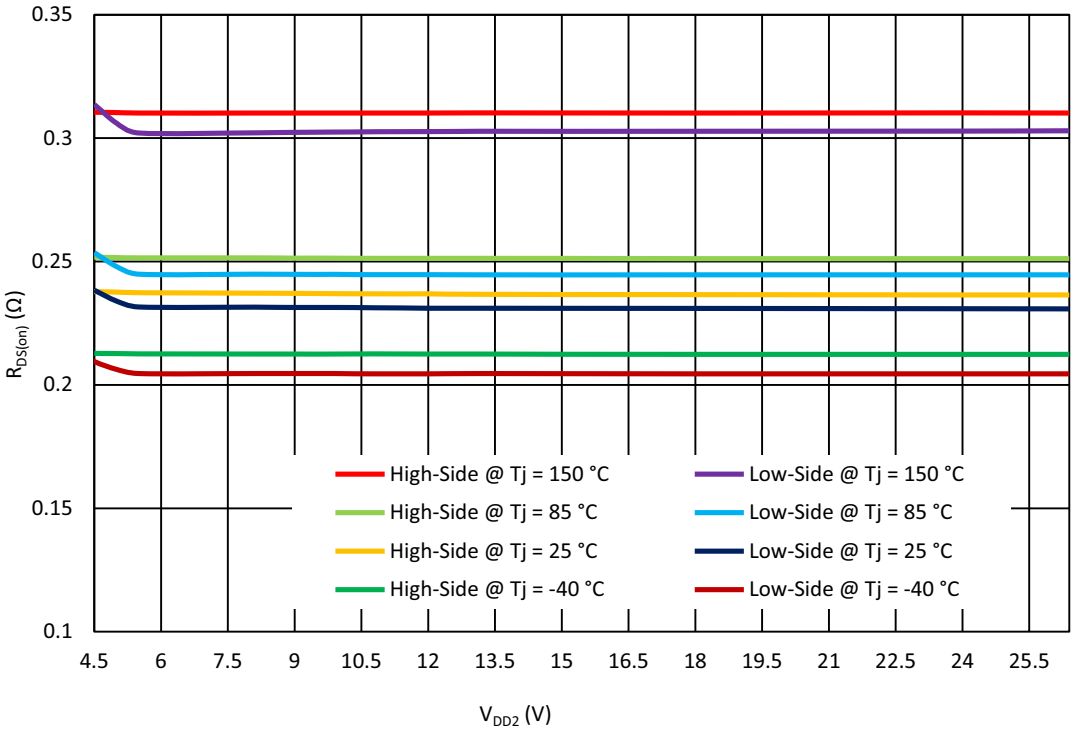


Figure 23. Full Bridge Typical Drain-Source On-Resistance vs. V_{DD2} at V_{DD} = 5.5 V, I_{LOAD} = 0.1 A

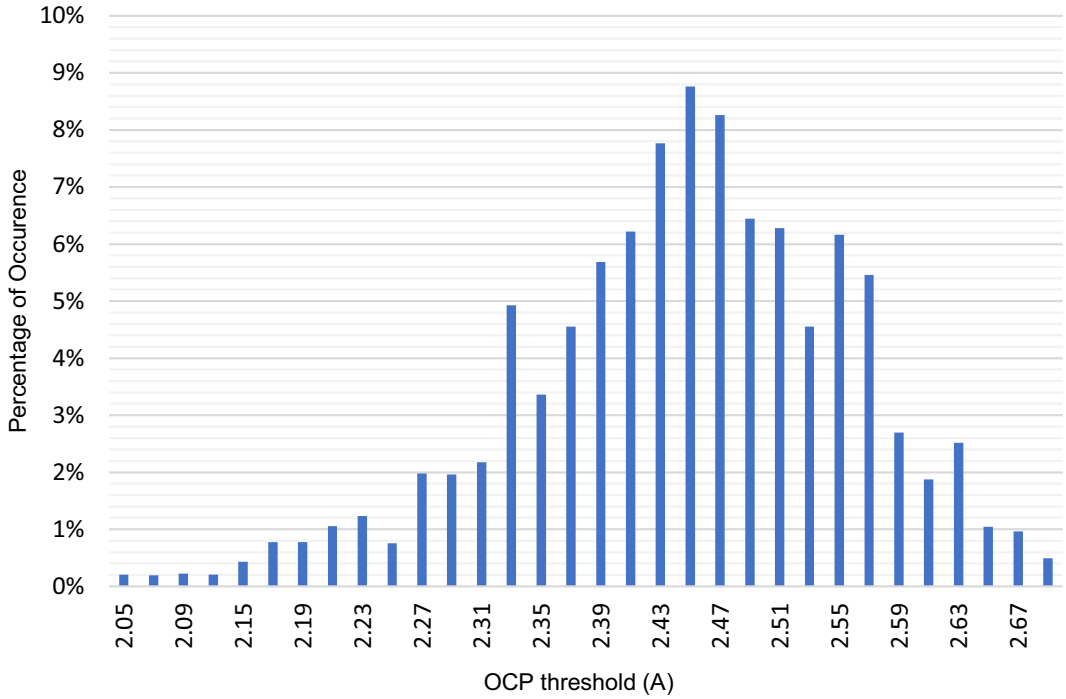


Figure 24. Full Bridge High-side OCP Threshold Distribution at V_{DD}=2.3V to 5.5V, V_{DD2}=3V to 26.4V, T_J=-40 °C to 150°C

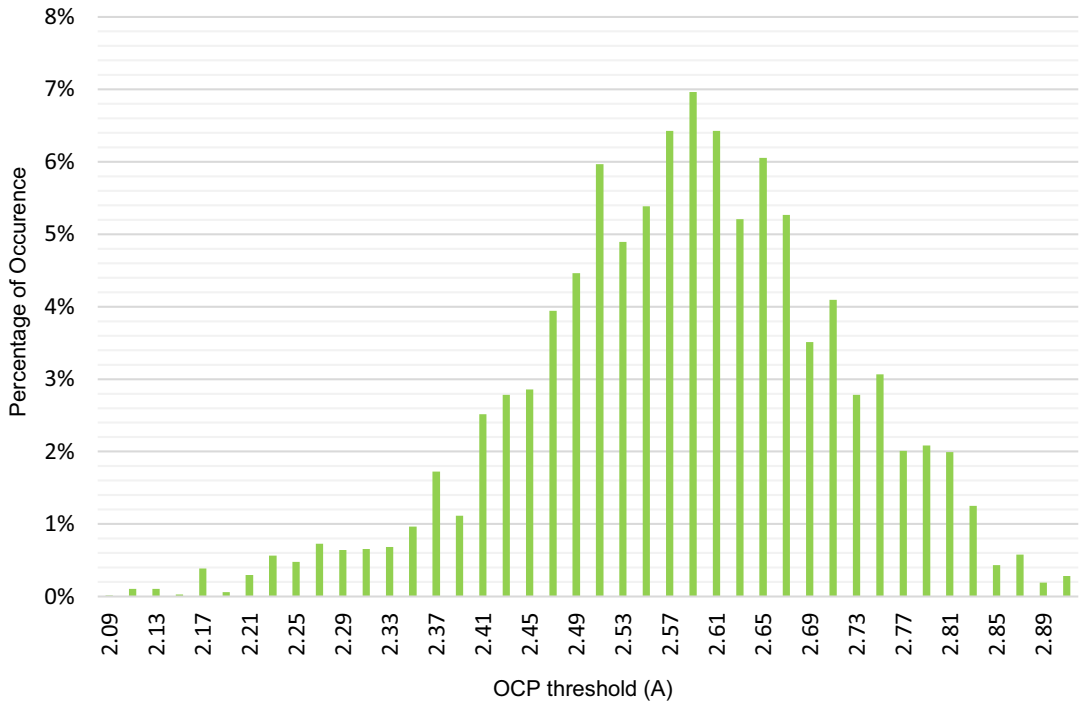


Figure 25. Full Bridge Low-side OCP Threshold Distribution at V_{DD}=2.3V to 5.5V, V_{DD2}=3V to 26.4V, T_J=-40 °C to 150°C

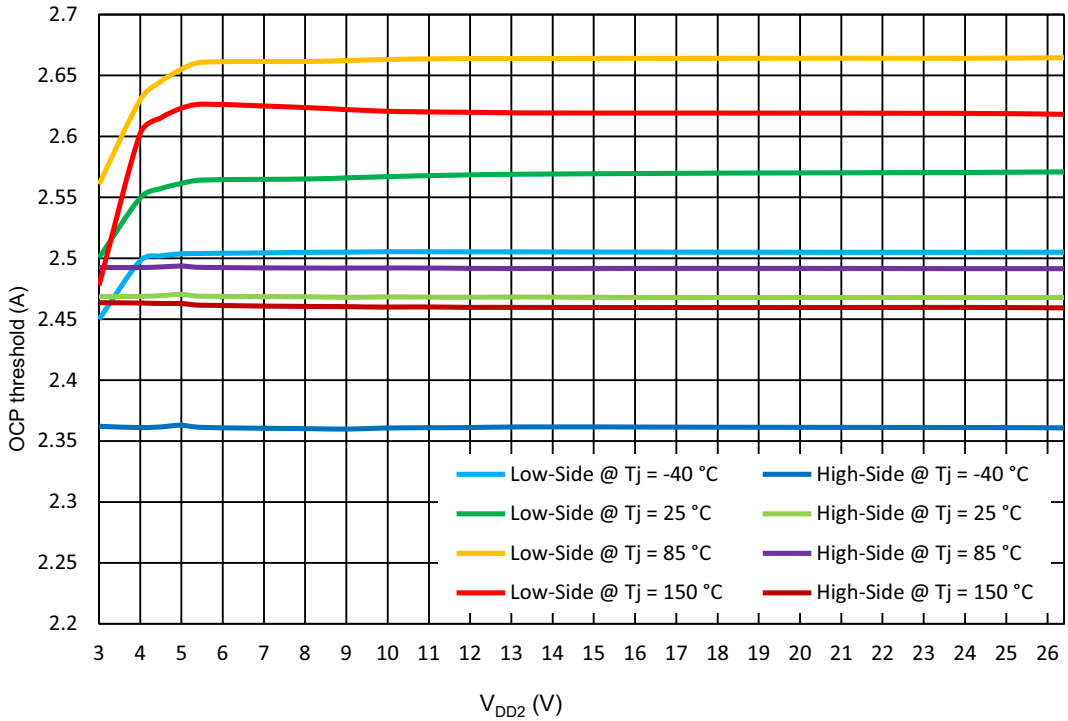


Figure 26. Full Bridge OCP Threshold vs. V_{DD2} at V_{DD} = 5.5 V

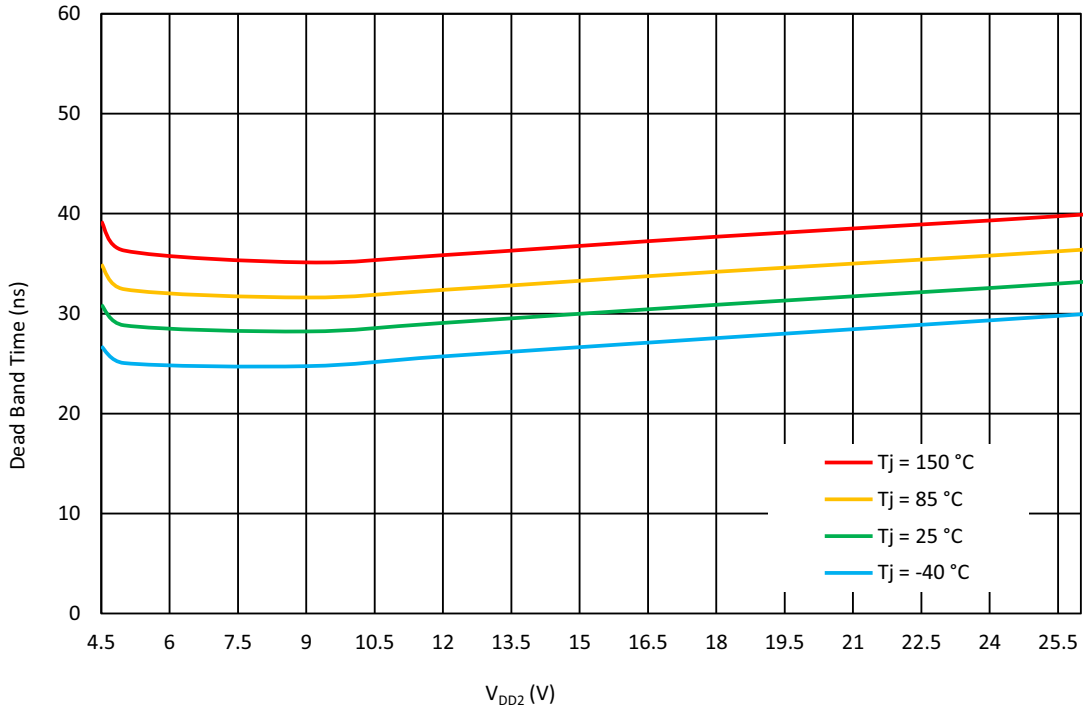


Figure 27. Half Bridge Dead Band Time vs. V_{DD2} at V_{DD} = 2.3 V to 5.5 V, Rising Signal, f = 50 kHz for Pre-Driver Mode

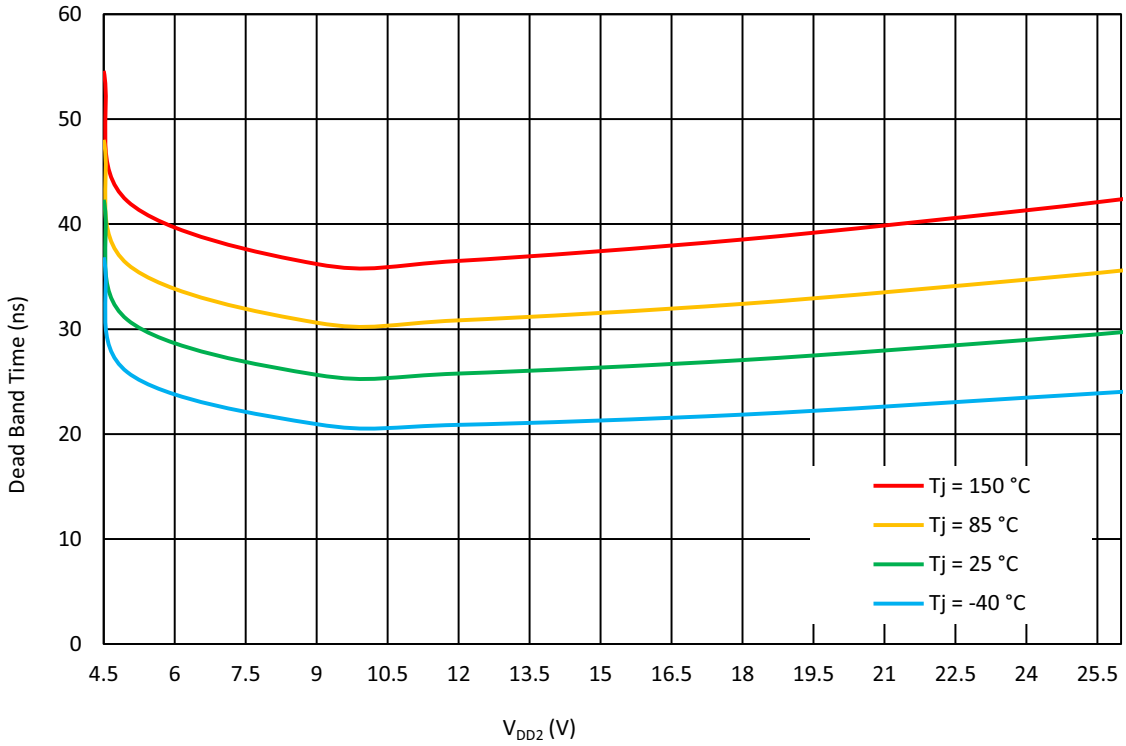


Figure 28. Half Bridge Dead Band Time vs. V_{DD2} at V_{DD} = 2.3 V to 5.5 V, Falling Signal, f = 50 kHz for Pre-Driver Mode

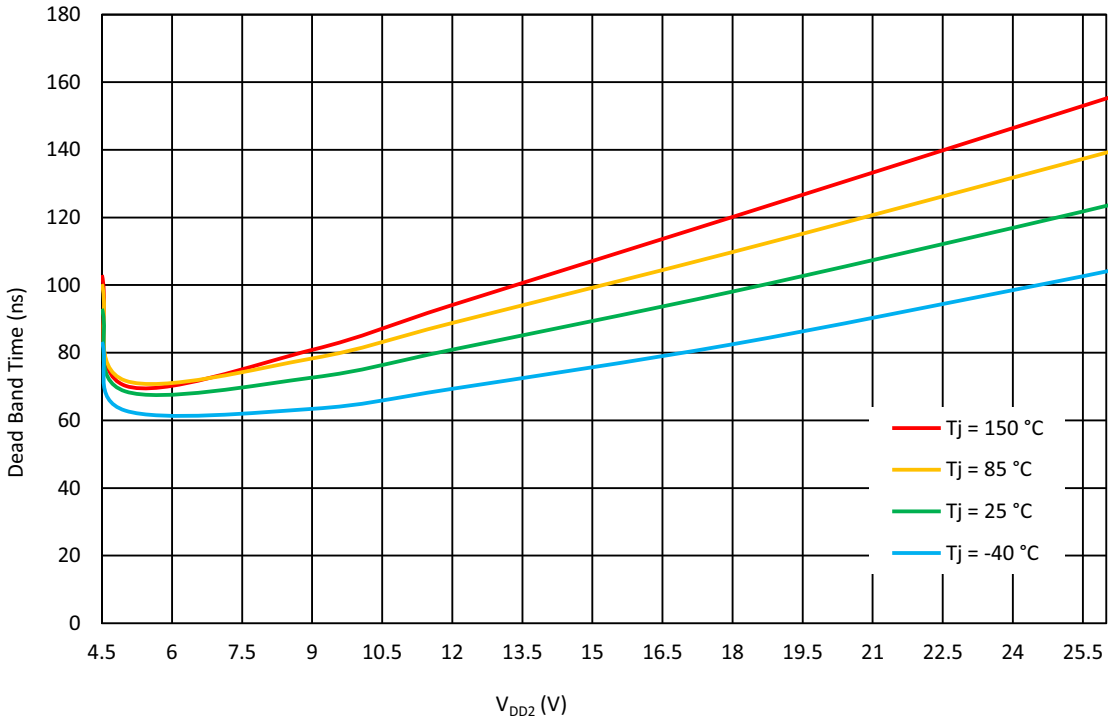


Figure 29. Half Bridge Dead Band Time vs. V_{DD2} at V_{DD} = 2.3 V to 5.5 V, Rising Signal, f = 50 kHz, for Regular Mode

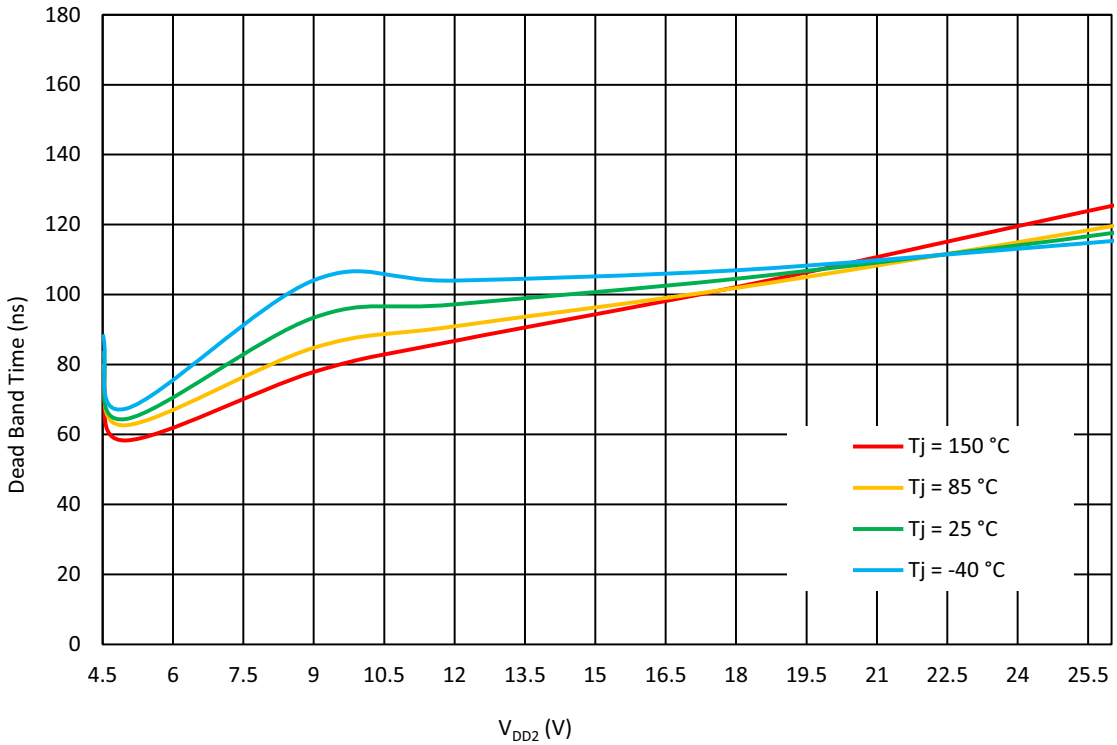


Figure 30. Half Bridge Dead Band Time vs. V_{DD2} at V_{DD} = 2.3 V to 5.5 V, Falling Signal, f = 50 kHz for Regular Mode

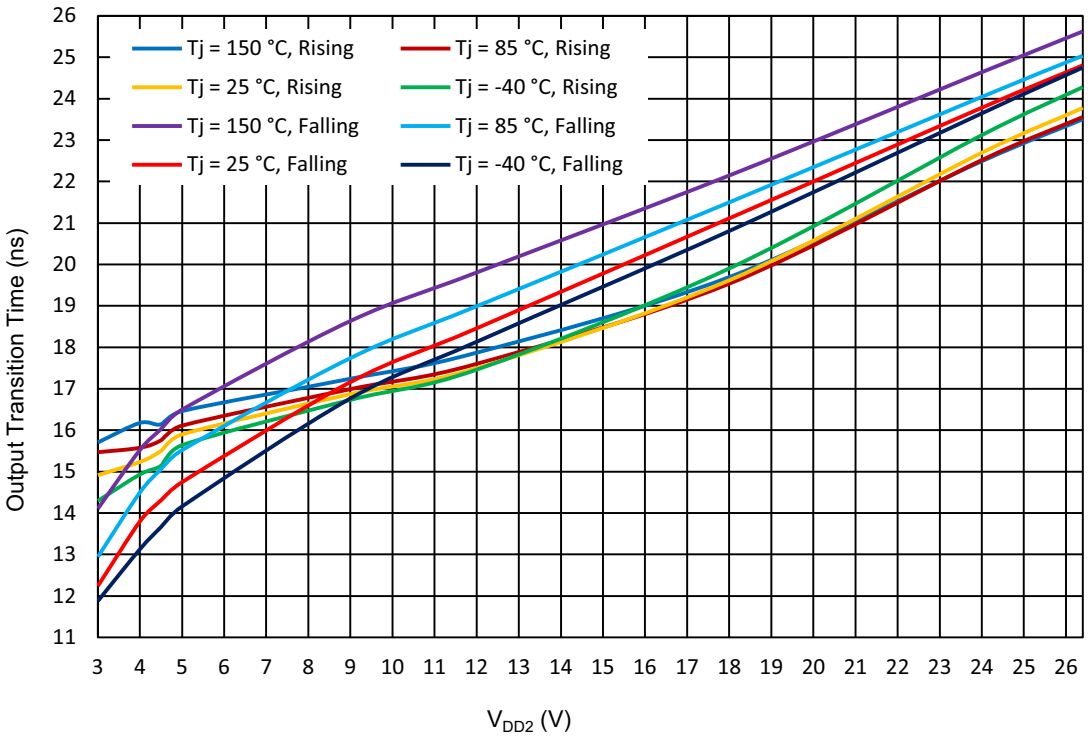


Figure 31. Half Bridge Output Transition Time vs. V_{DD2} at V_{DD} = 2.3 V to 5.5 V, f = 50 kHz for Pre-Driver Mode

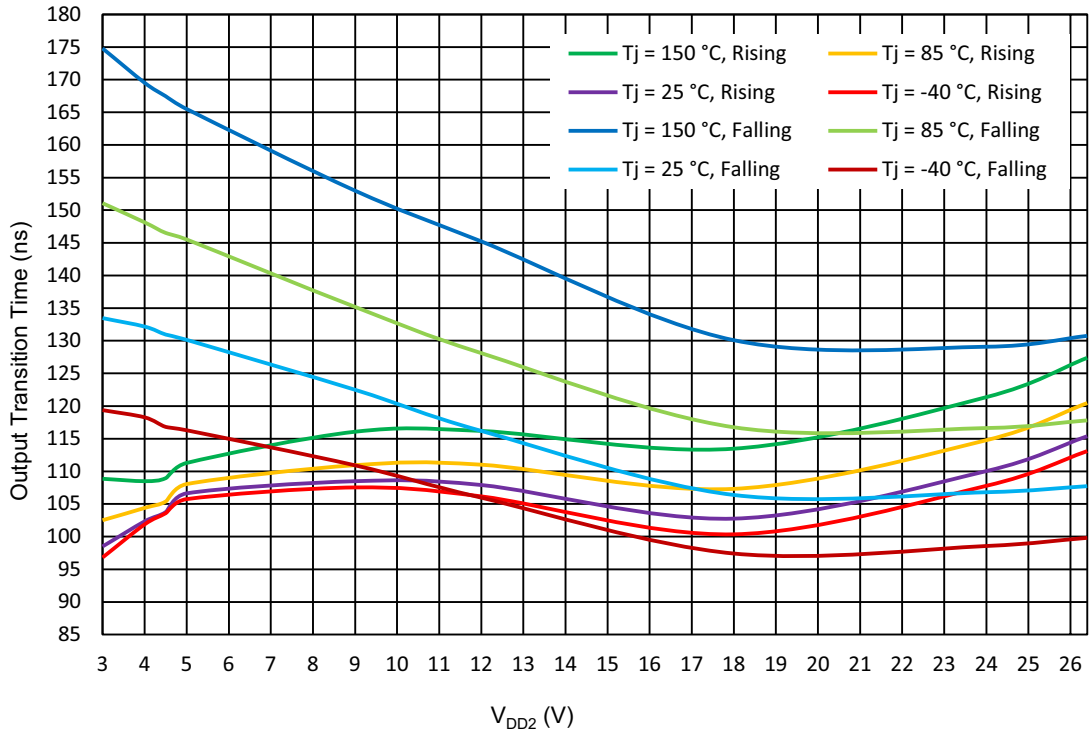


Figure 32. Half Bridge Output Transition Time vs. V_{DD2} at V_{DD} = 2.3 V to 5.5 V, f = 50 kHz for Regular Mode

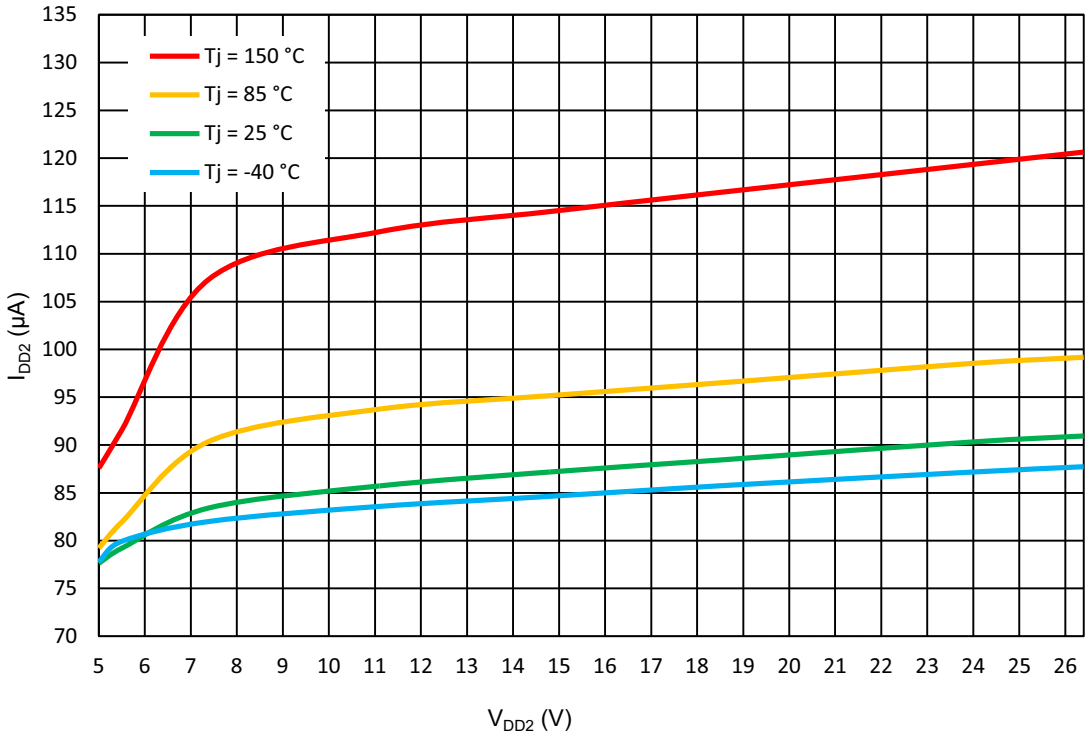


Figure 33. One Half Bridge I_{DD2} vs.V_{DD2} at V_{DD} = 5.5 V

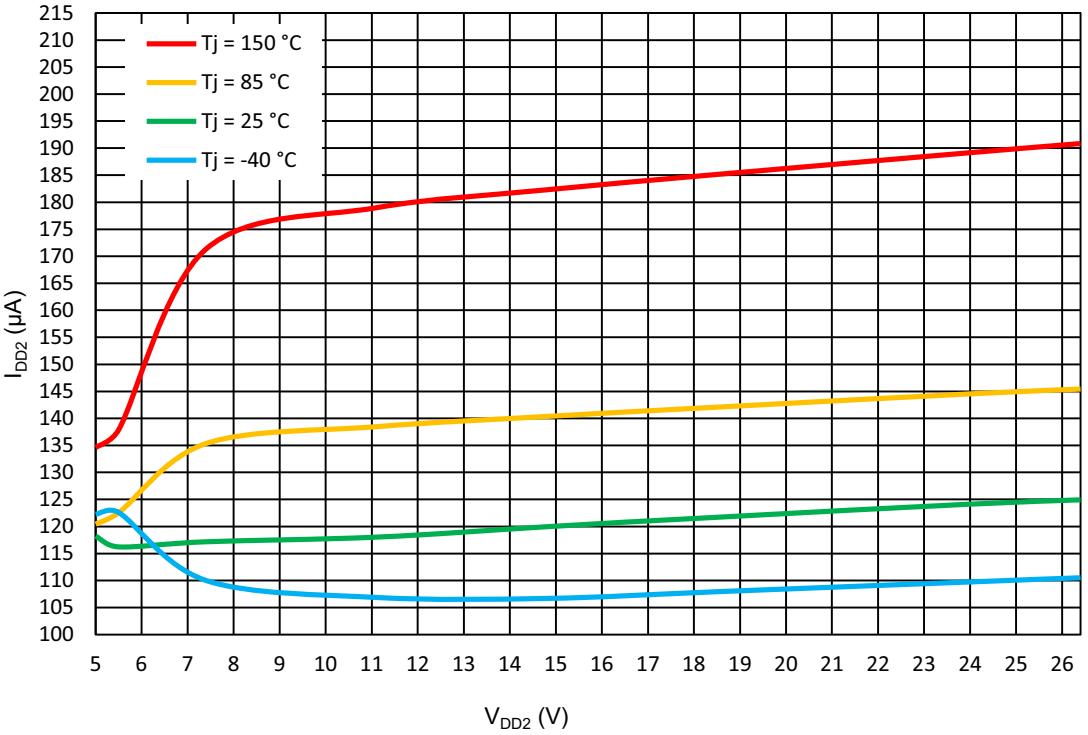


Figure 34. Full Bridge I_{DD2} vs. V_{DD2} at V_{DD} = 5.5 V

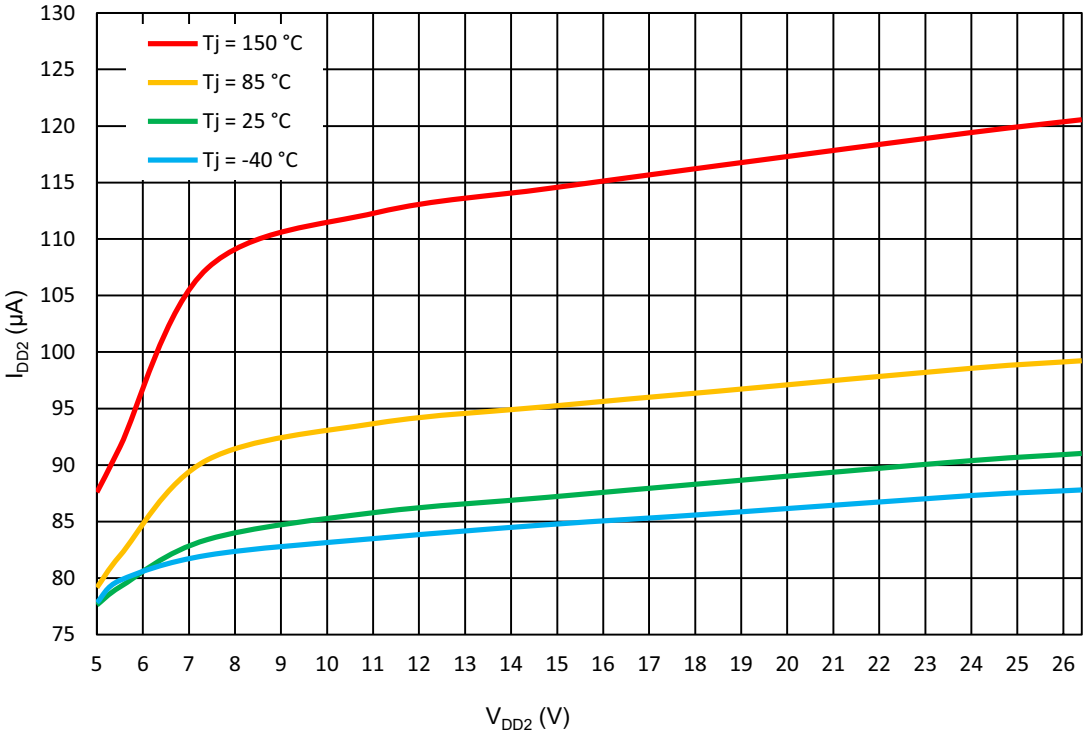


Figure 35. One Half Bridge + CCMP I_{DD2} vs. V_{DD2} at V_{DD} = 5.5 V

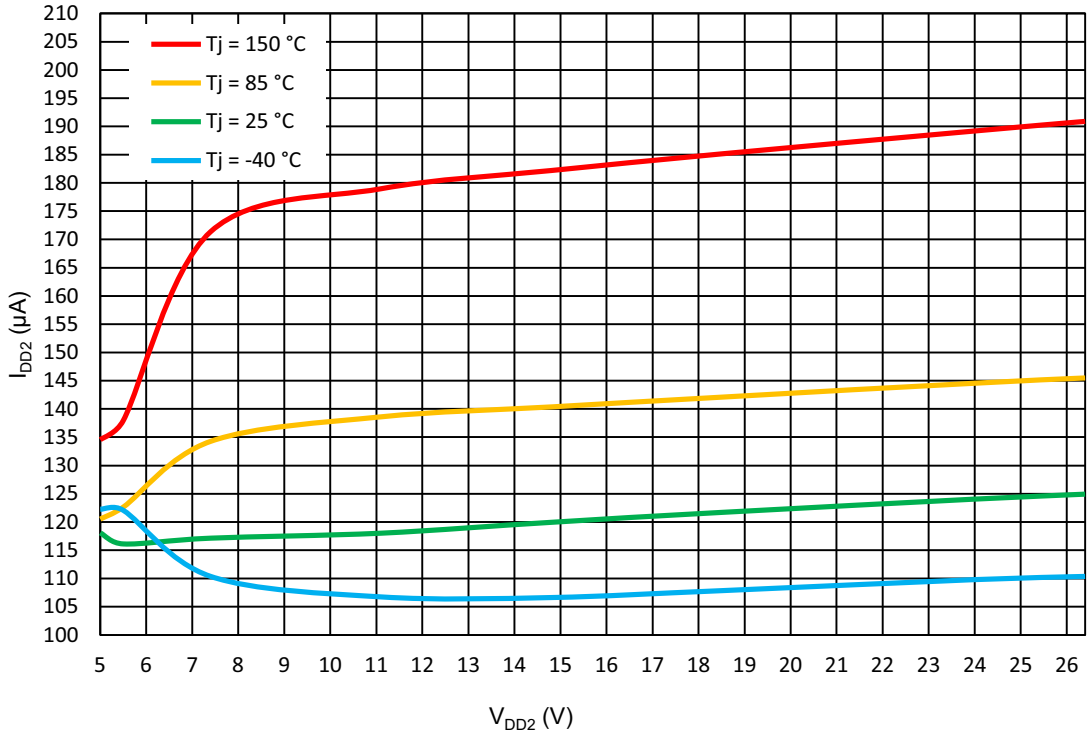


Figure 36. Full Bridge + CCMP I_{DD2} vs. V_{DD2} at V_{DD} = 5.5 V

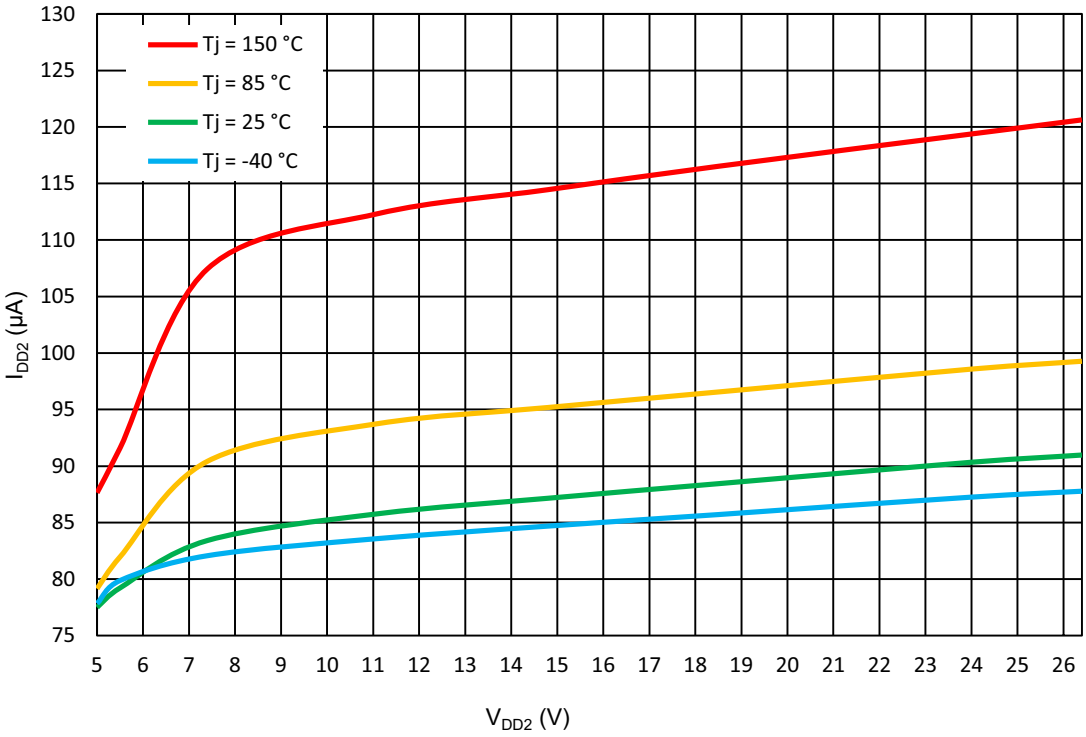


Figure 37. One Half Bridge + Integrator + PWM + OSC1 I_{DD2} vs. V_{DD2} at V_{DD} = 5.5 V

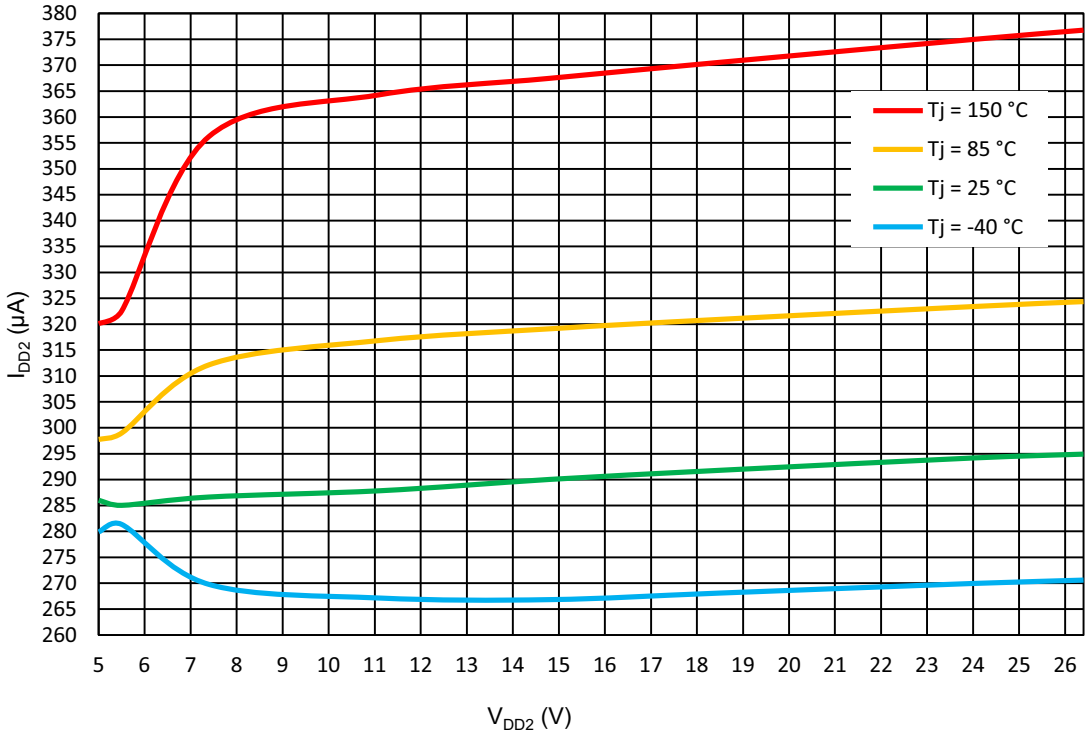


Figure 38. Full Bridge + Integrator + PWM + OSC1 I_{DD2} vs. V_{DD2} at V_{DD} = 5.5 V

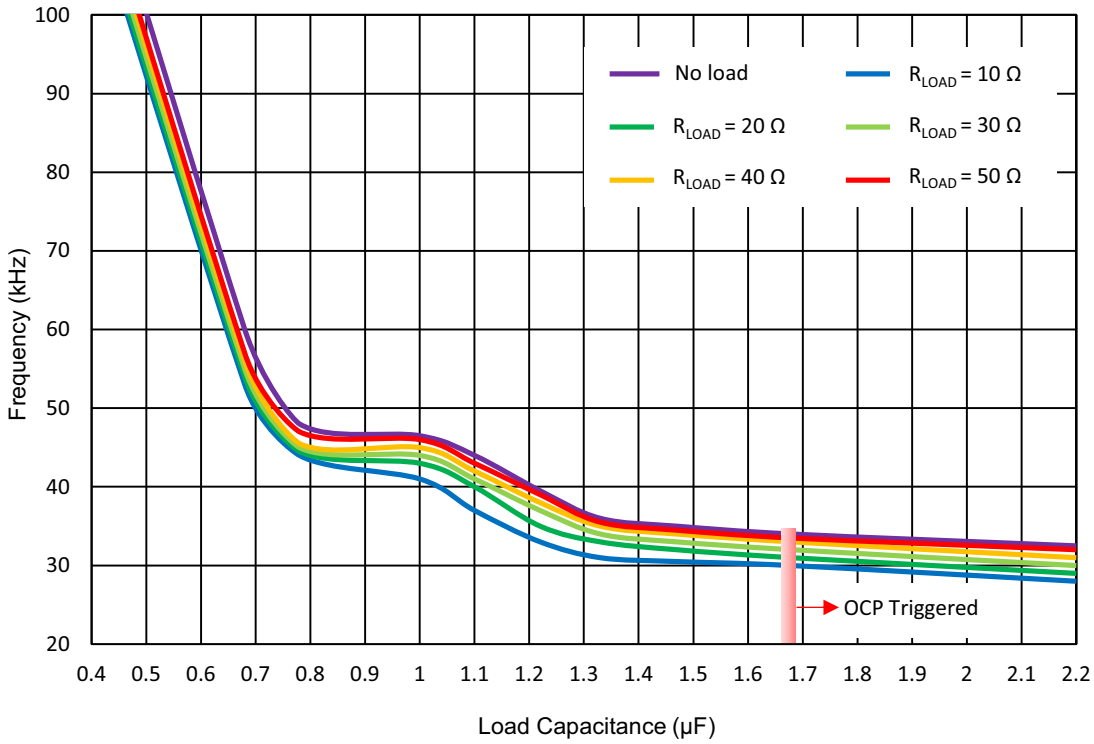


Figure 39. Two Half Bridges in Parallel Safe Operating Area. Frequency vs. C_{LOAD} at T_A = 25 °C, V_{DD2} = 24 V

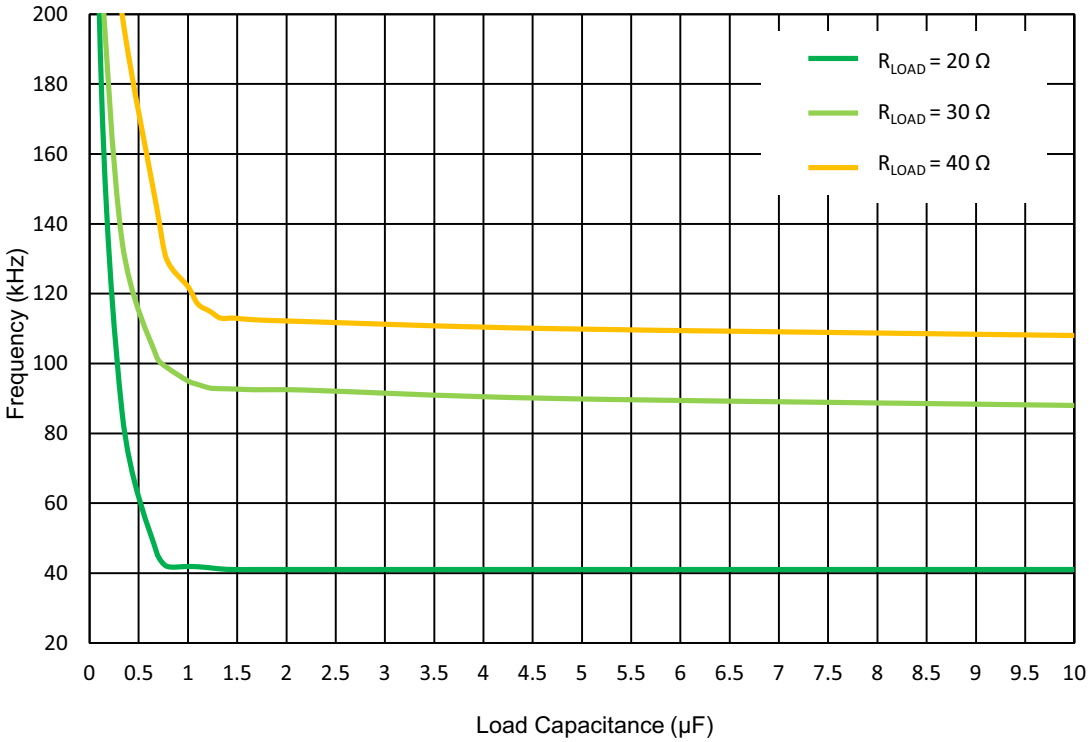


Figure 40. Full Bridge Safe Operating Area. Frequency vs. C_{LOAD} at T_A = 25 °C, V_{DD2} = 24 V

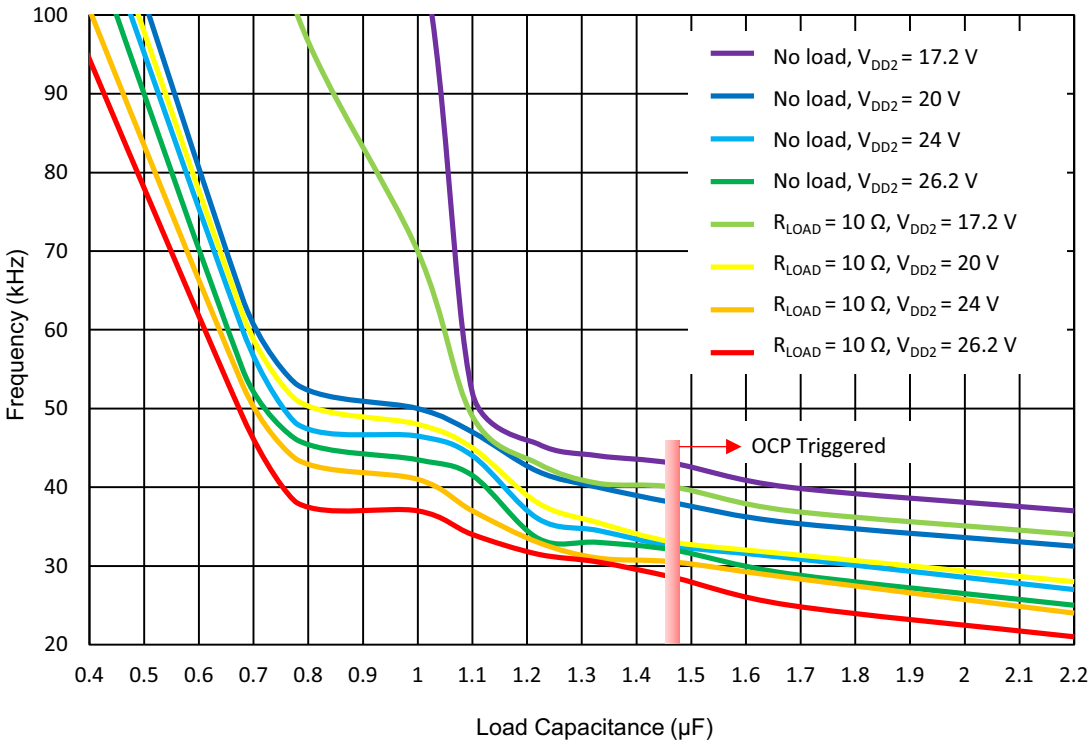


Figure 41. Two Half Bridges in Parallel Safe Operating Area. Frequency vs. C_{LOAD} at T_A = 25 °C

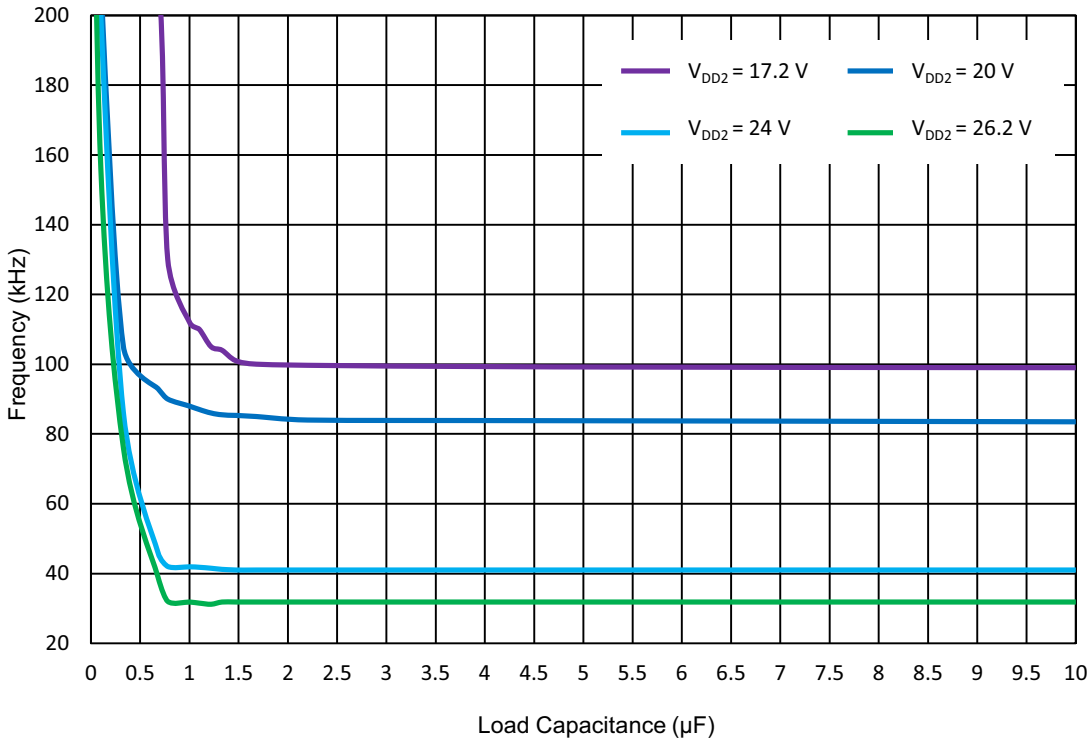


Figure 42. Full Bridge Safe Operating Area. Frequency vs. C_{LOAD} at T_A = 25 °C, R_{LOAD} = 20 Ω

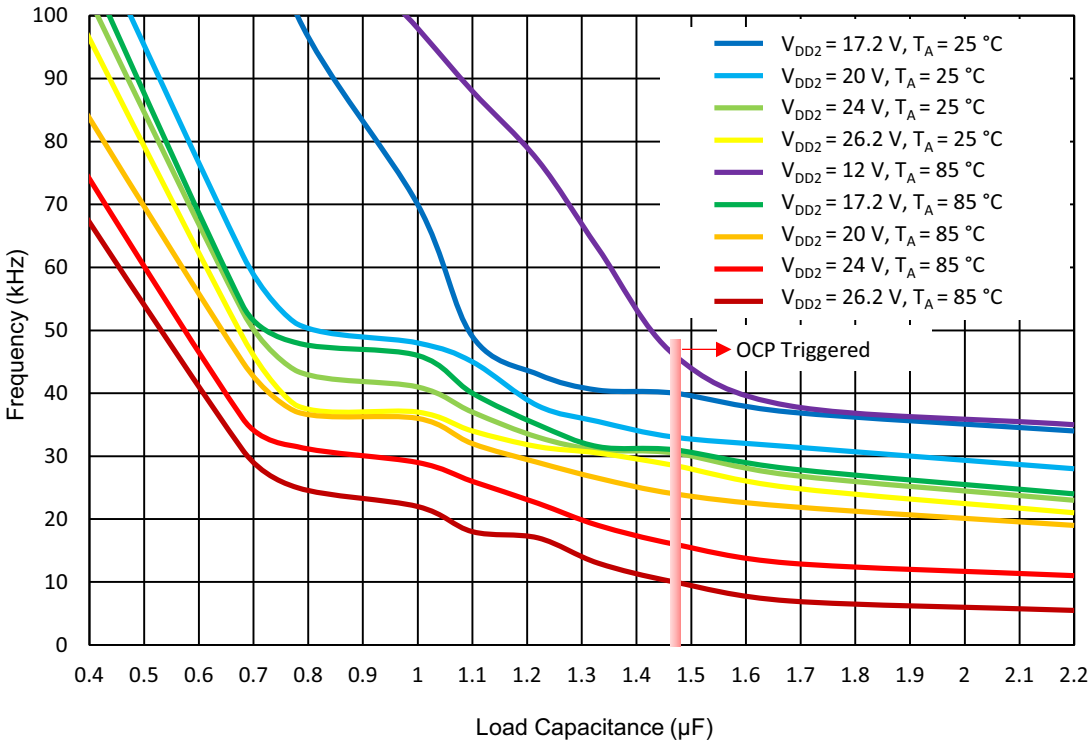


Figure 43. Two Half Bridges in Parallel Safe Operating Area. Frequency vs. C_{LOAD} at R_{LOAD} = 10 Ω

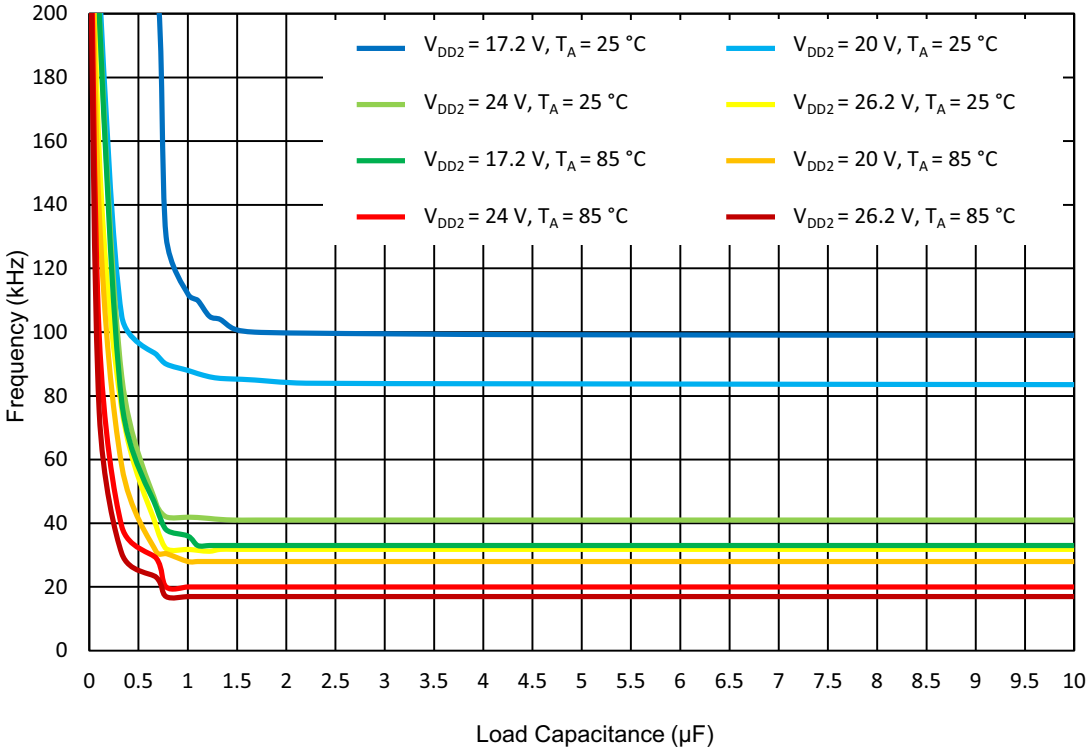


Figure 44. Full Bridge Safe Operating Area. Frequency vs. C_{LOAD} at R_{LOAD} = 20 Ω

8. Differential Amplifier with Integrator and Comparator

Differential Amplifier with Integrator and Analog Comparator is connected to HV_GPO0_HD and HV_GPO1_HD. This macrocell is useful when there is a need to keep the constant average voltage on Full Bridge load. Differential Amplifier with Integrator and Comparator has dedicated power-up input control (Connection Matrix output). During LOW on power-up input the Differential Amplifier with Integrator and Comparator is in power down state and its outputs are latched in previous state.

“Upward” output of macrocell is active LOW when average voltage difference on Full Bridge (integrated voltage) is higher than upper Vref of Comparator (including Differential Amplifier influence). “Upward” output can be optionally inverted by setting register [753] to 0.

"Equal" output is active HIGH when integrated voltage is equal to Comparator threshold.

The inputs of the Differential Amplifier can be:

- HV_GPO0_HD or HV_GPO1_HD outputs for non-inverting (“+”) input;
- HV_GPO1_HD or HV_GPO0_HD outputs for inverting ("-") input.

The internal multiplexer connects HV_GPOx_HD pins to Differential Amplifier inputs in right combination automatically, depending on Full Bridge logic inputs current state (in Full Bridge mode only).

The Comparator IN- voltage source is internal 32 mV - 2016 mV with 32 mV step or external voltage (GPIO0).

There is **0.25x or 0.125x selectable gain** divider after Differential Amplifier. Gain = 0.25x should be used for V_{DD2} < 13.2 V. For higher V_{DD2} voltage level a gain = 0.125x should be used.

The Differential Amplifier operation conditions:

- PWM0 is enabled
- HV OUT CRTL0 is configured in Full Bridge mode
- PWM frequency 44 kHz or higher to make sure that Integrator operates correctly.

The integrated DC voltage level is applied to the comparator negative input. The comparator outputs are used to control the PWM duty cycle. In this case, a closed loop system controls the PWM duty cycle to ensure the constant average output voltage level.

Note that PWM duty cycle CNT CLK requires the rate of update at latest two PWM period cycles or more.

Differential Amplifier with Integrator and Analog Comparator macrocell operates synchronously to PWM0 macrocell. So, to use Differential Amplifier with Integrator and Analog Comparator it is necessary to enable PWM0 macrocell and Oscillator, used by this PWM macrocell.

It's recommended not to use Hi-Z state of HV_GPO0_HD and HV_GPO1_HD pins when working with Differential Amplifier with Integrator and Comparator macrocell. Hi-Z state can decrease the accuracy of Differential Amplifier and may cause thermal shut down due to current flow through the diodes in the HV outputs, when Hi-Z state is enabled.

8.1 Differential Amplifier with Integrator Block Diagram

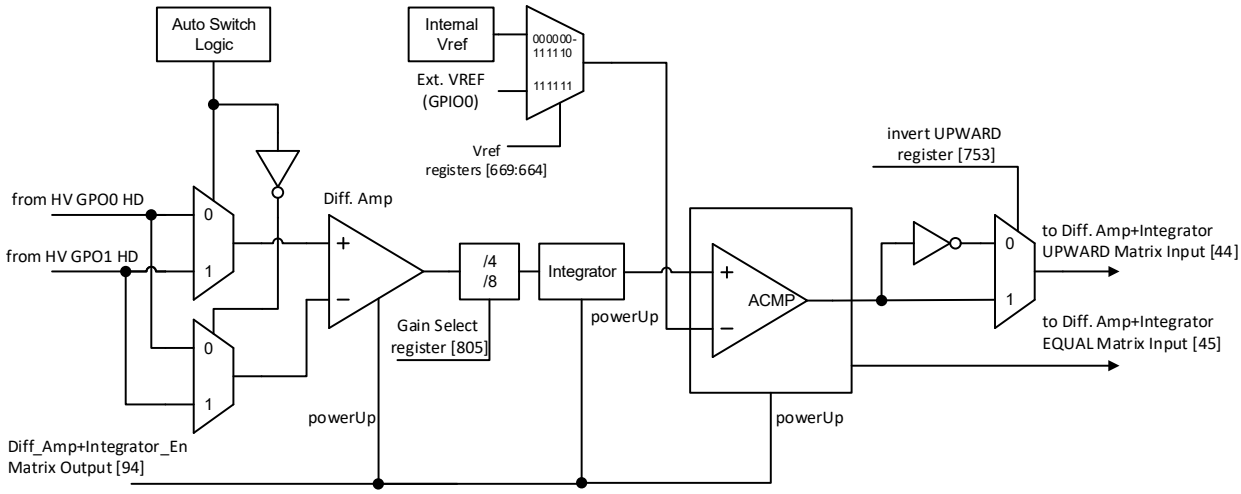


Figure 45. Differential Amplifier with Integrator Block Diagram

8.2 Differential Amplifier Load Regulation

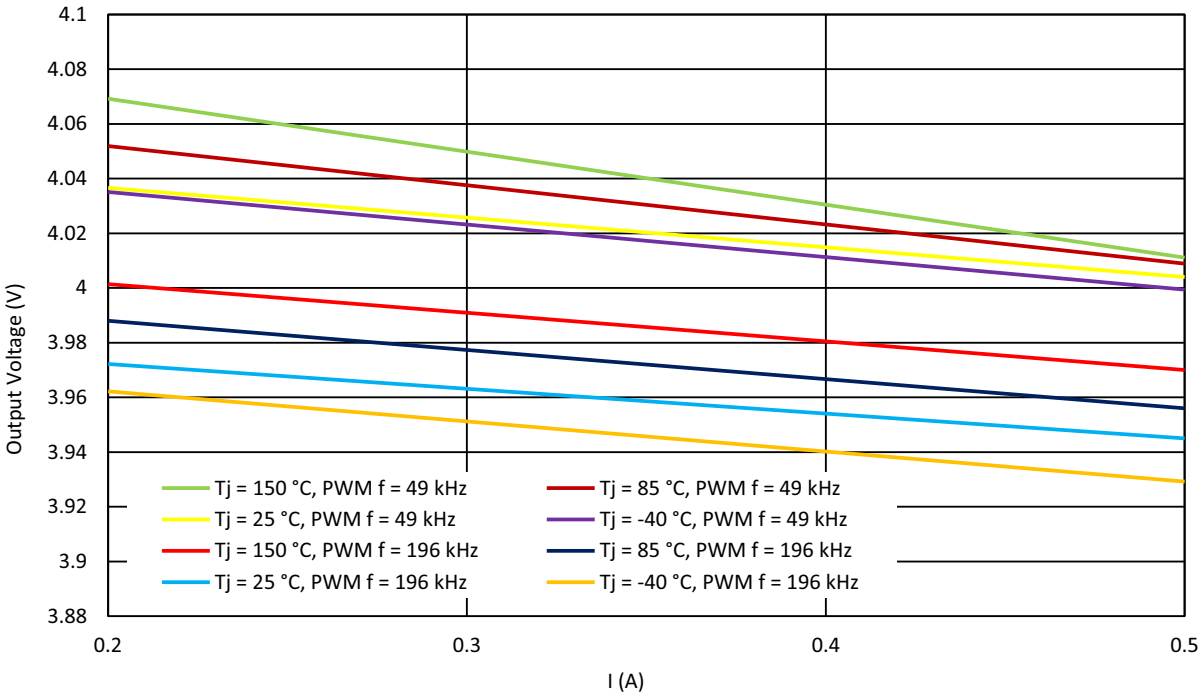


Figure 46. Typical Load Regulation at V_{OUT} = 4.096 V, V_{DD} = 2.3 V to 5.5 V, V_{DD2} = 5 V

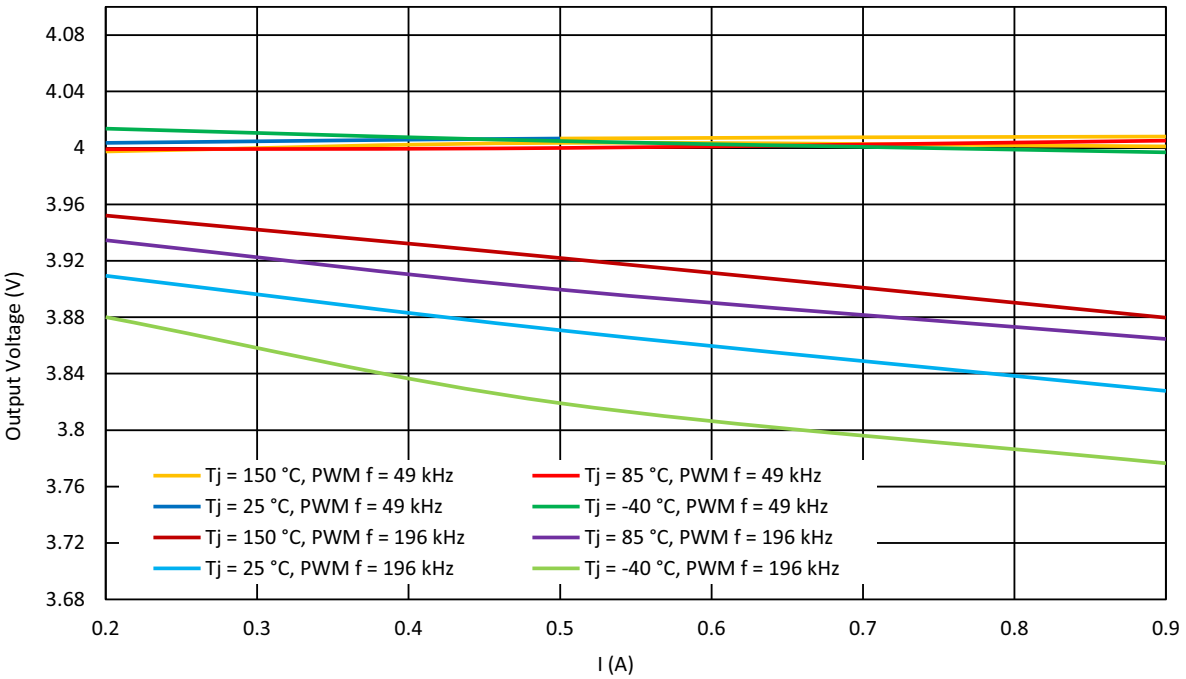


Figure 47. Typical Load Regulation at V_{OUT} = 4.096 V, V_{DD} = 2.3 V to 5.5 V, V_{DD2} = 9 V

9. Current Sense Comparator

The Current CMP macrocell has a positive input signal that is connected to SENSE pin through Selectable Gain block. The options for Selectable Gain are 4x or 8x.

The Current CMP macrocell has a negative input signal that can be connected to static or dynamic variable Vref. The static Vref value is selected via registers. The dynamically changed Vref values are selected with the help of the PWM0 block. In this case, 6-bit Vref is selected by 6 Low Significant bits of Synchro Buffer, which is a part of the PWM block (detailed in Section 13. Pulse Width Modulation Macrocell). For example, the Current Sense Comparator Vref can be changed “on the flight” from 16-bytes Register File, which is connected to the Synchro Buffer by PWM block settings, and where user-defined Vref values are stored. The Vref values are switched Up or Down depending on the level of PWM macrocell Up/Down input, each pulse on DUTY_CYCLE_CLK input.

Note 1: The PWM block can be active when 16-bytes Register File is used by Current Sense Comparator.
Note 2: The Vref can be changed in a range from 32 mV to 2016 mV with 32 mV step.

During power-up, the Current Sense Comparator output will remain LOW, and then become valid 12.5 µs (max) after power-up signal goes HIGH.

Current Sense Comparator IN+ is connected with SENSE pin through Selectable Gain.

9.1 Current Sense Comparator Block Diagram

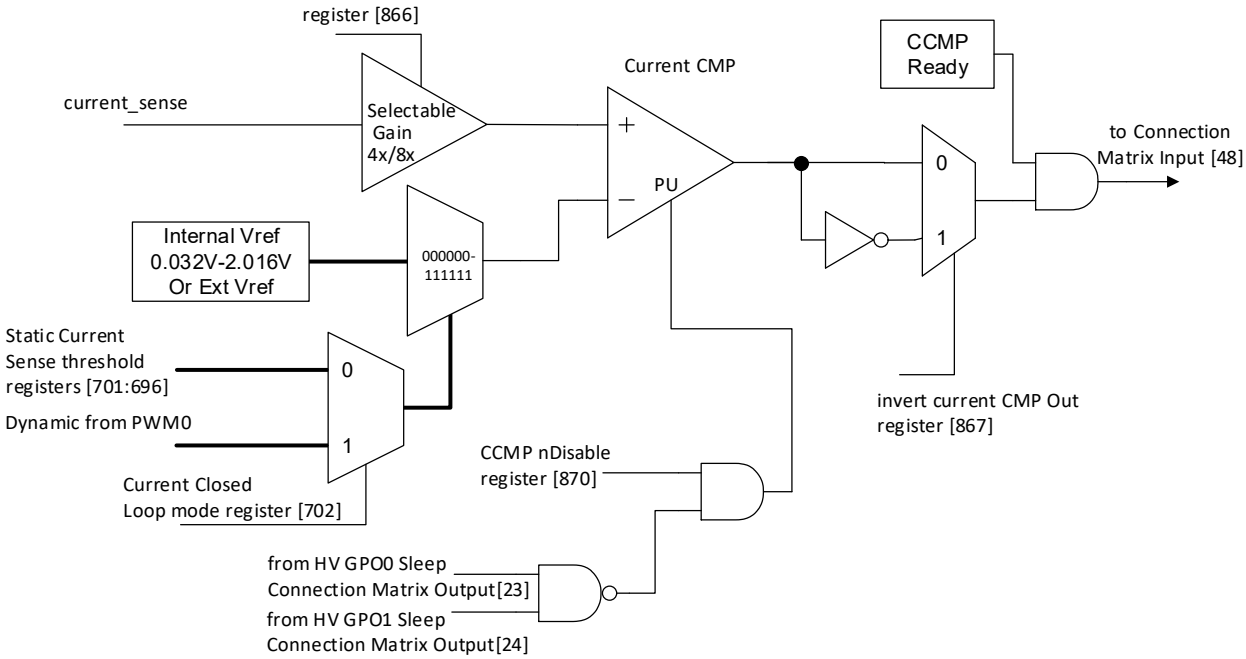


Figure 48. Current Sense Comparator Block Diagram

9.2 Current Regulation

To use the Current regulation, it is necessary to connect sense-resistors between SENSE pin and ground. The resistor value is calculated by the formula:

$$I[n] = \frac{Vref[n]}{Rsense \times GAIN}$$

Where:

- I[n]- Load Current (through controlled winding or resistive load) for selected $V_{ref}[n]$

- Vref[n]- reference voltage of Current Sense Comparator: constant value, external source, or selectable value from Register File
- R_{SENSE} - resistance of the sense resistor
- GAIN - selectable gain (4x or 8x, selectable by the register)

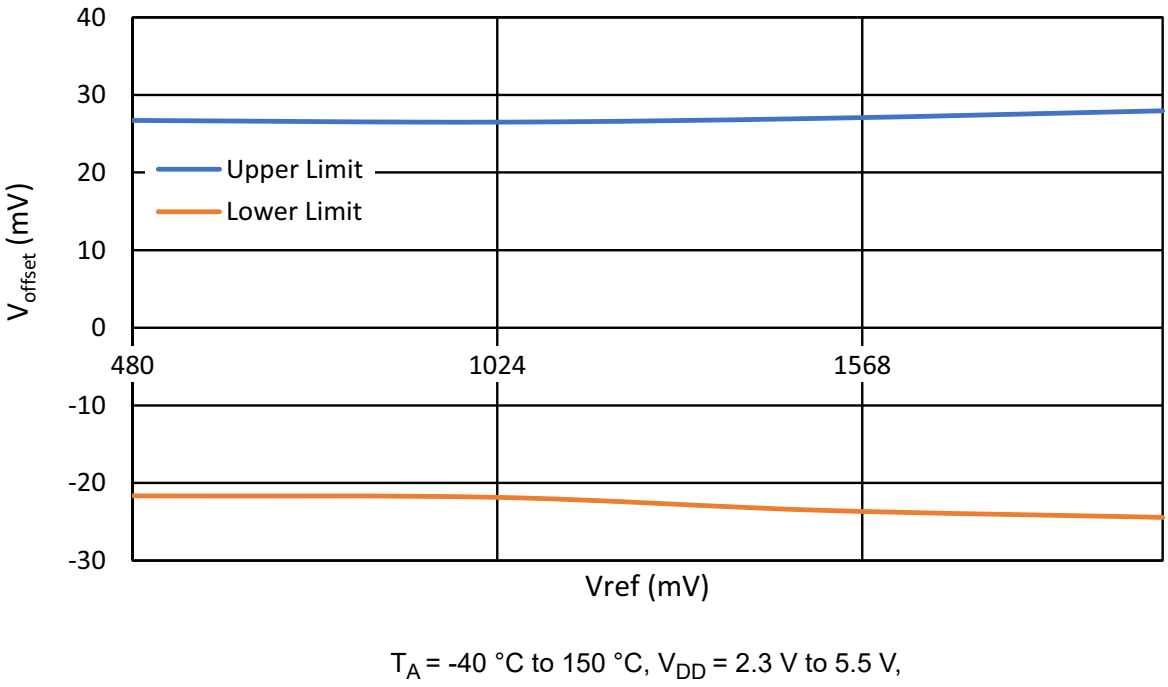
The reference voltage can be set statically or dynamically. For static reference voltage setting it is required to calculate R_{SENSE} for selected reference voltage and desired motor current.

For dynamic reference voltage setting it is required to calculate R_{SENSE} for the maximal user-defined reference voltage and maximal current via motor winding.

16 values in the Reg File can be used to determine the shape of motor current, for example, sin current for the stepper motor.

DUTY_CYCLE_CLK input of PWM macrocell is used to switch to the next Vref value, and UP/DOWN input of PWM macrocell selects the direction of Vref change (next or previous Vref value). For a more detailed description of Reg File see Section 13. Pulse Width Modulation Macrocell.

9.3 Current Sense Comparator Typical Performance



T_A = -40 °C to 150 °C, V_{DD} = 2.3 V to 5.5 V,

Figure 49. Input Offset Voltage Error vs. Vref for CCMP (Including Amplifier Offset and ACMP Offset)

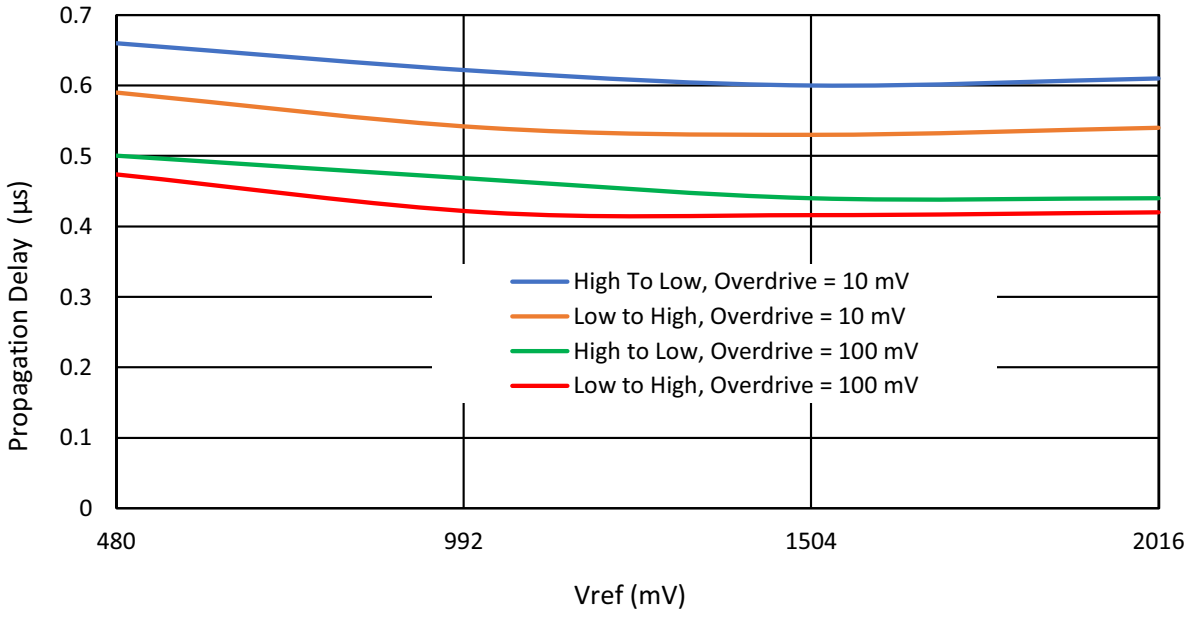


Figure 50. Typical Propagation Delay vs. Vref for CCMP at T_A = 25 °C, at V_{DD} = 2.3 V to 5.5 V, Gain = 4

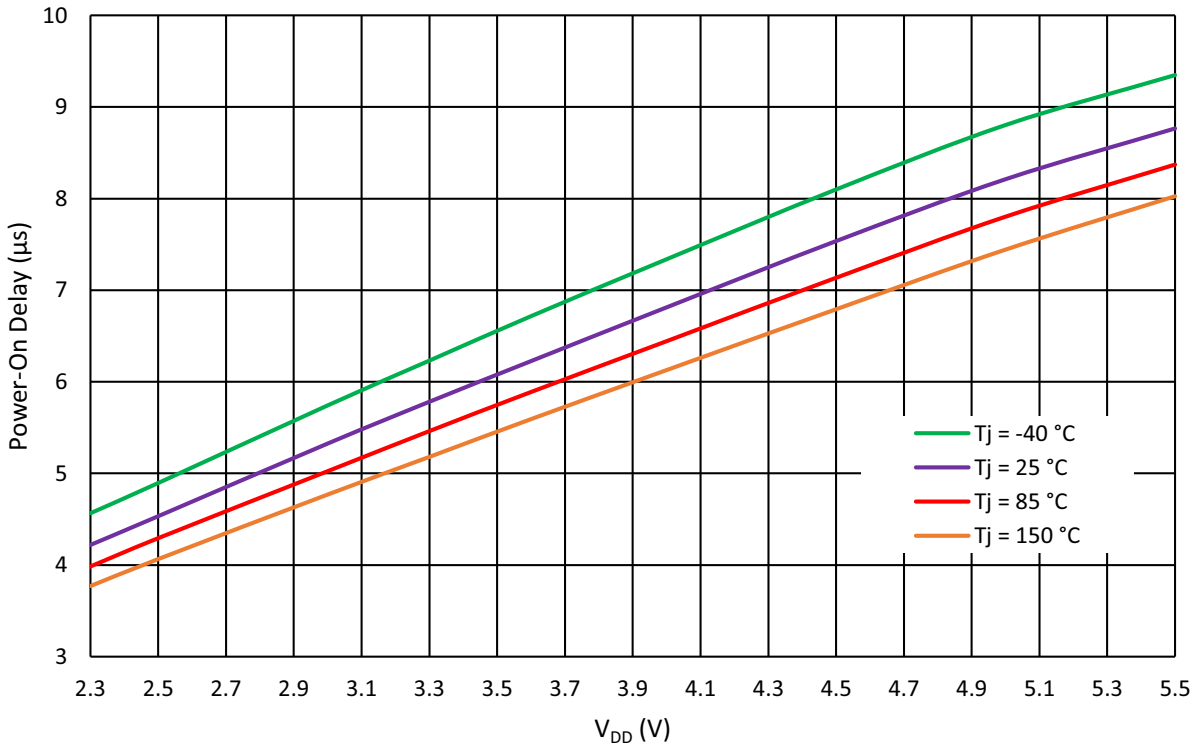


Figure 51. CCMP Power-On Delay vs. V_{DD} (BG is Forced On)

10. Connection Matrix

10.1 Connection Matrix Structure

The Connection Matrix in the SLG47115 is used to create the internal routing for internal functional macrocells of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test mode operation. The output of each functional macrocell within the SLG47115 has a specific digital bit code assigned to it, that is either set to active “HIGH”, or inactive “LOW”, based on the design that is created. Once the 2048 register bits within the SLG47115 are programmed, a fully custom circuit will be created.

The Connection matrix has 64 inputs and 96 outputs. Each of the 64 inputs to the Connection matrix is hard-wired to the digital output of a particular source macrocell, including IO pins, LUTs, analog comparators, other digital resources, such as V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG47115’s register table, see Section 23. Register Definitions.

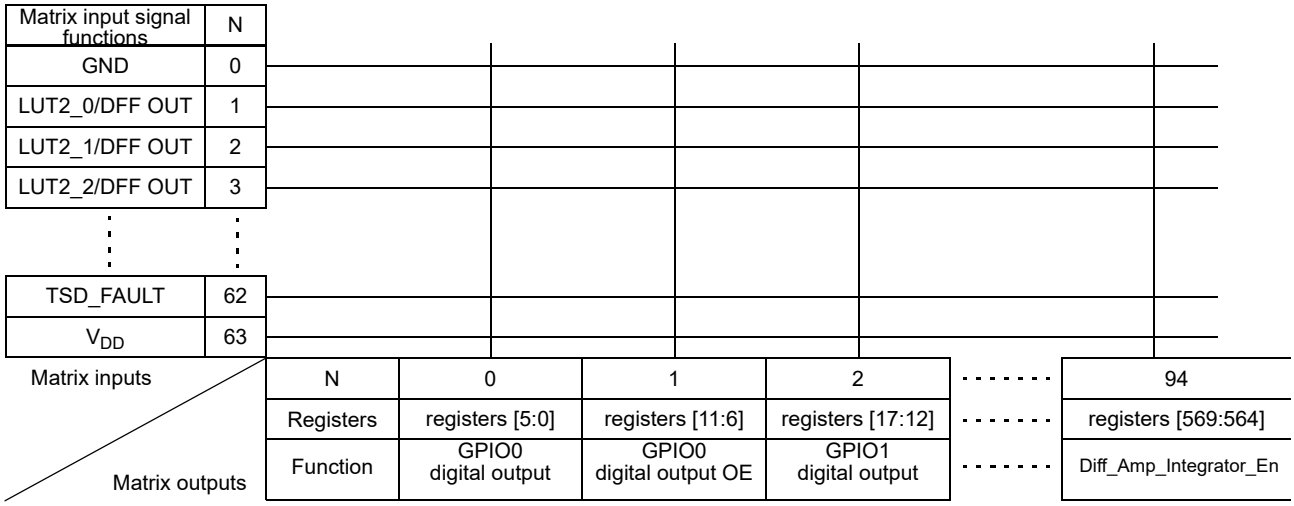


Figure 52. Connection Matrix

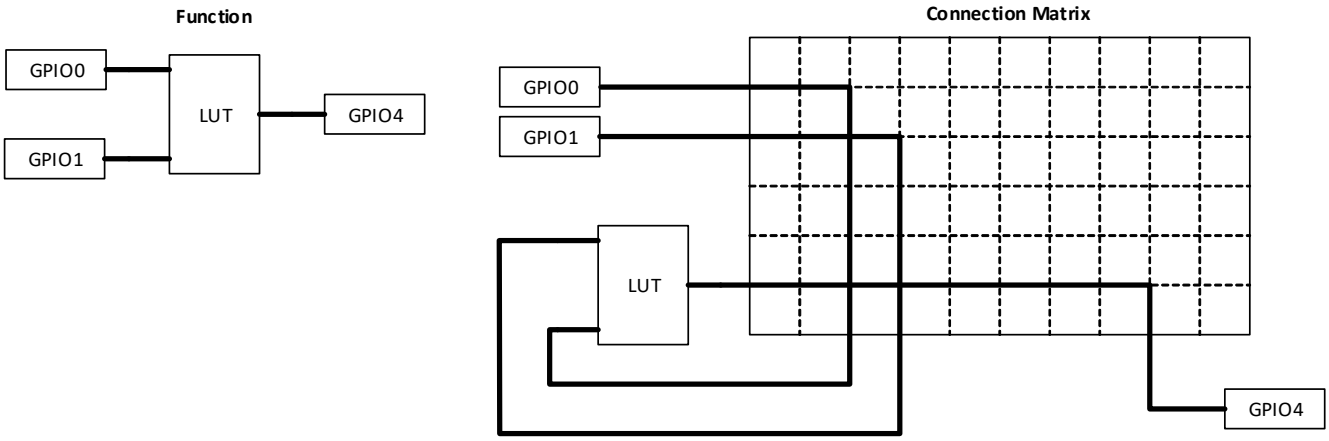


Figure 53. Connection Matrix Example

10.2 Matrix Input Table

Table 38. Matrix Input Table

Matrix input number	Matrix input signal function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	LUT2_0/DFF0 output	0	0	0	0	0	1
2	LUT2_1/DFF1 output	0	0	0	0	1	0
3	LUT2_2/DFF2 output	0	0	0	0	1	1
4	LUT2_3/PGen output	0	0	0	1	0	0
5	LUT3_0/DFF3 output	0	0	0	1	0	1
6	LUT3_1/DFF4 output	0	0	0	1	1	0
7	LUT3_2/DFF5 output	0	0	0	1	1	1
8	LUT3_3/DFF6 output	0	0	1	0	0	0
9	LUT3_4/DFF7 output	0	0	1	0	0	1
10	LUT3_5/DFF8 output	0	0	1	0	1	0
11	LUT4_0/DFF9 output	0	0	1	0	1	1
12	LUT3_6/PD/RIPP CNT output0	0	0	1	1	0	0
13	LUT3_6/PD/RIPP CNT output1	0	0	1	1	0	1
14	LUT3_6/PD/RIPP CNT output2	0	0	1	1	1	0
15	PROG_DLY_EDET_OUT	0	0	1	1	1	1
16	MULTFUNC_8BIT_1: DLY_CNT_OUT	0	1	0	0	0	0
17	MULTFUNC_8BIT_2: DLY_CNT_OUT	0	1	0	0	0	1
18	MULTFUNC_8BIT_3: DLY_CNT_OUT	0	1	0	0	1	0
19	MULTFUNC_8BIT_4: DLY_CNT_OUT	0	1	0	0	1	1
20	MULTFUNC_8BIT_1: LUT3_DFF_OUT	0	1	0	1	0	0
21	MULTFUNC_8BIT_2: LUT3_DFF_OUT	0	1	0	1	0	1
22	MULTFUNC_8BIT_3: LUT3_DFF_OUT	0	1	0	1	1	0
23	MULTFUNC_8BIT_4: LUT3_DFF_OUT	0	1	0	1	1	1
24	MULTFUNC_16BIT_0: DLY_CNT_OUT	0	1	1	0	0	0
25	MULTFUNC_16BIT_0: LUT4_DFF_OUT	0	1	1	0	0	1
26	GPIO0 digital Input	0	1	1	0	1	0
27	GPI digital Input	0	1	1	0	1	1
28	GPIO1 digital Input	0	1	1	1	0	0
29	GPIO4 digital Input	0	1	1	1	0	1
30	GPIO5 digital Input	0	1	1	1	1	0
31	GPIO6 digital Input	0	1	1	1	1	1
32	GPIO2 digital input or I^2C_virtual_0 input	1	0	0	0	0	0
33	GPIO3 digital input or I^2C_virtual_1 input	1	0	0	0	0	1
34	I^2C_virtual_2 input	1	0	0	0	1	0

Table 38. Matrix Input Table (Cont.)

Matrix input number	Matrix input signal function	Matrix Decode					
		5	4	3	2	1	0
35	I^2C_virtual_3 input	1	0	0	0	1	1
36	I^2C_virtual_4 input	1	0	0	1	0	0
37	I^2C_virtual_5 input	1	0	0	1	0	1
38	I^2C_virtual_6 input	1	0	0	1	1	0
39	I^2C_virtual_7 input	1	0	0	1	1	1
40	PWM0_OUT0+	1	0	1	0	0	0
41	PWM0_OUT1-	1	0	1	0	0	1
42	PWM1_OUT0+	1	0	1	0	1	0
43	PWM1_OUT1-	1	0	1	0	1	1
44	Diff. Amp +Integrator UPWARD	1	0	1	1	0	0
45	Diff. Amp +Integrator EQUAL	1	0	1	1	0	1
46	ACMP0H_OUT	1	0	1	1	1	0
47	ACMP1H_OUT	1	0	1	1	1	1
48	CurrentSenseComp_OUT	1	1	0	0	0	0
49	tieL	1	1	0	0	0	1
50	Fault	1	1	0	0	1	0
51	tieL	1	1	0	0	1	1
52	EDET_FILTER_OUT	1	1	0	1	0	0
53	Oscillator1 (25 MHz) output	1	1	0	1	0	1
54	Flex-Divider output	1	1	0	1	1	0
55	Oscillator0 (2.048 kHz) output 0	1	1	0	1	1	1
56	Oscillator0 (2.048 kHz) output 1	1	1	1	0	0	0
57	POR OUT	1	1	1	0	0	1
58	PWM0_PERIOD	1	1	1	0	1	0
59	PWM1_PERIOD	1	1	1	0	1	1
60	OCP_FAULT	1	1	1	1	0	0
61	tieL	1	1	1	1	0	1
62	TSD_FAULT	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

10.3 Matrix Output Table

Table 39. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[5:0]	GPIO0 digital output	0
[11:6]	GPIO0 digital output OE	1
[17:12]	GPIO1 digital output	2
[23:18]	GPIO1 digital output OE	3
[29:24]	GPIO2 digital output	4
[35:30]	GPIO3 digital output	5
[41:36]	GPIO4 digital output	6
[47:42]	GPIO4 digital output OE	7
[53:48]	GPIO5 digital output	8
[59:54]	GPIO5 digital output OE	9
[65:60]	GPIO6 digital output	10
[71:66]	GPIO6 digital output OE	11
[77:72]	HV GPO0 digital output	12
[83:78]	HV GPO0 digital output OE	13
[89:84]	Unused	14
[95:90]	Unused	15
[101:96]	HV GPO1 digital output	16
[107:102]	HV GPO1 digital output OE	17
[113:108]	Unused	18
[119:114]	Unused	19
[125:120]	Reserved	20
[131:126]	Reserved	21
[137:132]	Reserved	22
[143:138]	HV GPO0 SLEEP or power up Current Sense Comparator	23
[149:144]	Unused	24
[155:150]	HV GPO1 SLEEP or power up Current Sense Comparator	25
[161:156]	Unused	26
[167:162]	IN0 of LUT2_0 or clock input of DFF0	27
[173:168]	IN1 of LUT2_0 or data input of DFF0	28
[179:174]	IN0 of LUT2_3 or clock input of PGen	29
[185:180]	IN1 of LUT2_3 or nRST of PGen	30
[191:186]	IN0 of LUT2_1 or clock input of DFF1	31
[197:192]	IN1 of LUT2_1 or data input of DFF1	32
[203:198]	IN0 of LUT2_2 or clock input of DFF2	33
[209:204]	IN1 of LUT2_2 or data input of DFF2	34

Table 39. Matrix Output Table (Cont.)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[215:210]	IN0 of LUT3_0 or clock input of DFF3	35
[221:216]	IN1 of LUT3_0 or data input of DFF3	36
[227:222]	IN2 of LUT3_0 or nRST(nSET) of DFF3	37
[233:228]	IN0 of LUT3_1 or clock input of DFF4	38
[239:234]	IN1 of LUT3_1 or data input of DFF4	39
[245:240]	IN2 of LUT3_1 or nRST(nSET) of DFF4	40
[251:246]	IN0 of LUT3_2 or clock input of DFF5	41
[257:252]	IN1 of LUT3_2 or data input of DFF5	42
[263:258]	IN2 of LUT3_2 or nRST(nSET) of DFF5	43
[269:264]	IN0 of LUT3_3 or clock input of DFF6	44
[275:270]	IN1 of LUT3_3 or data input of DFF6	45
[281:276]	IN2 of LUT3_3 or nRST(nSET) of DFF6	46
[287:282]	IN0 of LUT3_4 or clock input of DFF7	47
[293:288]	IN1 of LUT3_4 or data input of DFF7	48
[299:294]	IN2 of LUT3_4 or nRST(nSET) of DFF7	49
[305:300]	IN0 of LUT3_5 or clock input of DFF8	50
[311:306]	IN1 of LUT3_5 or data input of DFF8	51
[317:312]	IN2 of LUT3_5 or nRST(nSET) of DFF8	52
[323:318]	IN0 of LUT3_6 or input of Pipe Delay or UP Signal of RIPP CNT	53
[329:324]	IN1 of LUT3_6 or nRST of Pipe Delay or STB of RIPP CNT	54
[335:330]	IN2 of LUT3_6 or clock of Pipe Delay_RIPP_CNT	55
[341:336]	IN0 of LUT4_0 or clock input of DFF9	56
[347:342]	IN1 of LUT4_0 or data input of DFF9	57
[353:348]	IN2 of LUT4_0 or nRST(nSET) of DFF9	58
[359:354]	IN3 of LUT4_0	59
[365:360]	MULTFUNC_8BIT_0: IN0 of LUT3_7 or clock input of DFF10; Delay1 input (or Counter1 nRST input)	60
[371:366]	MULTFUNC_8BIT_0: IN1 of LUT3_7 or nRST (nSET) of DFF10; Delay1 input (or Counter1 nRST input) or Delay/Counter1 External Clock Source	61
[377:372]	MULTFUNC_8BIT_0: IN2 of LUT3_7 or data input of DFF10; Delay1 input (or Counter1 nRST input)	62
[383:378]	MULTFUNC_8BIT_1: IN0 of LUT3_8 or clock input of DFF11; Delay2 input (or Counter2 nRST input)	63
[389:384]	MULTFUNC_8BIT_1: IN1 of LUT3_8 or nRST (nSET) of DFF11; Delay2 input (or Counter2 nRST input) or Delay/Counter2 External Clock Source	64
[395:390]	MULTFUNC_8BIT_1: IN2 of LUT3_8 or data input of DFF11; Delay2 input (or Counter2 nRST input)	65
[401:396]	MULTFUNC_8BIT_2: IN0 of LUT3_9 or clock input of DFF12; Delay3 input (or Counter3 nRST input)	66

Table 39. Matrix Output Table (Cont.)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[407:402]	MULTFUNC_8BIT_2: IN1 of LUT3_9 or nRST (nSET) of DFF12; Delay3 input (or Counter3 nRST Input) or Delay/Counter3 External Clock Source	67
[413:408]	MULTFUNC_8BIT_2: IN2 of LUT3_9 or data input of DFF12; Delay3 input (or Counter3 nRST Input)	68
[419:414]	MULTFUNC_8BIT_3: IN0 of LUT3_10 or clock input of DFF13; Delay4 input (or Counter4 nRST Input)	69
[425:420]	MULTFUNC_8BIT_3: IN1 of LUT3_10 or nRST (nSET) of DFF13; Delay4 input (or Counter4 nRST Input) or Delay/Counter4 External Clock Source	70
[431:426]	MULTFUNC_8BIT_3: IN2 of LUT3_10 or data input of DFF13; Delay4 input (or Counter4 nRST Input)	71
[437:432]	MULTFUNC_16BIT_0: IN0 of LUT4_1 or clock input of DFF14; Delay0 input (or Counter0 RST/SET input)	72
[443:438]	MULTFUNC_16BIT_0: IN1 of LUT4_1 or nRST of DFF14; Delay0 input (or Counter0 nRST Input) or Delay/Counter0 External Clock Source	73
[449:444]	MULTFUNC_16BIT_0: IN2 of LUT4_1 or nSET of DFF14 or KEEP input of FSM0 or External clock input of Delay0 (or Counter0)	74
[455:450]	MULTFUNC_16BIT_0: IN3 of LUT4_1 or data input of DFF14; Delay0 input (or Counter0 nRST Input) or UP input of FSM0	75
[461:456]	PWM0_UP/DOWN	76
[467:462]	PWM0_KEEP/STOP	77
[473:468]	PWM0_DUTY_CYCLE_CNT	78
[479:474]	PWM0_EXT_CLK	79
[485:480]	PWM0_Power-down	80
[491:486]	PWM1_UP/DOWN	81
[497:492]	PWM1_KEEP/STOP	82
[503:498]	PWM1_DUTY_CYCLE_CNT	83
[509:504]	PWM1_EXT_CLK	84
[515:510]	PWM1_Power-down	85
[521:516]	pd of ACMP0H from the matrix	86
[527:522]	pd of ACMP1H from the matrix	87
[533:528]	Filter/Edge detect input	88
[539:534]	Programmable delay/edge detect input	89
[545:540]	OSC0 ENABLE from matrix	90
[551:546]	OSC1 ENABLE from matrix	91
[557:552]	Temp sensor PD from matrix	92
[563:558]	BG Power-down from the matrix	93
[569:564]	Diff_Amp_Integrator_En	94
[575:570]	Reserved	95

10.4 Connection Matrix Virtual Inputs

As mentioned previously, the Connection matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I²C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection matrix to the digital inputs of other macrocells on the device. The I²C address for reading and writing these register values is at 0x4C (76).

An I²C write command to these register bits will set the signal values going into the Connection matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup) or the values from a previous write command (if that has happened).

Table 40. Connection Matrix Virtual Inputs

Matrix input number	Matrix input signal function	Register Bit addresses (d)
32	I²C_virtual_0 Input	[608]
33	I²C_virtual_1 Input	[609]
34	I²C_virtual_2 Input	[610]
35	I²C_virtual_3 Input	[611]
36	I²C_virtual_4 Input	[612]
37	I²C_virtual_5 Input	[613]
38	I²C_virtual_6 Input	[614]
39	I²C_virtual_7 Input	[615]

10.5 Connection Matrix Virtual Outputs

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time it is possible to read the state of each of the macrocell outputs as a register value via I²C. This option, called Connection Matrix virtual outputs, allows the user to remotely read the values of each macrocell output. The I²C addresses for reading these register values are registers [639:576]. Write commands to the same register values will be ignored (with the exception of the Virtual Input register bits at registers [615:608]).

11. Combination Function Macrocells

The SLG47115 has 12 combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells.

- Three macrocells that can serve as either 2-bit LUT or as D Flip-Flop
- Four macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset Input
- Two macrocells that can serve as either 3-bit LUTs, as D Flip-Flops with Set/Reset Input or as PWM Choppers
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay/Ripple Counter
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGen)
- One macrocell that can serve as either 4-bit LUT or as D Flip-Flop with Set/Reset Input

Inputs/Outputs for the 12 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of configuration bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

11.1 2-Bit LUT or D Flip-Flop Macrocells

There are three macrocells that can serve as either 2-bit LUT or as D Flip-Flop. When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change

LATCH: when CLK is LOW, then Q = D; otherwise Q remains its previous value (input D has no effect on the output when CLK is HIGH).

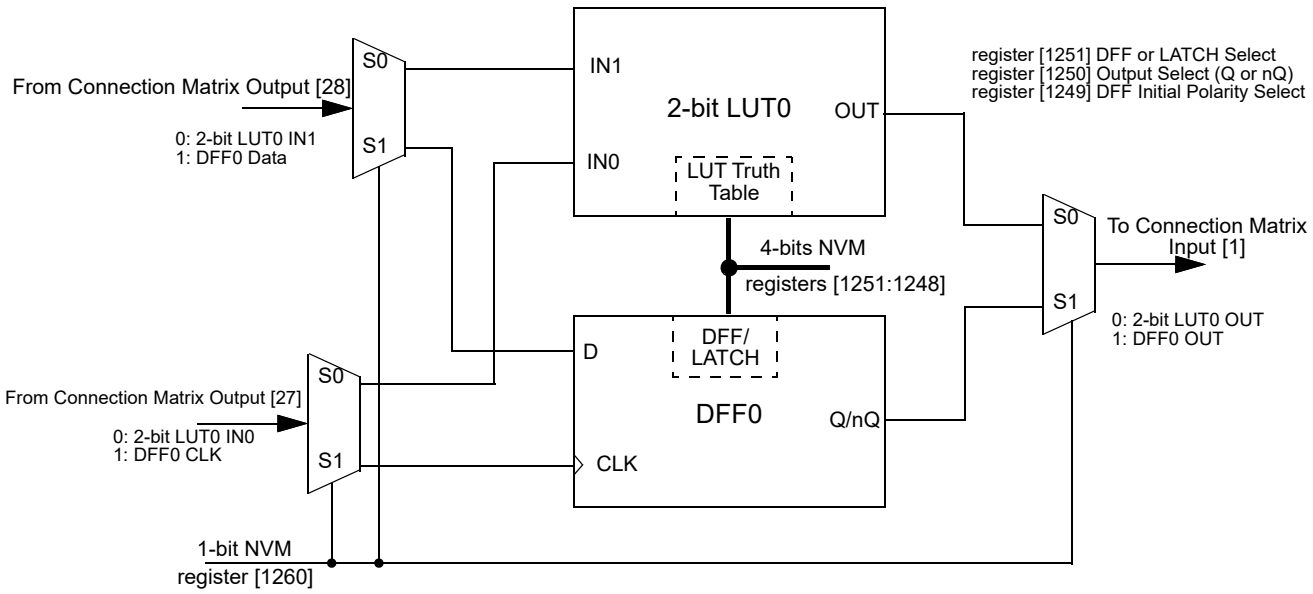


Figure 54. 2-bit LUT0 or DFF0

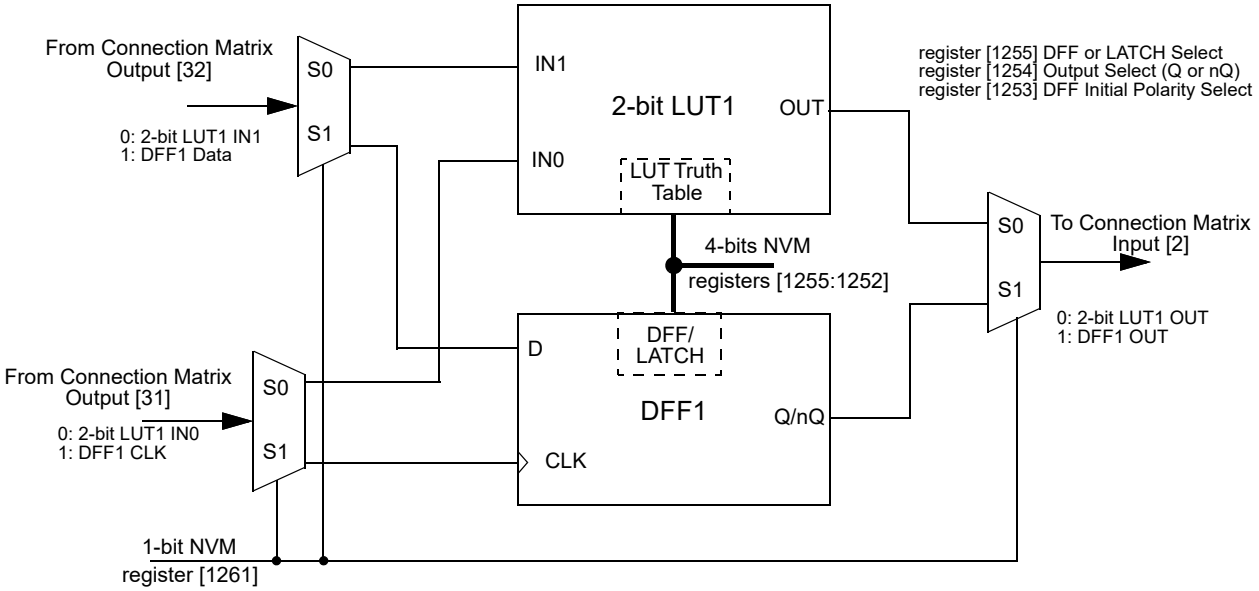


Figure 55. 2-bit LUT1 or DFF1

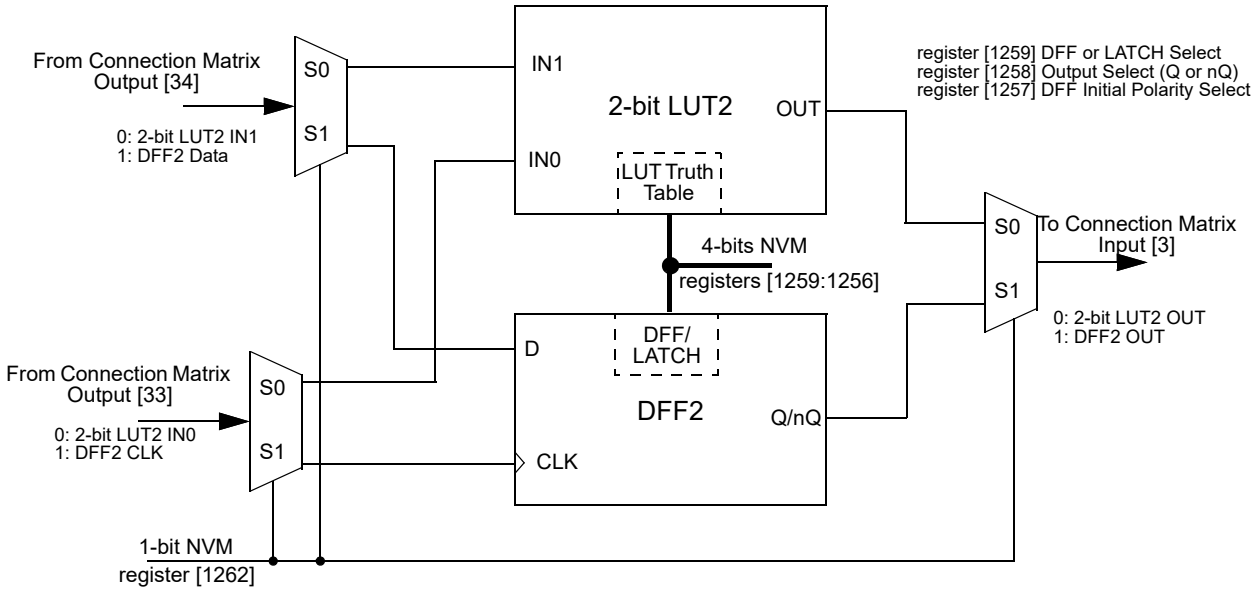


Figure 56. 2-bit LUT2 or DFF2

11.1.1 2-Bit LUT or D Flip-Flop Macrocell Used as 2-Bit LUT

Table 41. 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	register [1248]	LSB
0	1	register [1249]	
1	0	register [1250]	
1	1	register [1251]	MSB

Table 42. 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [1252]	LSB
0	1	register [1253]	
1	0	register [1254]	
1	1	register [1255]	MSB

Table 43. 2-bit LUT2 Truth Table

IN1	IN0	OUT	
0	0	register [1256]	LSB
0	1	register [1257]	
1	0	register [1258]	
1	1	register [1259]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-bit LUT0 is defined by registers [1251:1248]

2-bit LUT1 is defined by registers [1255:1252]

2-bit LUT2 is defined by registers [1259:1256]

Table 44 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 44. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

11.1.2 Initial Polarity Operations

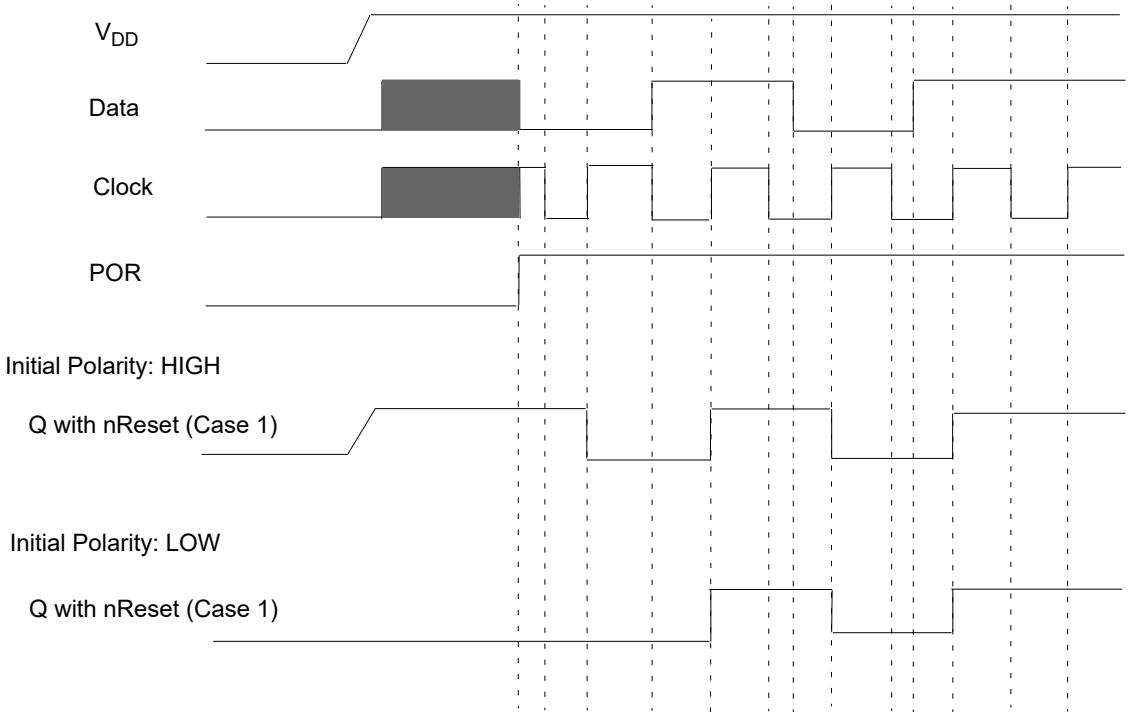


Figure 57. DFF Polarity Operations

11.2 2-bit LUT or Programmable Pattern Generator

The SLG47115 has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or a Programmable Pattern Generator (PGen).

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUT can be configured to any user-defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

It is possible to define the RST level for the PGEN macrocell. There are both High-level reset (RST) and a Low-level reset (nRST) options available, which are selected by register [1193]. When operating as the Programmable Pattern Generator, the output of the macrocell will clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats.

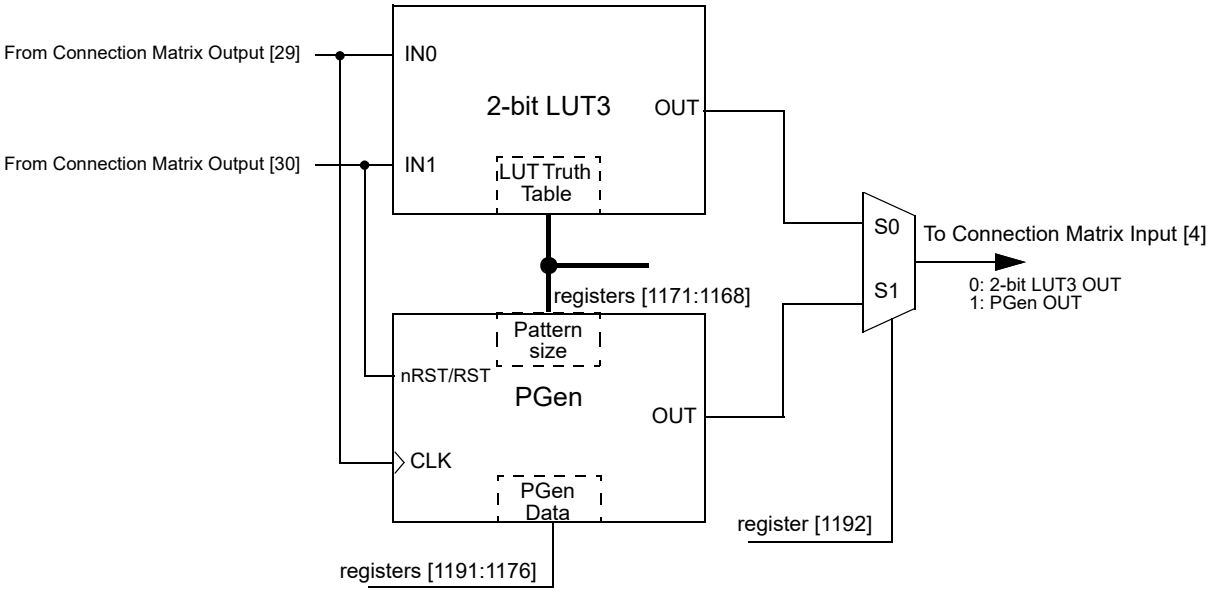


Figure 58. 2-bit LUT3 or PGen

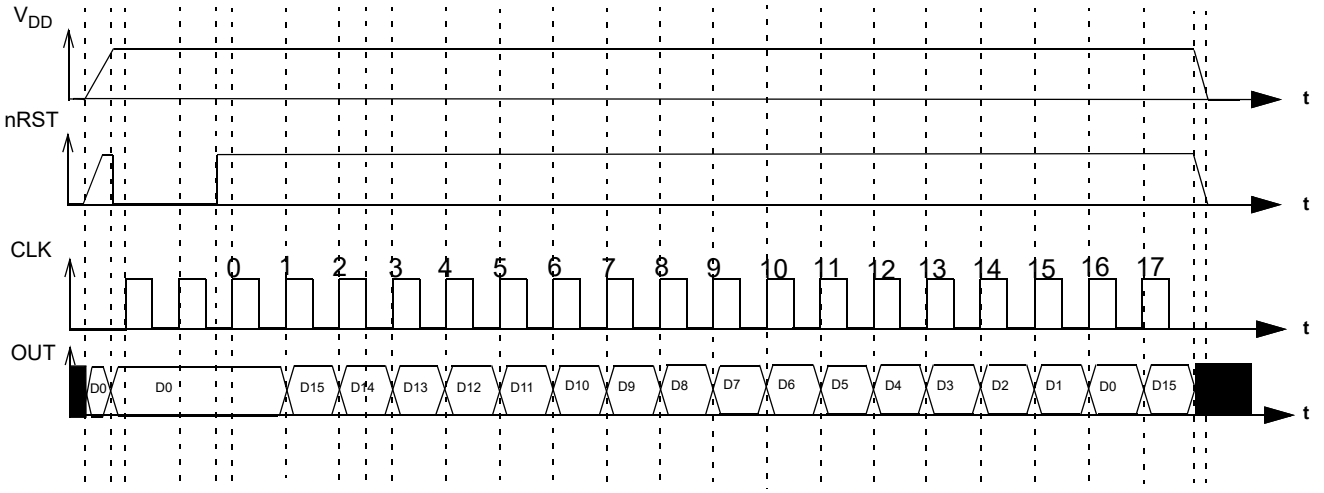


Figure 59. PGen Timing Diagram

2-Bit LUT or PGen Macrocell Used as 2-Bit LUT

Table 45. 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [1168]	LSB
0	1	register [1169]	
1	0	register [1170]	
1	1	register [1171]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-bit LUT3 is defined by registers [1171:1168]

Table 46 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 46. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

11.3 3-Bit LUT or D Flip-Flop with Set/Reset Macrocells

There are four macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix. It is possible to define the active level for the reset/set input of DFF/LATCH macrocell. There are both active High-level reset/set (RST/SET) and active low level reset/set (nRST/nSET) options available, which are selected by register [1226].

DFF3 functionality is different from the other DFFs. DFF3 operation will flow the functional description below:

- If register [1228] = 0, and the CLK is rising edge triggered, then Q = D, otherwise Q will not change.
- If register [1228] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK.

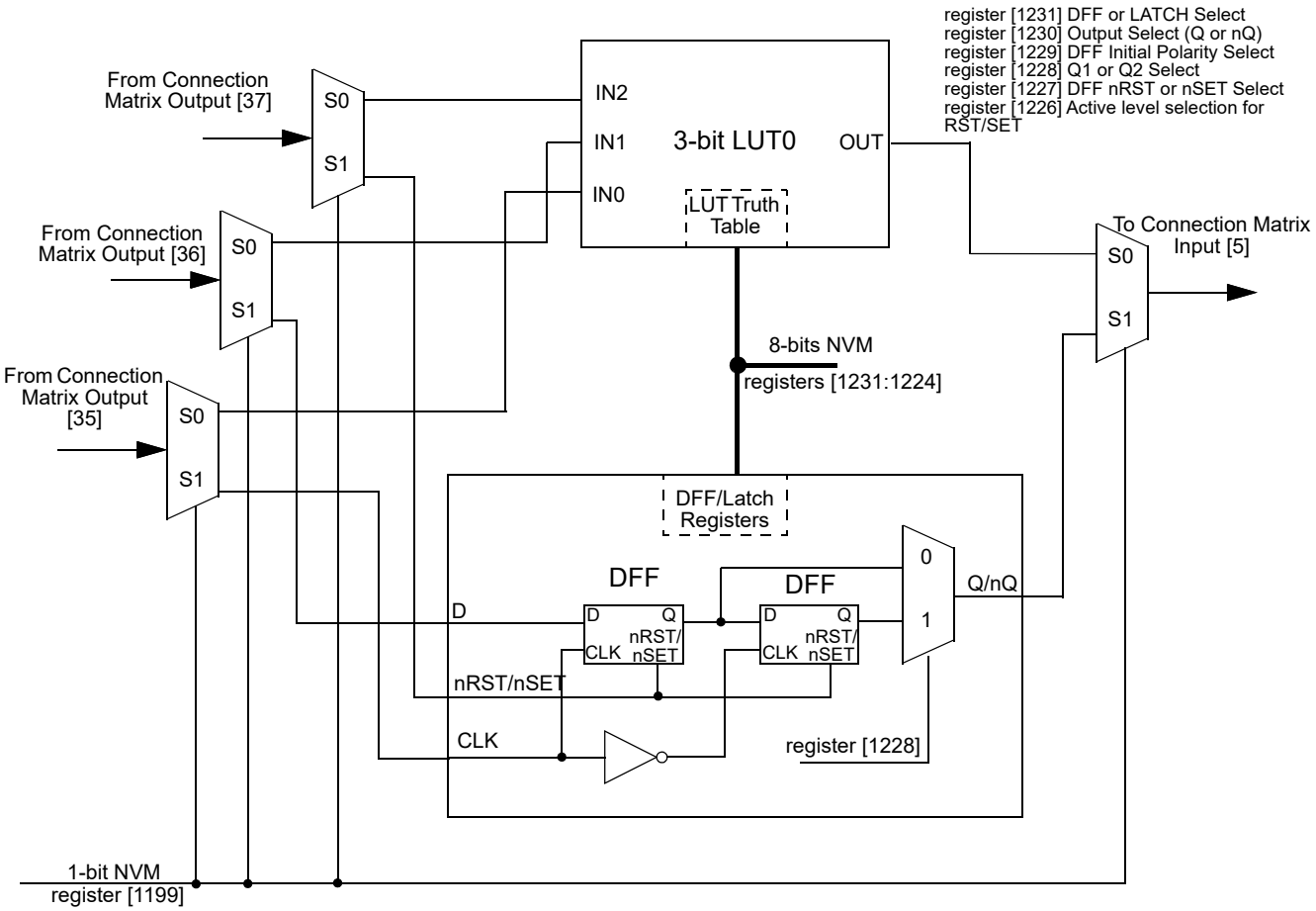


Figure 60. 3-bit LUT0 or DFF3

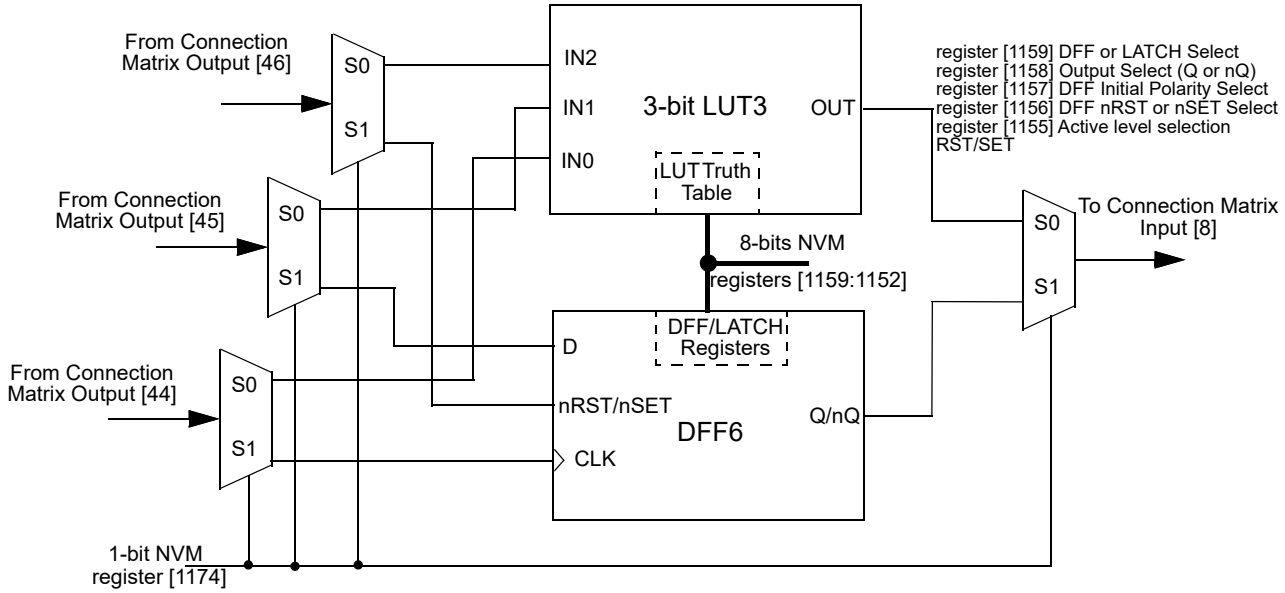


Figure 61. 3-bit LUT3 or DFF6

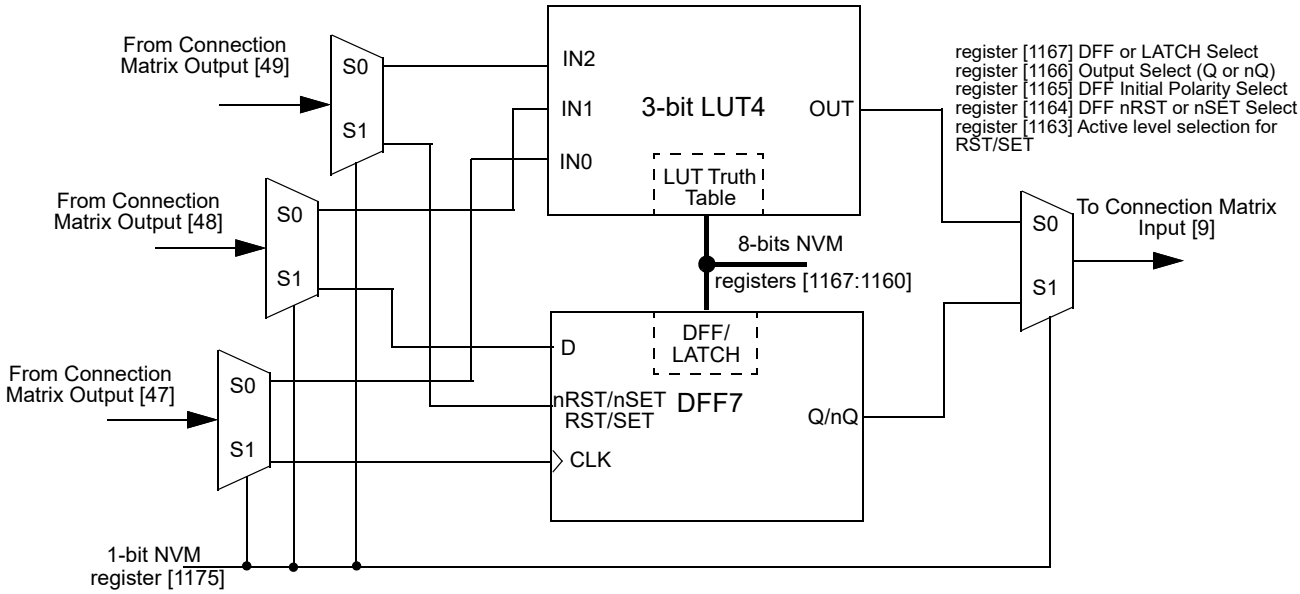


Figure 62. 3-bit LUT4 or DFF7

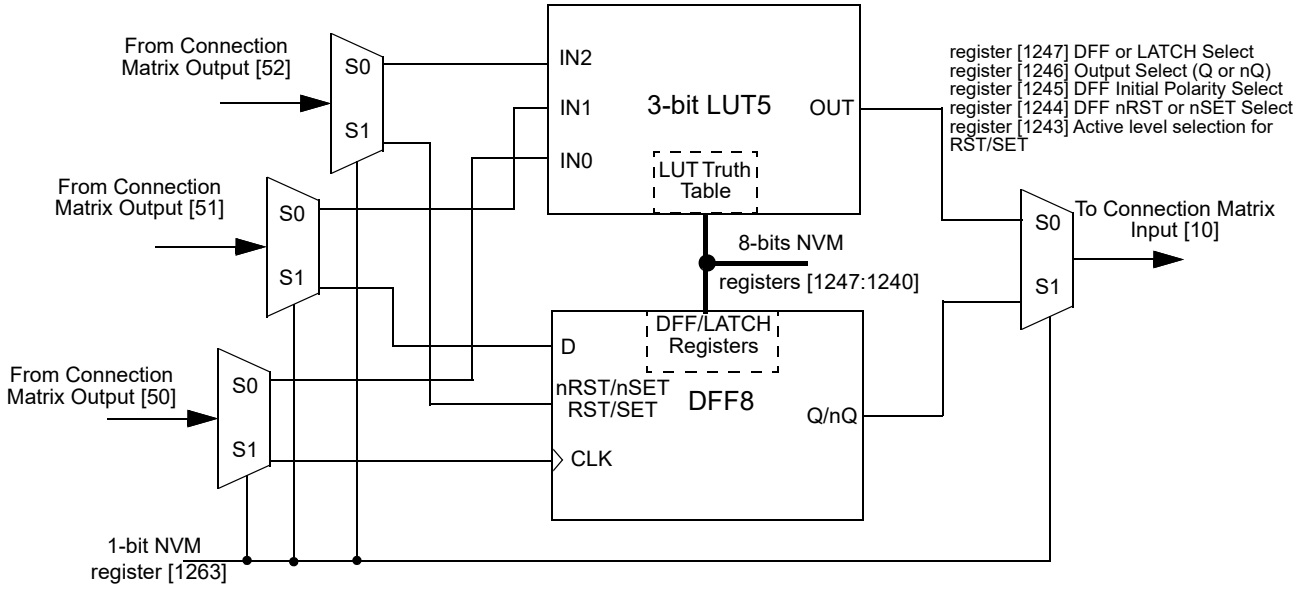


Figure 63. 3-bit LUT5 or DFF8

11.3.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Table 47. 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1224]	LSB
0	0	1	register [1225]	
0	1	0	register [1226]	
0	1	1	register [1227]	
1	0	0	register [1228]	
1	0	1	register [1229]	
1	1	0	register [1230]	
1	1	1	register [1231]	MSB

Table 48. 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1160]	LSB
0	0	1	register [1161]	
0	1	0	register [1162]	
0	1	1	register [1163]	
1	0	0	register [1164]	
1	0	1	register [1165]	
1	1	0	register [1166]	
1	1	1	register [1167]	MSB

Table 49. 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1152]	LSB
0	0	1	register [1153]	
0	1	0	register [1154]	
0	1	1	register [1155]	
1	0	0	register [1156]	
1	0	1	register [1157]	
1	1	0	register [1158]	
1	1	1	register [1159]	MSB

Table 50. 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1240]	LSB
0	0	1	register [1241]	
0	1	0	register [1242]	
0	1	1	register [1243]	
1	0	0	register [1244]	
1	0	1	register [1245]	
1	1	0	register [1246]	
1	1	1	register [1247]	MSB

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-bit LUT0 is defined by registers [1231:1224]

3-bit LUT3 is defined by registers [1159:1152]

3-bit LUT4 is defined by registers [1167:1160]

3-bit LUT5 is defined by registers [1247:1240]

Table 51 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

Table 51. 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

11.3.2 Initial Polarity Operations

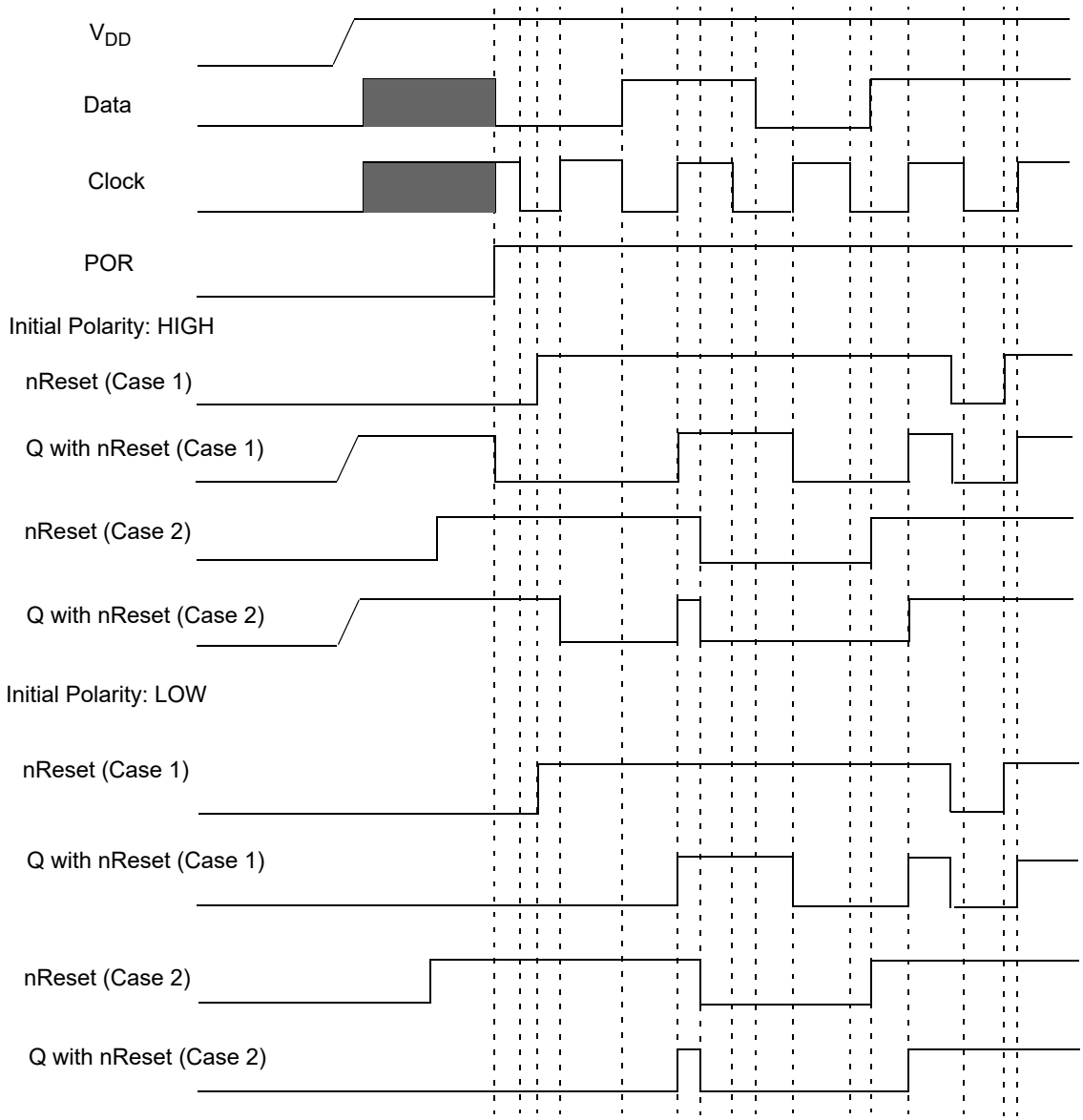


Figure 64. DFF Polarity Operations with nReset

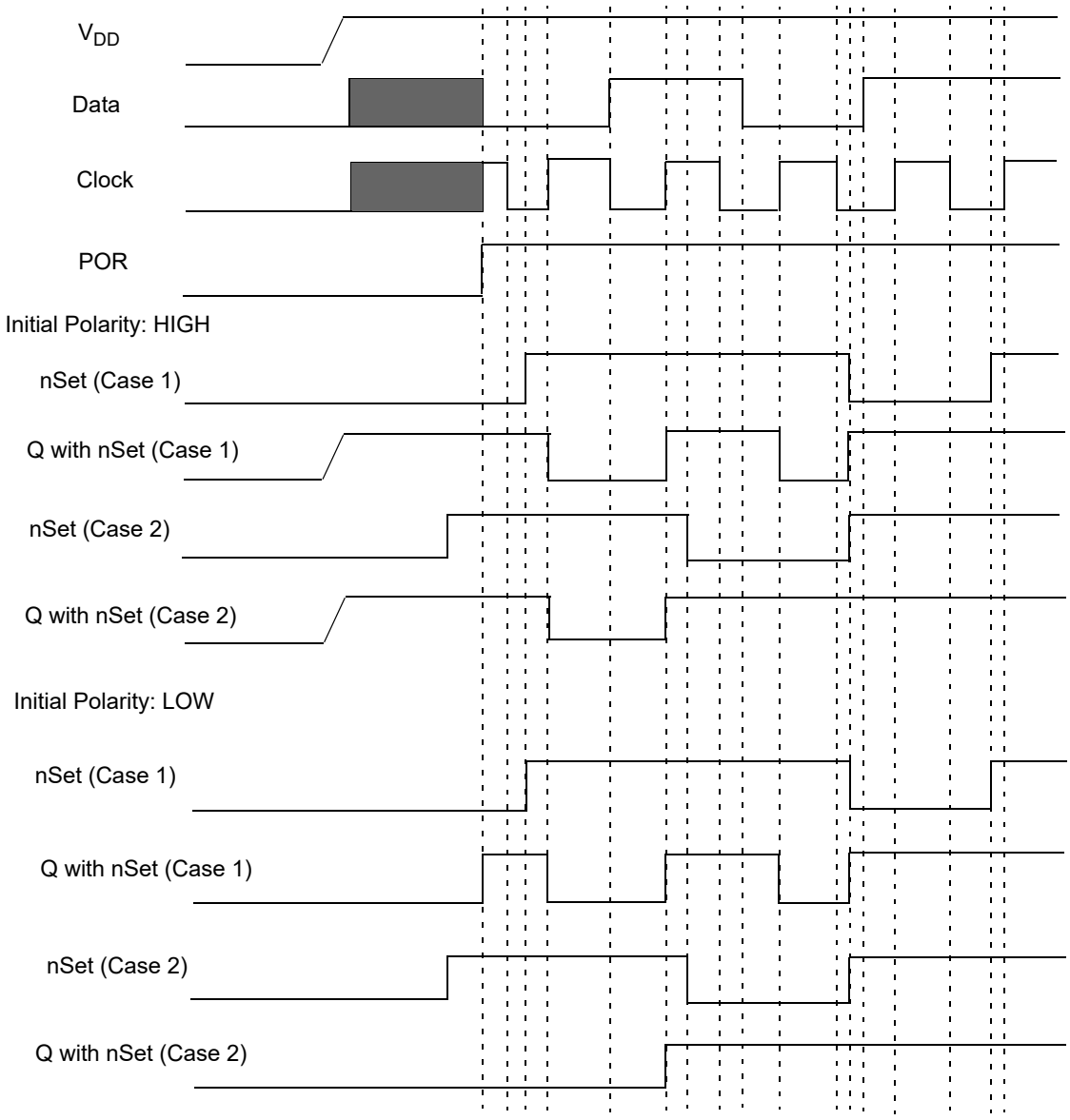


Figure 65. DFF Polarity Operations with nSet

11.4 3-Bit LUT or D Flip-Flop with Set/Reset Macrocell or PWM Chopper

There are two macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs, or as PWM Chopper. When used to implement LUT functions, the 3-bit LUTs each takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix. It is possible to define the active level for the reset/set input of DFF/LATCH macrocell. There are both active high-level reset/set (RST/SET) and active low-level reset/set (nRST/nSET) options available, which are selected by register [1139] and register [1147]. When used to implement PWM Chopper function, the three input signals from the connection matrix go to the PWM input (PWM) and Blanking Time input (Blanking Time), and Chopper input (Chop) for the PWM Chopper, with the output (OUT) going back to the connection matrix.

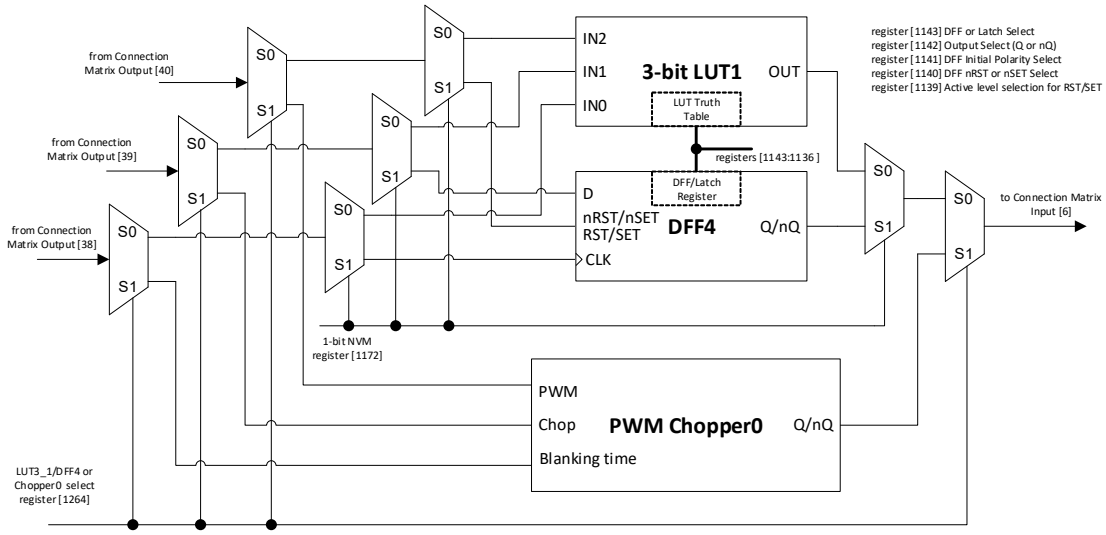


Figure 66. 3-bit LUT1 or DFF4

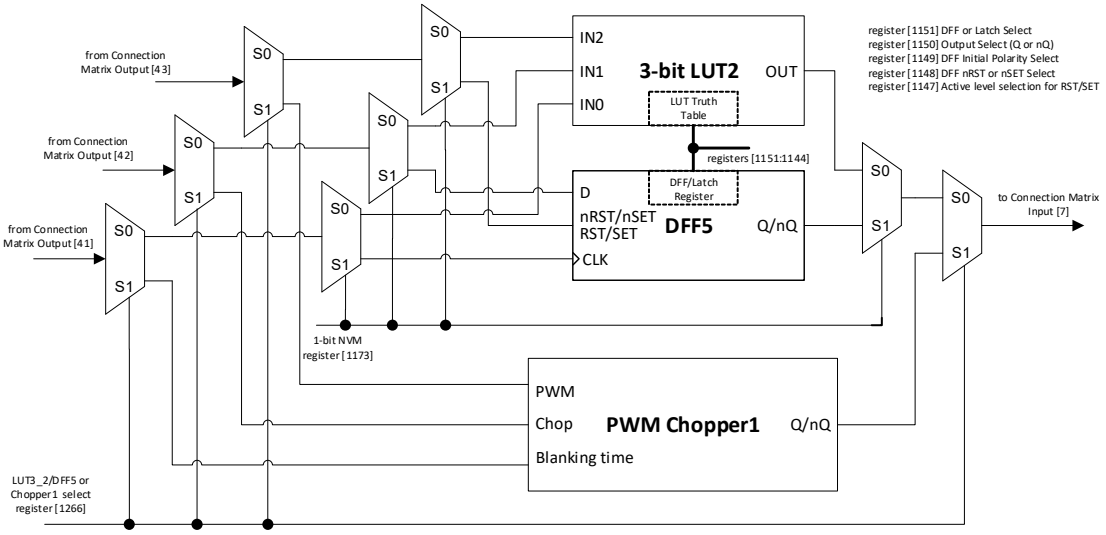


Figure 67. 3-bit LUT2 or DFF5

11.4.1 3-Bit LUT or D Flip-Flop or PWM Chopper Macrocells Used as 3-Bit LUTs

Table 52. 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1136]	LSB
0	0	1	register [1137]	
0	1	0	register [1138]	
0	1	1	register [1139]	
1	0	0	register [1140]	
1	0	1	register [1141]	
1	1	0	register [1142]	
1	1	1	register [1143]	MSB

Table 53. 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1144]	LSB
0	0	1	register [1145]	
0	1	0	register [1146]	
0	1	1	register [1147]	
1	0	0	register [1148]	
1	0	1	register [1149]	
1	1	0	register [1150]	
1	1	1	register [1151]	MSB

This macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-bit LUT1 is defined by registers [1143:1136]

3-bit LUT2 is defined by registers [1151:1144]

Table 54 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

Table 54. 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

11.4.2 PWM Chopper

PWM Chopper function can be used to chop PWM Duty Cycle by Current Comparator signal.

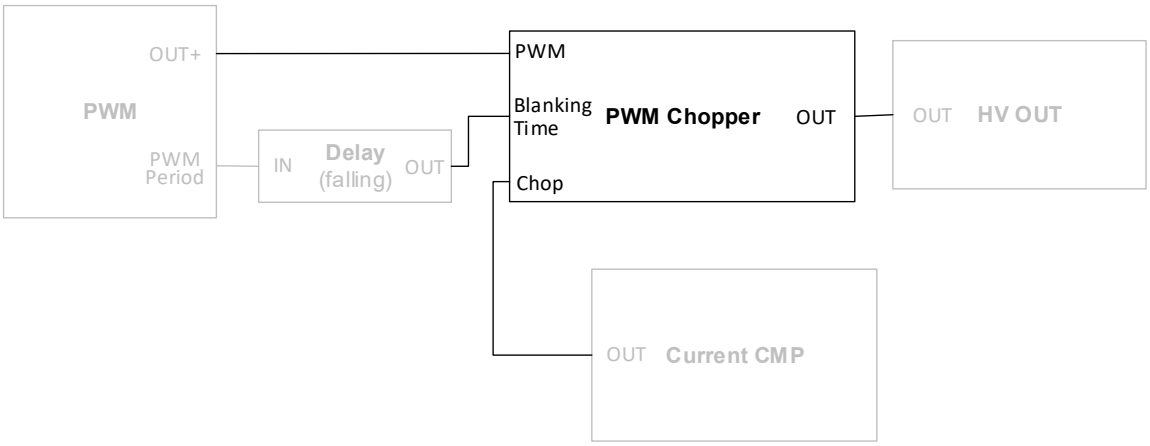


Figure 68. PWM Chopper Circuit Example

In PWM Chopper mode all internal components of 3-Bit LUT or D Flip-Flop, or PWM Chopper macrocell are connected as shown in Figure 69

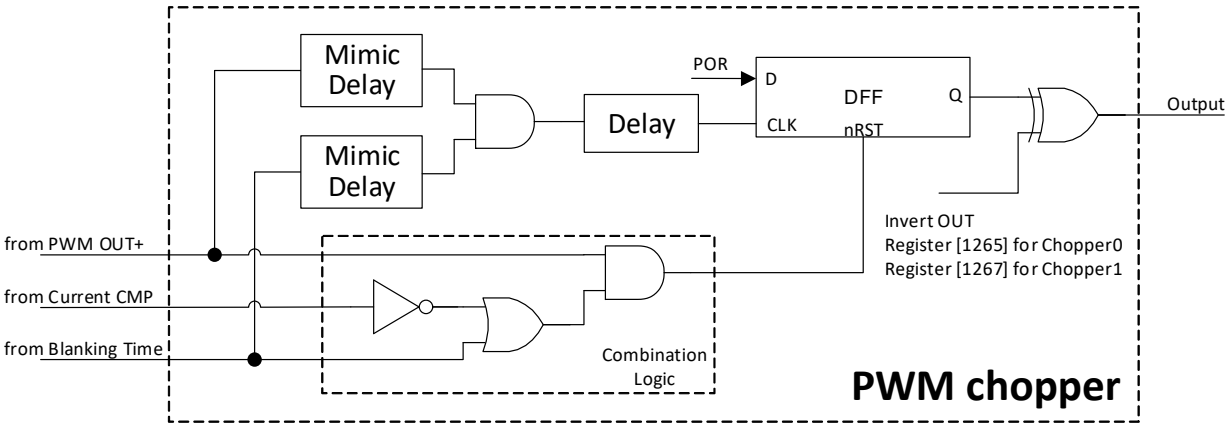


Figure 69. PWM Chopper Interconnection

This configuration allows ignoring Current Comparator signal during Blanking time during the motor start period. Any active signal from Current CMP after Blanking time causes PWM Duty Cycle chopping to currently Period end. The following figures demonstrate PWM Chopper operation.

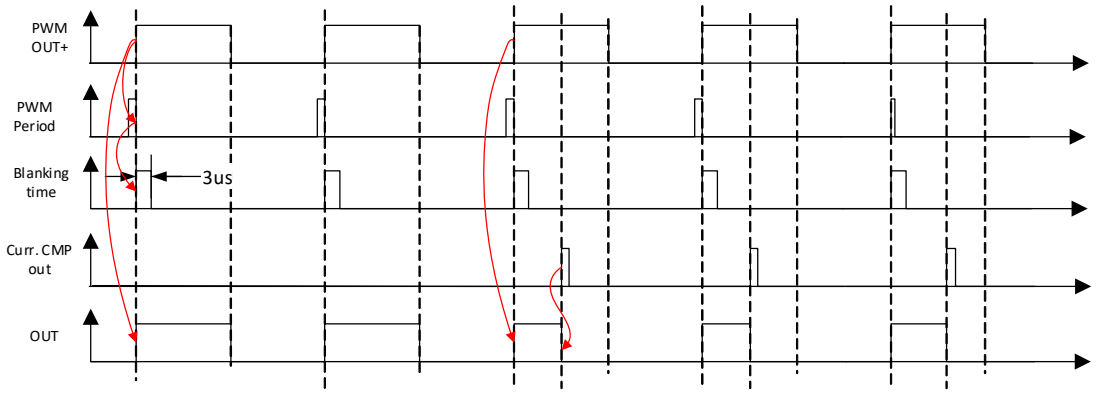


Figure 70. PWM Chopper. Overcurrent Timing Diagram

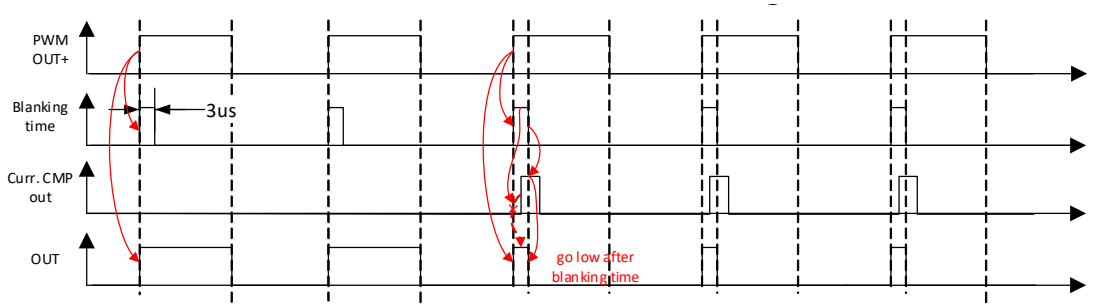


Figure 71. PWM Chopper. Overcurrent Start during Blanking Time

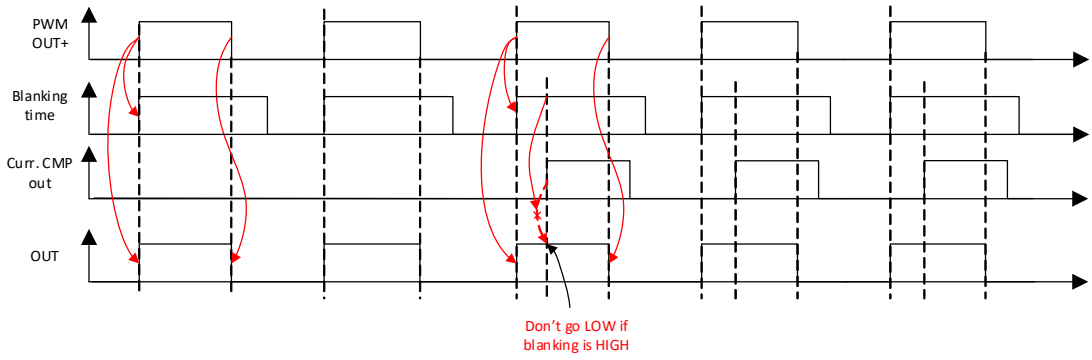


Figure 72. PWM Chopper. PWM Duty Cycle is Less than Blanking Time

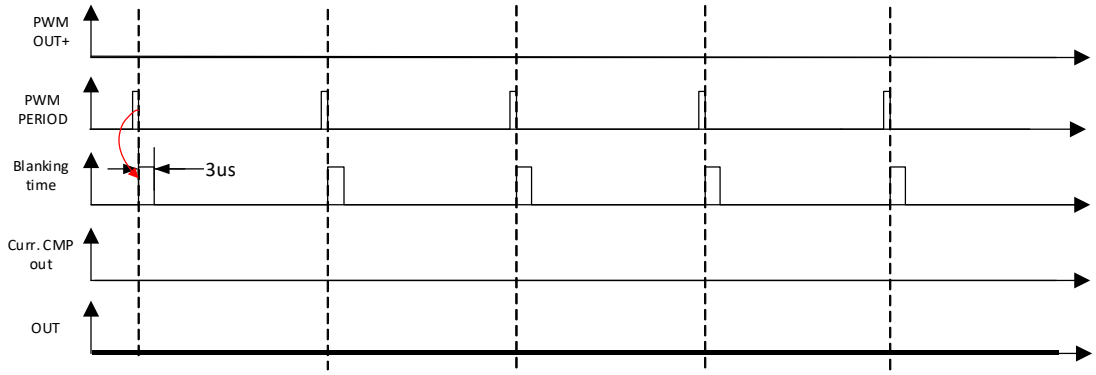


Figure 73. PWM Chopper. 0 % Duty Cycle

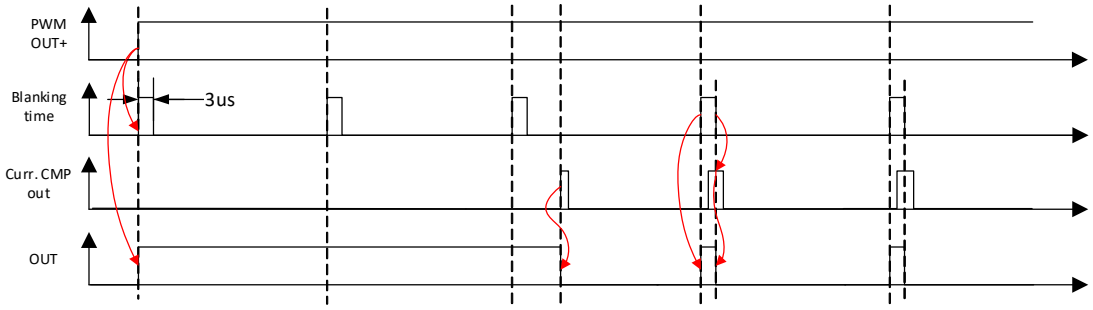


Figure 74. PWM Chopper. Overcurrent when 100 % Duty Cycle

11.4.3 Initial Polarity Operations

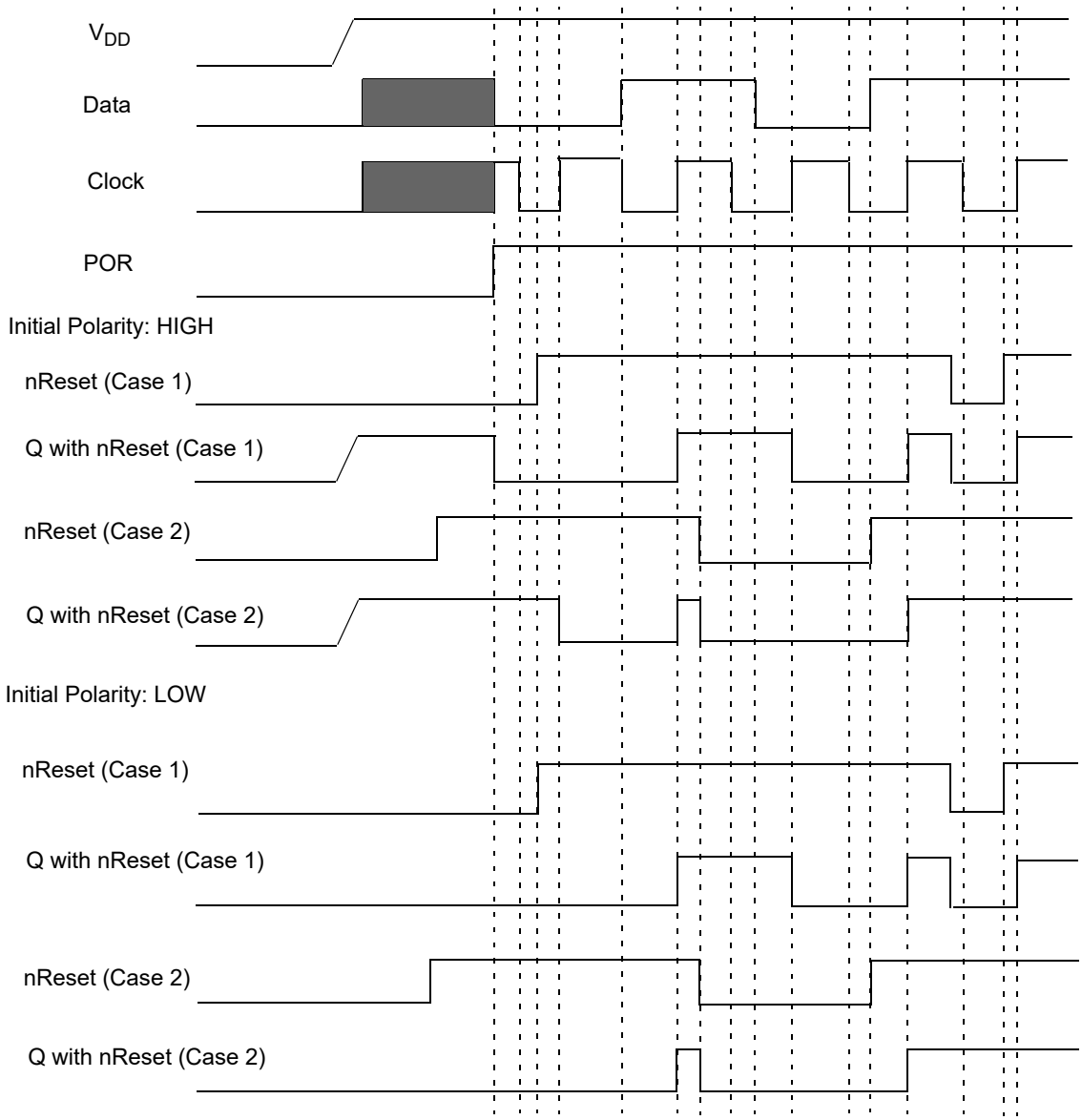


Figure 75. DFF Polarity Operations with nReset

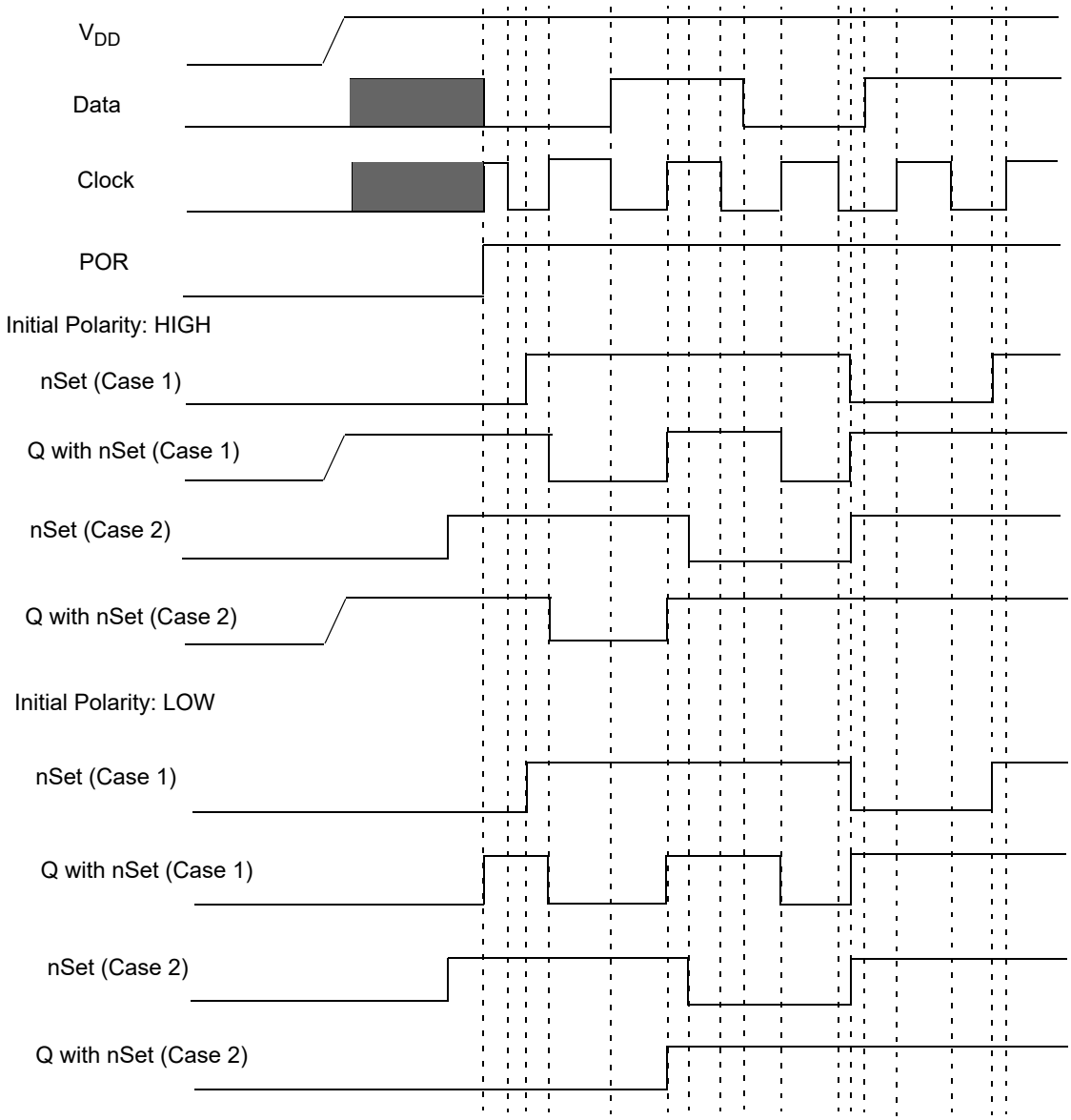


Figure 76. DFF Polarity Operations with nSet

11.5 3-Bit LUT or Pipe Delay/Ripple Counter Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay/Ripple Counter.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a Pipe Delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK), and Reset (nRST). The Pipe Delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell input (IN). Both of the two outputs (OUT0 and OUT1) provide user selectable options for 1 - 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled by registers [1203:1200] for OUT0 and registers [1207:1204] for OUT1. The 4-input mux is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG47115 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the internal Oscillator within the SLG47115). The sum of

the number of DFF cells used will be the total time delay of the Pipe Delay logic cell. OUT1 Output can be inverted (as selected by register [1197]).

In the Ripple Counter mode, there are 3 options for setting which use 7 bits. There are 3 bits to set nSET value (SV) in the range from 0 to 7. This value will be set into the Ripple Counter outputs when nSET input goes LOW. End value (EV) will use 3 bits for setting output code, which will be last code in the cycle. After reaching the EV, the Ripple Counter goes to the first code by the rising edge on CLK input. The Functionality mode option uses 1 bit. This setting defines how exactly Ripple Counter will operate.

The user can select one of the functionality modes by the register: RANGE or FULL. If the RANGE option is selected, the count starts from SV. If UP input is LOW the count goes down: SV→EV→EV-1 to SV+1→SV, and others (if SV is smaller than EV), or SV→SV-1 to EV+1→EV→SV (if SV is bigger than EV). If UP input is HIGH, the count starts from SV up to EV, and others.

In the FULL range configuration, the Ripple Counter functions as follows. If UP input is LOW, the count starts from SV and goes down to 0. The current counter value jumps to EV and goes down to 0, and others.

If UP input is HIGH, the count goes up starting from SV. The current counter value jumps to 0 and counts up to EV, and others. See Ripple Counter functionality example in Figure 78.

Every step is executed by the rising edge on CLK input.

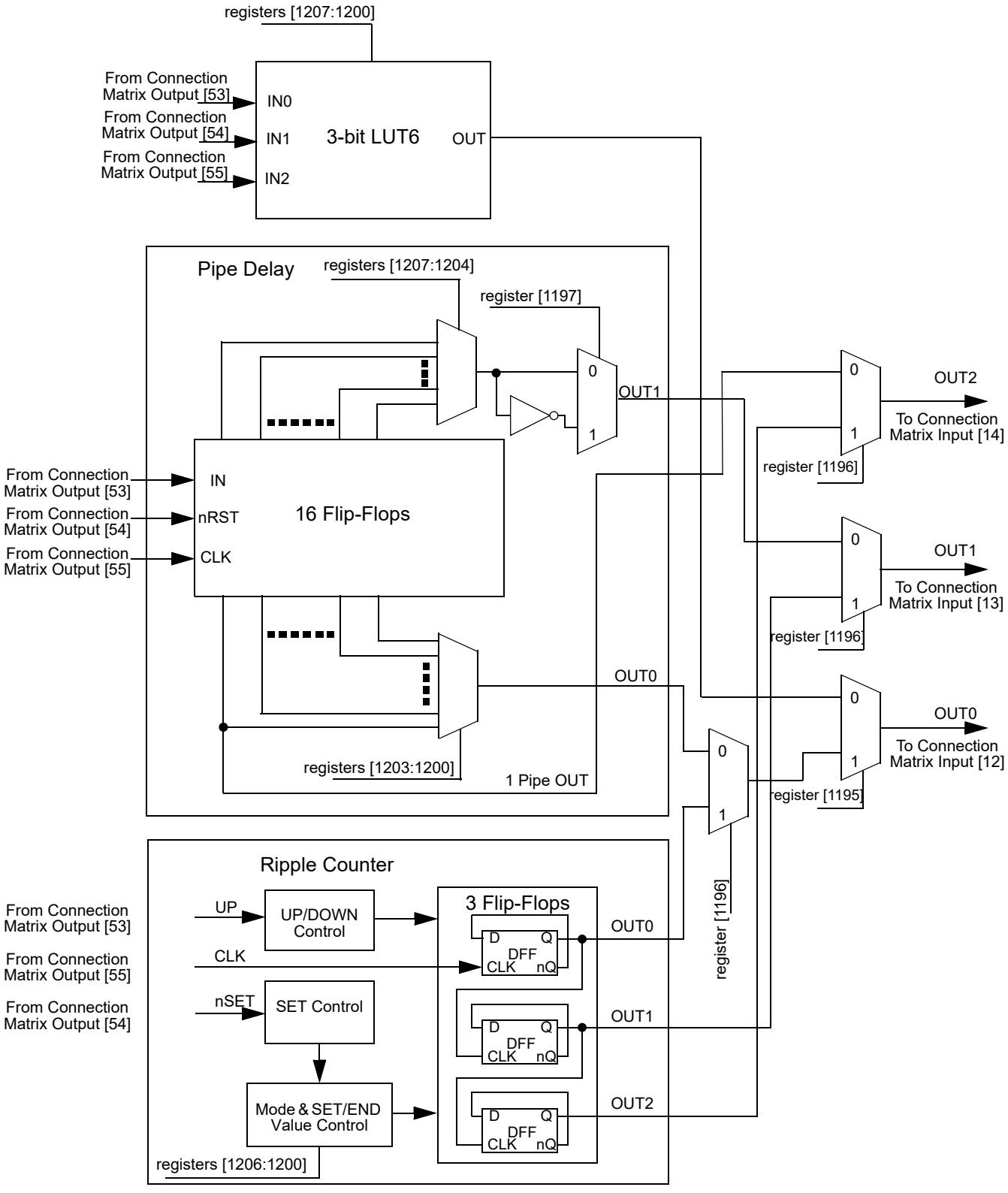


Figure 77. 3-bit LUT6/Pipe Delay/Ripple Counter

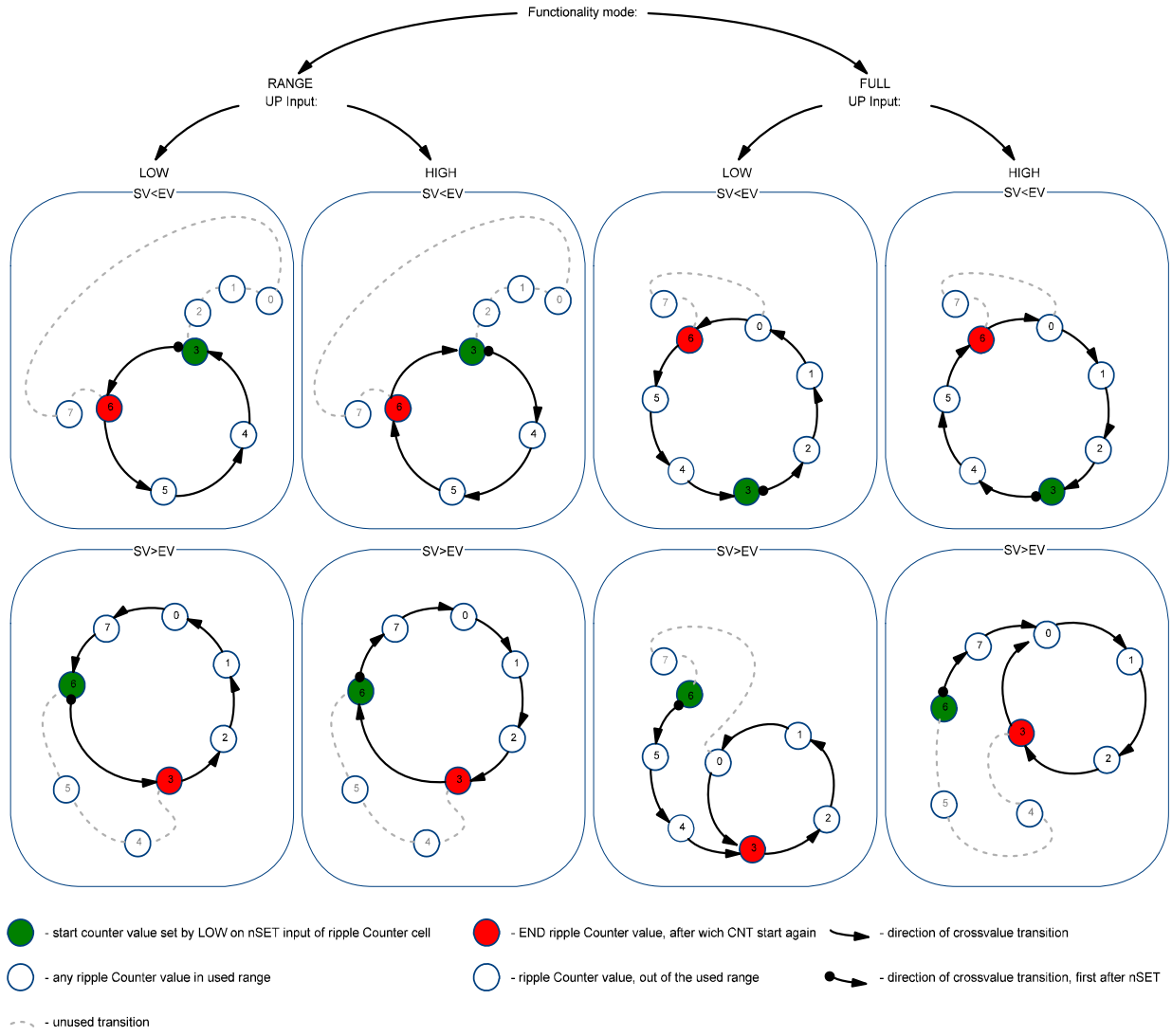


Figure 78. Example of Ripple Counter Functionality

11.5.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUT

Table 55. 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1200]	LSB
0	0	1	register [1201]	
0	1	0	register [1202]	
0	1	1	register [1203]	
1	0	0	register [1204]	
1	0	1	register [1205]	
1	1	0	register [1206]	
1	1	1	register [1207]	MSB

Macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

3-bit LUT6 is defined by registers [1207:1200]

11.6 4-Bit LUT or D Flip-Flop Macrocell

There is one macrocell that can serve as either 4-bit LUT or as D Flip-Flop. When used to implement LUT functions, the 4-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.

LATCH: when CLK is LOW, then Q = D; otherwise Q remains its previous value (input D has no effect on the output when CLK is HIGH).

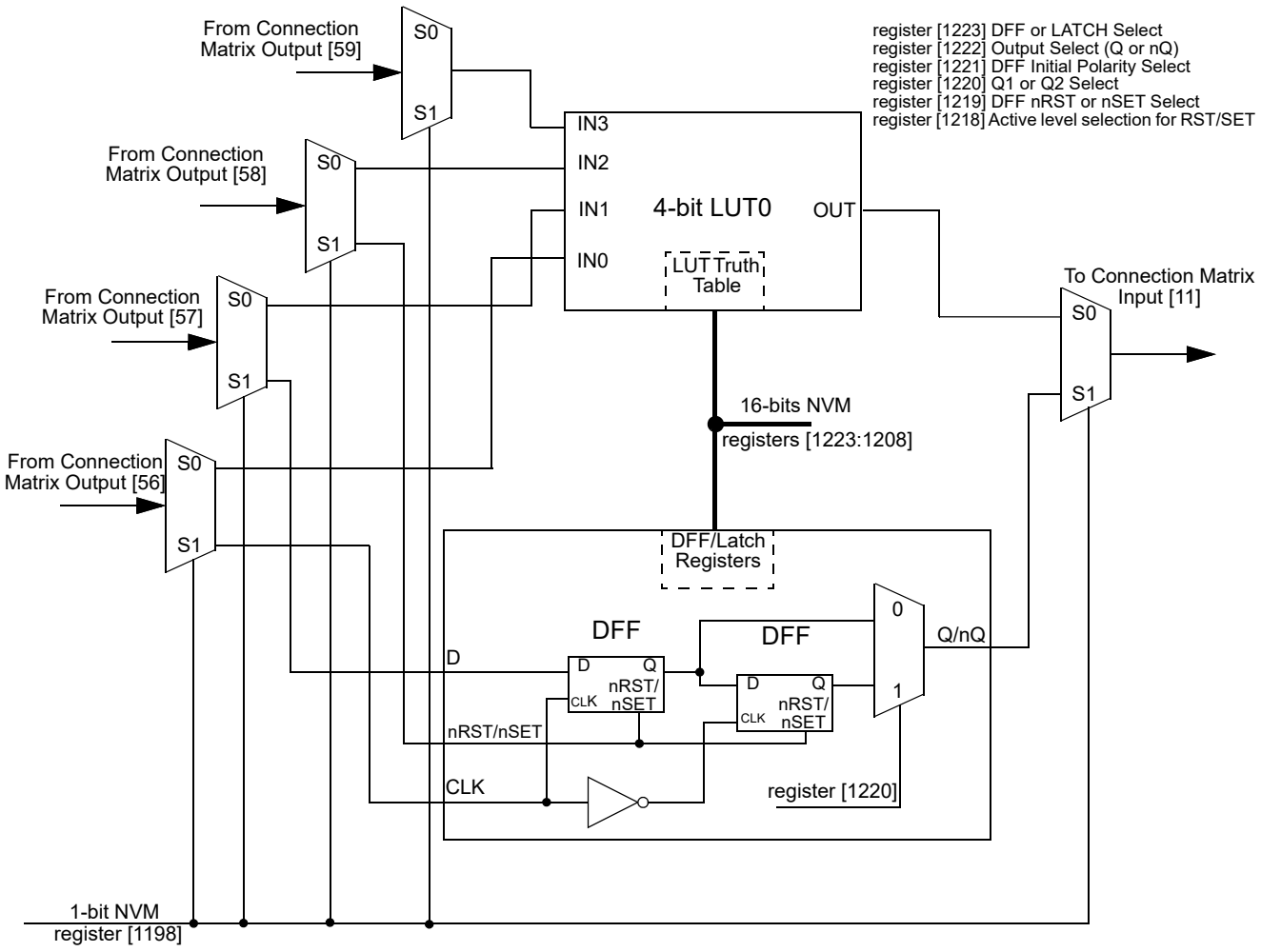


Figure 79. 4-bit LUT0 or DFF9

11.6.1 4-Bit LUT Macrocell Used as 4-Bit LUT

Table 56. 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [1208]	LSB
0	0	0	1	register [1209]	
0	0	1	0	register [1210]	
0	0	1	1	register [1211]	
0	1	0	0	register [1212]	
0	1	0	1	register [1213]	
0	1	1	0	register [1214]	
0	1	1	1	register [1215]	
1	0	0	0	register [1216]	
1	0	0	1	register [1217]	
1	0	1	0	register [1218]	
1	0	1	1	register [1219]	
1	1	0	0	register [1220]	
1	1	0	1	register [1221]	
1	1	1	0	register [1222]	
1	1	1	1	register [1223]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-bit LUT1 is defined by registers [1223:1208]

Table 57. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

12. Multi-Function Macrocells

The SLG47115 has 5 Multi-Function macrocells that can serve as more than one logic or timing function. In each case, they can serve as a LUT, DFF with flexible settings, or as CNT/DLY with multiple modes such as One Shot, Frequency Detect, Edge Detect, and others. Also, the macrocell is capable to combine those functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF, see Figure 80.

See the list below for the functions that can be implemented in these macrocells:

- Three macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays
- One macrocell that can serve as a 4-bit LUT/D Flip-Flop and as 16-Bit Counter/Delay/FSM

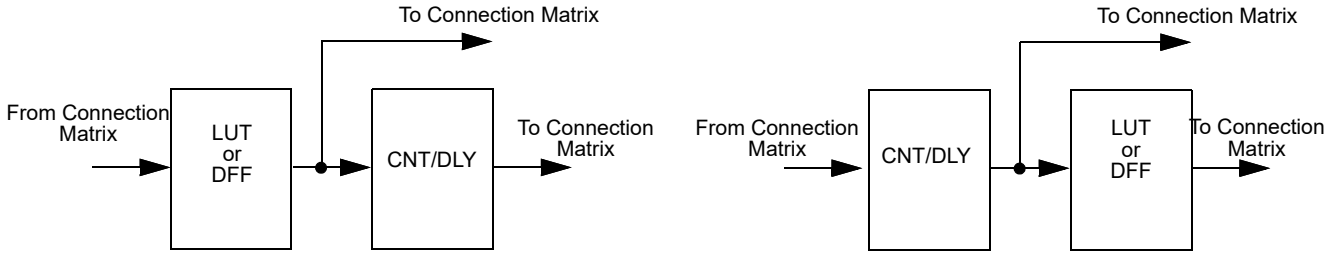


Figure 80. Possible Connections inside Multi-Function Macrocell

Inputs/Outputs for the 5 Multi-Function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user-defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

12.1 3-Bit LUT or DFF/LATCH with 8-Bit Counter/Delay Macrocells

There are four macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays.

When used to implement LUT functions, the 3-bit LUTs each takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix or can be connected to CNT/DLY's input.

When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D), clock (CLK), and Reset/Set (nRST/nSET) inputs of the Flip-Flop, with the output going back to the connection matrix or to the CNT/DLY's input.

When used to implement Counter/Delays, each macrocell has a dedicated matrix input connection. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count/delay circuits. These macrocells can also operate in a One-Shot mode, which will generate an output pulse of user-defined width. They can also operate in a Frequency Detection or Edge Detection mode.

Counter/Delay macrocell has an initial value, which defines its initial value after GPAK is powered up. It is possible to select initial LOW or initial HIGH, as well as the initial value defined by a Delay In signal.

For example, in case the initial LOW option is used, the rising edge delay will start operation.

For timing diagrams refer to Section 12.2 CNT/DLY/FSM Timing Diagrams.

Only CNT0 and CNT4 current count value can be read via I^2C. However, it is possible to change the counter data (value counter starts operating from) for any macrocell using I^2C write commands. In this mode, it is possible to load count data immediately (after two DFF[Note]) or after counter ends counting. See Section 21.5.4 Reading Current Counter Data via I2C for further details.

Note: After two DFF – counters initialize with counter data = 0 after POR.

Initial state = 1 – counters initialize with counter data = 0 after POR.

Initial state = 0 And After two DFF is bypass – counters initialize with counter data after POR.

12.1.1 3-Bit LUT or 8-Bit CNT/DLY Block Diagrams

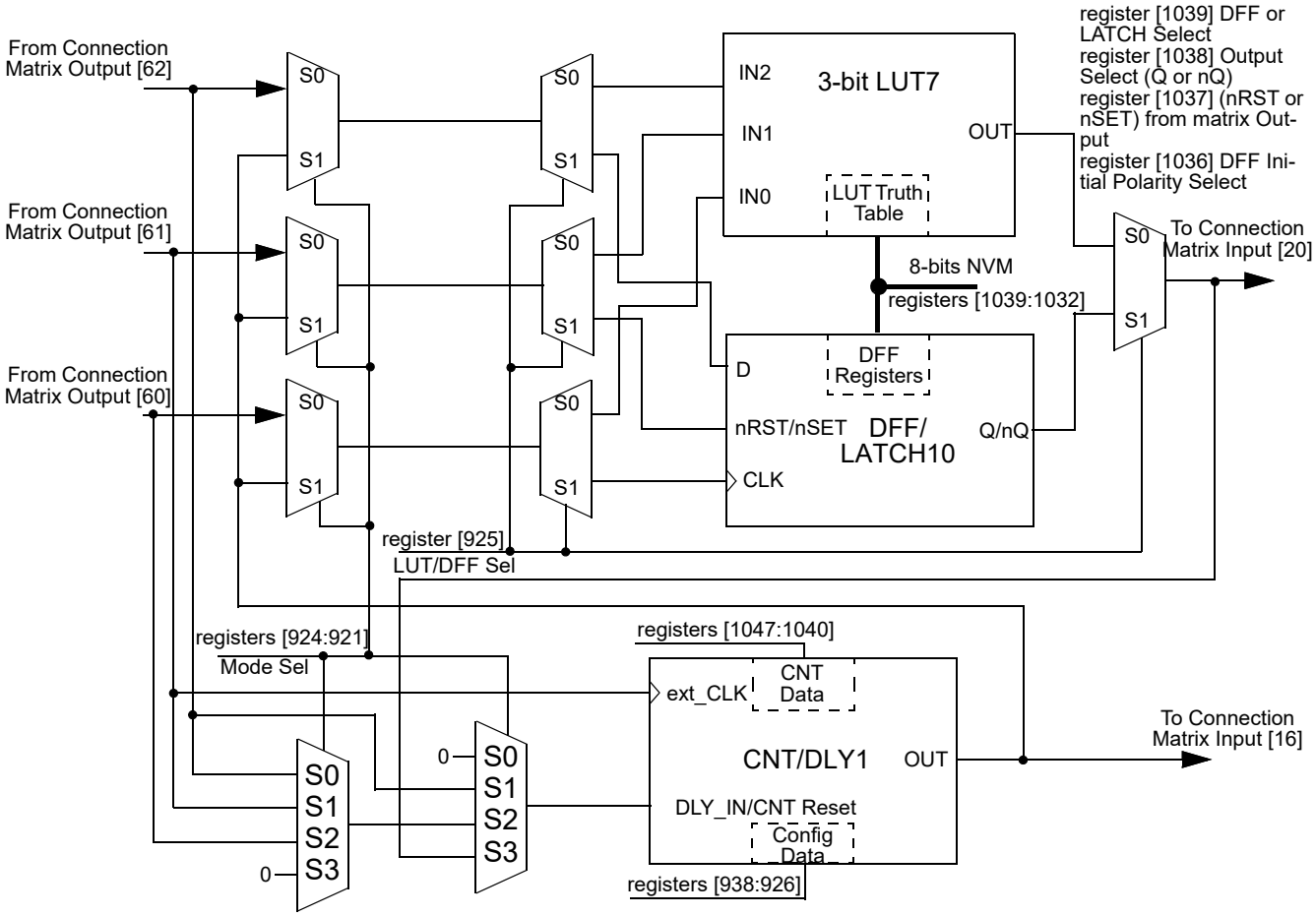


Figure 81. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT7/DFF10, CNT/DLY1)

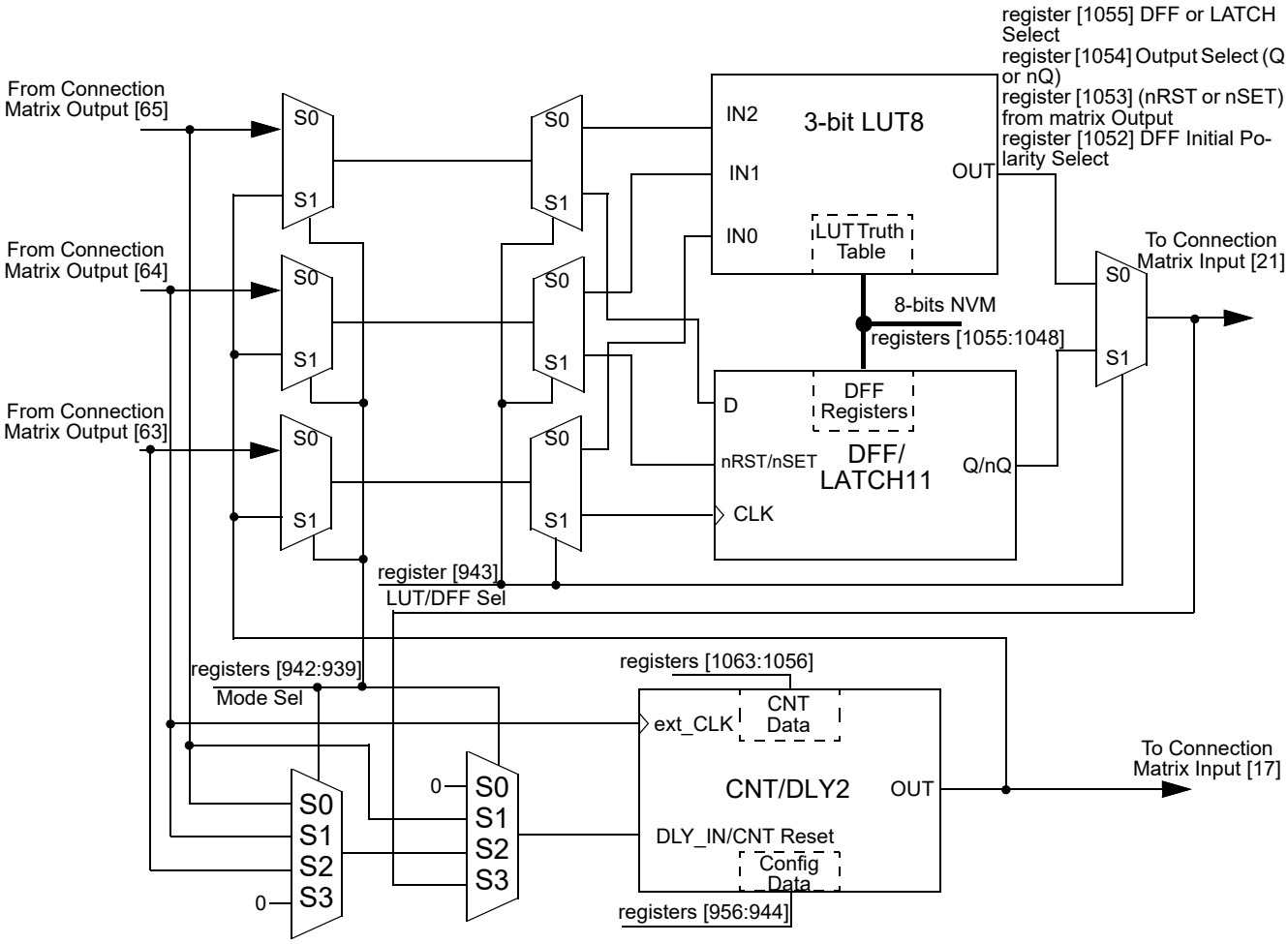


Figure 82. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT8/DFF11, CNT/DLY2)

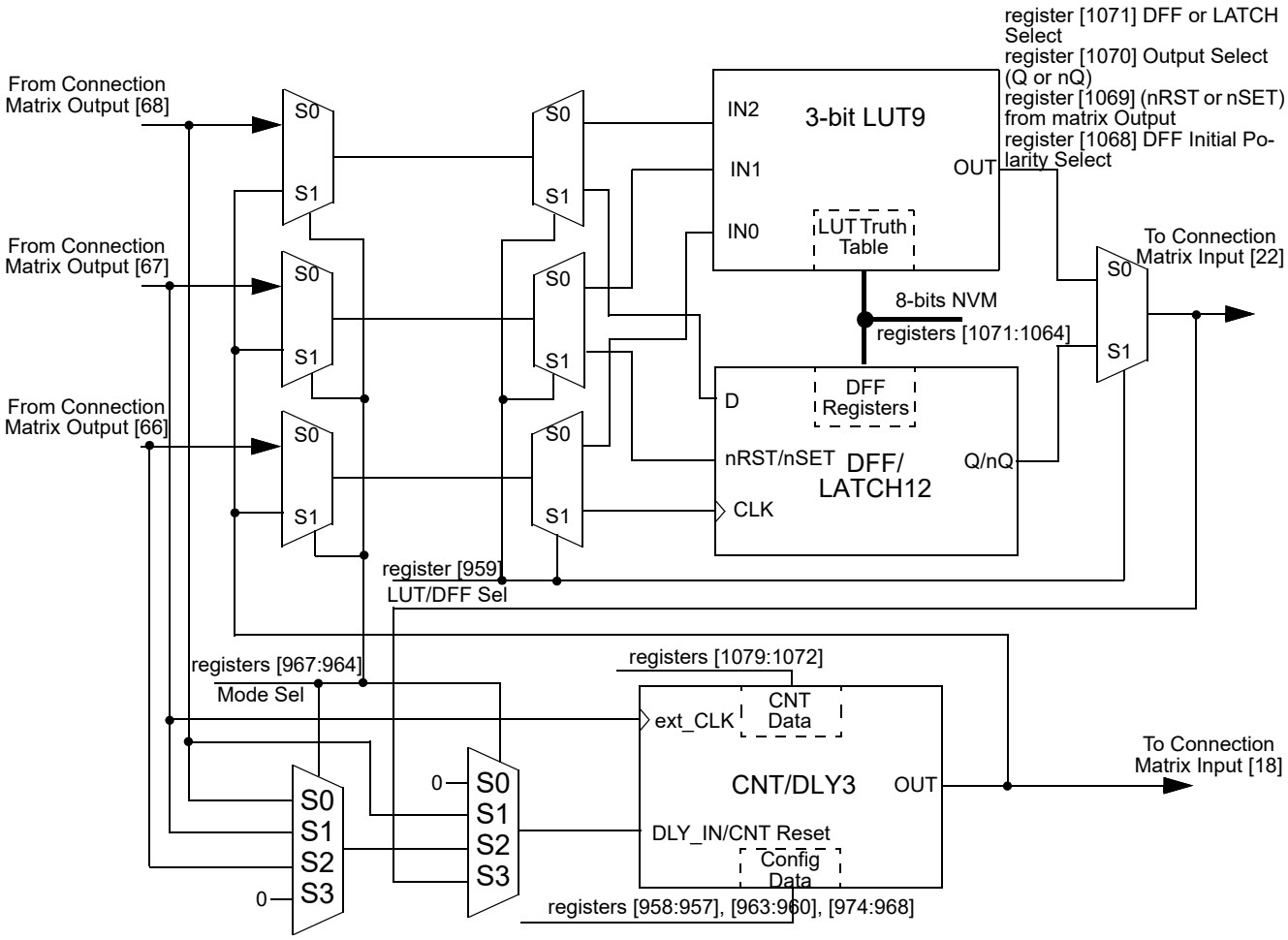


Figure 83. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT9/DFF12, CNT/DLY3)

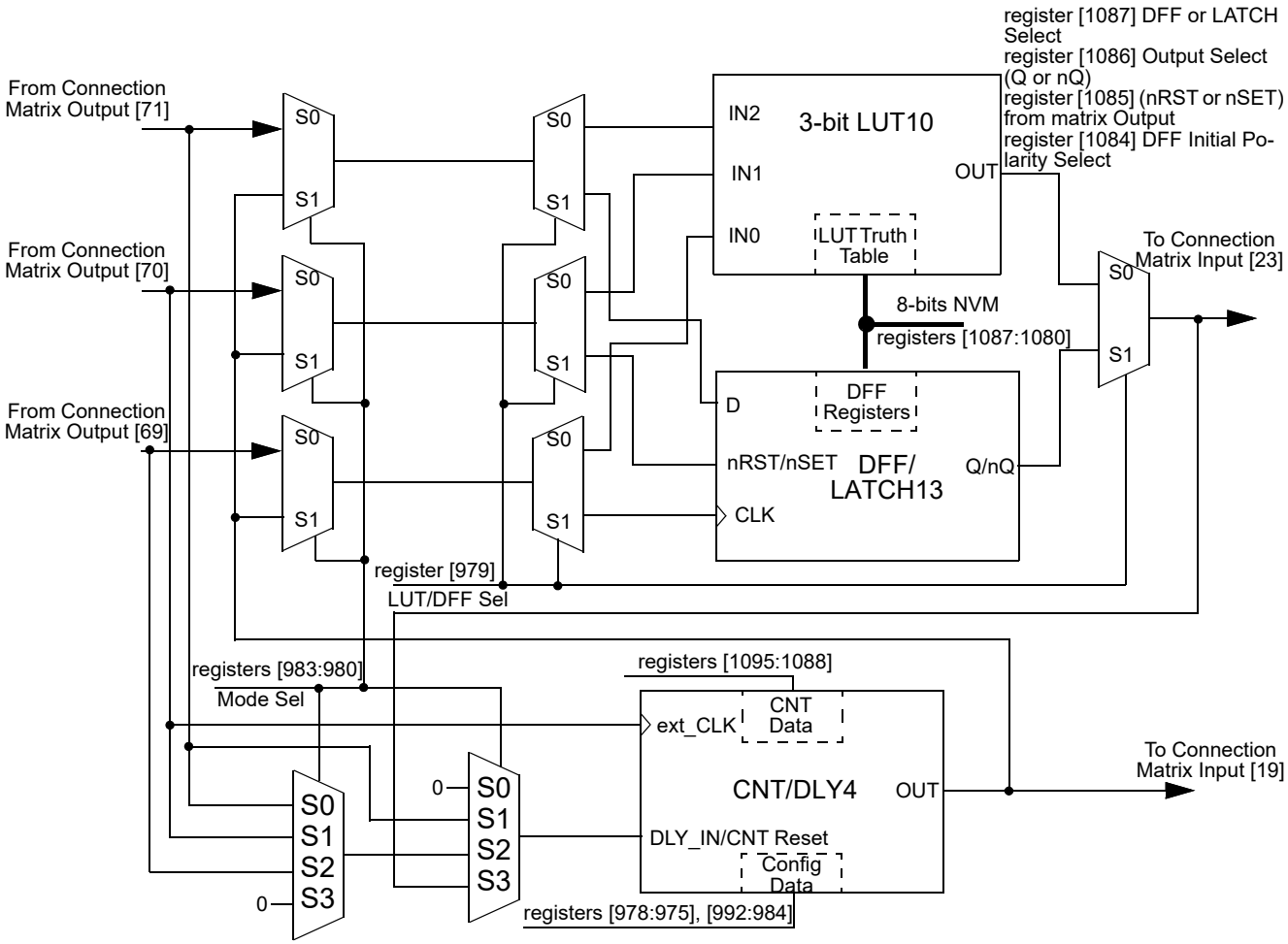


Figure 84. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT10/DFF13, CNT/DLY4)

There is a possibility to use LUT/DFF and CNT/DLY simultaneously[Note].

Note: It is not possible to use LUT and DFF at once, one of these macrocells must be selected.

- Case 1. LUT/DFF in front of CNT/DLY. Three input signals from the connection matrix go to previously selected LUT or DFF's inputs and produce a single output which goes to a CND/DLY input. In its turn Counter/Delay's output goes back to the matrix.
- Case 2. CNT/DLY in front of LUT/DFF. Two input signals from the connection matrix go to CND/DLY's inputs (IN and CLK). Its output signal can be connected to any input of previously selected LUT or DFF, after which the signal goes back to the matrix.
- Case 3. Single LUT/DFF or CNT/DLY. Also, it is possible to use a standalone LUT/DFF or CNT/DLY. In this case, all inputs and output of the macrocell are connected to the matrix.

12.1.2 3-Bit LUT or CNT/DLYs Used as 3-Bit LUTs

Table 58. 3-bit LUT7 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1032]	LSB
0	0	1	register [1033]	
0	1	0	register [1034]	
0	1	1	register [1035]	
1	0	0	register [1036]	
1	0	1	register [1037]	
1	1	0	register [1038]	
1	1	1	register [1039]	MSB

Table 59. 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1064]	LSB
0	0	1	register [1065]	
0	1	0	register [1066]	
0	1	1	register [1067]	
1	0	0	register [1068]	
1	0	1	register [1069]	
1	1	0	register [1070]	
1	1	1	register [1071]	MSB

Table 60. 3-bit LUT8 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1048]	LSB
0	0	1	register [1049]	
0	1	0	register [1050]	
0	1	1	register [1051]	
1	0	0	register [1052]	
1	0	1	register [1053]	
1	1	0	register [1054]	
1	1	1	register [1055]	MSB

Table 61. 3-bit LUT10 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1080]	LSB
0	0	1	register [1081]	
0	1	0	register [1082]	
0	1	1	register [1083]	
1	0	0	register [1084]	
1	0	1	register [1085]	
1	1	0	register [1086]	
1	1	1	register [1087]	MSB

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-bit LUT7 is defined by registers [1039:1032]

3-bit LUT8 is defined by registers [1055:1048]

3-bit LUT9 is defined by registers [1071:1064]

3-bit LUT10 is defined by registers [1087:1080]

12.2 CNT/DLY/FSM Timing Diagrams

12.2.1 Delay Mode CNT/DLY0 to CNT/DLY4

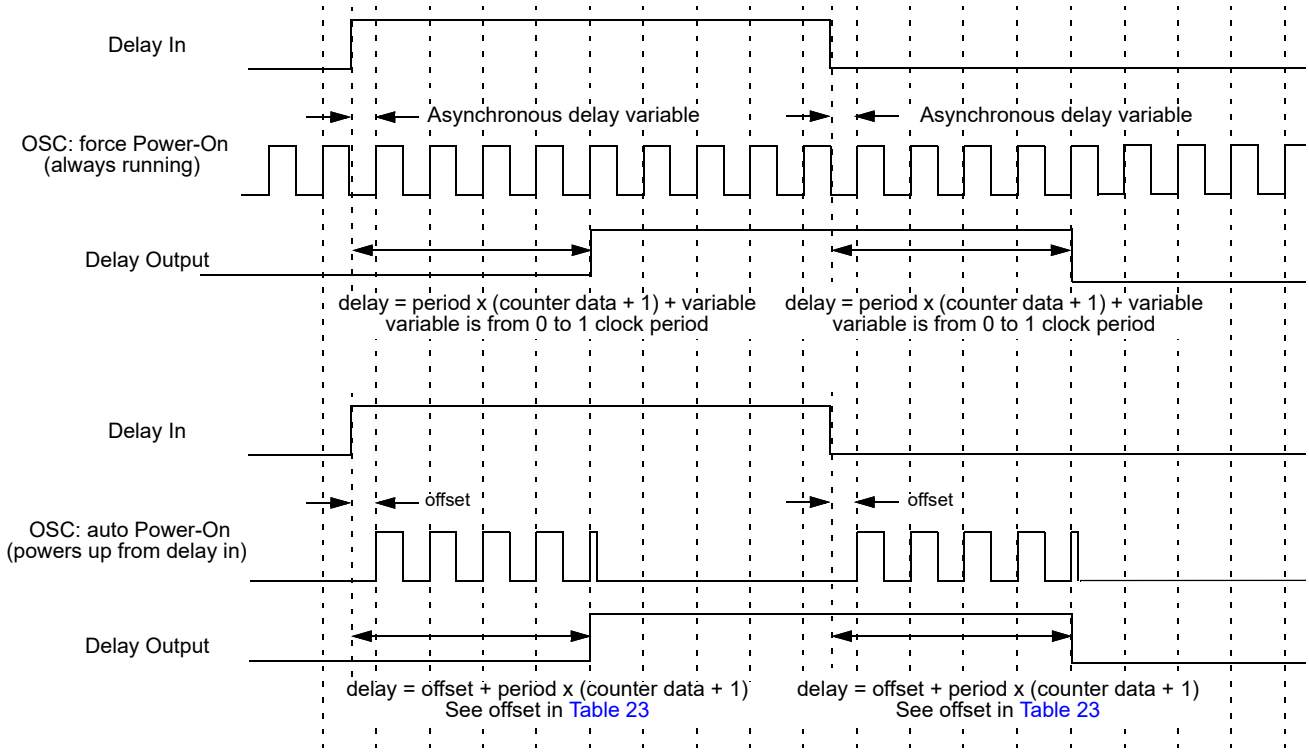


Figure 85. Delay Mode Timing Diagram, Edge Select: Both, Counter Data: 3

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter if the input signal is shorter than the delay time.

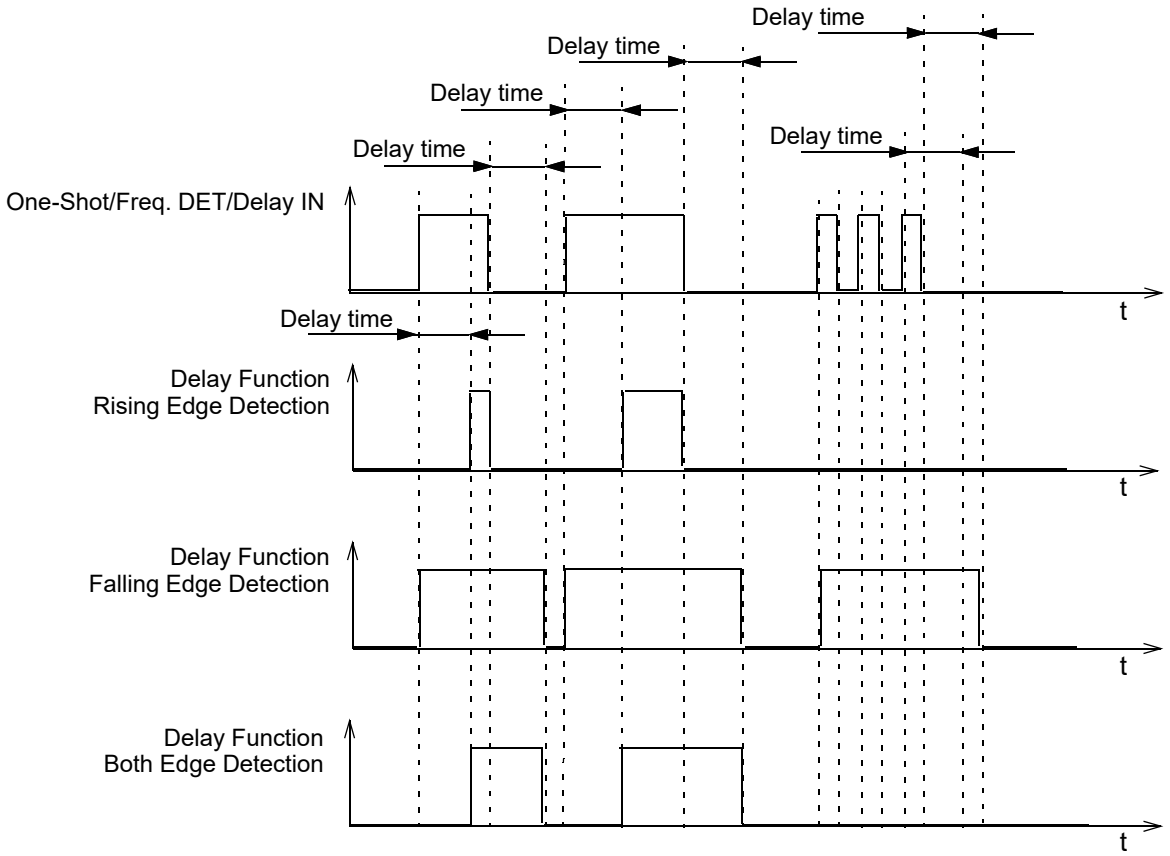


Figure 86. Delay Mode Timing Diagram for Different Edge Select Modes

12.2.2 Count Mode (Count Data: 3), Counter Reset (Rising Edge Detect) CNT/DLY0 to CNT/DLY4

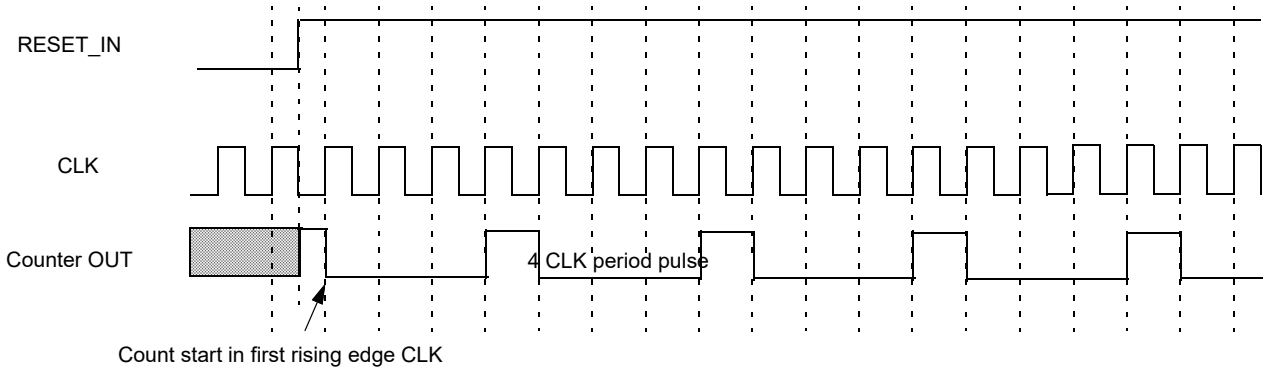


Figure 87. Counter Mode Timing Diagram without Two DFFs Synced Up

Note: This mode may cause counter data to be loaded wrong if reset releases at the same time when the clock appears. As a solution please use the mode with two DFFs synced up.

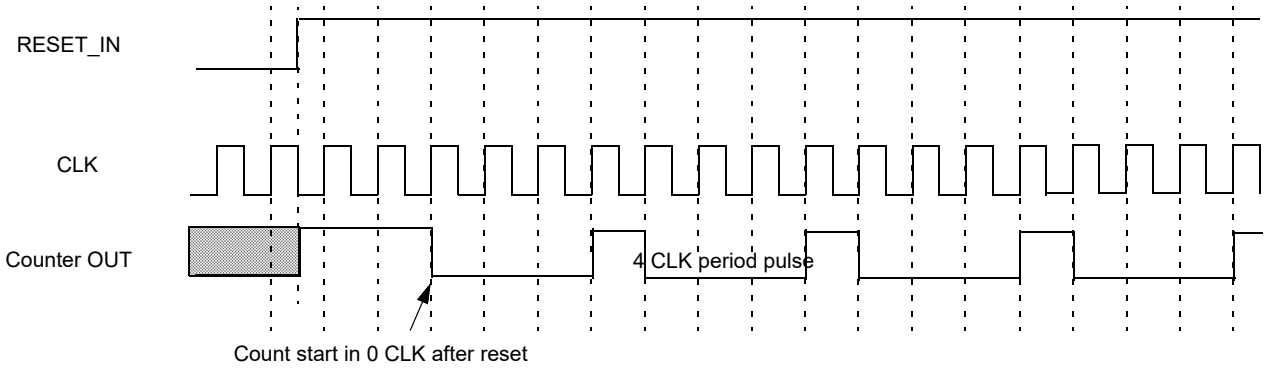


Figure 88. Counter Mode Timing Diagram with Two DFFs Synced Up

12.2.3 One-Shot Mode CNT/DLY0 to CNT/DLY4

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width is determined by counter data and clock selection properties.

The output pulse polarity (non-inverted or inverted) is selected by register bit. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.

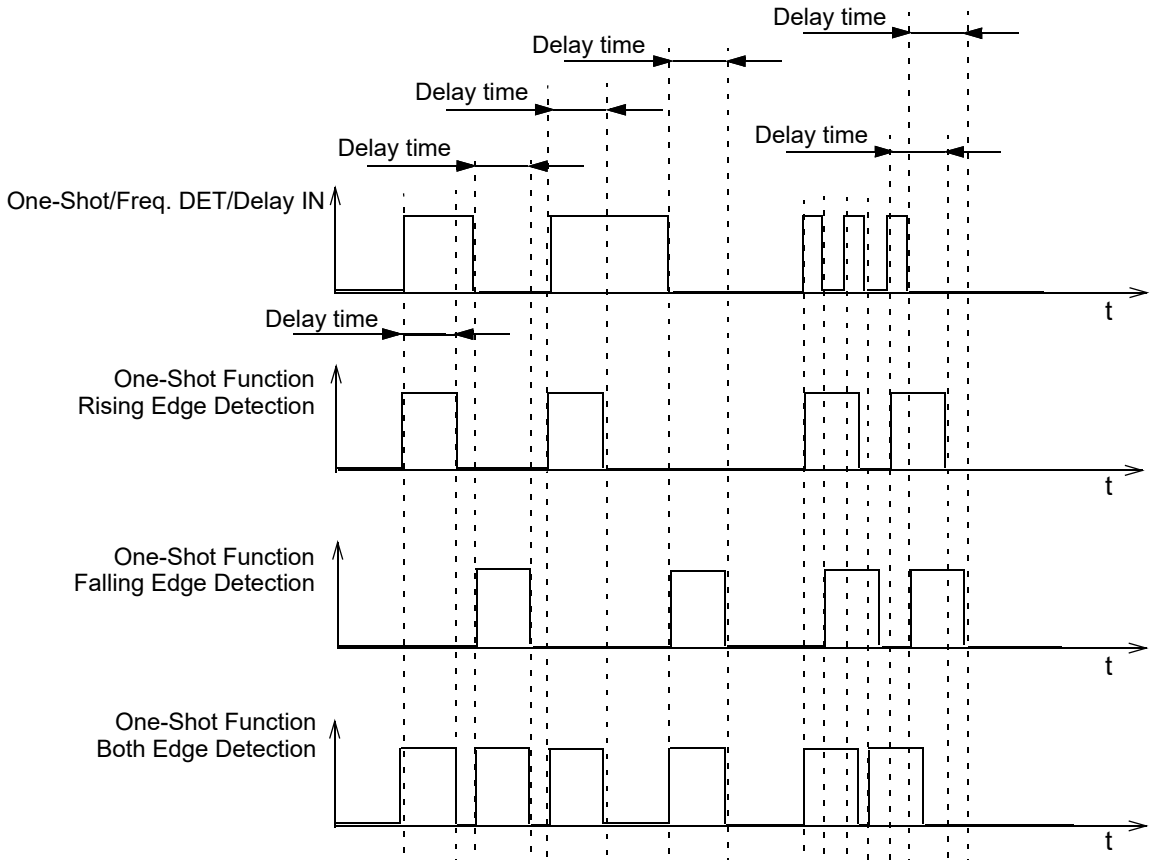


Figure 89. One-Shot Function Timing Diagram

This macrocell generates a high-level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is HIGH.

12.2.4 Frequency Detection Mode CNT/DLY0 to CNT/DLY4

Rising Edge: The output goes HIGH if the time between two successive edges is less than the delay. The output goes LOW if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes HIGH if the time between two falling edges is less than the set time. The output goes LOW if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes HIGH if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes LOW if after the last rising/falling edge and specified time, the second edge has not come.

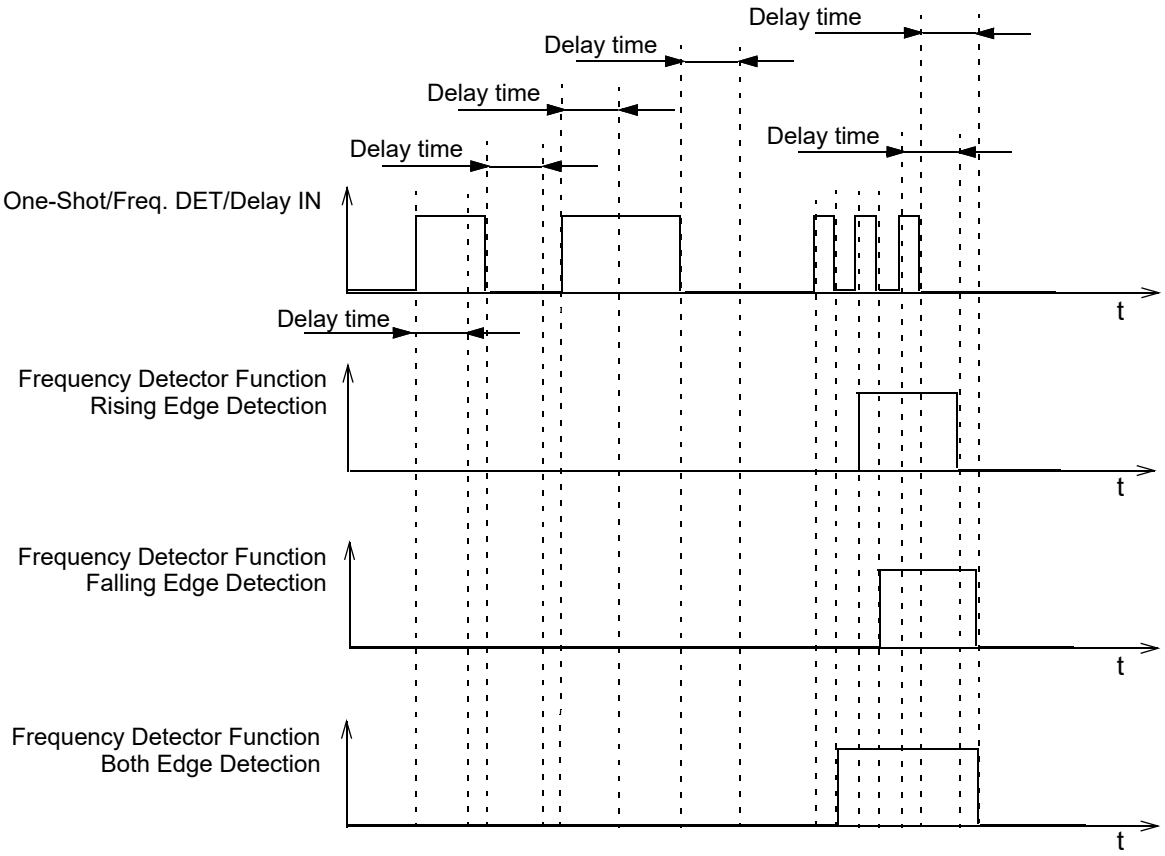


Figure 90. Frequency Detection Mode Timing Diagram

12.2.5 Edge Detection Mode CNT/DLY1 to CNT/DLY4

The macrocell generates high-level short pulse when detecting the respective edge.

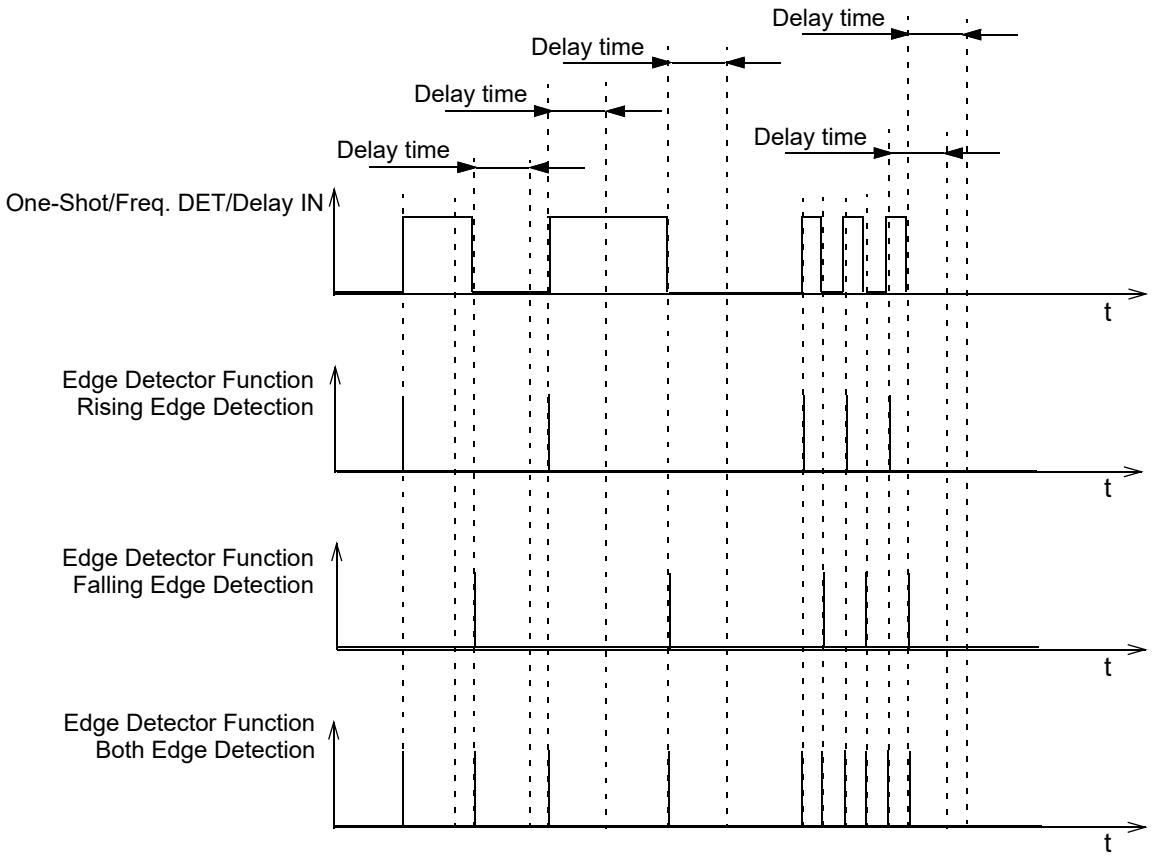


Figure 91. Edge Detection Mode Timing Diagram

12.2.6 Delayed Edge Detection Mode CNT/DLY0 to CNT/DLY4

In Delayed Edge Detection mode, High-level short pulses are generated on the macrocell output after the configured delay time, if the corresponding edge was detected on the input.

If the input signal is changed during the set delay time, the pulse will not be generated. See Figure 92.

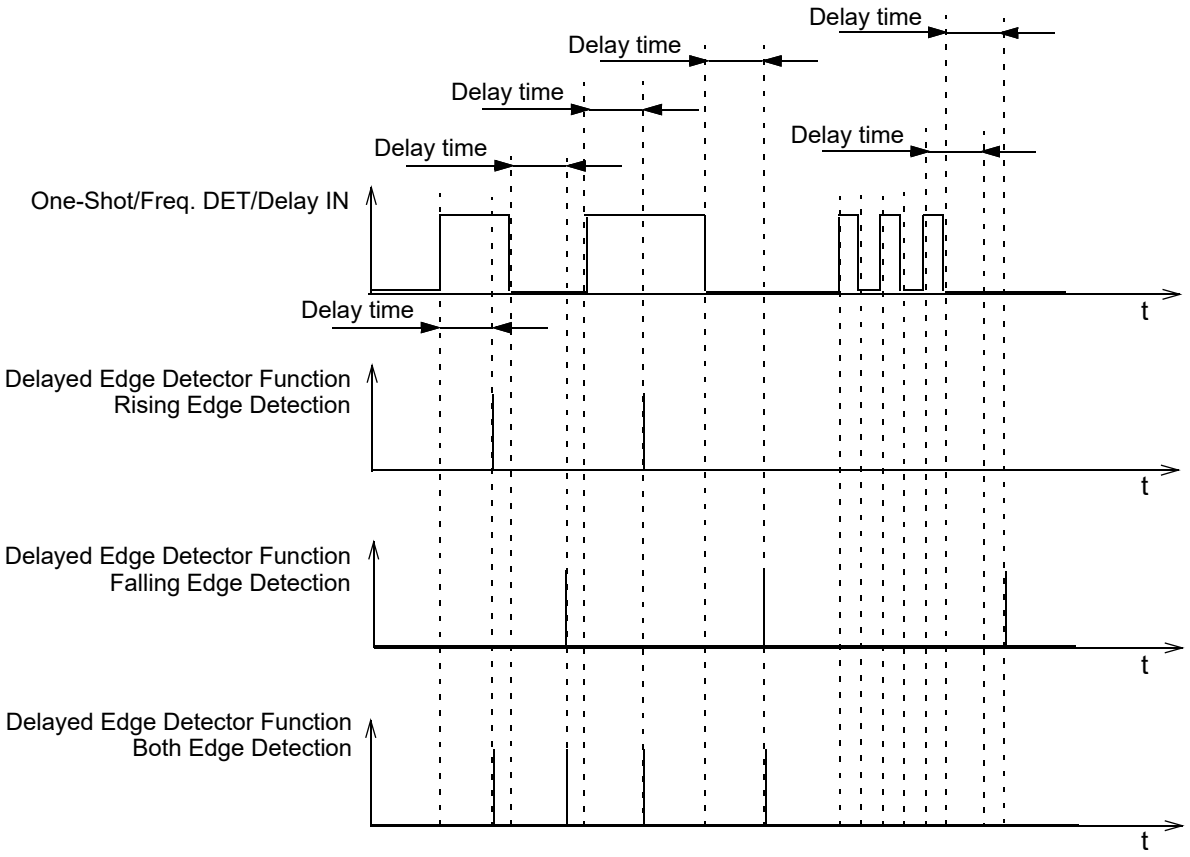


Figure 92. Delayed Edge Detection Mode Timing Diagram

12.2.7 CNT/FSM Mode CNT/DLY0

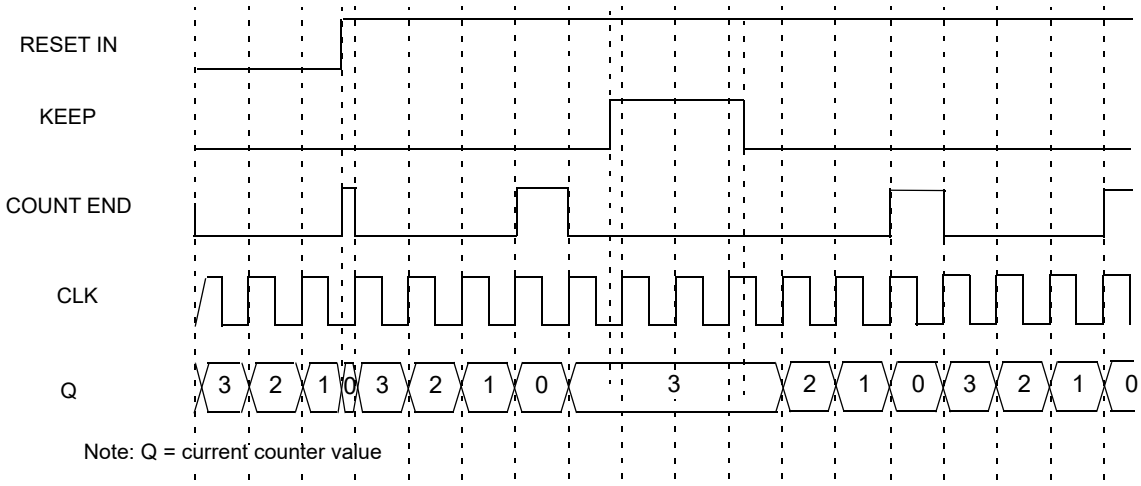


Figure 93. CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3

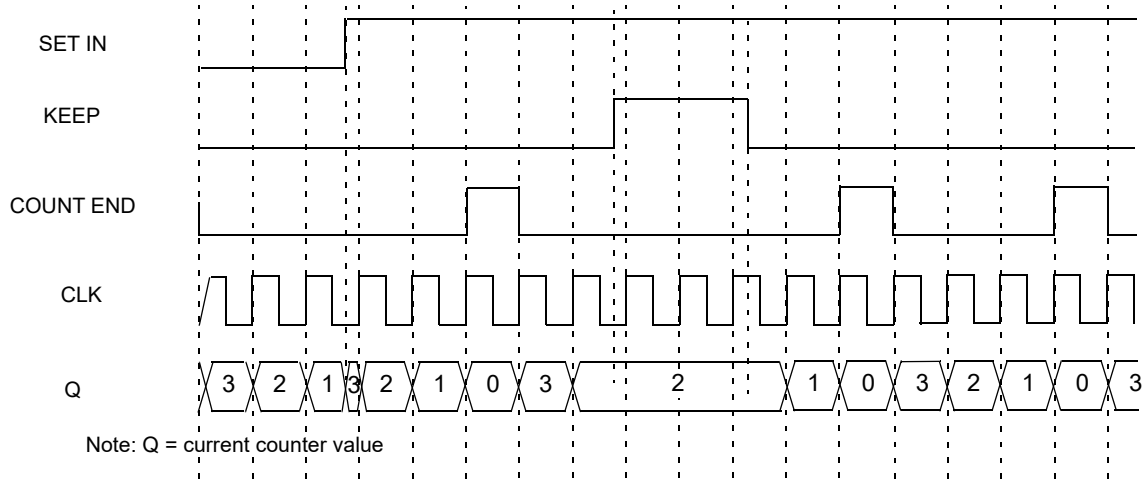


Figure 94. CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3

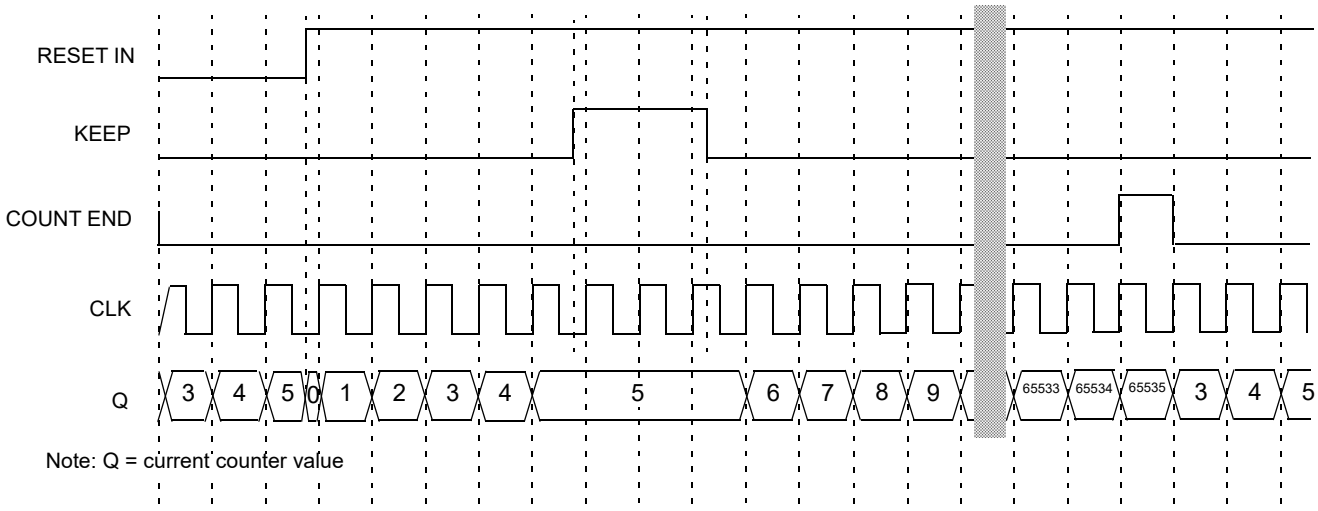


Figure 95. CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 1) for Counter Data = 3

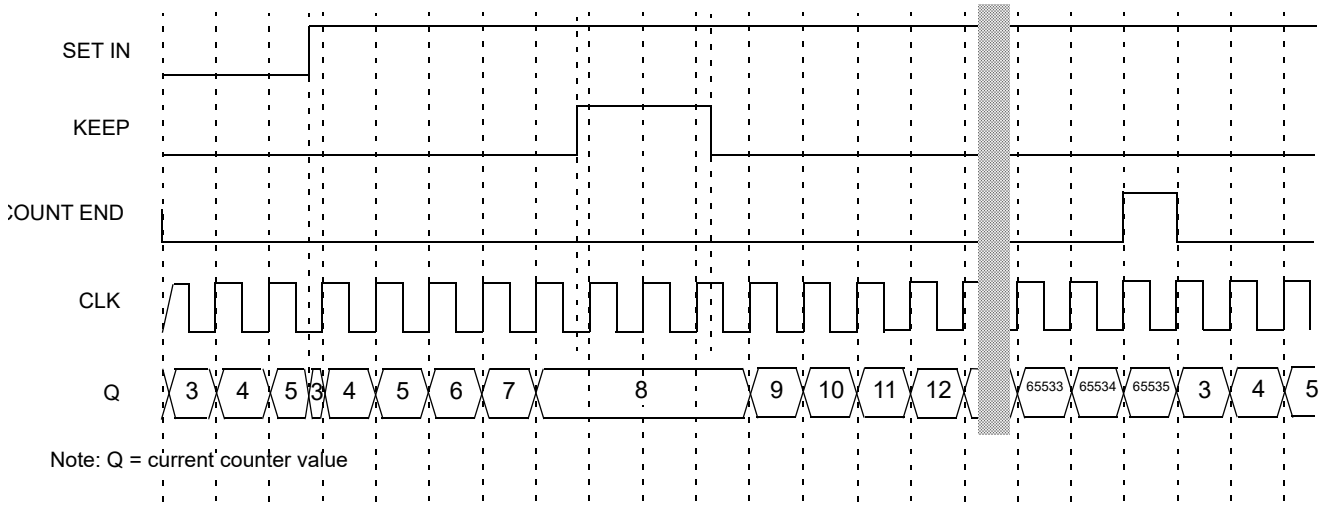


Figure 96. CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 1) for Counter Data = 3

12.2.8 The Difference in Counter Value for Counter, Delay, One-Shot, and Frequency Detect Modes

There is a difference in counter value for Counter and Delay/One-Shot/Frequency Detect modes. Compared to Counter mode, in Delay/One-Shot/Frequency Detect modes the counter value is shifted for two rising edges of the clock signal.

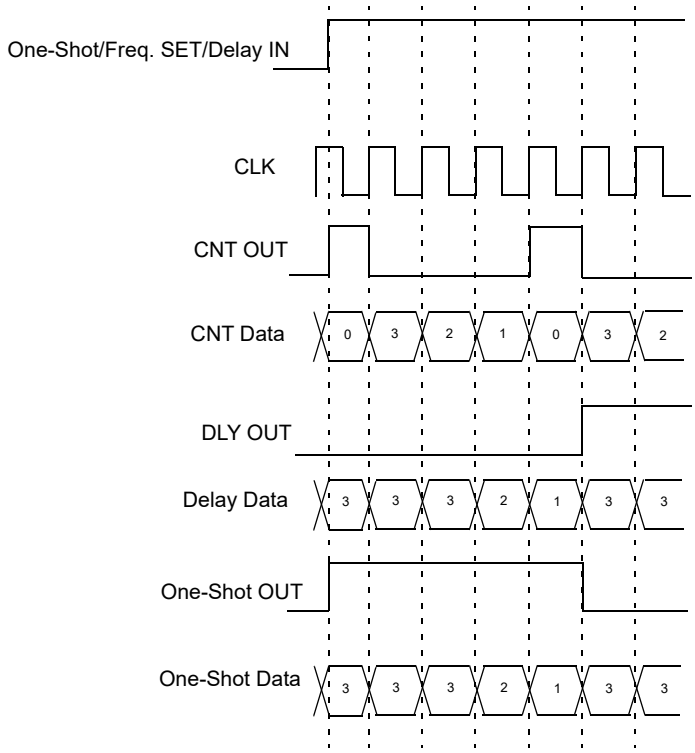


Figure 97. Counter Value, Counter Data = 3

12.3 4-Bit LUT or DFF/LATCH with 16-Bit Counter/Delay Macrocell

There is one macrocell that can serve as either 4-bit LUT or as 16-bit Counter/Delay. When used to implement LUT function, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix. When used to implement 16-Bit Counter/Delay function, two of four input signals from the connection matrix go to the external clock (EXT_CLK) and reset (DLY_IN/CNT Reset) for the Counter/Delay, with the output going back to the connection matrix.

This macrocell has an optional Finite State Machine (FSM) function. There are two additional matrix inputs for Up and Keep to support FSM functionality.

This macrocell can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

This macrocell can also operate in a frequency detection or edge detection mode.

This macrocell can have its active count value read via I^2C. See Section 21.5.4 Reading Current Counter Data via I2C for further details.

Note: After two DFF – counters initialize with counter data = 0 after POR.

Initial state = 1 – counters initialize with counter data = 0 after POR.

Initial state = 0 And After two DFF is bypass – counters initialize with counter data after POR.

12.3.1 4-Bit LUT or DFF/LATCH with 16-Bit CNT/DLY Block Diagram

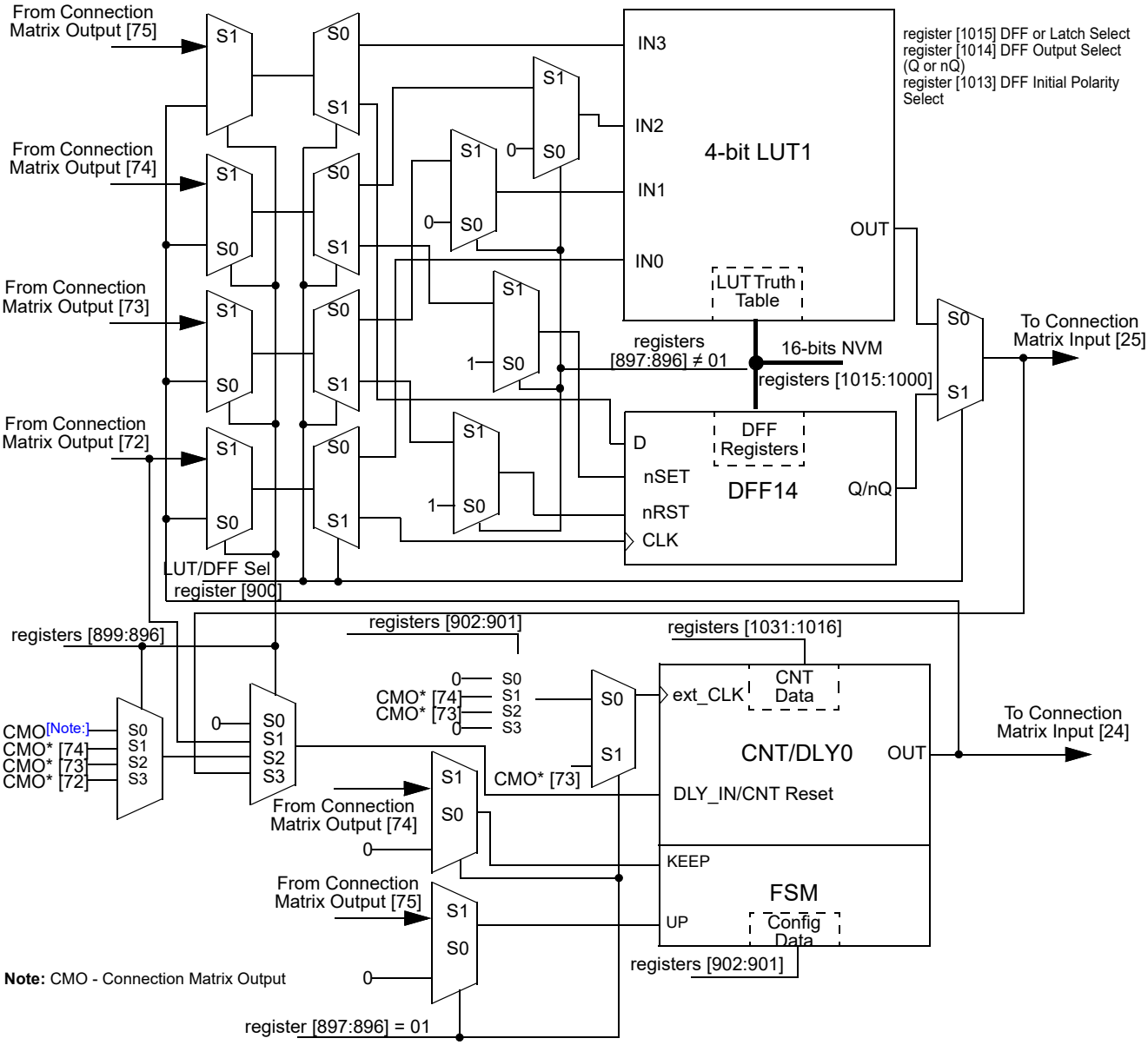


Figure 98. 16-bit Multi-Function Macrocell Block Diagram (4-bit LUT1/DFF14, CNT/DLY/FSM0)

12.3.2 4-Bit LUT or 16-Bit Counter/Delay Macrocells Used as 4-Bit LUTs

Table 62. 4-bit LUT1 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [1000]	LSB
0	0	0	1	register [1001]	
0	0	1	0	register [1002]	
0	0	1	1	register [1003]	
0	1	0	0	register [1004]	
0	1	0	1	register [1005]	
0	1	1	0	register [1006]	
0	1	1	1	register [1007]	
1	0	0	0	register [1008]	
1	0	0	1	register [1009]	
1	0	1	0	register [1010]	
1	0	1	1	register [1011]	
1	1	0	0	register [1012]	
1	1	0	1	register [1013]	
1	1	1	0	register [1014]	
1	1	1	1	register [1015]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-bit LUT1 is defined by registers [1015:1000]

Table 63. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	1

12.4 Wake and Sleep Controller

SLG47115 has a Wake and Sleep function for two General Purpose ACMPs. The macrocell CNT/DLY0 can be reconfigured for this purpose by setting register [918] = 1 and registers [904:903] = 11. The WS serves for power saving, it allows to switch on and off selected General Purpose ACMPs on a selected bit of 16-bit counter.

Note 1: BG/Analog_Good time is long and should be considered in the wake and sleep timing in case it dynamically powers on/off.
Note 2: Wake time should be long enough to make sure ACMP and Vref have enough time to get a sample before going to sleep.

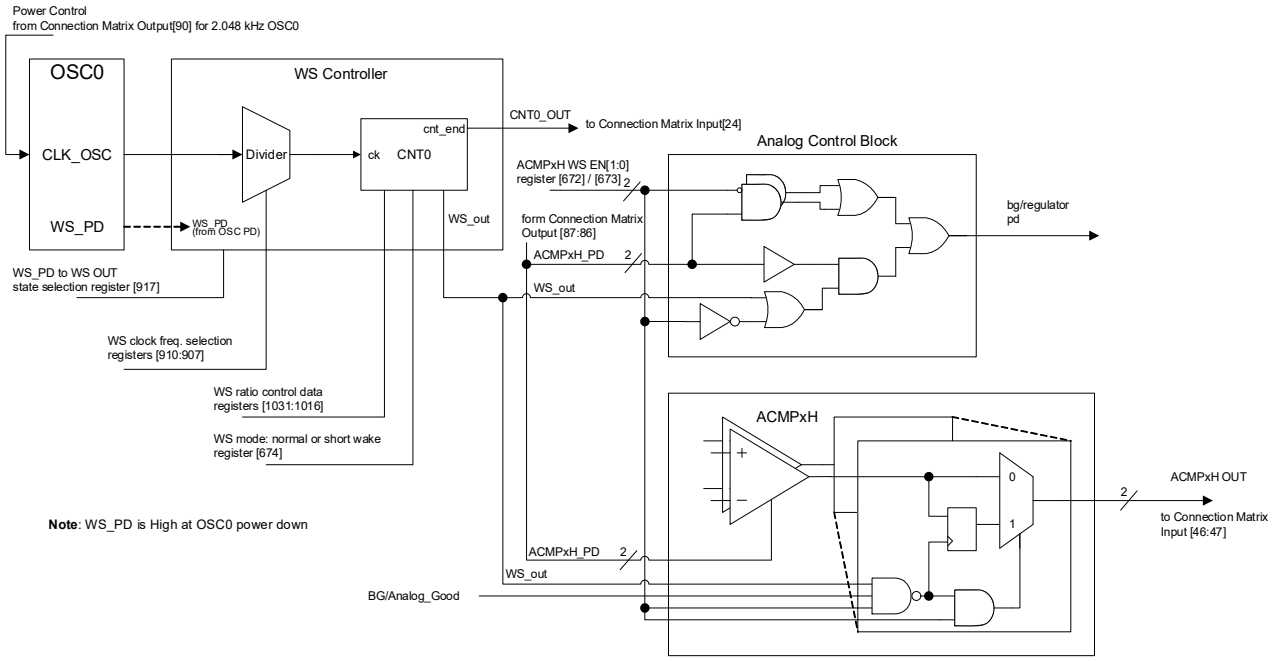
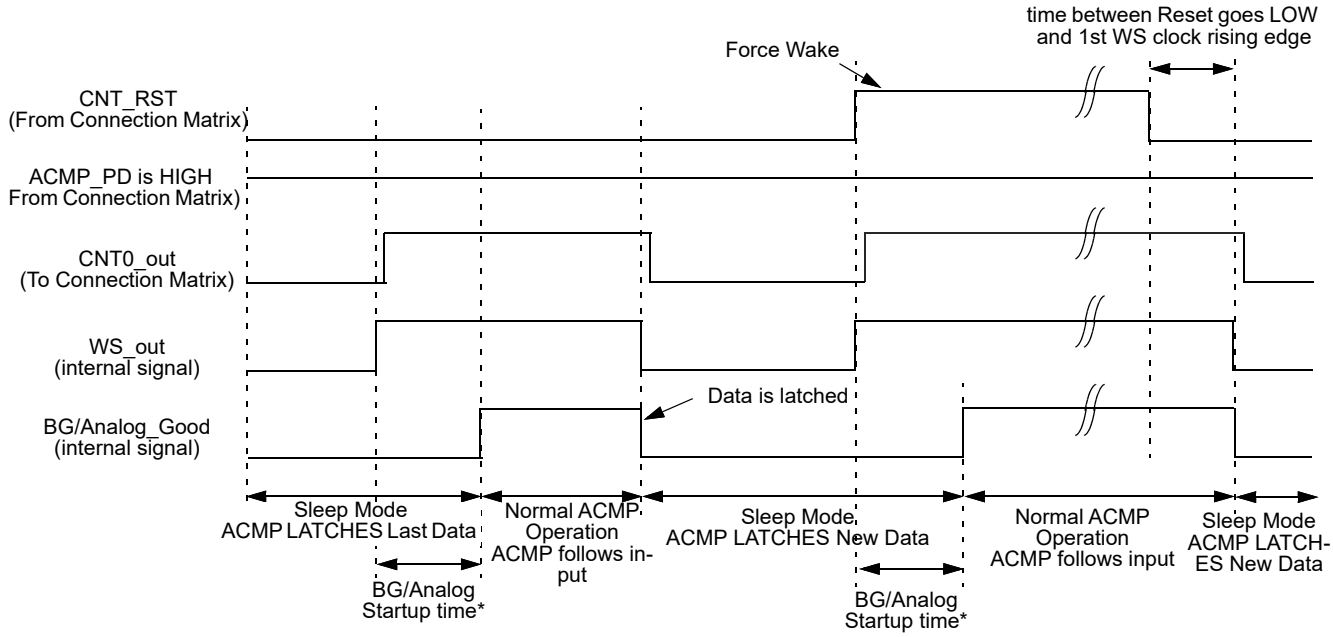
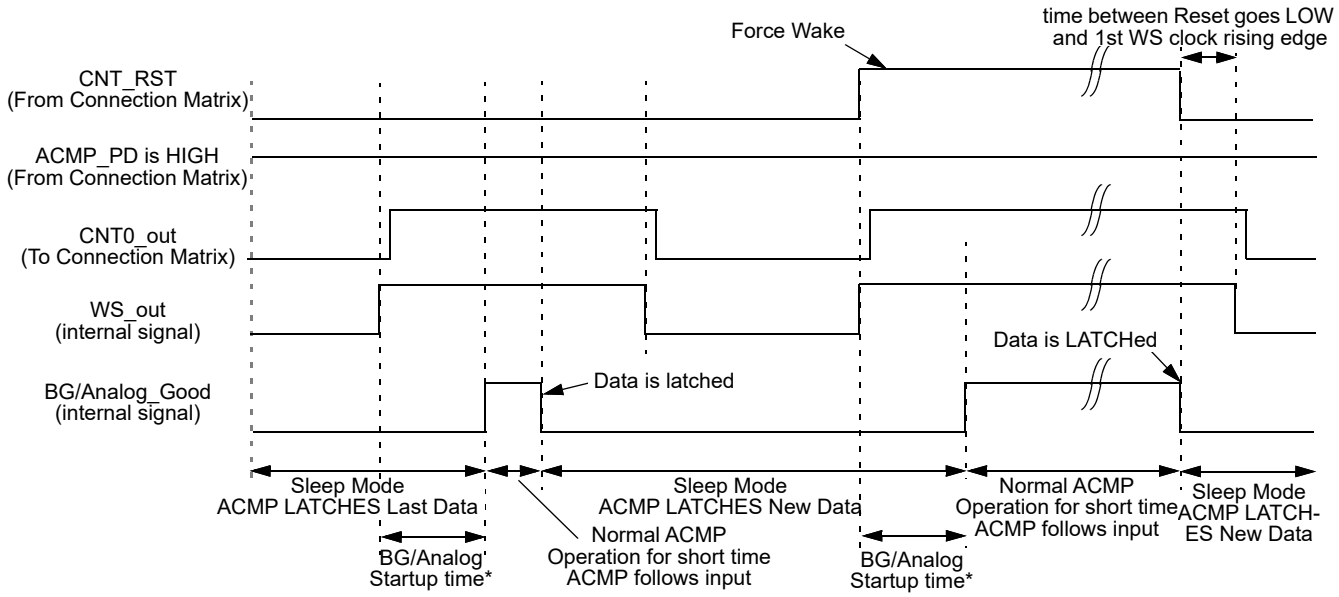


Figure 99. Wake/Sleep Controller



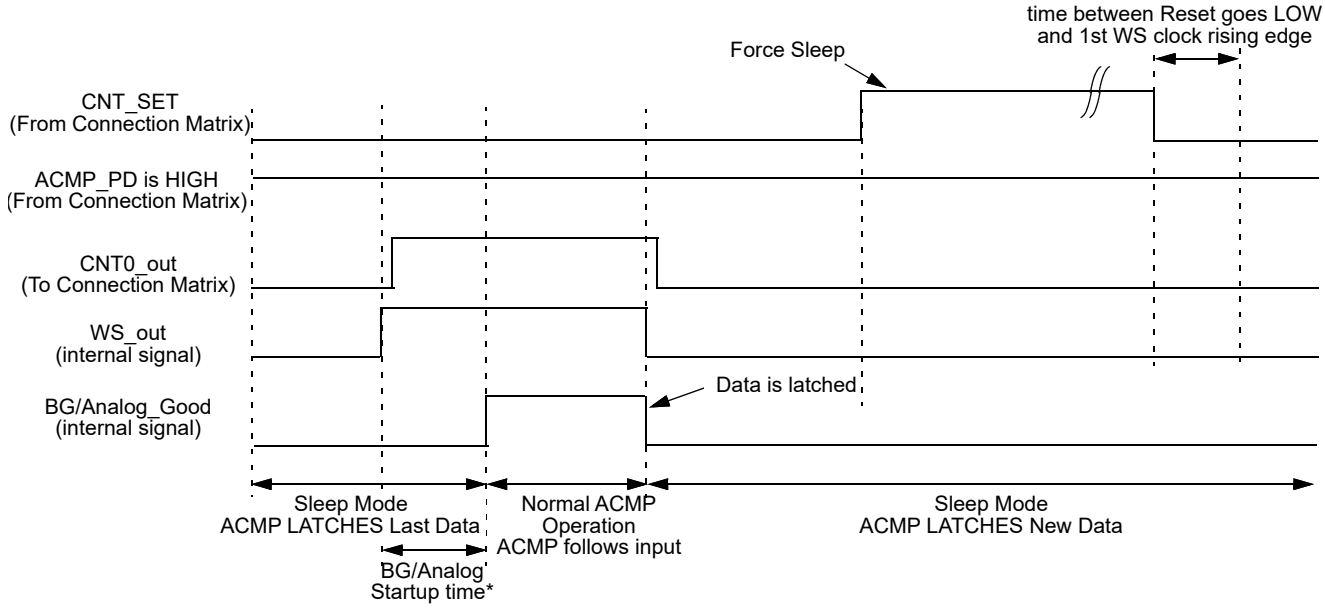
Note: CNT0_out is a delayed WS_out signal for 1us to make sure the data is correct during LATCH.

Figure 100. Wake/Sleep Timing Diagram, Normal Wake Mode, Counter Reset is Used



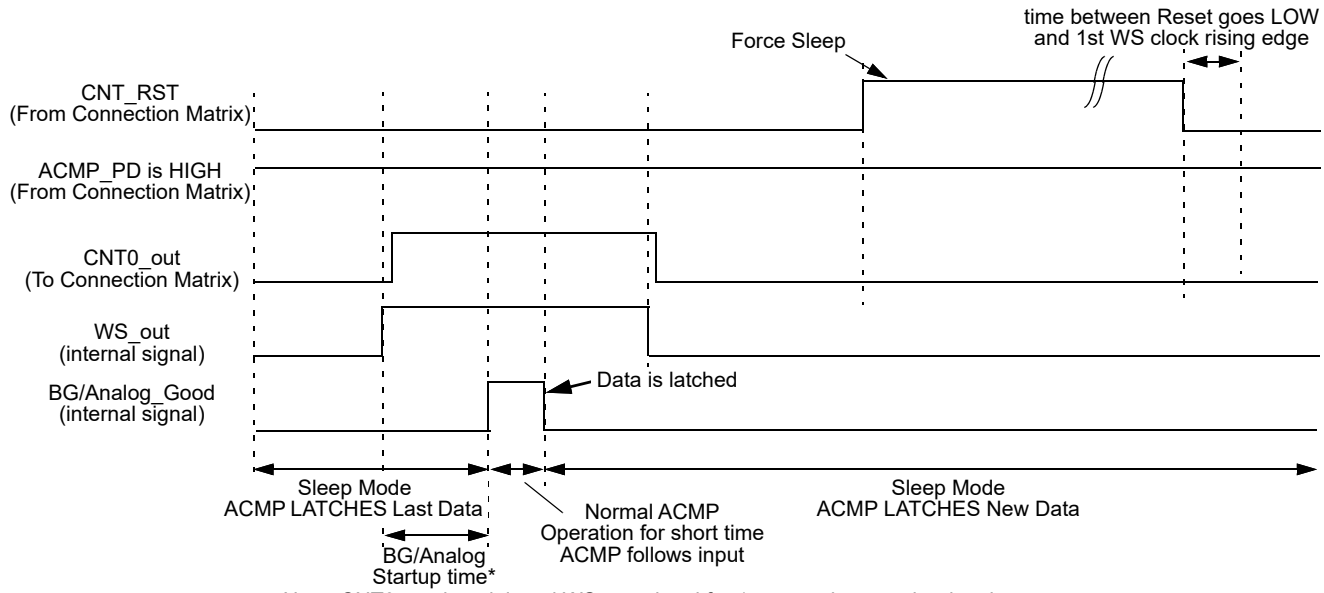
Note: CNT0_out is a delayed WS_out signal for 1us to make sure the data is correct during LATCH.

Figure 101. Wake/Sleep Timing Diagram, Short Wake Mode, Counter Reset is Used



Note: CNT0_out is a delayed WS_out signal for 1us to make sure the data is correct during LATCH.

Figure 102. Wake/Sleep Timing Diagram, Normal Wake Mode, Counter Set is Used



Note: CNT0_out is a delayed WS_out signal for 1us to make sure the data is correct

Figure 103. Wake/Sleep Timing Diagram, Short Wake Mode, Counter Set is Used

Note: If low power BG is powered on/off by WS, the wake time should be longer than 2.1 ms. The BG/analog startup time will take maximal 2 ms. Therefore, 8 periods of the Oscillator0 is recommended for the wake time, when BG is configured to Auto Power mode. If low power BG is always on, Oscillator0 period is longer than required wake time. The short wake mode can be used to reduce the current consumption. The short wake mode is edge triggered when the wake signal is latched by a rising edge and released the power-on signal after the ACMP output data is latched. This allows to have a valid ACMP data for any type of wake signal and have the optimized current consumption.
To use any ACMP under WS controller, the following settings must be done:

- ACMP Power-up Input from matrix = 1 (for each ACMP separately);
- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMP);
- Register WS → enable (for each ACMP separately);
- CNT/DLY0 set/reset input = 0 (for all ACMP).

As the OSC, any oscillator with any pre-divider can be used. The user can select a period of time while the ACMP is sleeping in a range of 1 - 65535 clock cycles. Before they are sent to sleep their outputs are latched, so the ACMPs remain their state (HIGH or LOW) while sleeping.

WS controller has the following settings:

- Wake and Sleep Output State (HIGH/LOW)
  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = HIGH, the ACMP is continuously on.
  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = LOW, the ACMP is continuously off.
  Both cases WS function is turned off.
- Counter Data (Range: 1 - 65535)
  The User can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time.
- Q mode - defines the state of WS counter data when Set/Reset signal appears Reset - when an active signal appears, the WS counter will reset to zero and the High-level signal on its output will turn on the ACMPs. When the Reset signal goes out, the WS counter will go LOW and turn off the ACMP until the counter counts up to the end. Set - when an active signal appears, the WS counter will stop and the Low-level signal on its output will turn off the ACMP. When Set signal goes out, the WS counter will go on counting and the High-level signal will turn on the ACMP while the counter is counting up to the end.

Note: The Oscillator0 matrix Power-down to control ACMP WS is not supported for short wait time option.

- Edge Select defines the edge for Q mode

  High-level Set/Reset - switches mode Set/Reset when level is HIGH

Note: Q mode operates only in case of "High-Level Set/Reset".

- Wake time selection - time required for wake signal to turn the ACMPxH on

  Normal Wake Time - when WS signal is HIGH, it takes BG/analog start up time to turn the ACMPs on. They will stay on until WS signal is LOW again. Wake time is one clock period. It should be longer than BG turn-on time and minimal required comparing the time of the ACMP.

  Short Wake Time - when WS signal is HIGH, it takes BG/analog start up time to turn the ACMPs on. They will stay on for 1 µs and turn off regardless of WS signal. The WS signal width does not matter.
- Keep - pauses counting while Keep = 1
- Up - reverses counting

  If Up = 1, CNT is counting up from user-selected value to 65535.

  If Up = 0, CNT is counting down from user-selected value to 1.

13. Pulse Width Modulation Macrocell

The SLG47115 has two Pulse Width Modulation (PWM) macrocell. Inputs/Outputs for the macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

PWM macrocell features:

- 8-bit (7-bit) PWM Resolution
- I2C /Matrix/Auto dynamically changeable Duty Cycle
- Changeable Period by changing PWM clock source
- Flexible OSC-integrated divider for PWM period selection
- I2C Duty cycle read/write
- Synchronous change of all PWM blocks by sequential I2C write command
- Configurable dead band option for OUT+ and OUT-
- 16 Preset Duty Cycle Registers Switching Mode (for PWM sine or other waveforms)
- Autostop at 0 % and 100 % of PWM duty cycle value
- Synchro OFF Mode (wait for PWM period end before stop block)
- Inv/non-Inv macrocell Output options
- From 0 %, 0.4 % to 99.6 %,100 % Duty cycle for 8-bit resolution.

13.1 8-bit or 7-bit PWM Configurations

When configured as PWM, this macrocell has an 8-bit resolution. It is also possible to select 7-bit PWM resolution if the higher PWM frequency is needed.

The PWM block consists of two 8-bit counters. First one, named PWM Period CNT, is used to create PWM period and the second one, named PWM Duty Cycle CNT, is used to set PWM Duty Cycle and to make dynamic changes in PWM functionality.

There is an ability to change the Duty Cycle from 0 % to 100 %. The PWM duty cycle step is 0.4 % for 8-bit resolution and 0.8 % for 7-bit resolution mode. This step is constant in the whole range. Both 0 % and 100 % are included.

13.2 PWM Inputs

- Duty Cycle CNT Up/Down is the signal for defining the direction of duty cycle change.
  - If Duty Cycle CNT Up/Down = 1, the duty cycle increases from current value up to 255.
  - If Duty Cycle CNT Up/Down = 0, the duty cycle decreases from current value down to 0.
- Duty Cycle CNT Keep/Stop.
  - When Keep function is selected (register [1461] = 0 for PWM0 and register [1479] = 0 for PWM1) HIGH logic level on this input disables the change of Duty Cycle CNT (clock for Duty Cycle CNT is blocked). However, PWM block still generates PWM output with a constant duty cycle.
  - When Stop function is selected (register [1461] = 1 for PWM0 and register [1479] = 1 for PWM1) HIGH logic level on this input disables the change of both Duty Cycle CNT and PWM Period CNT. Consequently, if Stop signal is active (logic HIGH) the output of PWM block remains constant.
    Note that if no other macrocells except PWM block use the internal OSC, the logic HIGH on Stop input disables the work of internal OSC that is used as a clock source for PWM Period CNT. For this case, logic LOW on this input enables OSC again.
- Duty Cycle CNT CLK is the clock signal for incrementing/decrementing duty cycle value. Keep in mind that the actual duty cycle value will be updated during the next PWM period.
- Power-down (PD) is an active high-level signal for updating Duty Cycle to default user-defined value. Keep in mind, that user can change the default Duty Cycle value via I2C. The PD signal will apply right away when Sync Off (register [1301] = 1 for PWM0 and register [1475] = 1 for PWM1) and after PWM period is completed when Sync On (register [1301] = 0 for PWM0 and register [1475] = 0 for PWM1[Note]). HIGH logic level on PD input disables the change of all PWM internal counters and stops the internal oscillator (if internal OSC isn't used by other macrocells) (see Section 13.10 Sync On/Off Setting for Power-Down Signal). This function is individual for each PWM block.

Note that for async mode a minimal time duration for High-level at PD input is 100 ns, which guarantee PWM response. A pulse shorter than 100 ns might be ignored. An input pulse will be extended internally to this minimal required time to power down the PWM block.

- Ext PWM Period CNT CLK is clock input for PWM Period CNT. The clock at this input defines PWM signal frequency. PWM Period CNT CLK comes from the internal predefined clock or from the matrix for the high flexibility of PWM frequency.

Note: First PWM period will be 2-3 clocks longer after PD signal is released.

13.3 PWM Outputs

- OUT+: PWM positive output
- OUT- : PWM negative output
- PWM_PERIOD: PWM start period pulse (the duration of the high-level is equal to one period of the PERIOD CNT CLK)

13.4 I²C/Matrix/Auto Dynamically Changeable Duty Cycle and Period

Duty Cycle in PWM macrocell can be changed in two ways:

1. PWM Duty Cycle CNT block has two parameters: Counter Data and Current Counter Value. The Current Counter Value defines PWM Duty Cycle. Counter Data of PWM Duty Cycle CNT can be changed by I²C commands with a reload into Current Counter Value. In this case I²C Master can change PWM Duty Cycle by I²C. Therefore, Counter Data of PWM Duty Cycle CNT must support change via I²C.

2. Matrix changeable Duty Cycle. In this case "Duty Cycle CNT CLK" and "Duty Cycle CNT Up/Down" inputs are used. Rising edge at "Duty Cycle CNT CLK" changes Current Counter Value corresponding to "Duty Cycle CNT Up/Down" input state: if "Duty Cycle CNT Up/Down" is LOW then Current Counter Value decreases and vice versa.

PWM period (frequency) can be changed only by changing PWM Period CNT Clock source. There are several different clock options available for user selection. Therefore, for PWM frequency flexibility an OSC-integrated CNT divider can be used.

13.5 I²C PWM Duty Cycle Read/Write

The master I²C should be able to reliably read and write duty cycle value into PWM block. Synchro Buffer is used for correct I²C reading of actual PWM duty cycle. The I²C command has some time duration. Synchro Buffer captures actual PWM duty cycle for read command and I²C Master can read this data without errors.[Note]

The I²C Master can change PWM duty cycle via I²C write command. The newly written PWM duty cycle value will be loaded (but not applied) to the PWM block as the default value. The load will happen when I²C "stop" command is issued. To apply a default value to PWM block user must set the "I²C trigger" bit to 1 via I²C interface. Note, that this value will be applied after the current PWM period.

If the user wants to change both PWM blocks simultaneously, I²C sequential write command must be used.

Note: Avoid the change of PD signal during I²C read, since it causes the buffer value to update.

13.6 Flexible OSC-Integrated Divider

The OSC-integrated divider is built into 25 MHz OSC to configure the PWM period. This divider can be used for other chip resources. There is 8-bit Counter with the source from OSC pre-divider and output to the matrix or directly to CNT/DLY block as one possible selection. In many cases, for all PWM macrocells, the same clock frequency is used. It is possible to use this Flexible OSC divider for fine frequency tuning of PWM cells.

The counter in flexible divider can be enabled/disabled by the register bit [741] only. When the counter in flexible divider is enabled it will start to count down from the counter data till 0. That is why the frequency division is counter data + 1. Minimum frequency after Flexible OSC-integrated Divider is at least twice smaller than input

Flexible OSC-integrated Divider frequency. Counter won‘t count with 0b00000000 counter data. There is a separate register bit selection to enable the flexible divider output to the connection matrix.

13.7 Inverted Output Option

By default, PWM output begins from HIGH logic level and after reaching duty cycle value, output changes to LOW logic level. Optionally the user can invert outputs of PWM block.

Each PWM macrocell outputs has an inverter option enabled by registers. It is necessary for simple driving of different LED types (common Anode, common Cathode), and others. Each OUT+ and OUT- outputs has one separate register to select its inverted/non-inverted output option.

13.8 Changeable Dead Band Option for OUT+ and OUT-

Dead band parameter is needed to drive external power FETs. The dead band helps to avoid short through for high power FETs. Dead band parameter is configurable for driving different external transistor. It is possible to select no dead band time or dead band equal to one, two or three PWM Period clock cycles.

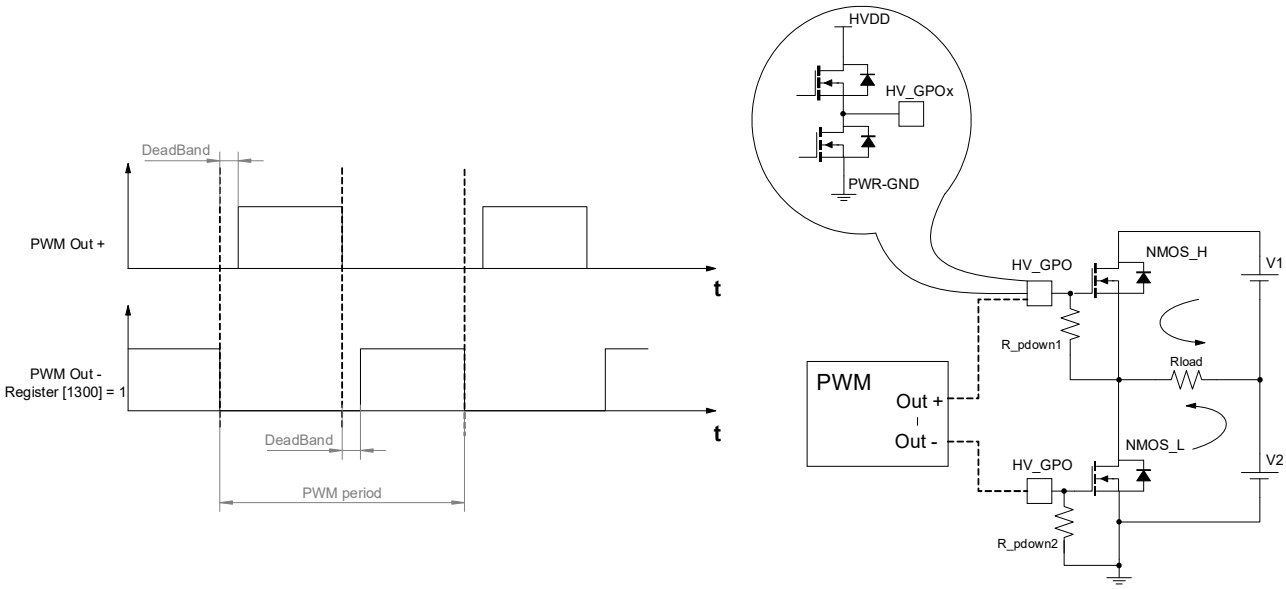


Figure 104. PWM Output Waveforms and Test Circuit Example for Driving NMOS FETs

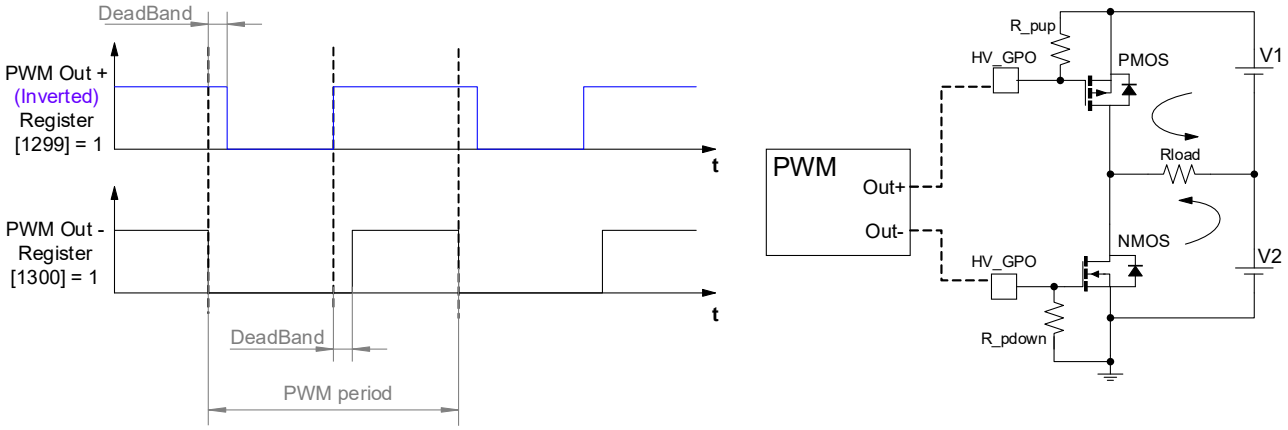


Figure 105. PWM Output Waveforms and Test Circuit Example for Driving NMOS and PMOS FETs

Note that external FETs must have Pull-up/Pull-down resistors between Gate and Source terminals to avoid unpredictable behavior of FETs when output pins of SLG47115 are in Hi-Z state (Sleep Mode).

The waveforms for Phase Correct PWM Mode are shown in Figure 106. Note that in Phase Correct PWM mode dead band delay is applied after phase correction, Figure 112.

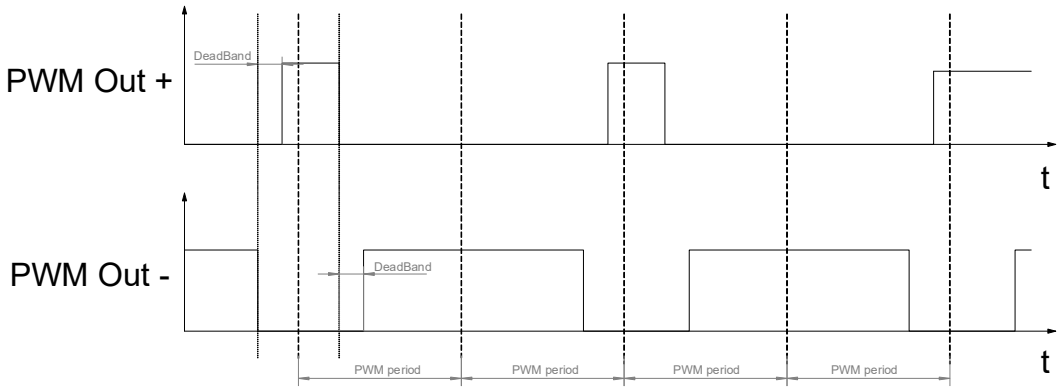


Figure 106. PWM Output Waveforms for Phase Correct PWM Mode

13.9 Initial PWM Value

Initial PWM duty cycle value is selected by Counter Data of PWM Duty Cycle CNT for regular mode. If Preset Registers Mode is selected, the initial value of PWM Duty Cycle CNT (Counter Data) is the preset registers address. Please refer to Section 13.11 Regular/Preset Registers Mode.

13.10 Sync On/Off Setting for Power-Down Signal

"SYNC On/Off" registers define the behavior of power-down signal. This is the individual setting for each PWM macrocell. If this option is disabled (register [1301] for PWM0 = 1 and register [1475] = 1 for PWM0), the PWM output goes LOW right away by active Power-down, Figure 107. If this option is enabled (register [1301] for PWM0 = 0 and register [1475] = 0 for PWM0), the PWM block will finish the current PWM period and then will go LOW, Figure 110.

SYNC On/Off has no effect on duty cycle change via I^2C. In the case of duty cycle change via I^2C interface, new duty cycle value will be applied to PWM macrocell only after finishing the current PWM period.

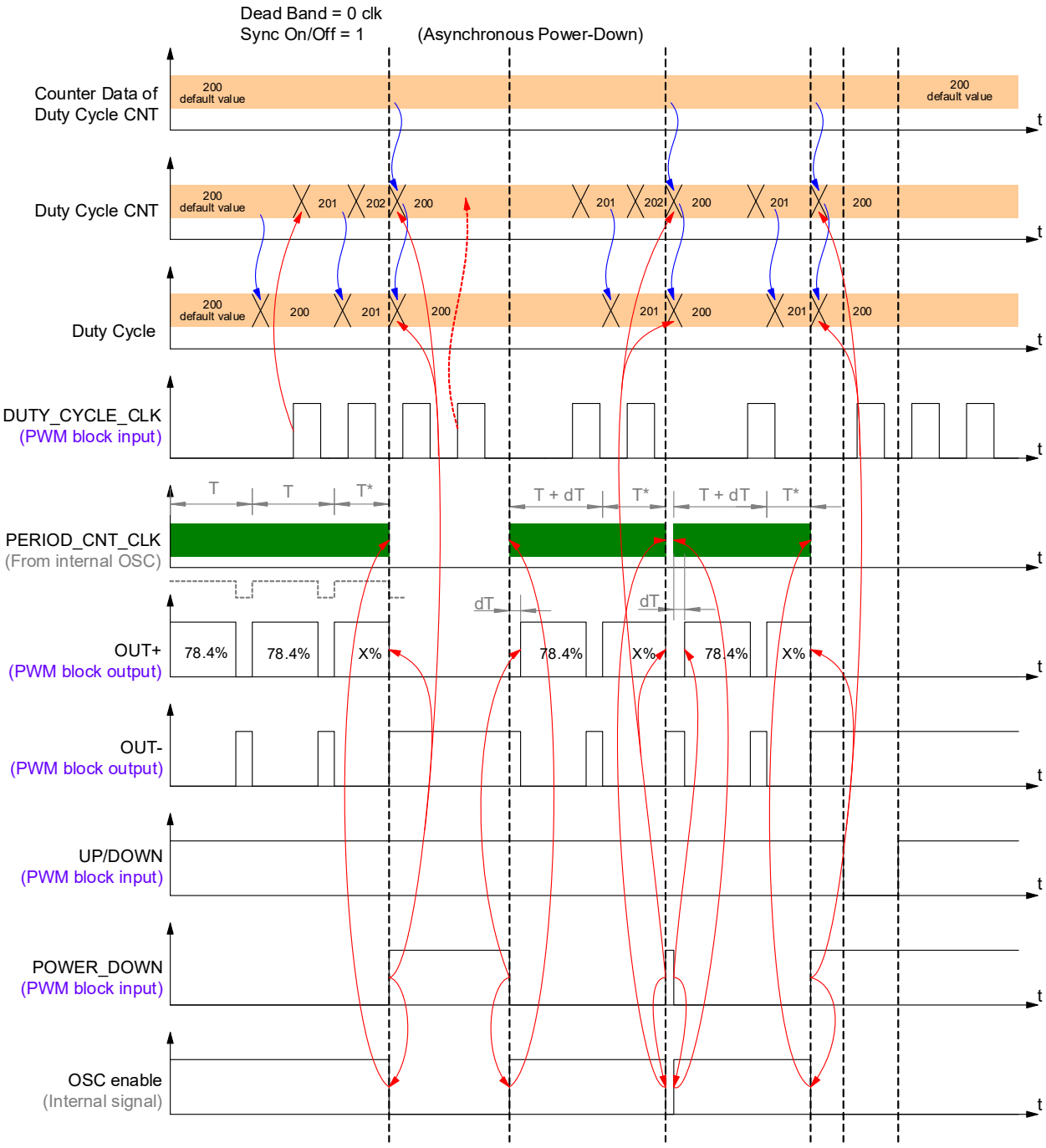


Figure 107. Power-Down with SYNC On/Off = 1 and Dead Band = 0 CLK

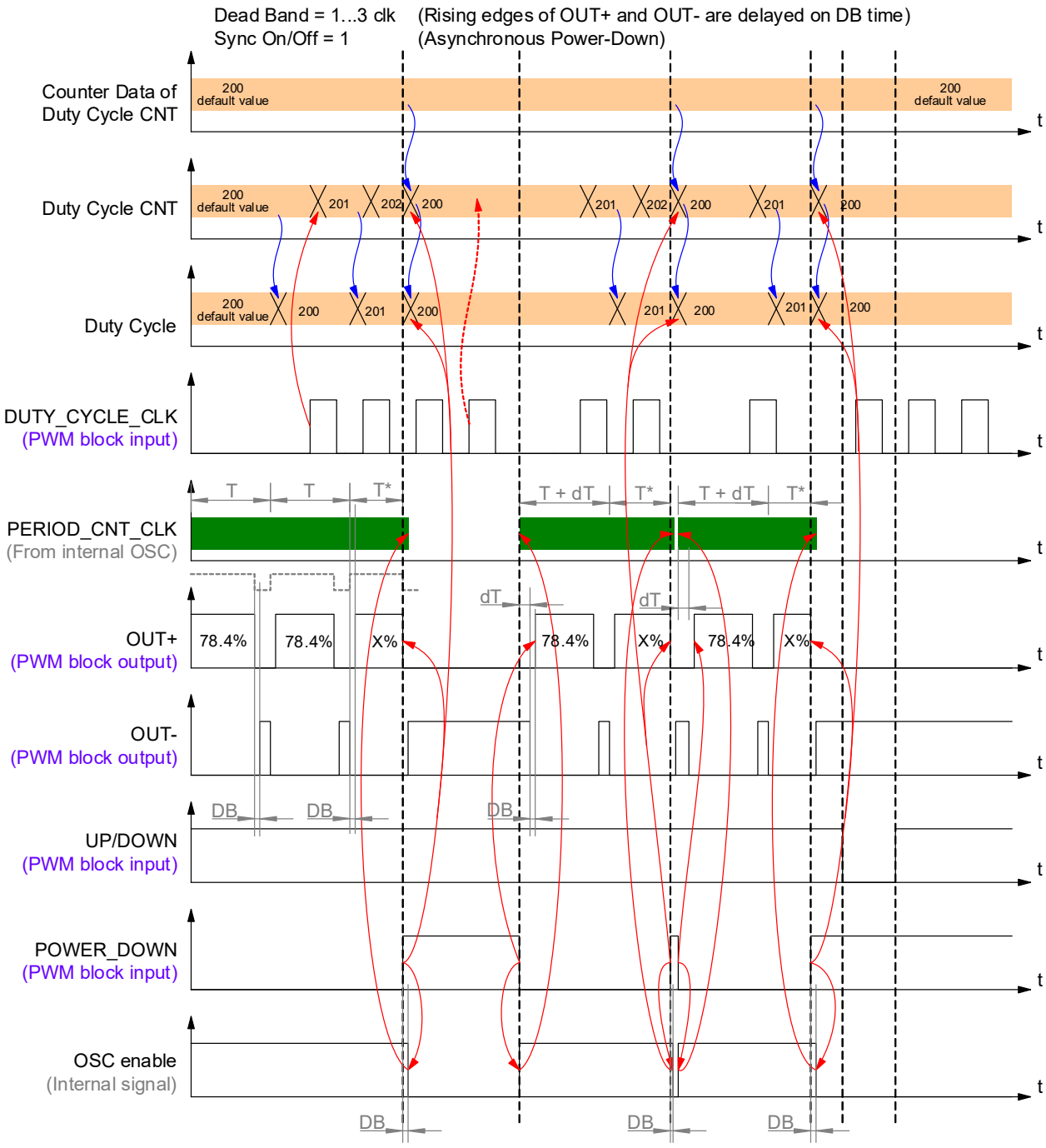


Figure 108. Power-Down with SYNC On/Off = 1 and Dead Band = 1 to 3 CLK

In Figure 107 to Figure 110:

- dT = 2-3 CLK and it is the additional number of clock pulses, that make first PWM period longer, after releasing PD signal;
- DB - user selected Dead Band time between OUT+ and OUT-;
- T* means the short period of x % duty cycle (T* < 255 PERIOD_CNT_CLK), that is finished at the moment of PD signal coming.

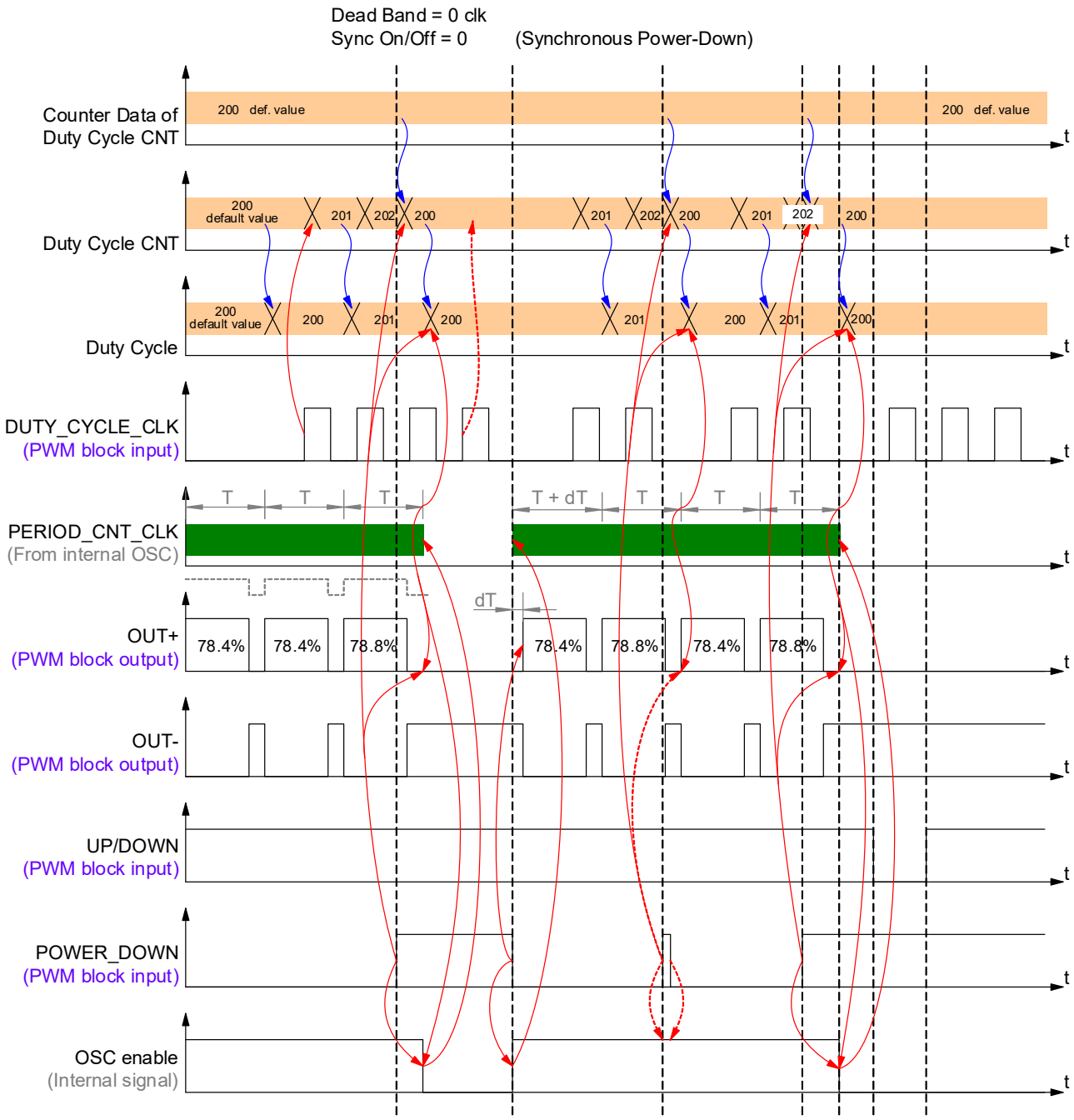


Figure 109. Power-Down with SYNC On/Off = 0 and Dead Band = 0 CLK

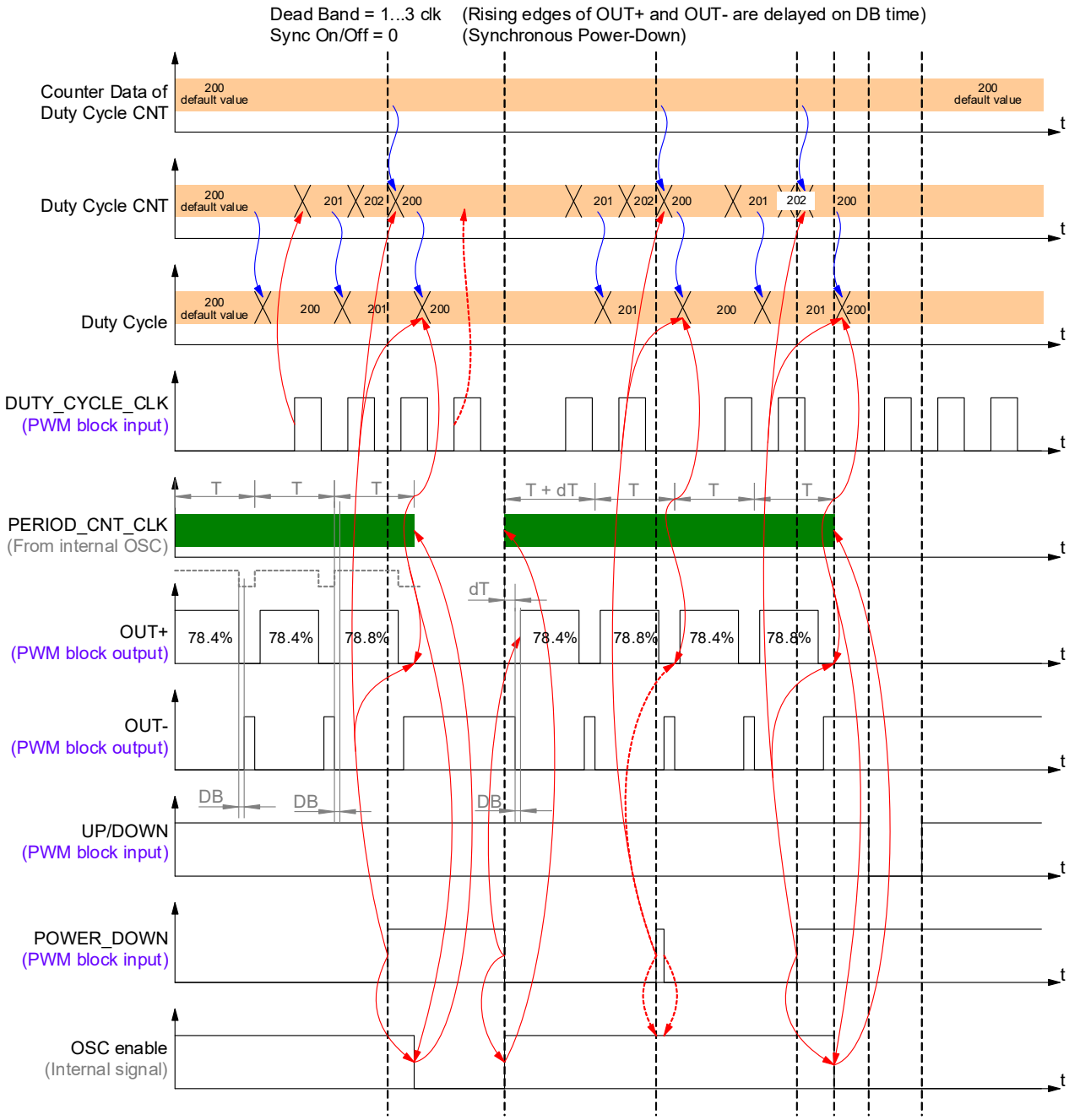


Figure 110. Power-Down with SYNC On/Off = 0 and Dead Band = 1 to 3 CLK

13.11 Regular/Preset Registers Mode

In Regular mode the value of duty cycle is changed every rising edge on Duty Cycle CNT CLK input. In Preset Registers mode the duty cycle is changed according to 16 predefined values, named Reg File, every rising edge on Duty Cycle CNT CLK input.

Selectable Preset registers are reserved to determine 16 different PWM Duty Cycle values. In Preset Registers mode the "Up/Down" input and "Duty Cycle CNT CLK input" change the address of Preset Register, that will be applied to PWM block at the rising edge on "Duty Cycle CNT CLK input".

One 16-byte Preset Register is shared between two PWM macrocells.

Each PWM block can select Reg File as Duty Cycle source. When the Reg file is selected as a source, there are three options: use all 16 bytes, use less significant 8 bytes or use most significant 8 bytes. In this case, 4-bits (when using 16-Bytes Reg File) or 3-bits (when using any of 8 bytes Reg File) LSB Current Value of PWM Duty Cycle CNT is used to select data address inside the Reg File. The counter data of the Duty Cycle CNT will define the initial starting point in the Reg file. So, each PWM block has its own initial position in the Reg File.

Table 64. Regular/Preset Mode Registers

Register name	Mode of operation	Register definition
PWMx: Duty Cycle source	Regular mode	00: from PWM Duty Cycle CNT
	Preset Registers mode	01: 8-byte MSB of RegFile
		10: 8-byte LSB of RegFile
		11: 16-byte RegFile

For more detailed description see Table 66 and Table 67.

13.12 PWM Continuous/Autostop Mode

“Continuous/Autostop Mode” register enables Autostop Mode. This mode can be used with both Preset Registers or Regular Mode.

If PWM block works in Continuous mode (register [1302] = 0 for PWM0 or register [1476] = 0 for PWM1), PWM Duty Cycle CNT will overflow when it reaches boundaries. For example, for PWM Duty Cycle Counter counts up: $254^{th} \rightarrow 255^{th} \rightarrow 0^{th} \rightarrow 1^{st}$, and for PWM Duty Cycle Counter counts down: $1^{st} \rightarrow 0^{th} \rightarrow 255^{th} \rightarrow 254^{th}$ …

Or in Preset Registers Mode, when Continuous Mode is selected (register [1302] = 0 for PWM0 or register [1476] = 0 for PWM1): counting up $14^{th} \rightarrow 15^{th} \rightarrow 0^{th} \rightarrow 1^{st}$, and counting down $1^{st} \rightarrow 0^{th} \rightarrow 15^{th} \rightarrow 14^{th}$ …

If Autostop Mode is active (register [1302] = 1 for PWM0 or register [1476] = 1 for PWM1), PWM duty cycle counter will stop when it reaches boundaries. The conditions of Autostop are the next:

- PWM Duty Cycle reaches the value 0 in Regular mode or Least Significant Byte of Preset registers in Preset Registers Mode, and Up/Down is LOW logic level (counting Down).
- PWM Duty Cycle reaches the value 255 (127 in 7-bit mode) or Most Significant Byte of Preset registers in Preset Registers Mode and Up/Down is HIGH logic level (counting Up).

13.13 Internal Oscillator Auto Disable Mode

There is an OSC Auto Disable/Enable control, in which internal OSC is enabled only when it is required for PWM block. This Auto Disable mode will operate only if user selects internal oscillator as a clock source for PWM Period Clock Counter ("PWM0 Period Clock Source selection" registers have a value from b0000 to b1001).

If the user selected PWM Period CNT overflow event as a clock source for Duty Cycle Counter (registers [1469:1468] = 01, or registers [1469:1468] = 10, or registers [1469:1468] = 11 for PWM0 and registers [1485:1484] = 01, or registers [1485:1484] = 10, or registers [1485:1484] = 11 for PWM1), then no clocks will be on Duty Cycle Counter clock input when PWM enters to Autostop State (see Table 65).

The conditions, in which internal OSC will be automatically disabled, are shown in Table 65.

Table 65. Conditions for Disabling/Enabling an Internal Oscillator

N0	Disable condition	Delay before OSC in disabled	Enable condition
1	PD signal goes HIGH	Disable OSC immediately if SYNC On/Off register [1301] = 1 for PWM0 and register [1475] = 1 for PWM1	PD signal goes LOW
		Disable OSC after current duty cycle period if SYNC On/Off register [1301] = 0 for PWM0 and register [1475] = 0 for PWM1	
2	Stop signal goes HIGH	Disable OSC immediately	Stop signal goes LOW
3	Up/Down is logic HIGH (counting up) and actual PWM value is 255 (127 for 7-bit submode), "PWM boundary OSC automatically disable" (register [1303] = 1 for PWM0 or register [1477] = 1 for PWM1) "Continuous/Autostop mode"(register [1302] = 1 for PWM0 or register [1476] = 1 for PWM1) Figure 111	Disable OSC after one full PWM period.	Up/Down signal changes its level to logic LOW (count down) Figure 111
4	Up/Down is logic LOW (counting down) and actual PWM value is 0, "PWM boundary OSC automatically disable"(register [1303] = 1 for PWM0 or register [1477] = 1 for PWM1) and "Continuous/Autostop mode"(register [1302] = 1 for PWM0 or register [1476] = 1 for PWM1)	Disable OSC after one full PWM period.	Up/Down signal changes its level to logic HIGH (count up)

Note 1: If PWM boundary OSC automatically disable register [1303] = 1 for PWM0 or register [1477] = 1 for PWM1 and PWM works with Preset Registers (registers [1467:1466] = 01 or registers [1467:1466] = 10, or registers [1467:1466] = 11 for PWM0 and registers [1483:1482] = 01 or registers [1483:1482] = 10, or registers [1483:1482] = 11 for PWM1), internal OSC will stop if Preset Registers Index = 15 (7 when LSByte mode of Preset Registers is used) the Preset Register Index remains unchanged until Up/Down signal changes. The same behavior has zero Preset Register Index (8 when MSByte mode of Preset Registers is used). When this index will be reached and OSC Auto Disable mode is active the Preset Register Index remains unchanged until Up/Down signal changes.
Note 2: Other macrocells that use OSC, can start it or keep it enabled even if OSC Auto Disable mode is active and condition for disabling OSC occurs.
Note 3: If dead band is different from 0, then OSC will be disabled for Dead Band Time later.

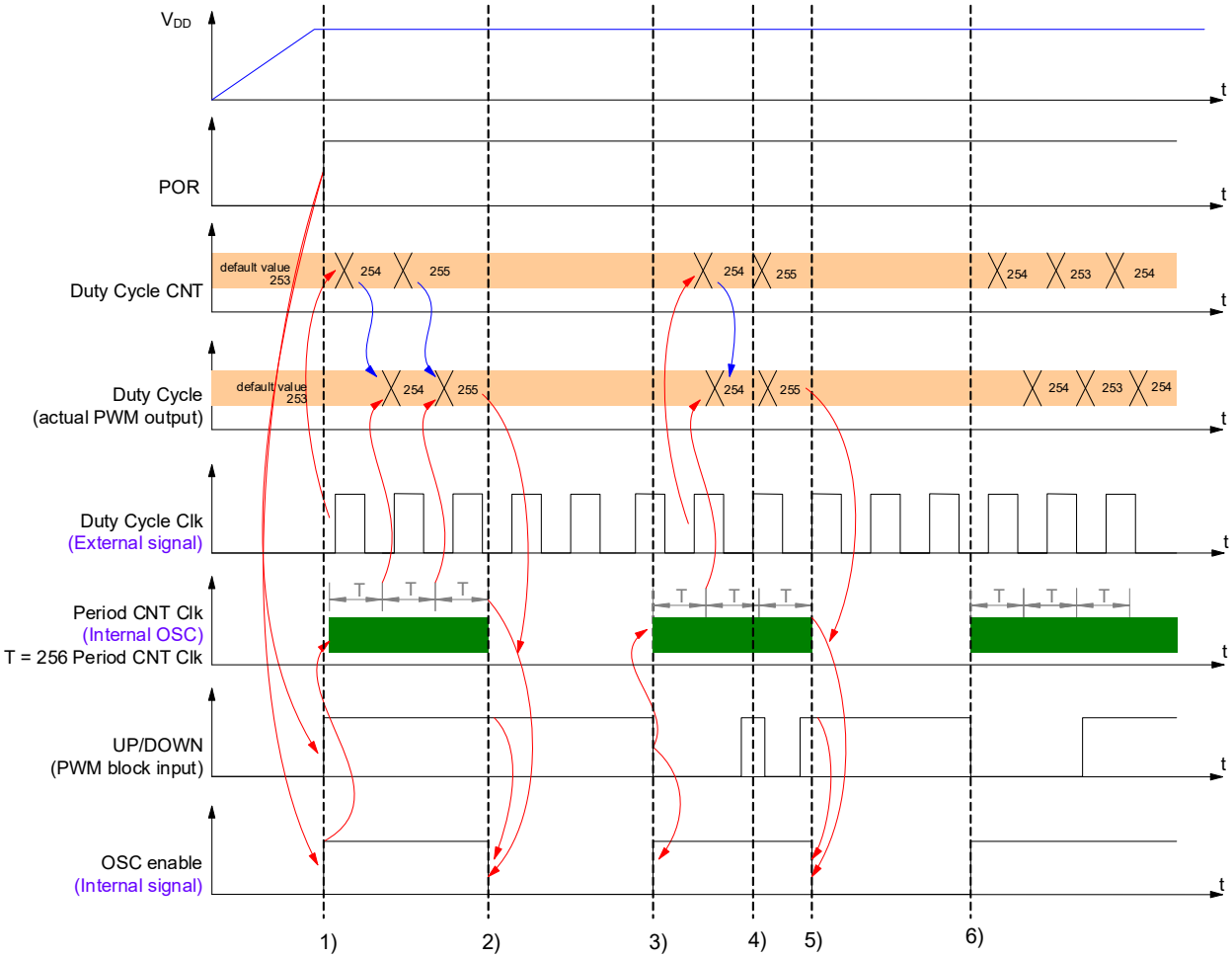


Figure 111. Example of PWM Auto Oscillator Control

In the example in Figure 111, Duty Cycle CLK is external to PWM block signal, Period CNT CLK is a signal from internal OSC. "PWM boundary OSC automatically disable" register [1303] = 1 for PWM0 or register [1477] = 1 for PWM1. Autostop mode is active too ("Continuous/Autostop mode" register [1302] = 1 for PWM0 or register [1476] = 1 for PWM1). The key events of Autostop are the next:

- Event 1) after chip start-up, OSC is enabled. The clock from internal OSC is used to generate PWM period. Duty Cycle CNT counts up since Up/Down input of PWM macrocell is logic HIGH. Note that first OSC pulse is delayed when OSC becomes enabled (see Table 23).
- Event 2) the value of Duty Cycle CNT is updated every rising edge at Duty Cycle CLK input. This value becomes valid at the beginning of every PWM period.
- When the Duty Cycle value of 100 % is reached and Up/Down input is logic HIGH, PWM macrocell disables internal OSC after one full PWM period.
- Event 3) internal OSC starts working because Up/Down signal becomes LOW and Duty Cycle = 100 %. This is the scenario for starting OSC after it was automatically disabled.
- Event 4) the Up/Down signal changes the direction of Duty Cycle counting because at the moment of signals rising edge on Duty Cycle CLK input, the level of Up/Down input is logic HIGH.
- Event 5) OSC is disabled because the value of Duty Cycle is 100 % and at the beginning of the next PWM period the Up/Down input is logic HIGH.
- Event 6) Since Up/Down goes LOW and Duty Cycle is equal to 100 %, this is the scenario for starting up the OSC.

13.14 Phase Correct PWM Mode

In normal mode, PWM output is HIGH, then LOW for each PWM period. When Phase correct PWM (also called Center Align) register is active (register [1460] = 1 for PWM0 or register [1478] = 1 for PWM1), the PWM output is HIGH, then LOW for the first period, then LOW again and HIGH for the second period. So, there are less edges (or less output switches) for the Phase correct PWM mode.

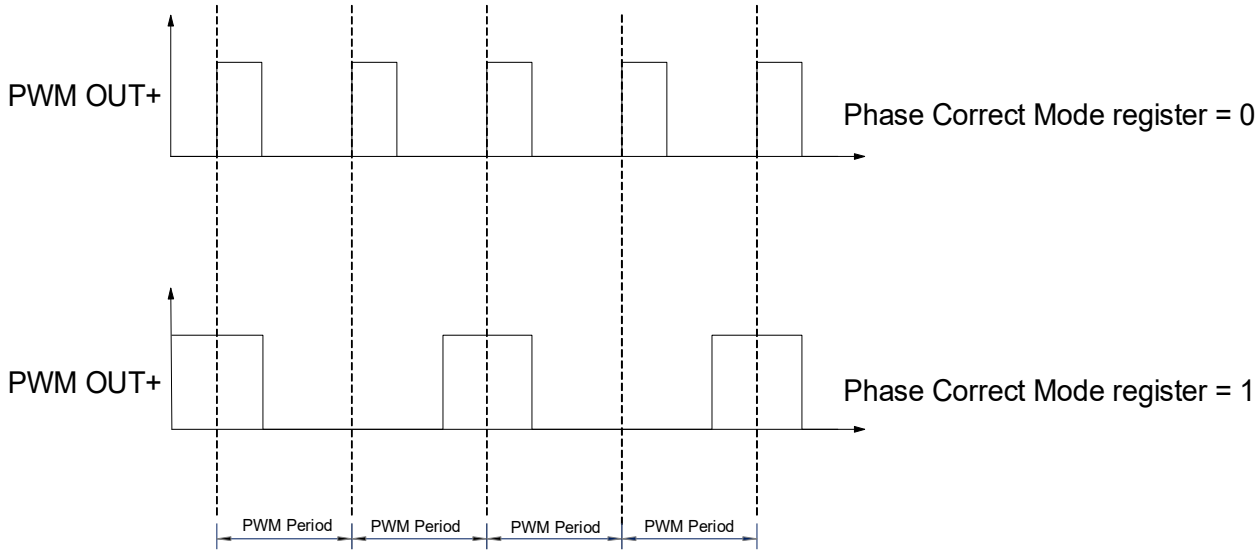


Figure 112. Phase Correct PWM Mode

13.15 PWM Period Output

PWM_PERIOD output indicates the start of the new PWM period at PWM_OUT+. This output doesn't depend on the PWM duty cycle. The duration of the high-level is equal to one period of the PERIOD_CNT_CLK.

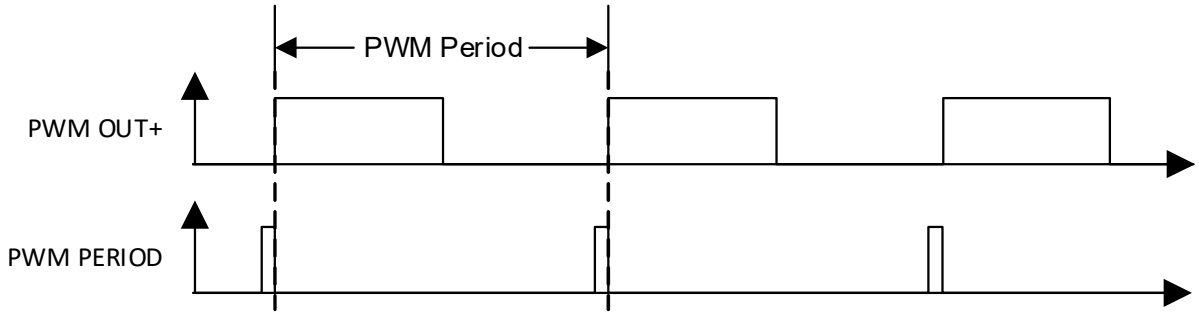


Figure 113. PWM Period Waveform

13.16 PWM Block Diagrams

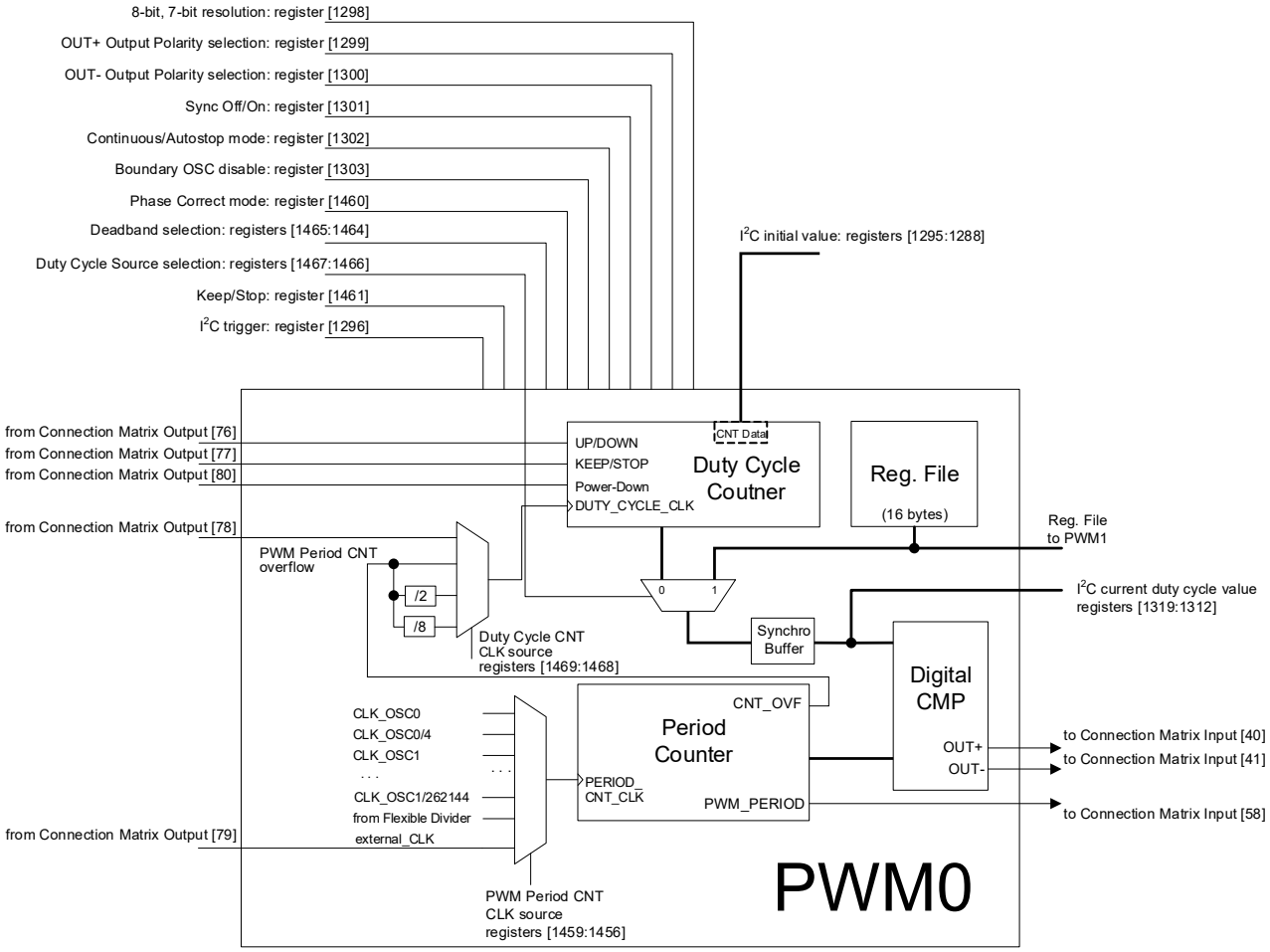


Figure 114. PWM0 Functional Diagram

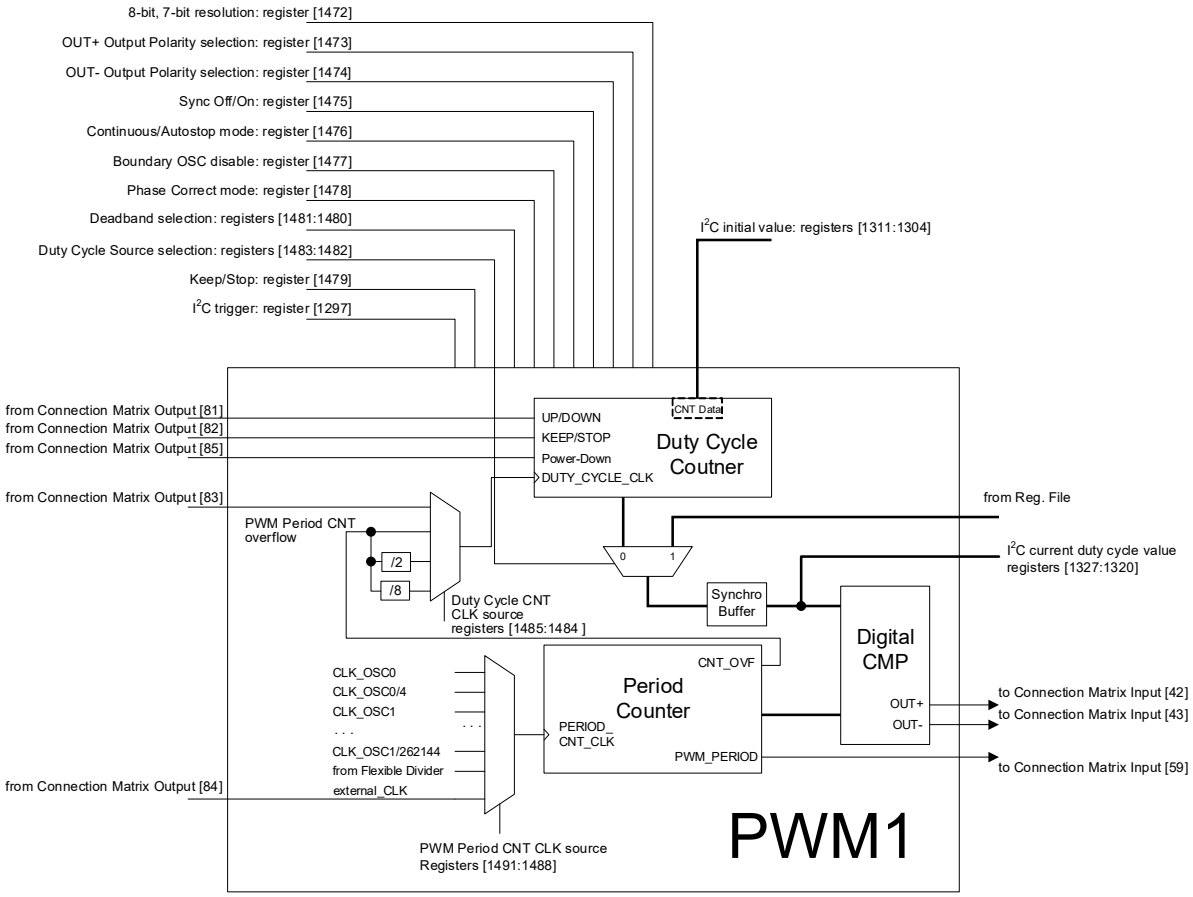


Figure 115. PWM1 Functional Diagram

13.17 PWM Register Settings

Table 66. PWM0 Register Settings

Signal function	Register Bit address	Register definition
PWM0: 8-bit or 7-bit resolution	1 bit [1298] register	0: 8-bit PWM0 1: 7-bit PWM0
PWM0: OUT+ polarity selection	1 bit [1299] register	0: Non-Inverted Output 1: Inverted Output
PWM0: OUT- polarity selection	1 bit [1300] register	0: Non-Inverted Output 1: Inverted Output
PWM0: SYNC On/Off	1 bit [1301] register	0: Synchronous Power-Down 1: Asynchronous Power-Down
PWM0: Continuous/Autostop mode	1 bit [1302] register	0: Continuous mode 1: PWM Duty Cycle Counter Autostop at 0 % or 100 %
PWM0: Boundary OSC disable	1 bit [1303] register	0: OSC is always enabled at boundaries 1: Automatically Disable OSC
PWM0: Phase Correct mode	1 bit [1460] register	0: Disable 1: Enable
PWM0: Deadband selection	2 bits [1465:1464] registers	00: No Deadband 01: 1 PWM0 clock cycles 10: 2 PWM0 clock cycles 11: 3 PWM0 clock cycles
PWM0: Keep/Stop selection	1 bit [1461] register	0: Keep 1: Stop
PWM0: I^2C trigger	1 bit [1296] register	0: Don't update duty cycle value 1: Update duty cycle value
PWM0: Duty Cycle source	2 bits [1467:1466] registers	00: from PWM Duty Cycle CNT (Regular mode) 01: 8-byte MSB of RegFile (Preset Registers mode) 10: 8-byte LSB of RegFile (Preset Registers mode) 11: 16-byte RegFile (Preset Registers mode)
PWM0 Period Counter Clock Source selection	4 bits [1459:1456] registers	0000: CLK_OSC0 0001: CLK_OSC0/4 0010: CLK_OSC1 0011: CLK_OSC1/8 0100: CLK_OSC1/64 0101: CLK_OSC1/512 0110: CLK_OSC1/4096 0111: CLK_OSC1/32768 1000: CLK_OSC1/262144 1001: From Flexible Divider 1010: Reserved 1011: Matrix OUT [79] (external clock)
PWM0: Duty Cycle Counter Clock Source selection	2 bits [1469:1468] registers	00: Matrix output 01: PWM Period CNT overflow 10: every 2nd pulse of PWM Period CNT overflow 11: every 8th pulse of PWM Period CNT overflow
PWM0: Preset 16-byte Registers byte [0...15]	16 bytes [1455:1328] registers	Preset 16 bytes Duty Cycle values

Table 66. PWM0 Register Settings (Cont.)

Signal function	Register Bit address	Register definition
PWM0: Initial value	8 bits [1295:1288] registers	Initial PWM0 Duty Cycle value
PWM0: Current duty cycle value	8 bits [1319:1312] registers	Current PWM0 duty cycle value for I^2C read

Table 67. PWM1 Register Settings

Signal Function	Register Bit Address	Register Definition
PWM1: Initial value	8 bits [1311:1304] registers	Initial PWM1 Duty Cycle value
PWM1: Current duty cycle value	8 bits [1327:1320] registers	Current PWM1 duty cycle value for I^2C read
PWM1: 8-bit or 7-bit resolution	1 bit [1472] register	0: 8-bit PWM1 1: 7-bit PWM1
PWM1: OUT+ output polarity selection	1 bit [1473] register	0: Non-Inverted Output 1: Inverted Output
PWM1: OUT- polarity selection	1 bit [1474] register	0: Non-Inverted Output 1: Inverted Output
PWM1: SYNC On/Off	1 bit [1475] register	0: Synchronous Power-Down 1: Asynchronous Power-Down
PWM1: Continuous/Autostop mode	1 bit [1476] register	0: Continuous mode 1: PWM Duty Cycle Counter Autostop at 0 % or 100 %
PWM1: Boundary OSC disable	1 bit [1477] register	0: OSC is always enabled at boundaries 1: Automatically Disable OSC
PWM1: Phase Correct mode	1 bit [1478] register	0: Disable 1: Enable
PWM1: Deadband selection	2 bits [1481:1480] registers	00: No Deadband 01: 1 PWM1 clock cycles 10: 2 PWM1 clock cycles 11: 3 PWM1 clock cycles
PWM1: Keep/Stop Selection	1 bit [1479] register	0: Keep 1: Stop
PWM1: I^2C trigger	1 bit [1297] register	0: Don't update duty cycle value 1: Update duty cycle value
PWM1: Duty Cycle source	2 bits [1483:1482] registers	00: from PWM Duty Cycle CNT (Regular mode) 01: 8-byte MSB of RegFile (Preset Registers mode) 10: 8-byte LSB of RegFile (Preset Registers mode) 11: 16-byte RegFile (Preset Registers mode)

Table 67. PWM1 Register Settings (Cont.)

Signal Function	Register Bit Address	Register Definition
PWM1 Period Counter Clock Source selection	4 bits [1491:1488] registers	0000: CLK_OSC0 0001: CLK_OSC0/4 0010: CLK_OSC1 0011: CLK_OSC1/8 0100: CLK_OSC1/64 0101: CLK_OSC1/512 0110: CLK_OSC1/4096 0111: CLK_OSC1/32768 1000: CLK_OSC1/262144 1001: From Flexible Divider 1010: Reserved 1011: Matrix OUT [84] (external clock)
PWM1: Duty Cycle Counter Clock Source selection	2 bits [1485:1484] registers	00: Matrix output 01: PWM Period CNT overflow 10: every 2nd pulse of PWM Period CNT overflow 11: every 8th pulse of PWM Period CNT overflow

"Keep/Stop" register defines which function will be performed by "Duty Cycle CNT Keep/Stop" input. Keep/Stop signal is active High-level.

"PWM Period Clock Source selection" registers define clock source for "PWM Period CNT CLK" input: from the matrix, from OSCx and OSCx dividers, from the flexible OSC-integrated divider. Also, there is an option to select counter overflow condition as a source for PWM Period Clock.

"PWM: Duty Cycle Source selection" defines the clock source for changing the duty cycle. It can be:

- clock source from the connection matrix;
- clock pulse that is generated after the end of PWM cycle period (PWM Period Counter overflow). This pulse is generated every 255 (for 8-bit option) or 127 (for 7-bit option) PWM Period Clocks;
- clock pulse that is generated once per 2 PWM period, or every 510 (for 8-bit option) or 254 (for 7-bit option) PWM Period Clocks;
- clock pulse that is generated once per 8 PWM period, or every 2040 (for 8-bit option) or 1016 (for 7-bit option) PWM Period Clocks.

"I²C trigger" register allows to update duty cycle value via I²C command:

- When I²C_trigger = 0, PWM duty cycle isn't updated;
- When I²C_trigger = 1, PWM duty cycle is updated from register at I²C stop pulse after the current PWM period is completed.

The I²C_trigger bit will be automatically cleared after the I²C stop pulse.

"SYNC On/Off" registers define the Power-down signal behavior on PWM block. This is the individual setting for each PWM macrocell. If this option is disabled (register [1301] = 1 for PWM0 or register [1475] = 1 for PWM1), then PWM output is changed right away by active Power-down. If this option is enabled (register [1301] = 0 for PWM0 or register [1475] = 0 for PWM1), the PWM block will finish the current PWM period and then will react to Power-down signal.

"Continuous/Autostop mode" register enables Autostop mode. This mode can be used with both Preset Registers or Regular mode. If PWM block works in Continuous mode (register [1302] = 0 for PWM0 or register [1476] = 0 for PWM1), PWM Duty Cycle CNT will overflow when it reaches boundaries. For example, for PWM Duty Cycle Counter counts up: 254th → 255th → 0th → 1st, and for PWM Duty Cycle Counter counts down: 1st → 0th → 255th → 254th … If Autostop mode is active (register [1302] = 1 for PWM0 or register [1476] = 1 for PWM1), PWM duty cycle counter will stop when it reaches boundaries. Please refer to Section 13.12 PWM Continuous/Autostop Mode.

"PWMx boundary OSC disable" is the function, that allows disabling internal oscillator when there is no need for PWM to be clocked (boundary is reached in Autostop mode only). This feature is useful for energy saving, but the user can optionally disable it and keeps the oscillator always enabled.

"Phase Correct mode". In normal mode, PWM output is HIGH, then LOW for each PWM period. When Phase correct PWM (also called Center Align) register is active (register [1460] = 1 for PWM0 or register [1478] = 1 for PWM1), then PWM output is HIGH, then LOW for the first period, then LOW again, and HIGH for the second period. So, there are less edges (or less output switches) for the Phase correct PWM mode.

"Duty Cycle source" (registers [1467:1466] for PWM0 or registers [1483:1482] for PWM1) defines the Regular mode of operation (registers [1467:1466] = 00 for PWM0 or registers [1483:1482] = 00 for PWM1) or Preset Registers mode (registers [1467:1466] = 01, registers [1467:1466] = 10, registers [1467:1466] = 11 for PWM0 or registers [1483:1482] = 01, registers [1483:1482] = 10, registers [1483:1482] = 11 for PWM1). In Regular mode, the value of duty cycle is changed every rising edge on Duty Cycle CNT CLK input. In Preset Registers mode the duty cycle is changed according to values, saved in 8-byte MSB of RegFile (registers [1467:1466] = 01 for PWM0 or registers [1483:1482] = 01 for PWM1), 8-byte LSB of RegFile (registers [1467:1466] = 10 for PWM0 or registers [1483:1482] = 10 for PWM1) or 16-byte of RegFile (registers [1467:1466] = 11 for PWM0 or registers [1483:1482] = 11 for PWM1). The address of RegFile value, that is applied to PWM block, is changed every rising edge on Duty Cycle CNT CLK input.

"OUT+ polarity selection" registers enable/disable inverted option for Output+ of PWM macrocell.

"OUT- polarity selection" registers enable/disable inverted option for Output- of PWM macrocell.

"Deadband selection" registers [1465:1464] for PWM0 and registers [1481:1480] for PWM1 chose dead band time between OUT+ and OUT- signals. It is 0, 1, 2, or 3 clock period of PWM Period CNT CLK signal.

"8-bit or 7-bit PWM resolution". It is possible to select 7-bit instead of default 8-bit resolution for the PWM to increase the PWM speed. If the 7-bit resolution is selected, the maximum value of the duty cycle counter is 127.

14. Analog Comparators

There are two General Purpose Rail-to-Rail Analog Comparator (ACMP) macrocells in the SLG47115. In order for the ACMP cells to be used in a GreenPAK design, the power-up signals (ACMP0H_pdb, ACMP1H_pdb) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be on continuously, off continuously, or switched on periodically, based on a digital signal coming from the Connection Matrix. When ACMP is powered down, the output is LOW (the output remains its state while sleeping).

The General-Purpose Rail-to-Rail Analog Comparators are optimized for high-speed operation (ACMP0H and ACMP1H).

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources and can also have a selectable gain stage before connection to the analog comparator. Each of the ACMP cells has a negative input signal that is either created from an internal Vref or provided by a way of the external sources.

Power-Up = 1 => ACMP is powered up.

Power-Up = 0 => ACMP is powered down.

During power-up, the ACMP output will remain LOW, and then becomes valid after power up signal goes HIGH for ACMP0H and ACMP1H (see parameter t_{start} in Table 26). Input bias current < 1 nA (typ). The gain divider is unbuffered and consists of 1 MΩ resistors. Internally generated IN- voltage range is: 0.032 - 2.016 V, while external IN- voltage range is 0 - V_{DD}.

Each cell also has a hysteresis selection, to offer hysteresis of (0, 32, 64, 192) mV. The hysteresis option is available when using an internal Vref only.

The ESD resistors should be taken into consideration when using pull-up/pull-down resistors. It may affect V_{IH} and V_{IL}. See sections 6.6 ESD Protectionto 6.9 Matrix OE IO Structure (VDD Group).

ACMP0H IN+ options are GPIO5, V_{DD}
ACMP1H IN+ options are GPIO6, ACMP0H IN+ MUX output, Temp Sensor OUT.

14.1 ACMP0H Block Diagram

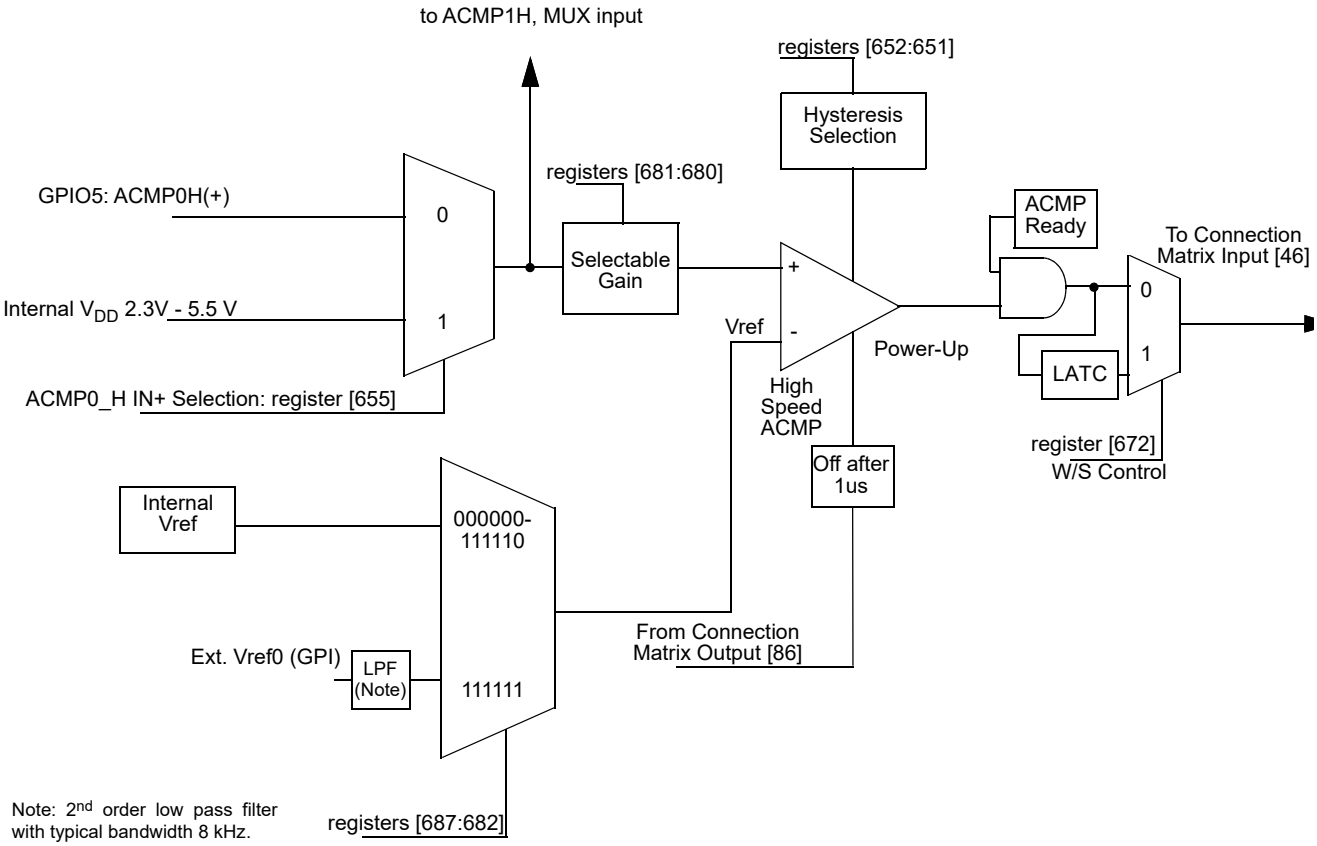


Figure 116. ACMP0H Block Diagram

14.2 ACMP1H Block Diagram

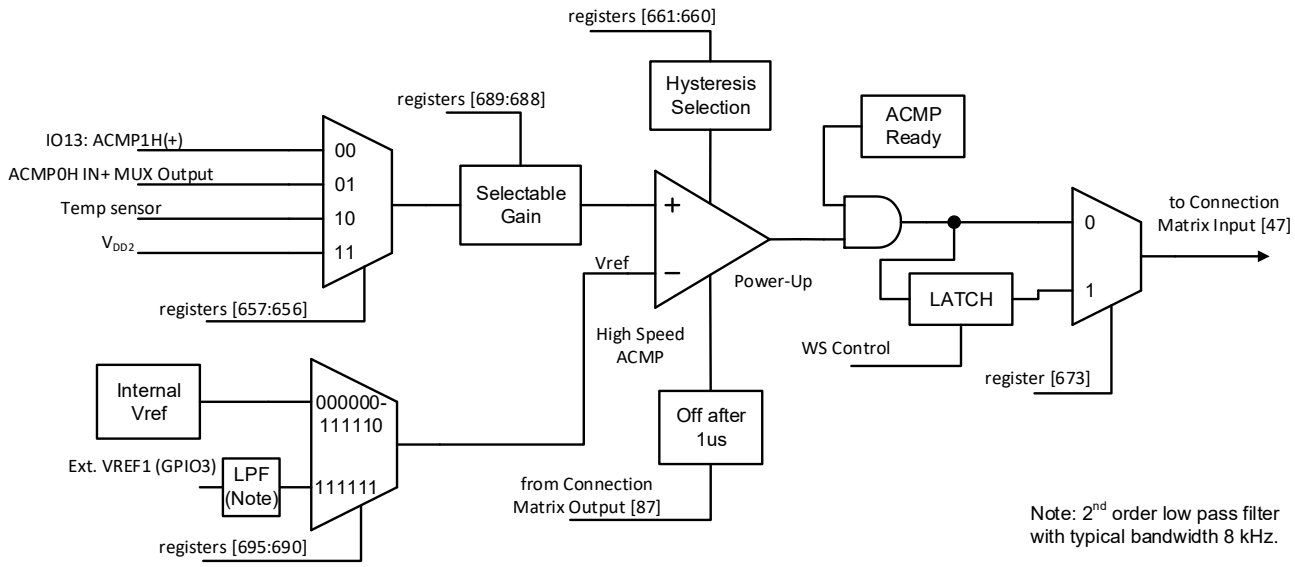


Figure 117. ACMP1H Block Diagram

14.3 ACMP Typical Performance

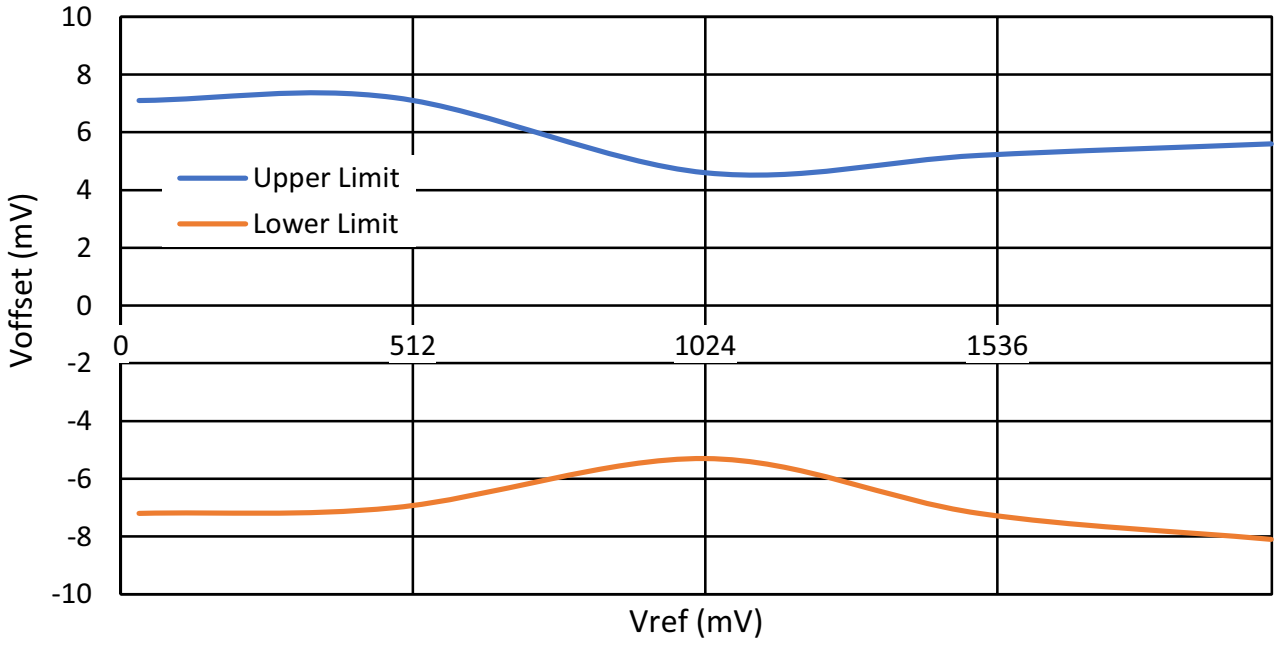


Figure 118. ACMPxH Input Offset Voltage vs. Vref at V_{DD} = 2.3 V to 5.5 V, T_A = -40 °C to 85 °C,

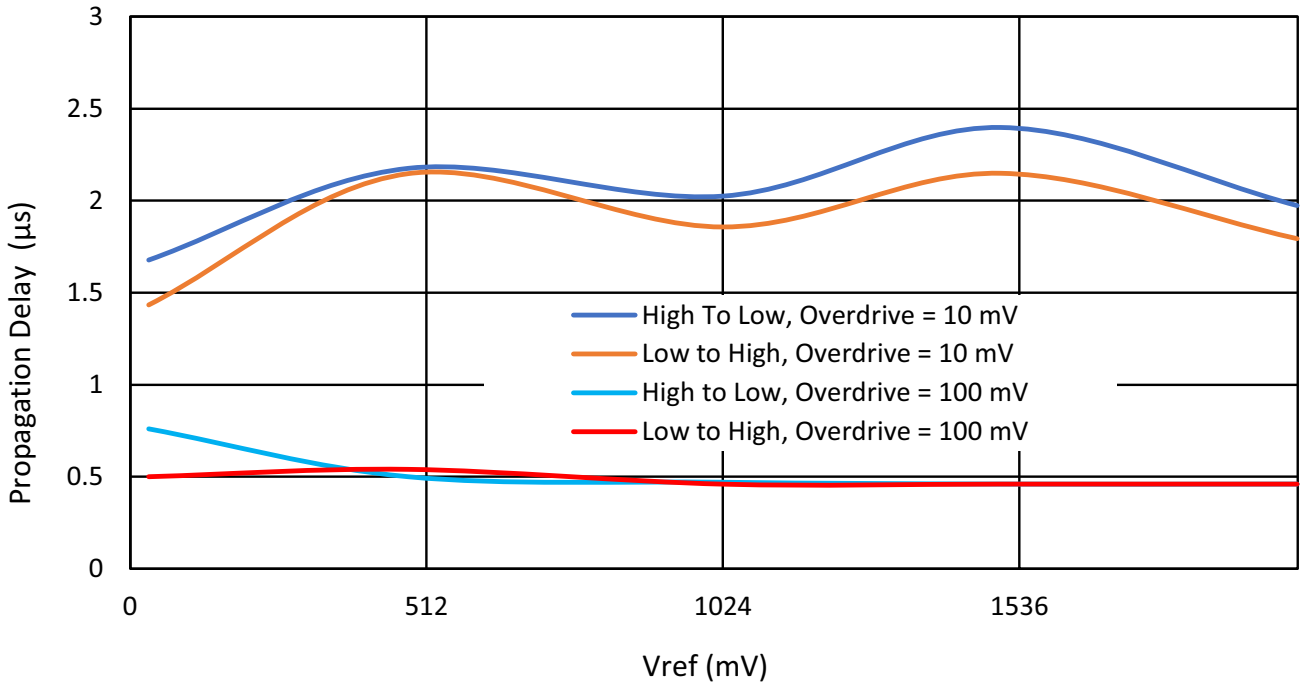


Figure 119. Propagation Delay vs. Vref for ACMPxH at T_A = 25 °C, at V_{DD} = 2.3 V to 5.5 V, Gain = 1, Hysteresis = 0

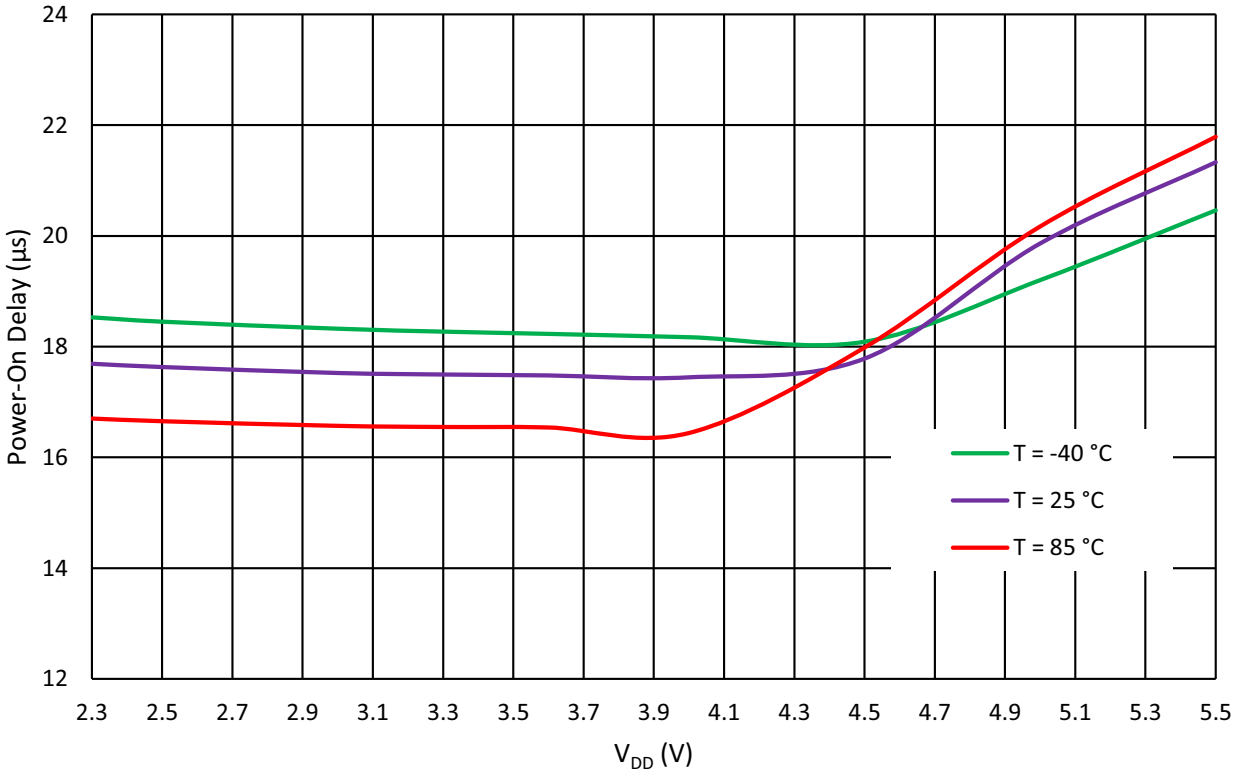


Figure 120. ACMPxH Power-On Delay vs. V_{DD}

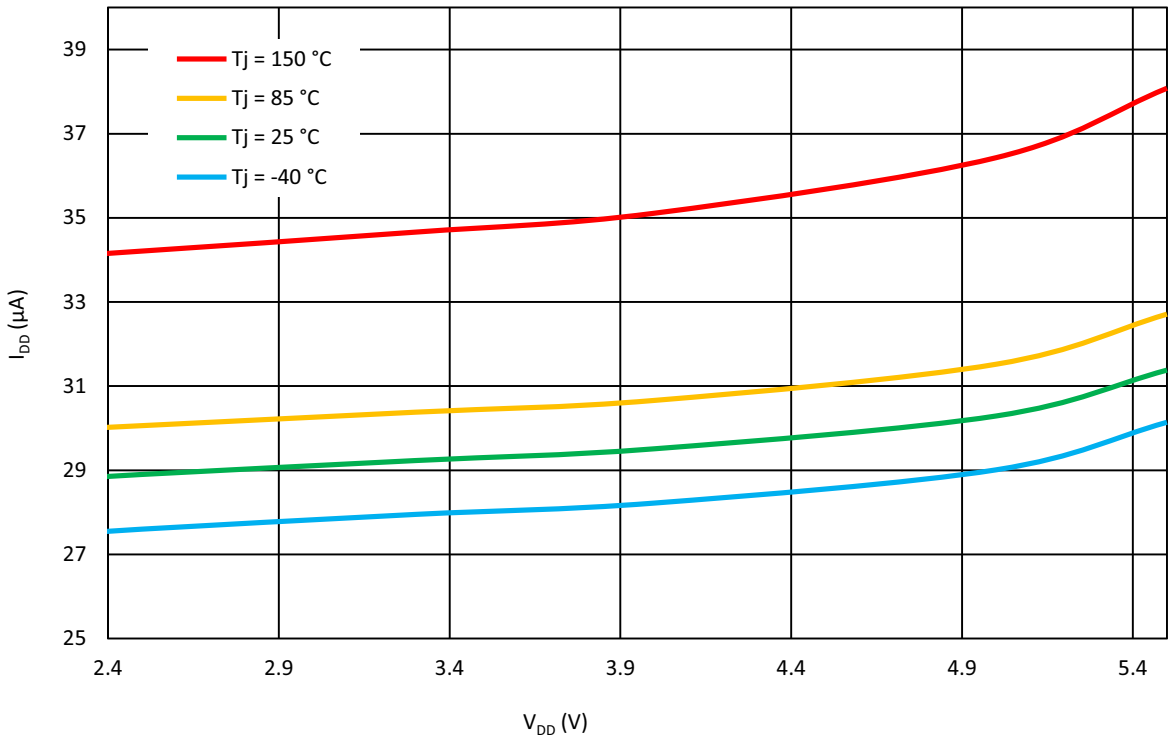


Figure 121. ACMPxH Current Consumption vs. V_{DD} at Vref = 32 mV

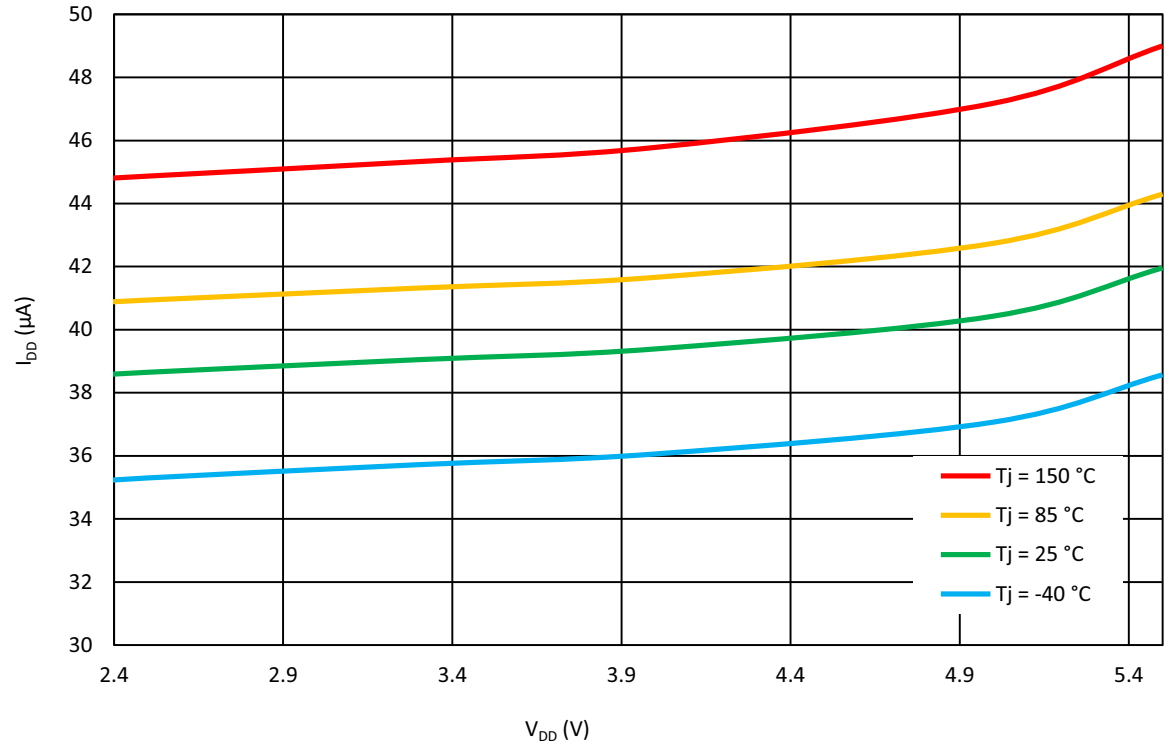


Figure 122. ACMPxH Current Consumption vs. V_{DD} at Vref = 1024 mV

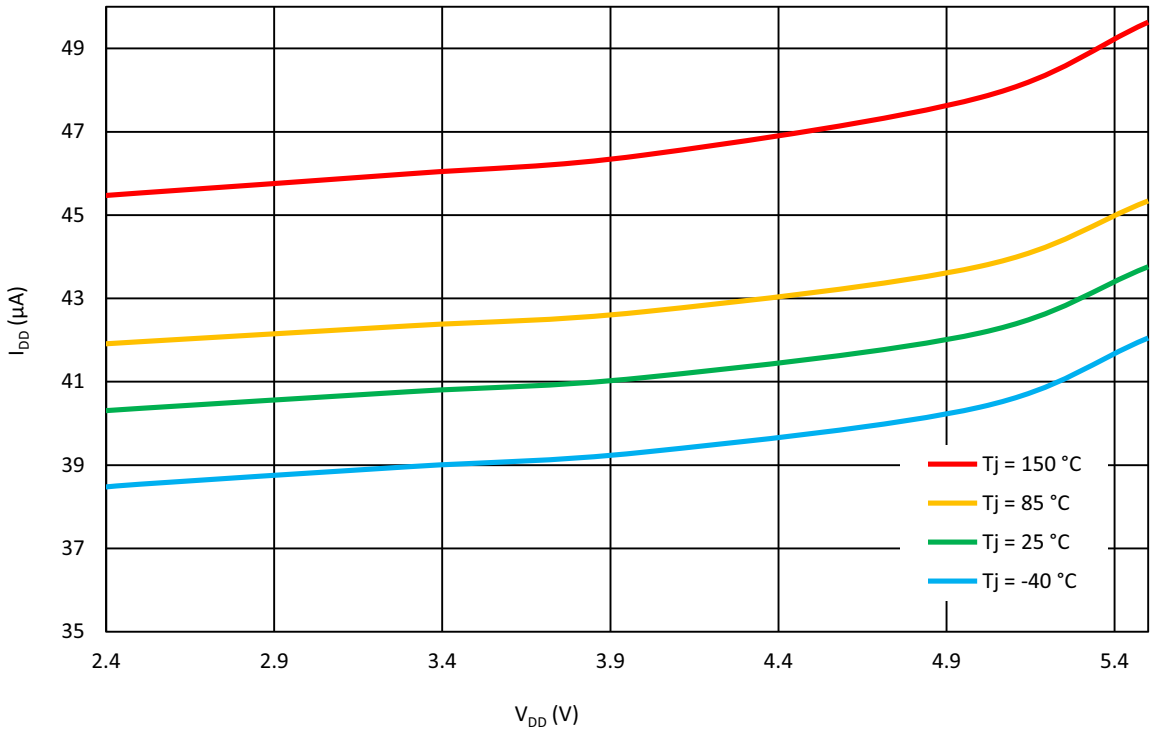


Figure 123. ACMPxH Current Consumption vs. V_{DD} at Vref = 2016 mV

15. Programmable Delay/Edge Detector

The SLG47115 has a programmable time delay logic cell that can generate a delay that is selectable from one of four timings (time2) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay, as well as glitch rejection during the delay period. See Figure 124 for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

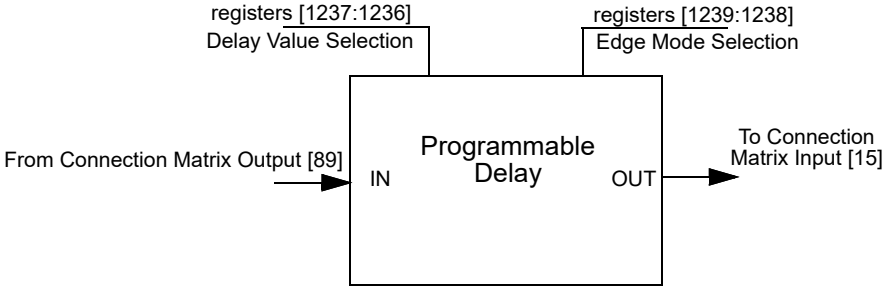


Figure 124. Programmable Delay

15.1 Programmable Delay Timing Diagram - Edge Detector Output

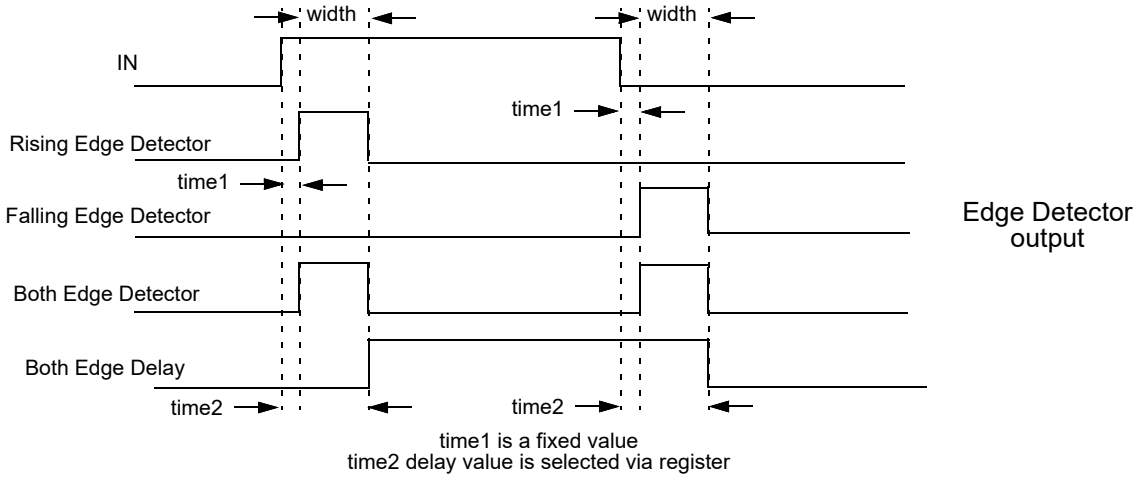


Figure 125. Edge Detector Output

Please refer to Table 15.

16. Additional Logic Function. Deglitch Filter

The SLG47115 has one Deglitch Filter macrocell with inverter function that is connected directly to the Connection matrix inputs and outputs. In addition, this macrocell can be configured as an Edge Detector, with the following settings:

- Rising Edge Detector
- Falling Edge Detector
- Both Edge Detector
- Both Edge Delay

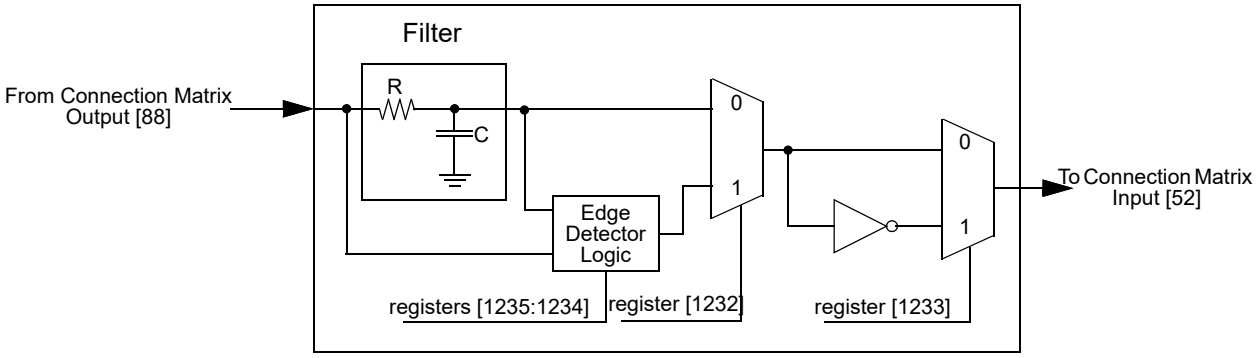


Figure 126. Deglitch Filter/Edge Detector

17. Voltage Reference

17.1 Voltage Reference Overview

The SLG47115 has a Voltage Reference macrocell to provide references to the two analog comparators. This macrocell can supply a user selection of fixed voltage references, or temperature sensor output. See Table 68 for the available selections for each analog comparator.

Also, see Figure 127, which shows the reference output structure.

17.2 Vref Selection Table

Table 68. Vref Selection Table

SEL	SEL[5:0]	Vref	SEL	SEL[5:0]	Vref
0	000000	0.032	32	100000	1.056
1	000001	0.064	33	100001	1.088
2	000010	0.096	34	100010	1.12
3	000011	0.128	35	100011	1.152
4	000100	0.16	36	100100	1.184
5	000101	0.192	37	100101	1.216
6	000110	0.224	38	100110	1.248
7	000111	0.256	39	100111	1.28
8	001000	0.288	40	101000	1.312
9	001001	0.32	41	101001	1.344
10	001010	0.352	42	101010	1.376
11	001011	0.384	43	101011	1.408
12	001100	0.416	44	101100	1.44
13	001101	0.448	45	101101	1.472
14	001110	0.48	46	101110	1.504
15	001111	0.512	47	101111	1.536
16	010000	0.544	48	110000	1.568
17	010001	0.576	49	110001	1.6
18	010010	0.608	50	110010	1.632
19	010011	0.64	51	110011	1.664
20	010100	0.672	52	110100	1.696
21	010101	0.704	53	110101	1.728
22	010110	0.736	54	110110	1.76
23	010111	0.768	55	110111	1.792
24	011000	0.8	56	111000	1.824
25	011001	0.832	57	111001	1.856
26	011010	0.864	58	111010	1.888
27	011011	0.896	59	111011	1.92
28	011100	0.928	60	111100	1.952

Table 68. Vref Selection Table (Cont.)

SEL	SEL[5:0]	Vref	SEL	SEL[5:0]	Vref
29	011101	0.96	61	111101	1.984
30	011110	0.992	62	111110	2.016
31	011111	1.024	63	111111	External

17.3 Mode Selection

Table 69. Mode Selection Table

Conditions	M[2]	M[1]	M[0]	Mode
GPIO0 isn't configured as Analog IO (registers [756:755] ≠ 11) OR GPIO0 OE is HIGH	0	0	0	Analog Power-down
	0	0	1	Analog Power-down
	0	1	0	Vref_OUT to ACMP only
	0	1	1	Vref_OUT to ACMP only
	1	0	0	Analog Power-down
	1	0	1	Vts_OUT to ACMP only
	1	1	0	Vts_OUT to ACMP only
	1	1	1	Analog Power-down
GPIO0 is configured as Analog IO (registers [756:755] = 11) AND GPIO0 OE is LOW	0	0	0	Analog Power-down
	0	0	1	Vref_OUT to GPIO0 only
	0	1	0	Vref_OUT to ACMP only
	0	1	1	Vref_OUT to GPIO0 and ACMP
	1	0	0	Vts_OUT to GPIO0 only
	1	0	1	Vts_OUT to ACMP only
	1	1	0	Vts_OUT to GPIO0 and ACMP
	1	1	1	Vref_OUT to GPIO0 bypass analog buffer

Note: Voltage Reference can be outputted to GPIO0 according to M[2:0] state when this GPIO is configured as Analog IO (registers [756:755] = 11) AND GPIO0 OE is LOW.

17.4 Vref Block Diagram

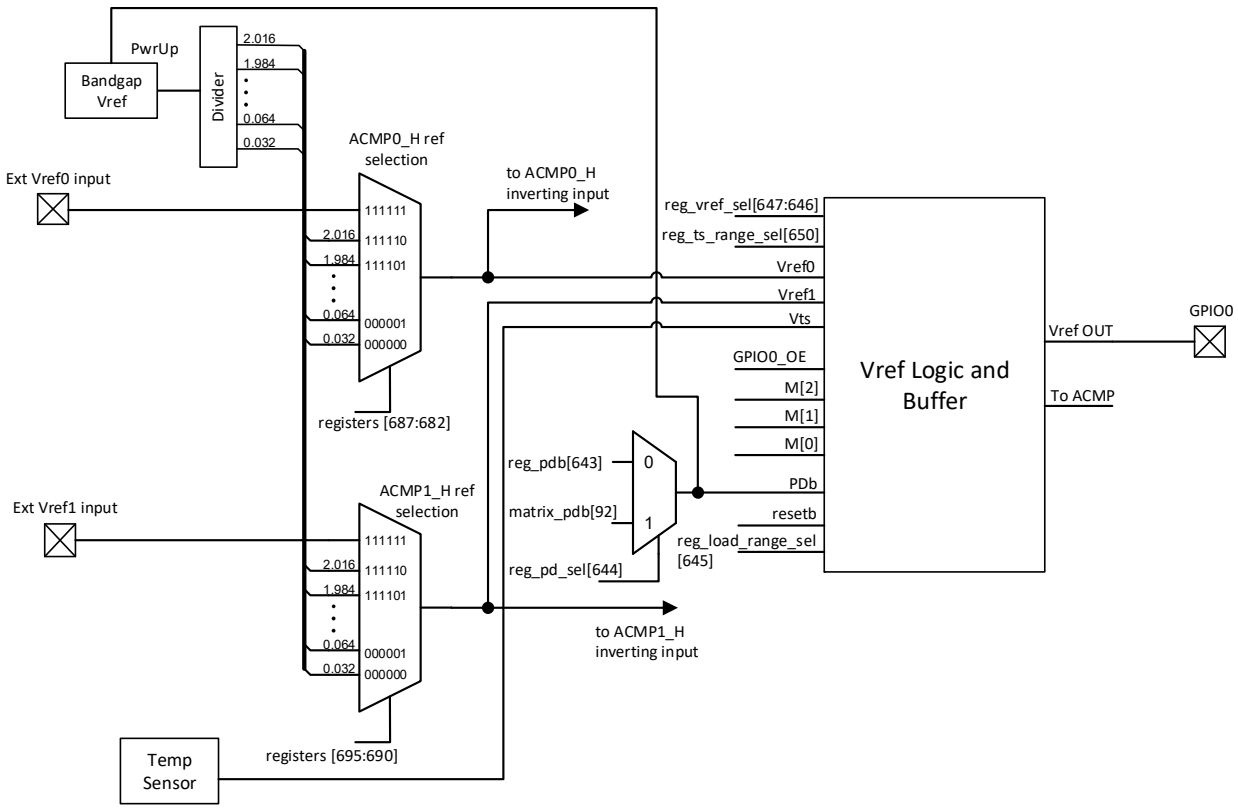


Figure 127. Voltage Reference Block Diagram

Note 1: reg_ts_range_sel register, that defines voltage range of Vref Block Output, is valid for Temp Sensor source only.
Note 2: reg_load_range_sel register should be set to 1 for better stability when the load resistance at GPIO0 is more than 100 kΩ. This option affects consumption current.

17.5 Vref Load Regulation

It is not recommended to use Vref connected to external pin without buffer.

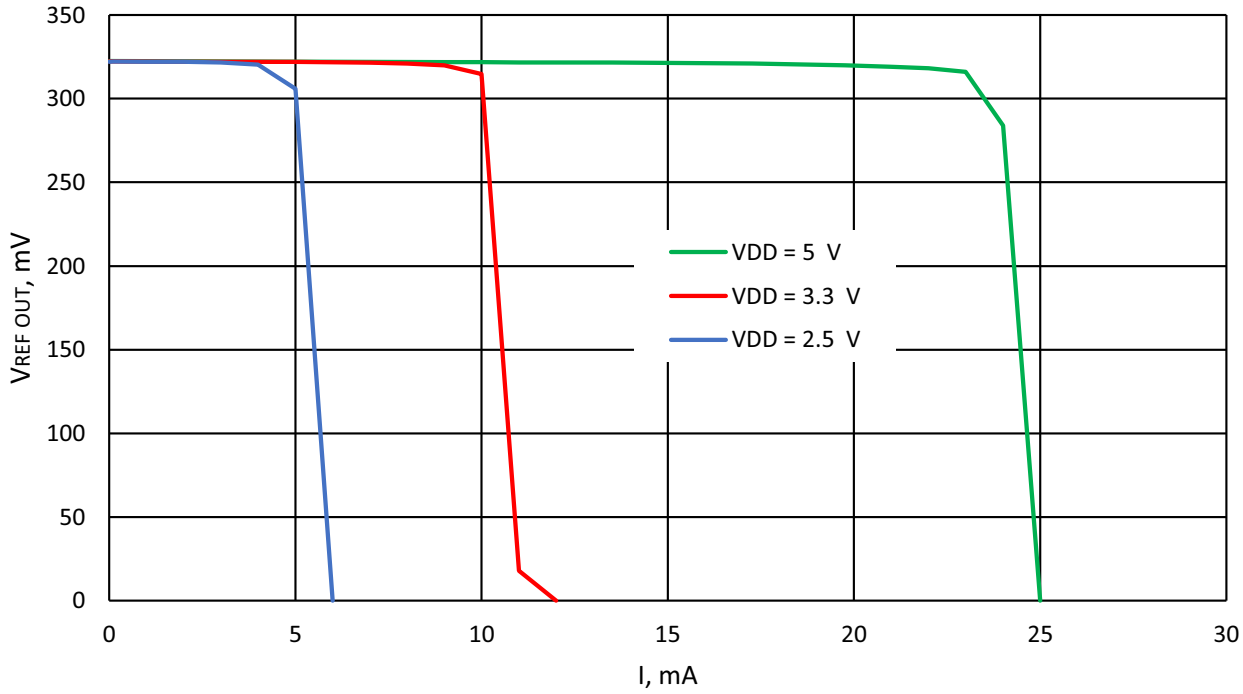


Figure 128. Typical Load Regulation, Vref = 320 mV, T_A = -40 °C to +85 °C, Buffer - Enabled

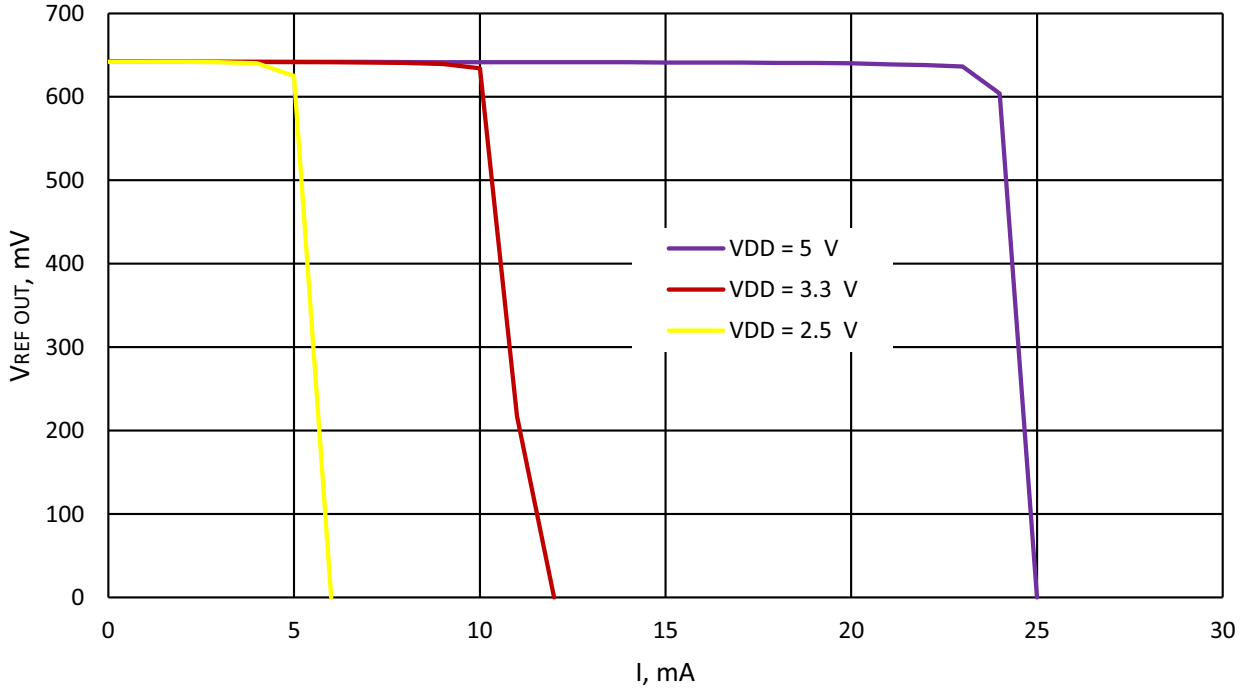


Figure 129. Typical Load Regulation, Vref = 640 mV, T_A = -40 °C to +85 °C, Buffer - Enabled

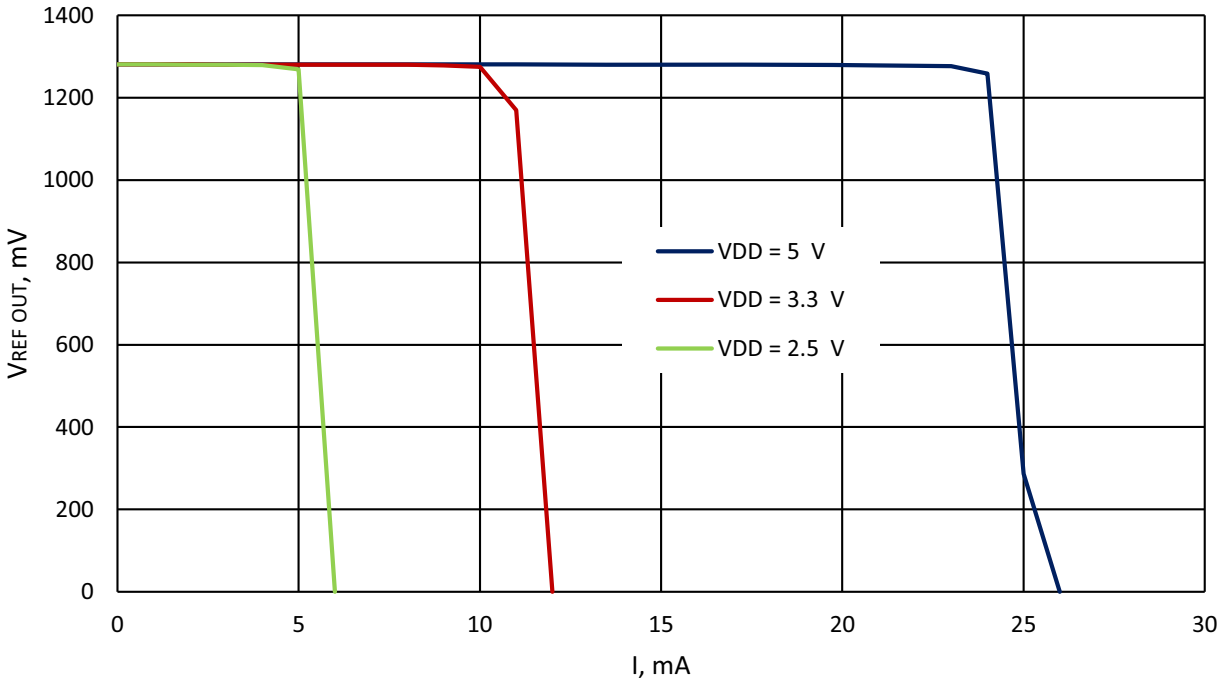


Figure 130. Typical Load Regulation, Vref = 1280 mV, T_A = -40 °C to +85 °C, Buffer - Enabled

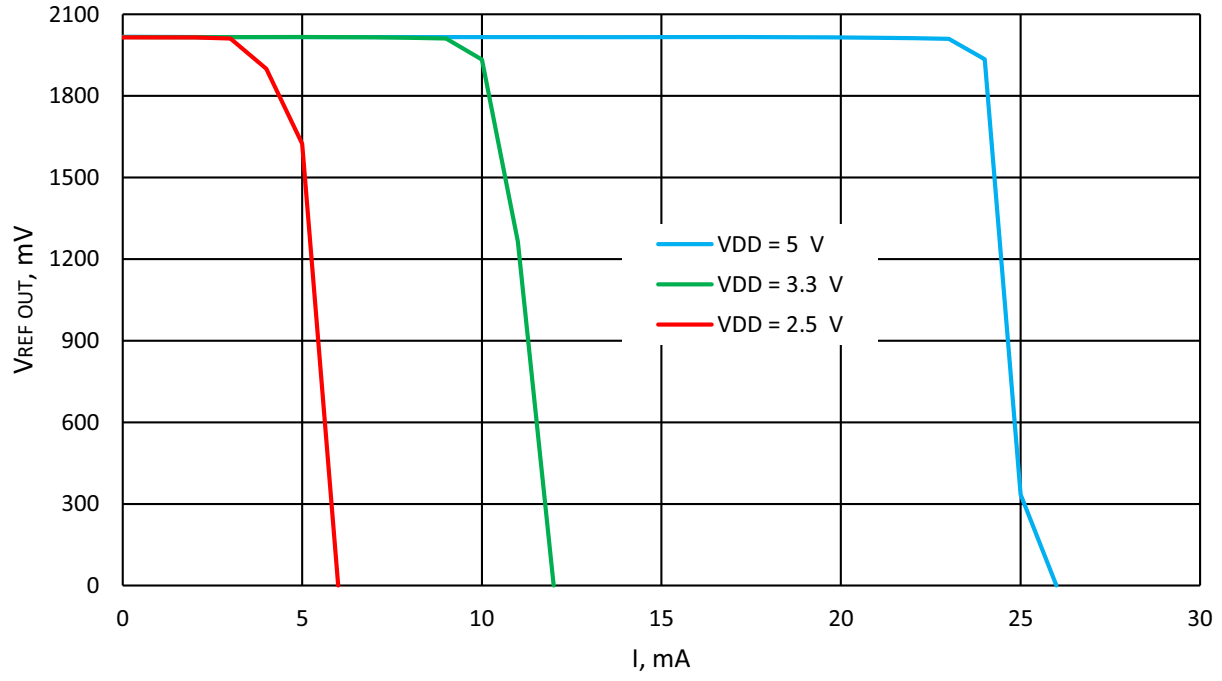


Figure 131. Typical Load Regulation, Vref = 2016 mV, T_A = -40 °C to +85 °C, Buffer - Enabled

18. Clocking

18.1 OSC General Description

The SLG47115 has two internal oscillators to support a variety of applications:

- Oscillator0 (2.048 kHz)
- Oscillator1 (25 MHz).

There are two divider stages for each oscillator that gives the user flexibility for introducing clock signals to the connection matrix, as well as various other macrocells. The Pre-divider (first stage) for Oscillator allows the selection of /1, /2, /4 or /8, and /12 in Oscillator1(25 MHz) to divide down frequency from the fundamental. The second stage divider has an input of frequency from the Pre-divider, and outputs one of eight different frequencies divided by /1, /2, /3, /4, /8, /12, /24, or /64 on Connection Matrix Input lines [53], [54], [55], and [56]. Please see Figure 132 for more details on the SLG47115 clock scheme.

Oscillator1 (25 MHz) has an additional function of 100 ns delayed startup, which can be enabled/disabled by register [722]. This function is recommended to use when analog blocks are used along with the Oscillator.

The Matrix Power-down/Force On function allows switching off or force on the oscillator using an external pin. The Matrix Power-down/Force-On (Connection Matrix Output [90], [91]) signal has the highest priority. The OSC operates according to the following table:

Table 70. Oscillator Operation Mode Configuration Settings

POR	External Clock selection	Signal from Connection matrix	Register: Power-Down or Force On by matrix input	Register: Auto Power-On or Force On	OSC Enable Signal from CNT/DLY macrocells	OSC operation mode
0	X	X	X	X	X	OFF
1	1	X	X	X	X	Internal OSC is OFF, logic is ON
1	0	1	0	X	X	OFF
1	0	1	1	X	X	ON
1	0	0	X	1	X	ON
1	0	0	X	0	CNT/DLY requires OSC	ON
1	0	0	X	0	CNT/DLY does not require OSC	OFF

[1] The OSC will run only when any macrocell that uses OSC is powered on.

18.2 Oscillator0 (2.048 kHz

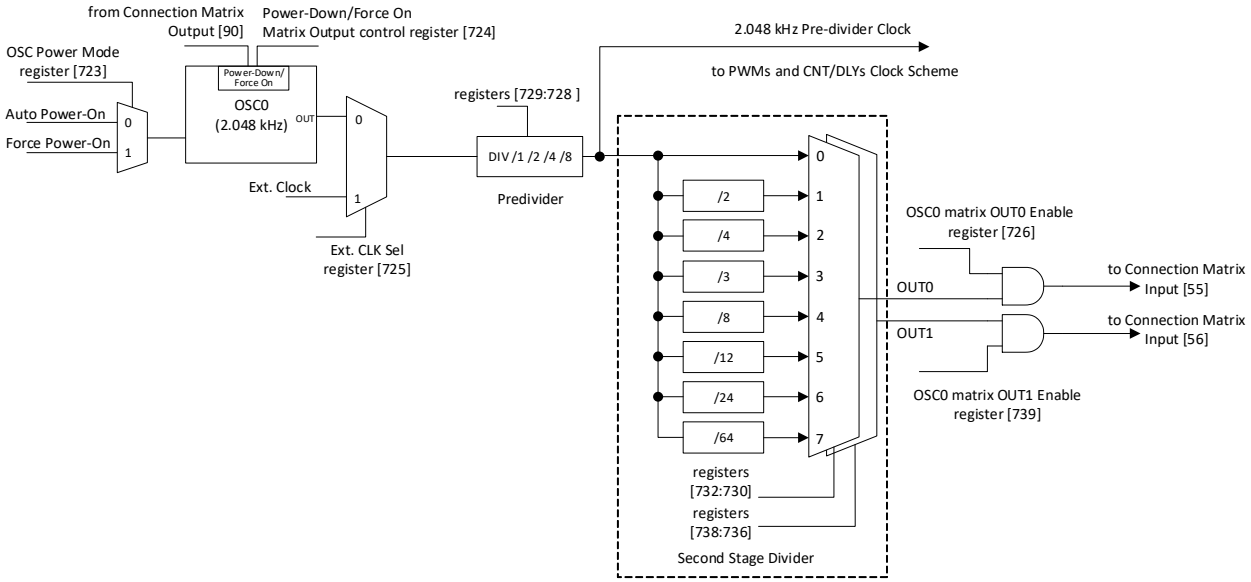


Figure 132. Oscillator0 Block Diagram

18.3 Oscillator1 (25 MHz)

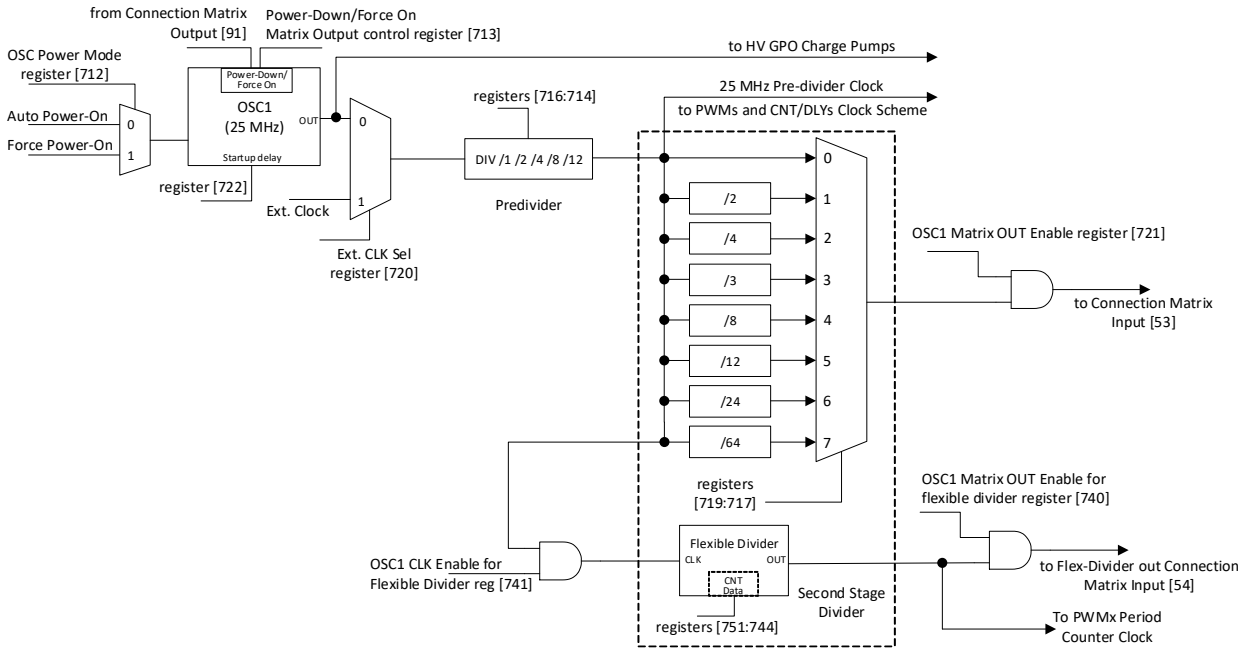


Figure 133. Oscillator1 Block Diagram

The OSC-integrated divider is built into 25 MHz OSC for saving chip resources. Actually, this divider is created especially for PWM, but it can be used for other chip resources thanks to its output to the matrix. There is 8-bit Counter with the source from OSC pre-divider and output to the matrix. In many cases for all PWM macrocells, the same frequency is a need. In these cases, it is possible to use this PWM divider for fine frequency tuning of PWM cells by I^2C or from NVM.

18.4 CNT/DLY Clock Scheme

Each CNT/DLY within Multi-Function macrocell has its own additional clock divider connected to oscillators pre-divider. Available dividers are:

- OSC0/1, OSC0/8, OSC0/64, OSC0/512, OSC0/4096, OSC0/32768, OSC0/262144
- OSC1/1, OSC1/4

It is possible also to connect input from CNT(x-1) overflow or from Connection matrix OUT.

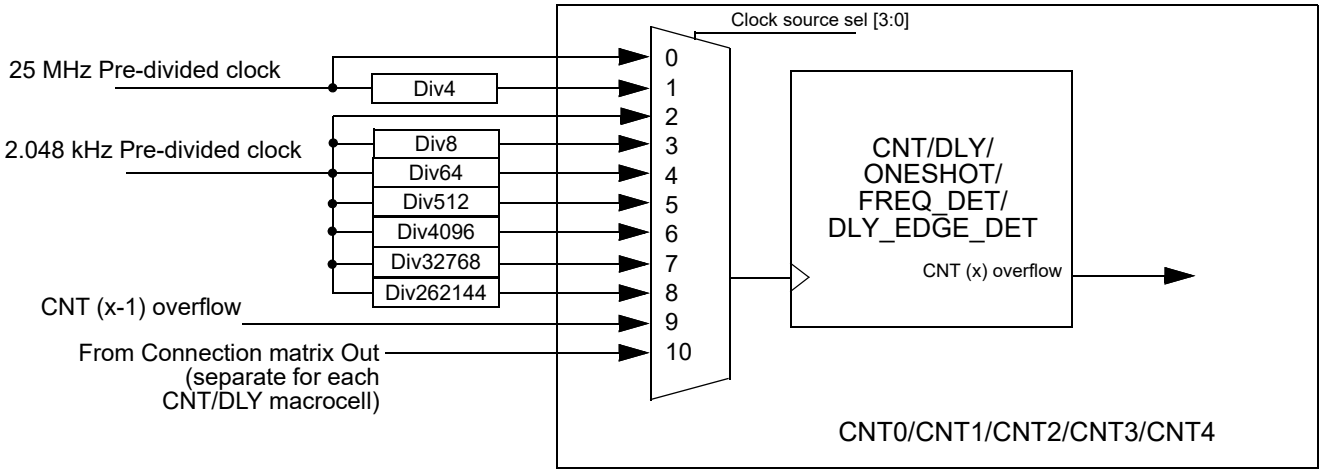


Figure 134. Clock Scheme

18.5 PWM Clock Scheme

Each PWM macrocell has its own additional clock divider connected to oscillators pre-divider. Available dividers are:

- OSC1/1, OSC1/8, OSC1/64, OSC1/512, OSC1/4096, OSC1/32768, OSC1/262144
- OSC0/1, OSC0/4

It is possible also to connect input from Flexible Divider (OSC1 clock divider) or from Connection matrix OUT.

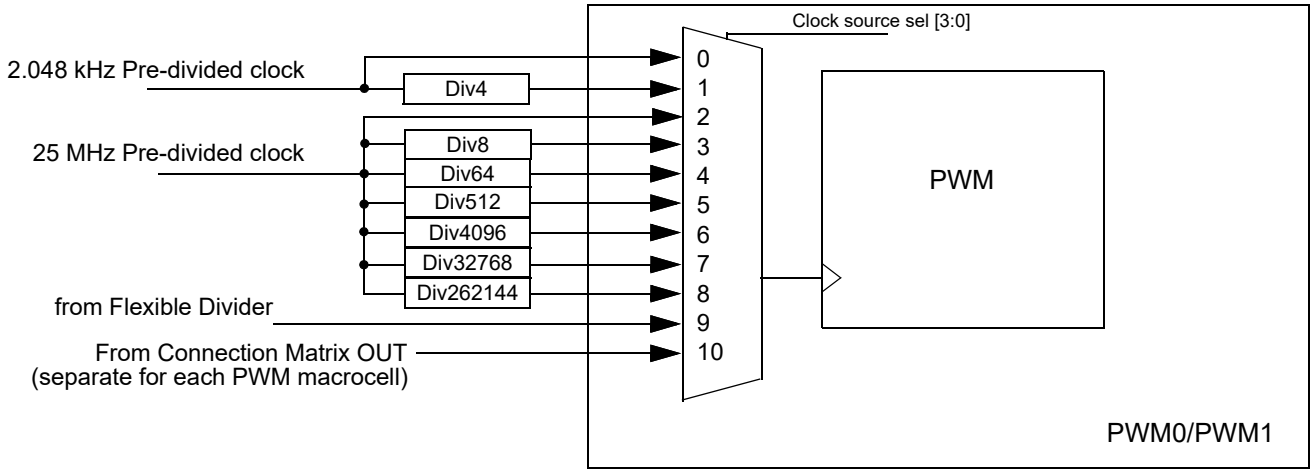


Figure 135. PWM Clock Scheme

18.6 External Clocking

The SLG47115 supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

Note that the Low Voltage Digital Input pin type can only support up to 1 MHz.

18.6.1 GPIO1 Source for Oscillator0 (2.048 kHz)

When register [725] is set to 1, an external clocking signal on GPIO1 will be routed in place of the internal oscillator derived 2.048 kHz clock source. See Figure 132. The low and high limits for external frequency that can be selected are 0 MHz and 10 MHz.

18.6.2 GPIO4 Source for Oscillator1 (25 MHz)

When register [720] is set to 1, an external clocking signal on GPIO4 will be routed in place of the internal oscillator derived 25 MHz clock source. See Figure 133. The external frequency range is 0 MHz to 20 MHz at V_{DD} = 2.3 V, 30 MHz at V_{DD} = 3.3 V, 50 MHz at V_{DD} = 5.0 V. When an external clock is selected for OSC1, the oscillator's output signal will be inverted with respect to the GPIO4 input signal.

18.7 Oscillators Power-On Delay

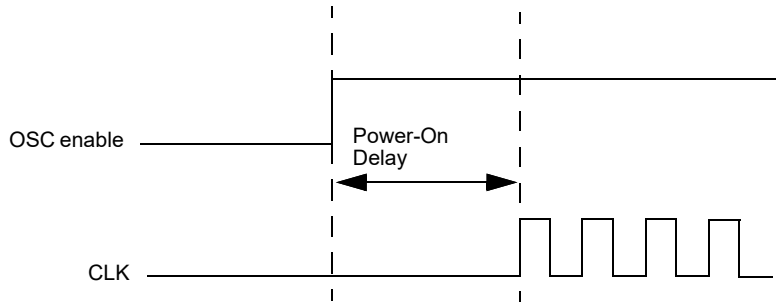


Figure 136. Oscillator Startup Diagram

Note 1: OSC power mode: “Auto Power-On”.
Note 2: OSC enable” signal appears when any macrocell that uses OSC is powered on.

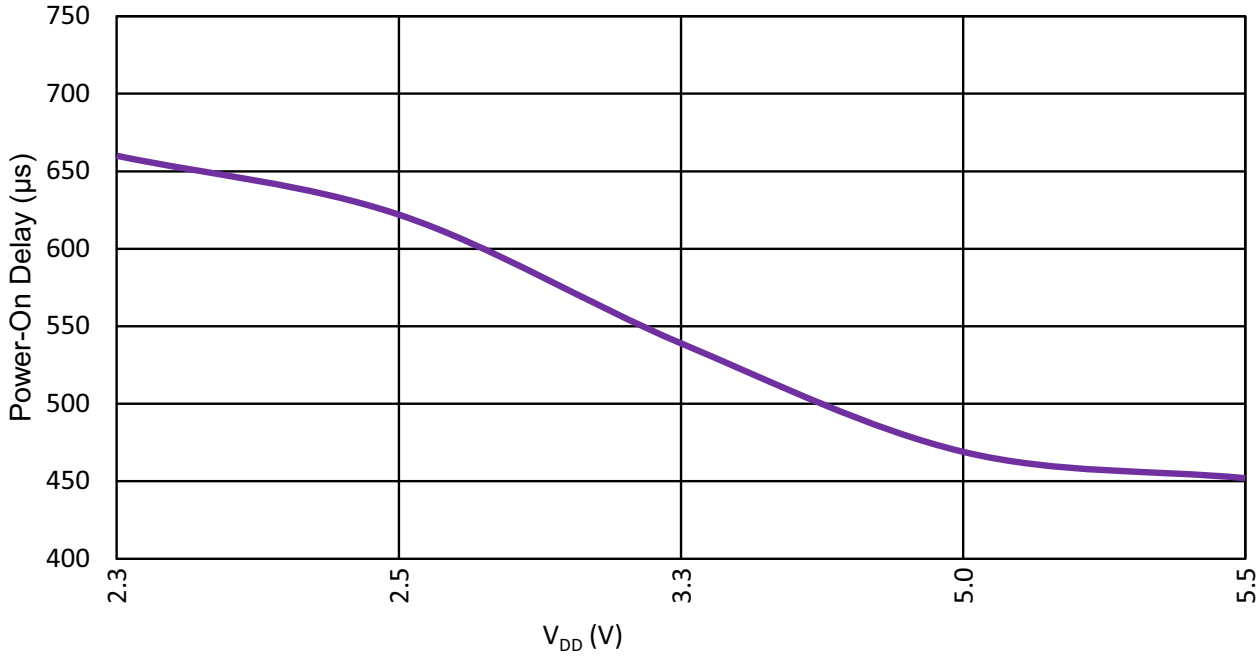


Figure 137. Oscillator0 Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, OSC0 = 2.048 kHz

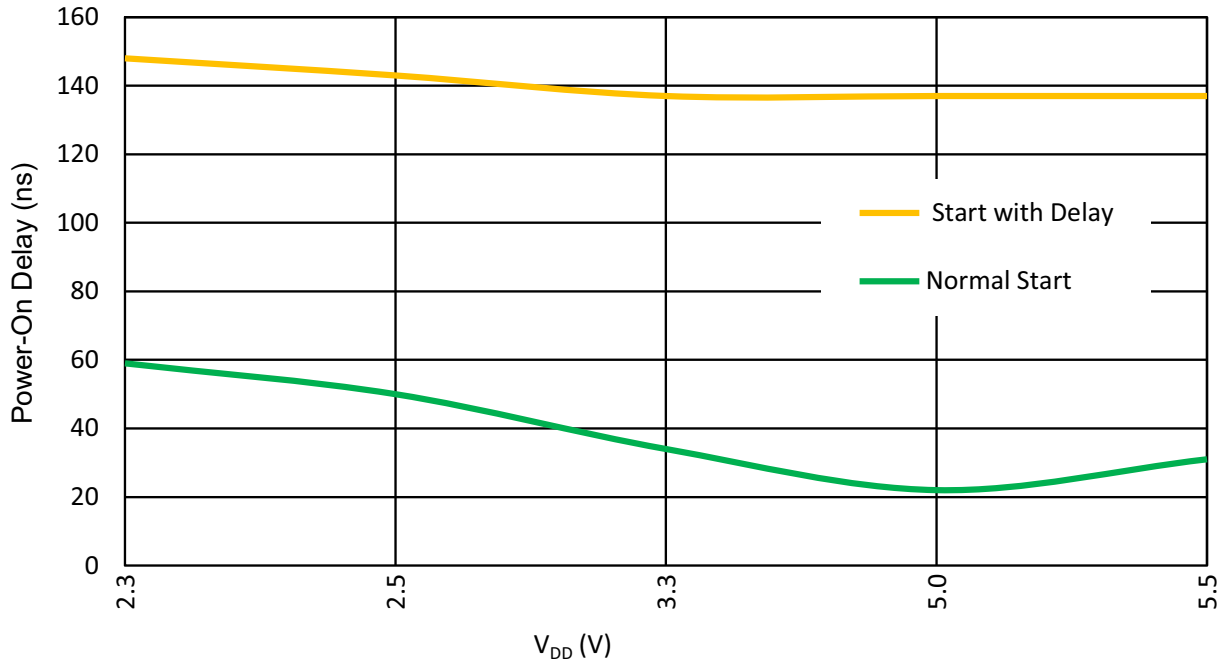


Figure 138. Oscillator1 Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, OSC1 = 25 MHz

18.8 Oscillators Accuracy

Note: OSC power setting: force Power-On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

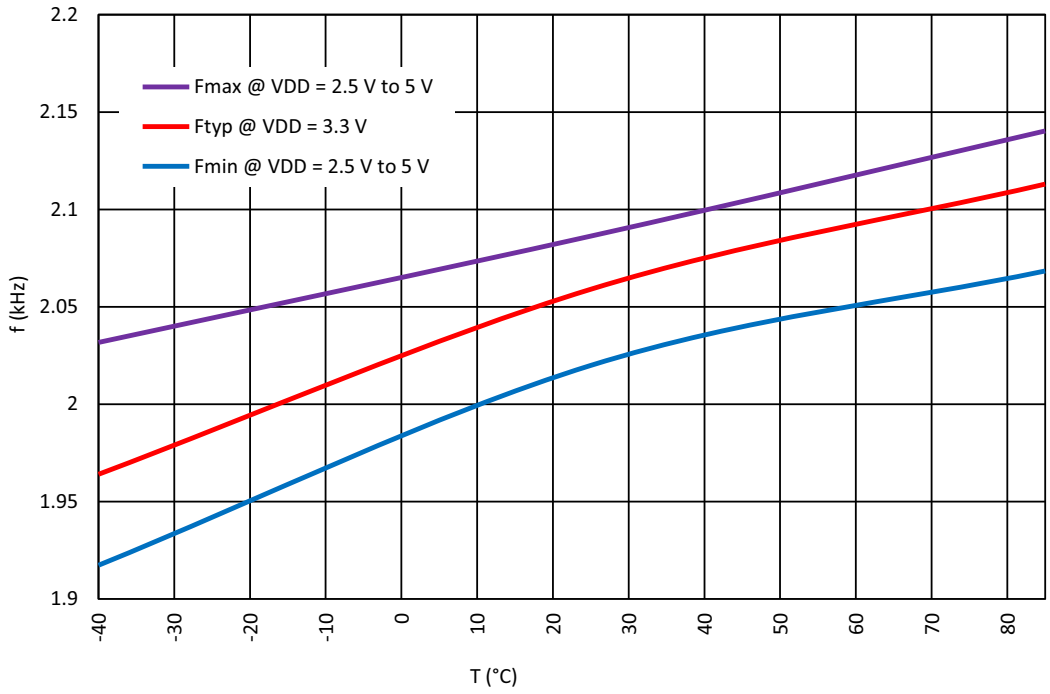


Figure 139. Oscillator0 Frequency vs. Temperature, OSC0 = 2.048 kHz

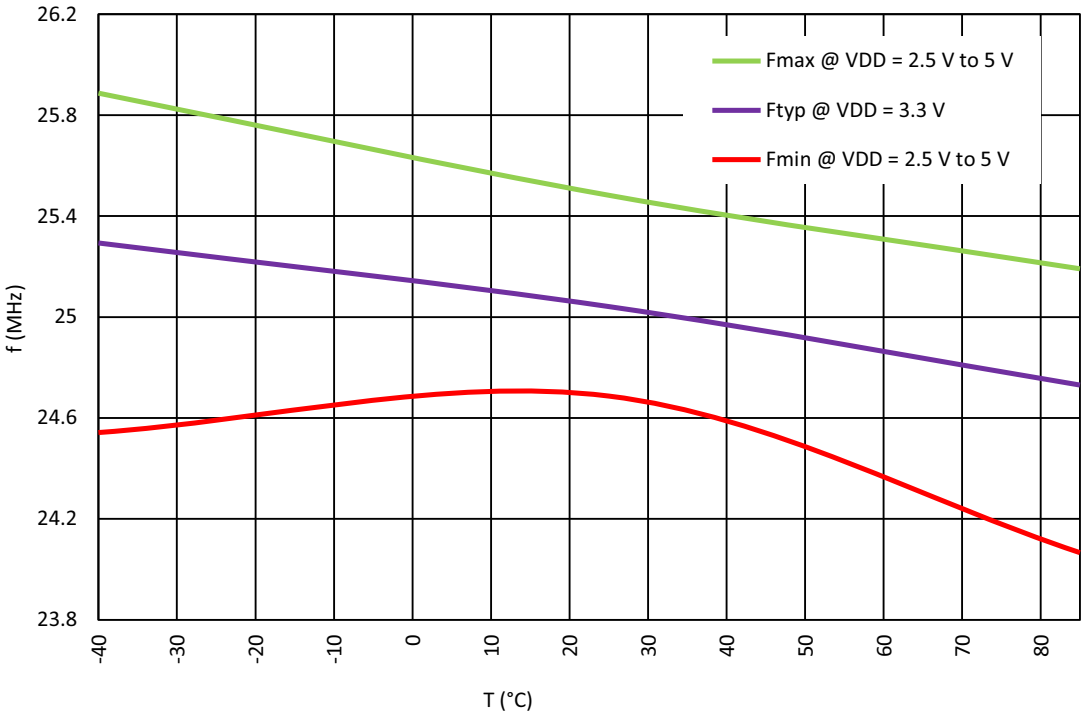


Figure 140. Oscillator1 Frequency vs. Temperature, OSC1 = 25 MHz

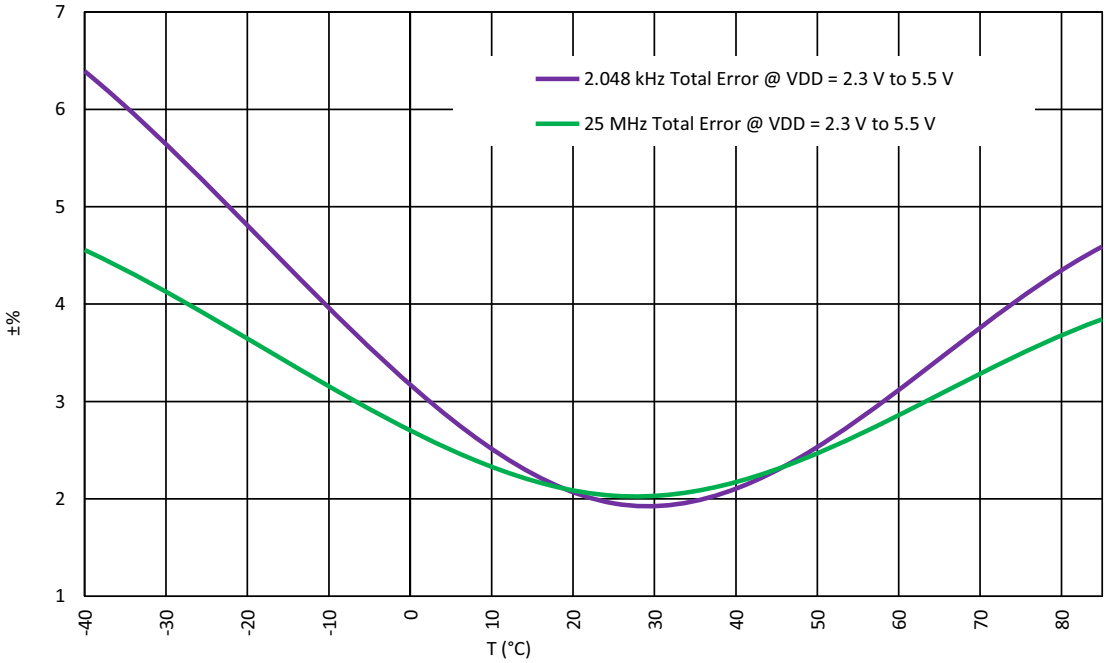


Figure 141. Oscillators Total error vs. Temperature

Note: For more information see section 3.12 Oscillator Specifications.

18.9 Oscillators Settling Time

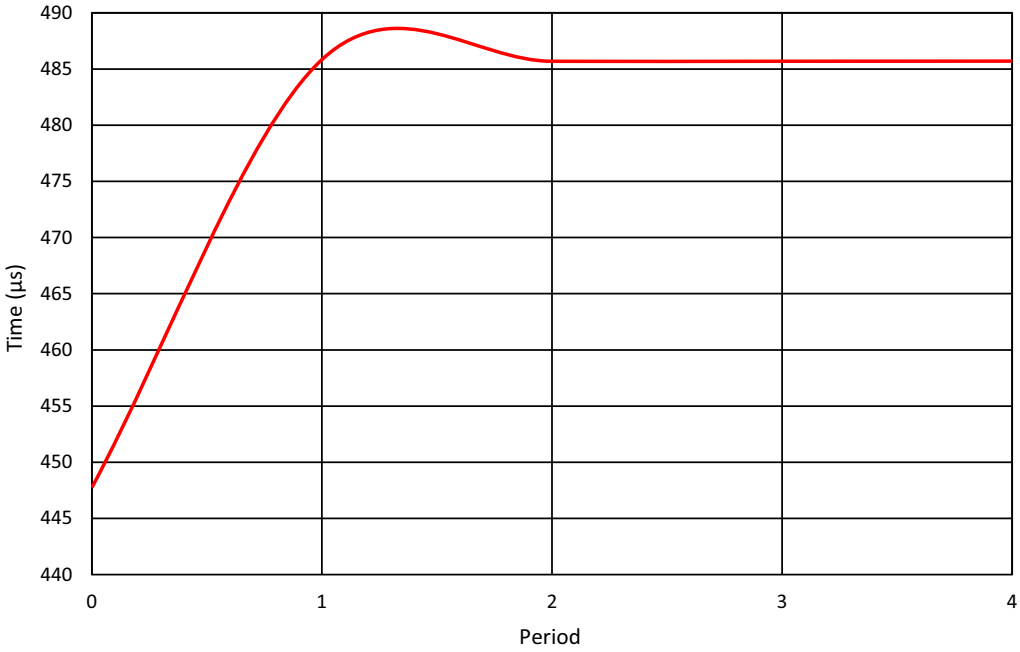


Figure 142. Oscillator0 Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC0 = 2 kHz

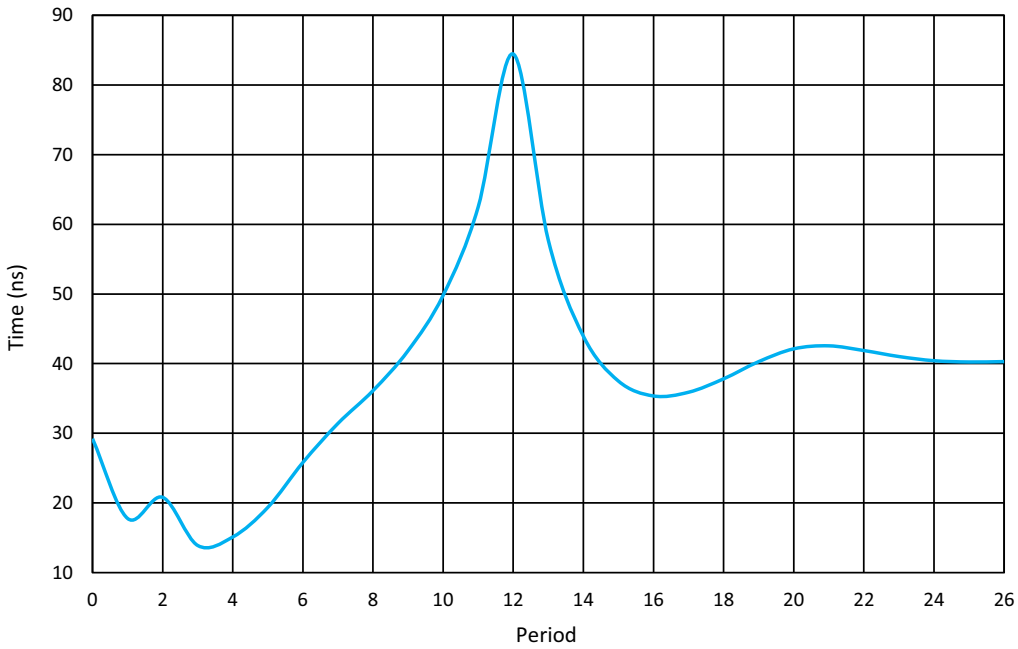


Figure 143. Oscillator1 Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC1 = 25 MHz (Normal Start)

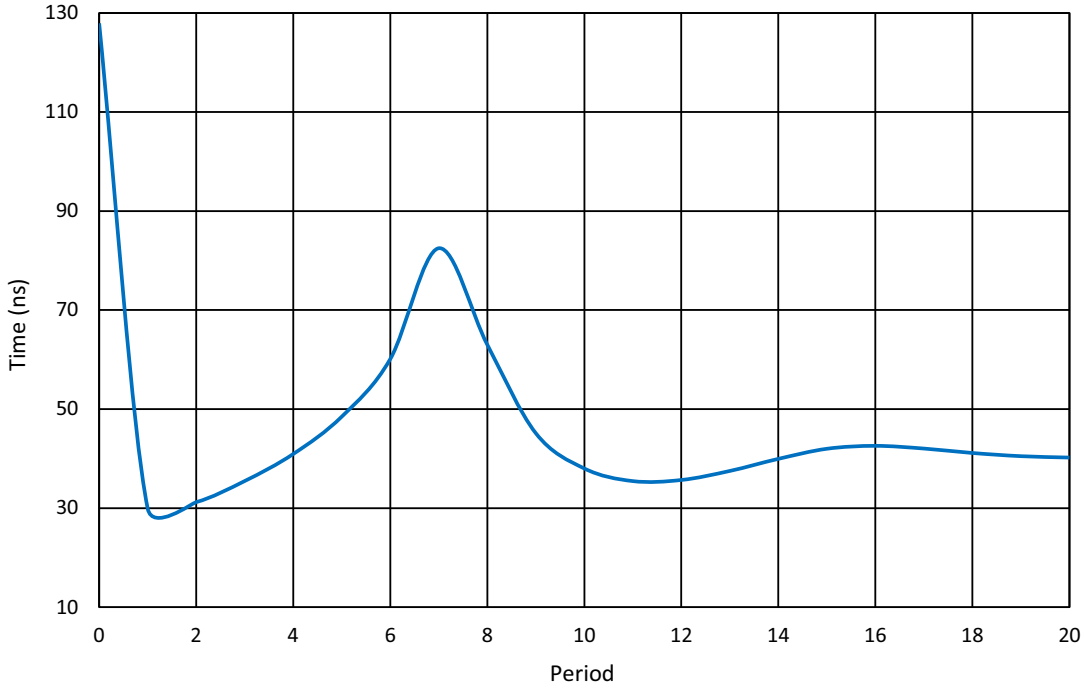


Figure 144. Oscillator1 Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC1 = 25 MHz (Start with Delay)

18.10 Oscillators Current Consumption

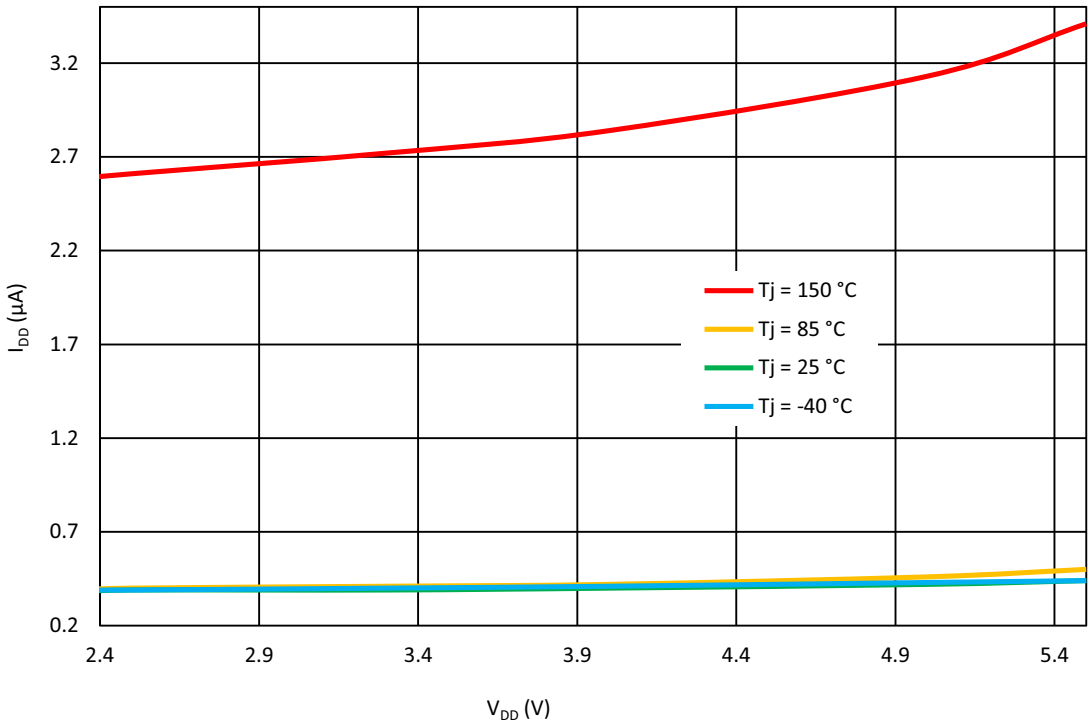


Figure 145. OSC0 Current Consumption vs. V_{DD} (All Pre-Dividers)

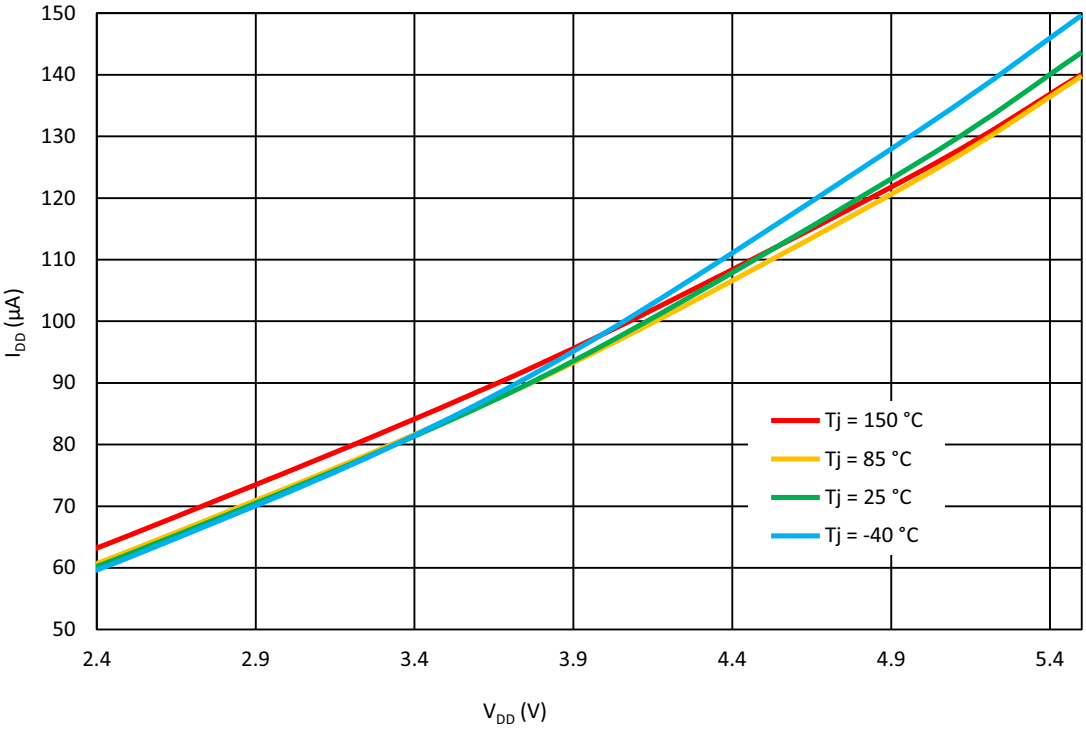


Figure 146. OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 1)

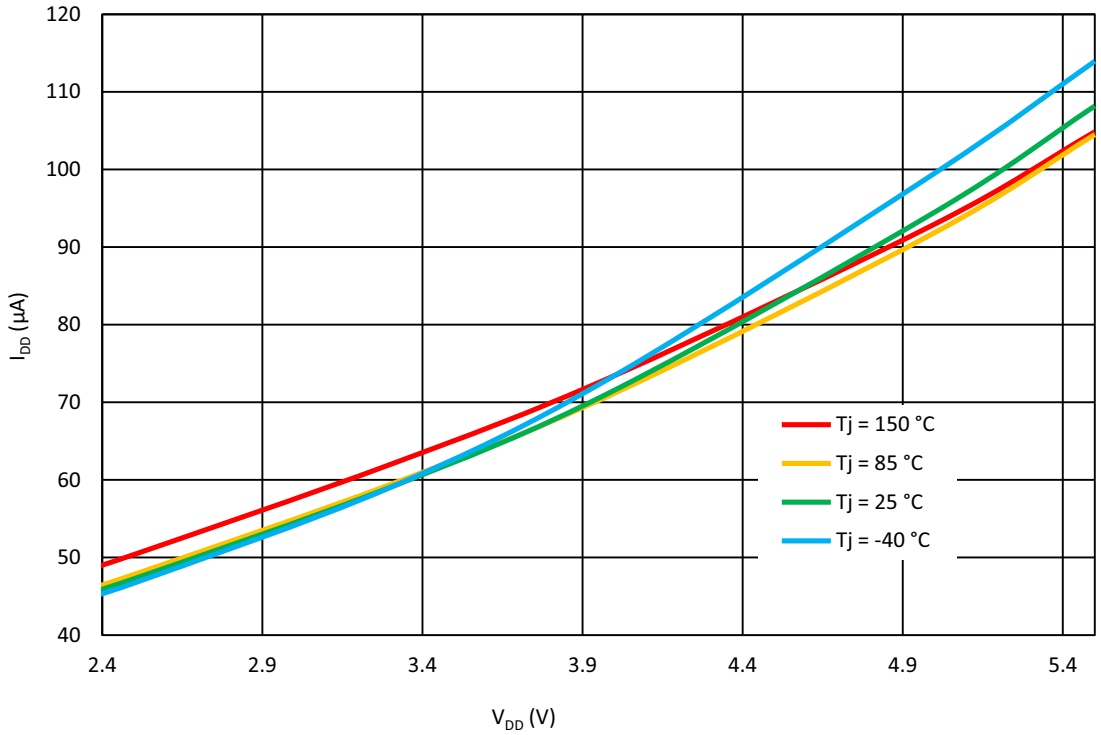


Figure 147. OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 2)

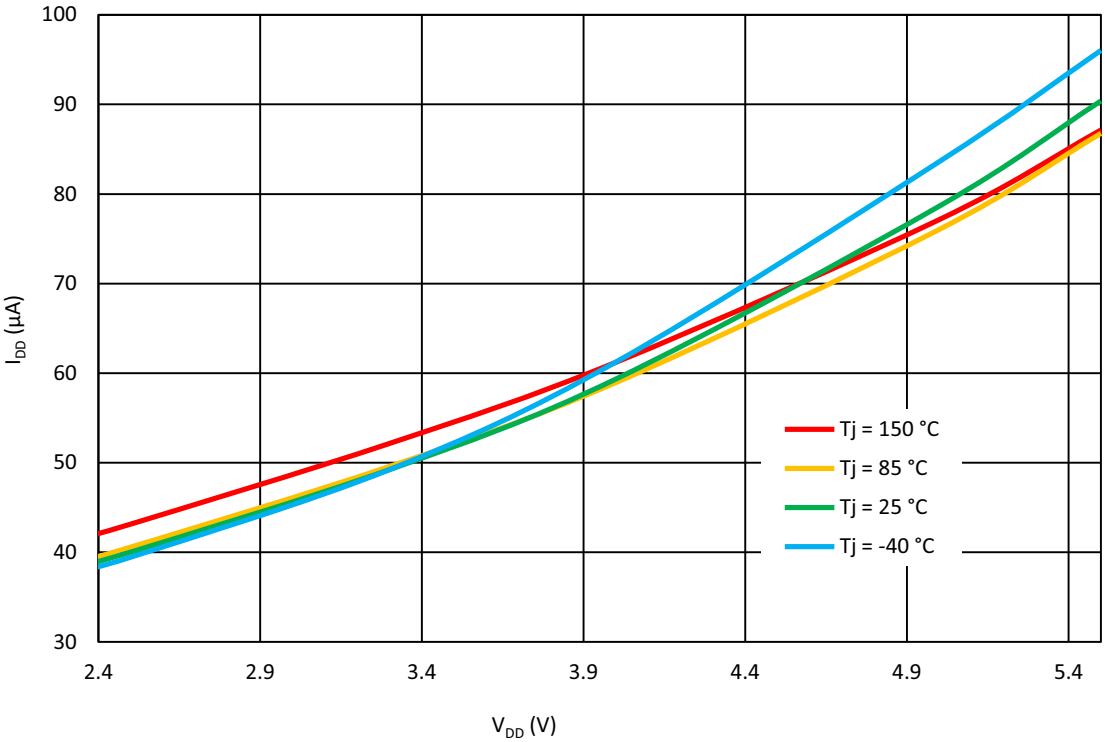


Figure 148. OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 4)

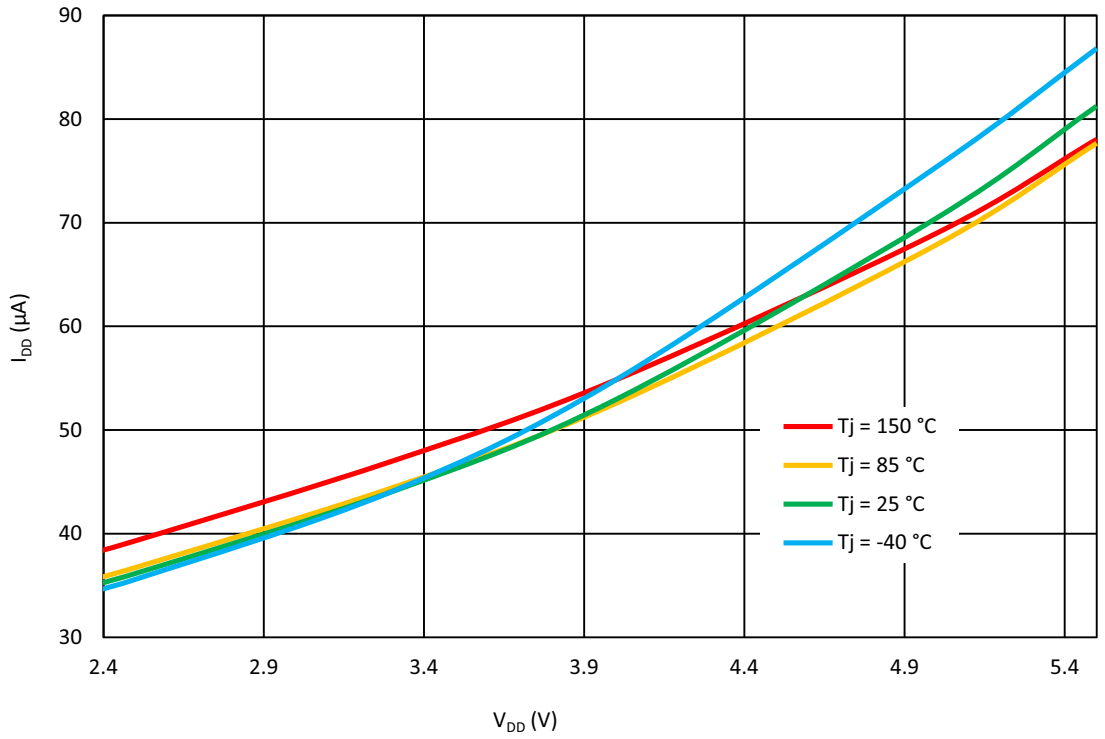


Figure 149. OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 8)

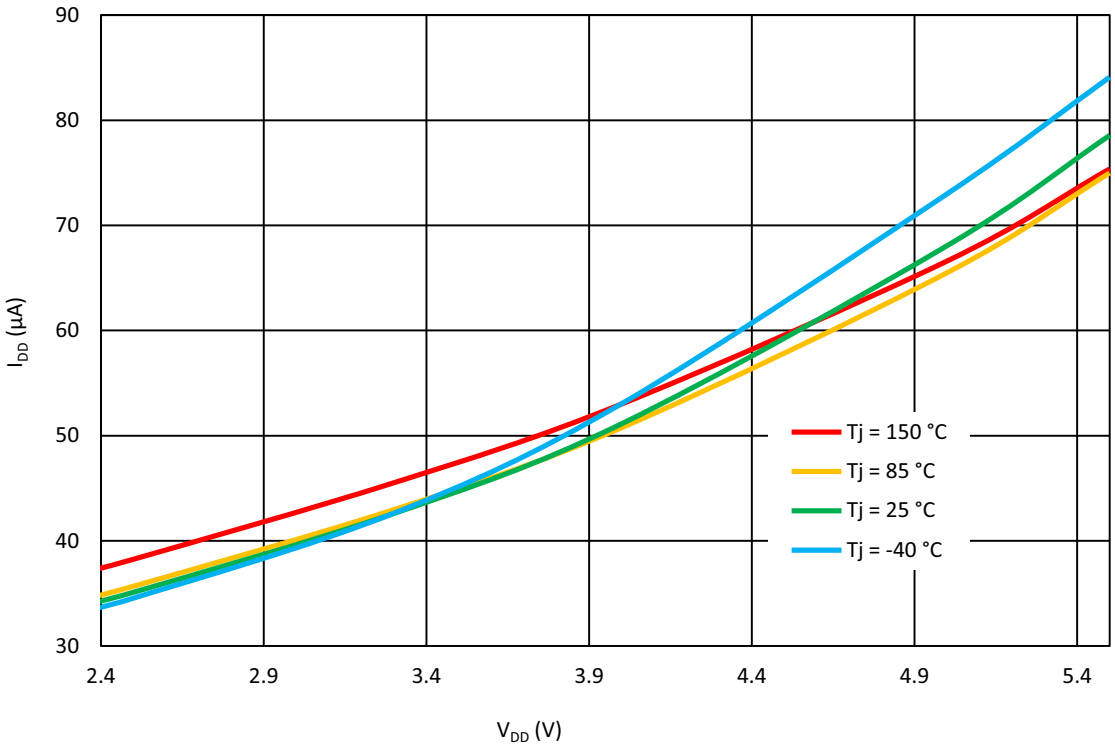


Figure 150. OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 12)

19. Low Power Bandgap

Low Power Bandgap (LP_BG) is the analog part, that is used by analog macrocells in HV PAK, such as 25 MHz OSC1, ACMPs, HV GPOs, UVLO, and others. The high efficiency low power Bangap consumes just 400 nA. However, it requires about 2 ms Start Up Time for stable functionality. For these reasons, it is recommended to keep LP_BG always on.

It is still possible to turn off the LP_BG through the connection matrix when no analog blocks are used.

Please note that OSC0 (2.048 kHz) does not use LP_BG.

20. Power-On Reset

The SLG47115 has a Power-On Reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during Power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IOs.

20.1 General Operation

The SLG47115 is guaranteed to be powered down and non-operational when the V_{DD} voltage (voltage on Pin 1) is less than Power-Off Threshold (see in Table 7), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher[Note] than the V_{DD} voltage is applied to any other Pin. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other pin is incorrect, and can lead to incorrect or unexpected device behavior.

Note: There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG47115, the voltage applied on the V_{DD} should be higher than the Power-On Threshold[Note]. The full operational V_{DD} range for the SLG47115 is 2.3 V to 5.5 V. This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power-On threshold. After the POR sequence is started, the SLG47115 will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device) and will be ready and completely operational after the POR sequence is complete.

Note: The Power-On Threshold is defined in Table 7.

To power down the chip the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down it should be less than Power-Off threshold.

All Pins are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also, as it was mentioned before the voltage on Pins can't be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

20.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 151.

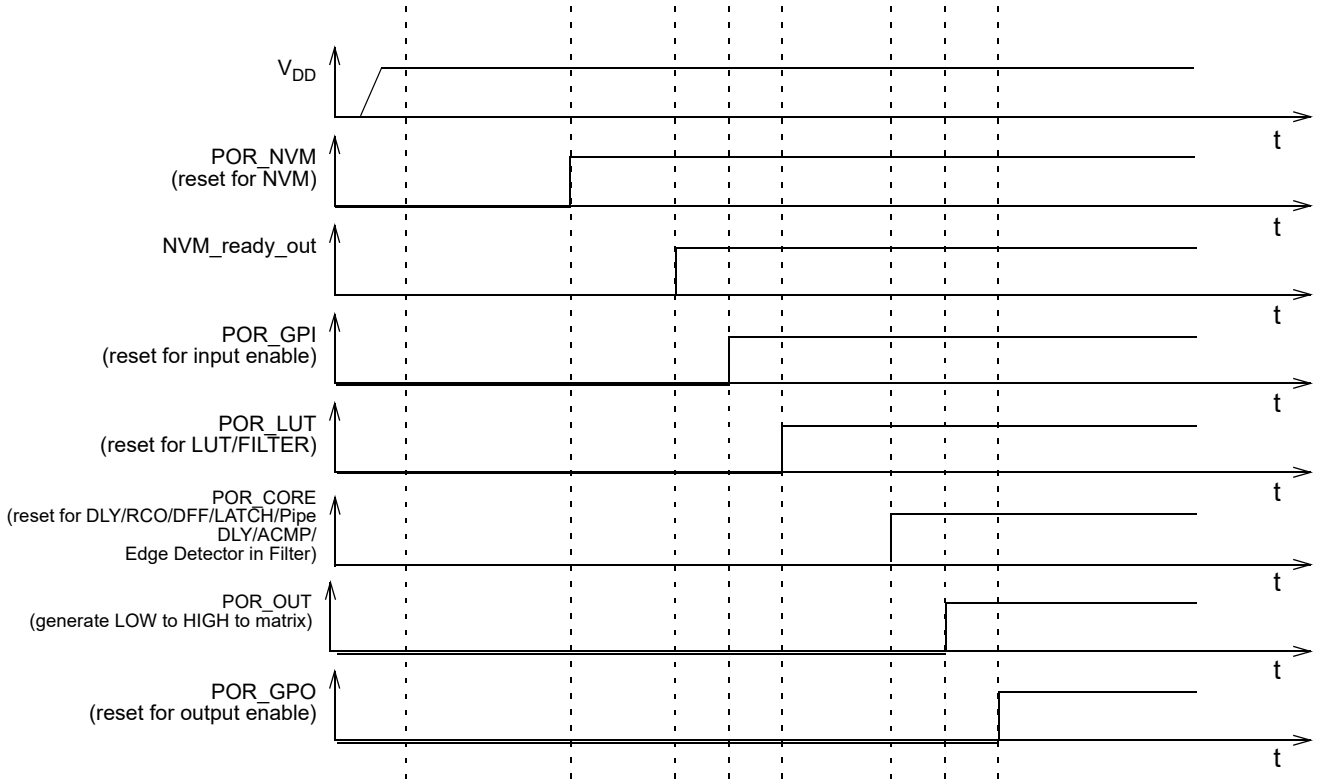


Figure 151. POR Sequence

As can be seen from Figure 151 after the V_{DD} has started ramping up and crosses the Power-On threshold, first, the on-chip NVM memory is reset. Next, the chip reads the data from NVM and transfers this information to a CMOS LATCH, that serves to configure each macrocell, and the Connection Matrix, which routes signals between macrocells. The third stage causes the reset of the input pins, and then enables them. After that, the LUTs are reset and become active. After LUTs, the Delay cells, OSCs, DFFs, LATCHES, and Pipe Delay are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output pins, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature, and even will vary from chip to chip (process influence).

20.3 Macrocells Output States during POR Sequence

To have a full picture of SLG47115 operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (Figure 152 describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output pins which are in HIGH impedance state). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P DLY macrocell configured as edge detector becomes active at this time. After that input pins are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output pins that become active and determined by the input signals.

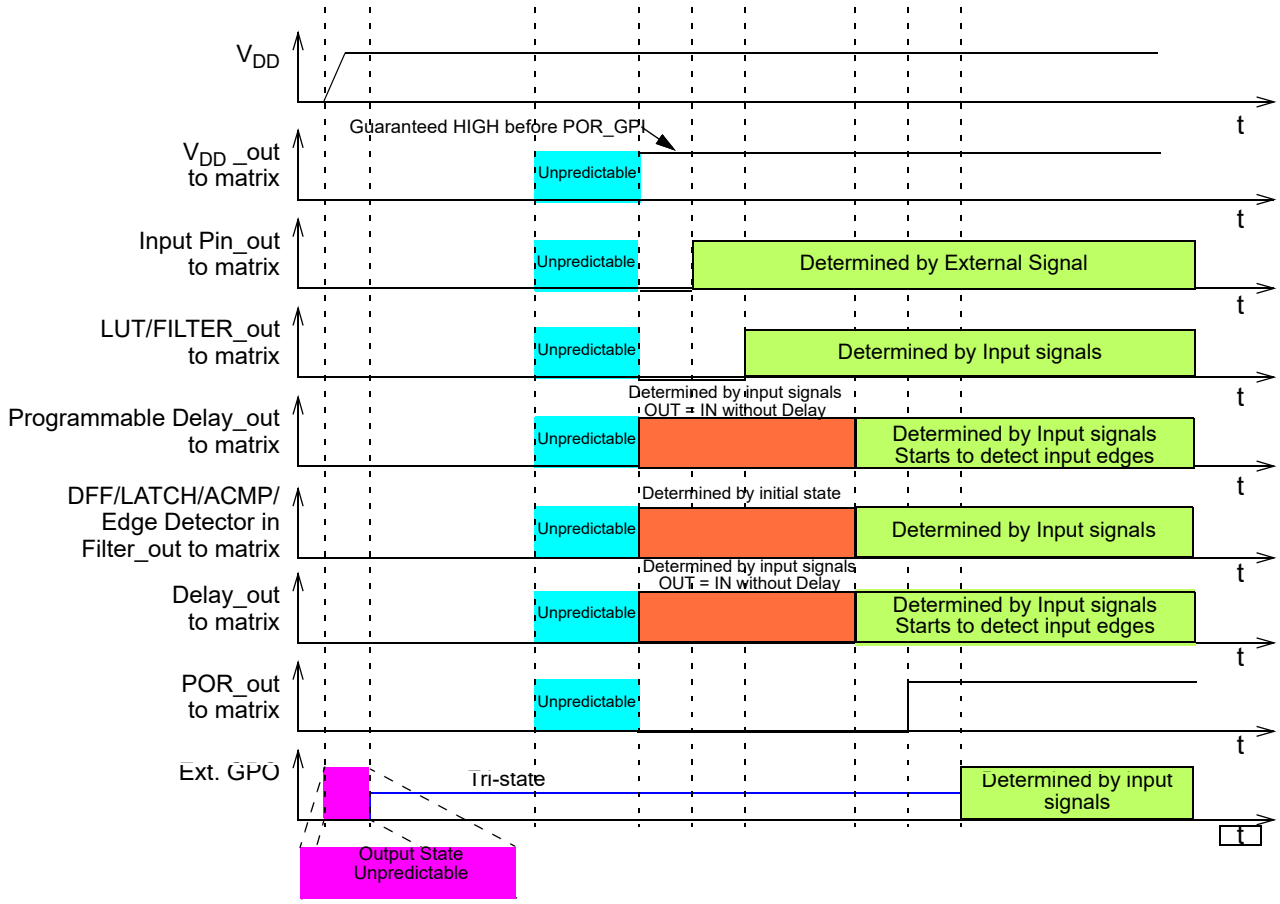


Figure 152. Internal Macrocell States during POR Sequence

20.3.1 Initialization

All internal macrocells by default have initial low level. Starting from indicated power-up time of 1.8 V to 2.2 V, macrocells in SLG47115 are powered on while forced to the reset state. All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

- Input pins, ACMP, Pull-up/down[Note].
- LUTs.
- DFFs, Delays/Counters, Pipe Delay.
- POR output to matrix.
- Output pin corresponds to the internal logic.

The Vref output pin driving signal can precede POR output signal going HIGH by 3 µs to 5 µs. The POR signal going HIGH indicates the mentioned power-up sequence is complete.

Note: The maximum voltage applied to any pin should not be higher than the V_{DD} level. There are ESD Diodes between pin → V_{DD} and pin → GND on each pin. So, if the input signal applied to pin is higher than V_{DD}, then current will sink through the diode to V_{DD}. Exceeding V_{DD} results in leakage current on the input pin, and V_{DD} will be pulled up, following the voltage on the input pin.There is no effect from input pin when input voltage is applied at the same time as V_{DD}.

20.3.2 Power-Down

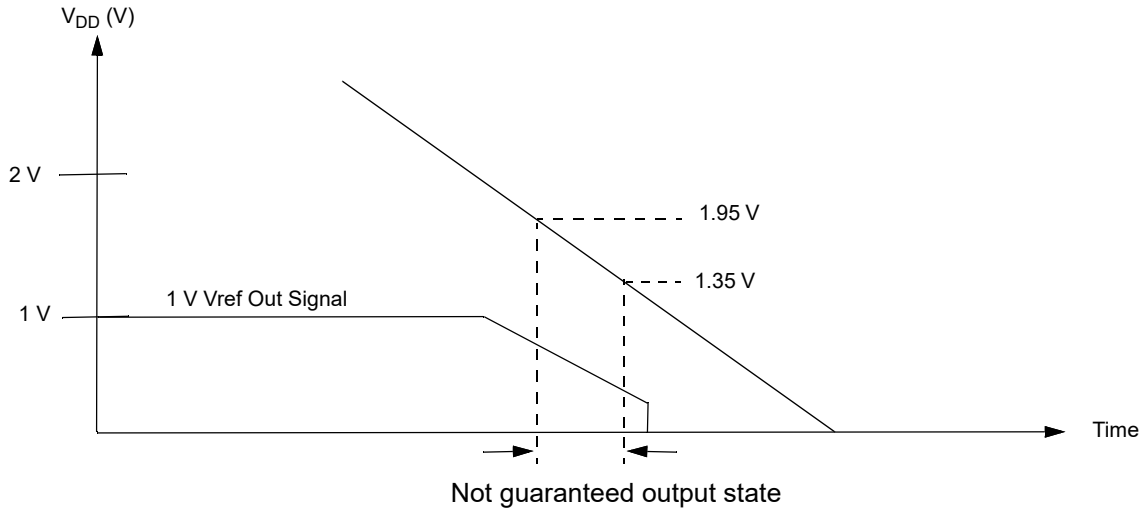


Figure 153. Power-Down

During Power-down, macrocells in SLG47115 are powered off after V_{DD} falling down below Power-Off threshold. Please note that during a slow rampdown, outputs can possibly switch state during this time.

21. I²C Serial Communications Macrocell

21.1 I²C Serial Communications Macrocell Overview

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I²C Serial Communications Macrocell in this device allows an I²C bus Master to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells and remote changes to signal chains within the device.

The I²C bus Master is also able to read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving the I²C bus Master the capability to remotely read the current value of any macrocell.

The user has the flexibility to control read access and write access via registers bits registers [1967:1965]. See Section 21.5.1 Register Read/Write Protection for more details on I²C read/write memory protection.

21.2 I²C Serial Communications Device Addressing

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 154. After the Start bit, the first four bits are a control code. Each bit in a control code can be sourced independently from the register or by value defined externally by GPI, GPIO6, GPIO4, and GPIO1. The LSB of the control code is defined by the value of GPI, while the MSB is defined by the value of GPIO1. The address source (either register bit or Pin) for each bit in the control code is defined by registers [2027:2024]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/W bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I²C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device choses to set the Control Code to either "1111" or "0000" in a system with other slave device, please consult the I²C-bus specification and user manual to understand the addressing and implementation of these special functions, to ensure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I²C Macrocell on the SLG47115 are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9, and A8) will be "0" for all commands to the SLG47115.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. Figure 154 shows this basic command structure.

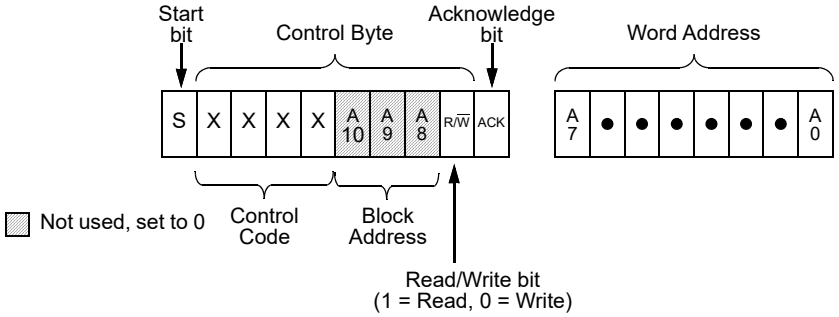


Figure 154. Basic Command Structure

21.3 I²C Serial Communications General Timing

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 155. Timing specifications can be found in the AC Characteristics section.

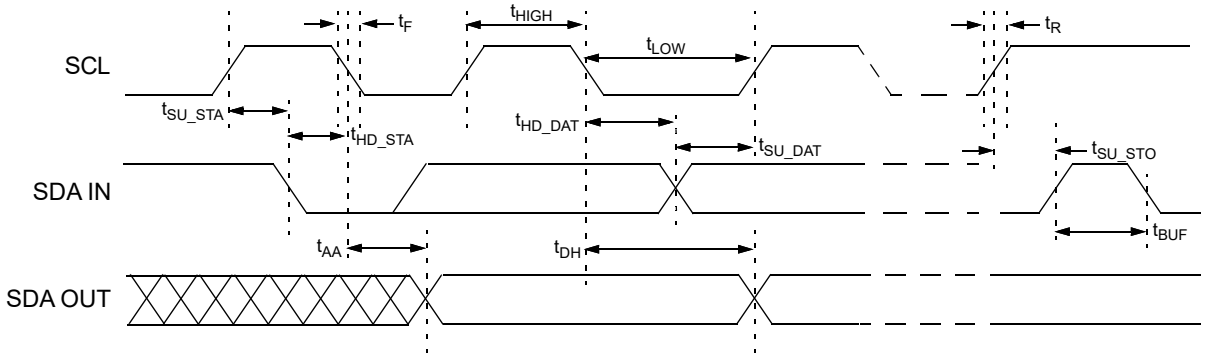


Figure 155. I²C General Timing Characteristics

21.4 I²C Serial Communications Commands

21.4.1 Byte Write Command

Following the Start condition from the Master, the Control Code [4 bits], the Block Address [3 bits], and the R/W bit (set to “0”) are placed onto the I²C bus by the Master. After the SLG47115 sends an Acknowledge bit (ACK), the next byte transmitted by the Master is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG47115, where the data byte is to be written. After the SLG47115 sends another Acknowledge bit, the Master will transmit the data byte to be written into the addressed memory location. The SLG47115 again provides an Acknowledge bit and then the Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG47115 generates the Acknowledge bit.

It is possible to latch all IOs during I²C write command, register [1971] = 1 - Enable. It means that IOs will remain their state until the write command is done.

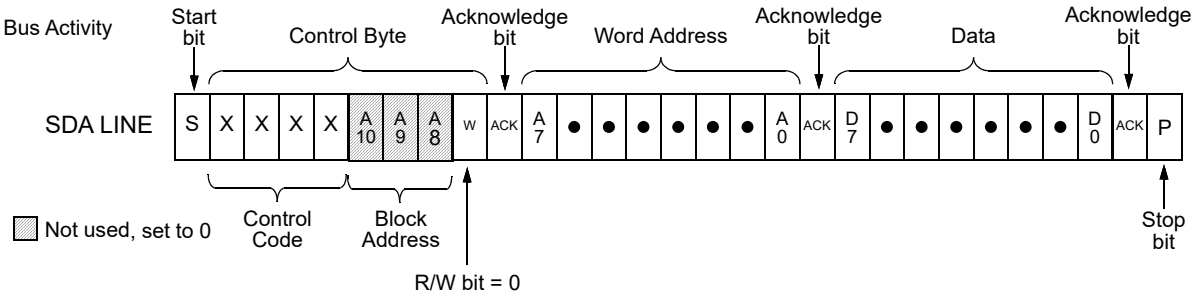


Figure 156. Byte Write Command, R/W = 0

21.4.2 Sequential Write Command

The write Control Byte, Word Address, and the first data byte are transmitted to the SLG47115 in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Bus Master continues to transmit data bytes to the SLG47115. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG47115 generates the Acknowledge bit.

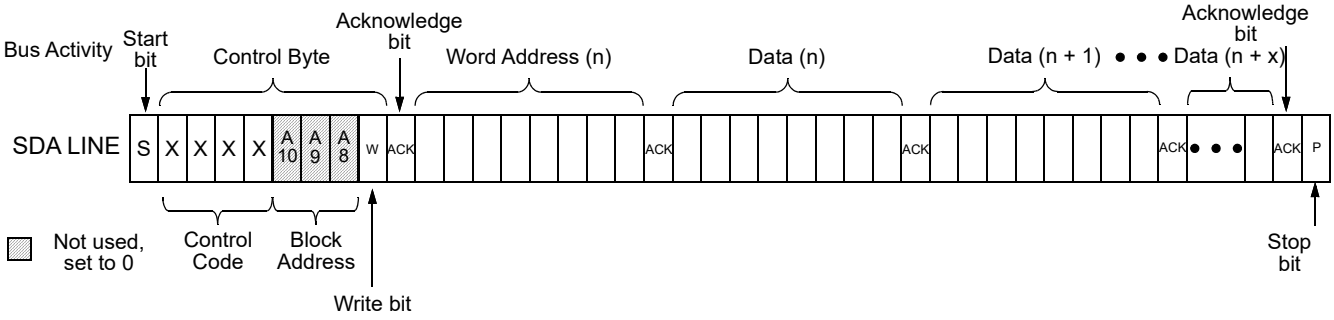


Figure 157. Sequential Write Command

21.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Sequential Read Command (which contains a write control byte) reads data up to address n, the address pointer would get incremented to n + 1 upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at n + 1. The Current Address Read Command contains the Control Byte sent by the Master, with the R/W bit = “1”. The SLG47115 will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Master will not issue an Acknowledge bit, and follow immediately with a Stop condition.

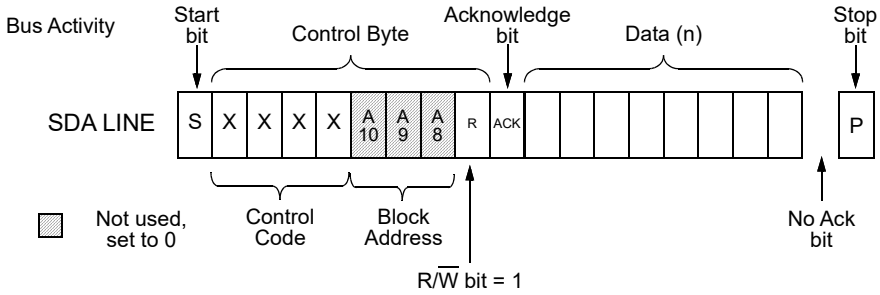


Figure 158. Current Address Read Command, R/W = 1

21.4.4 Random Read Command

The Random Read Command starts with a Control Byte (with R/W bit set to “0”, indicating a Write Command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/W bit set to “1”, after which the SLG47115 issues an Acknowledge bit, followed by the requested eight data bits.

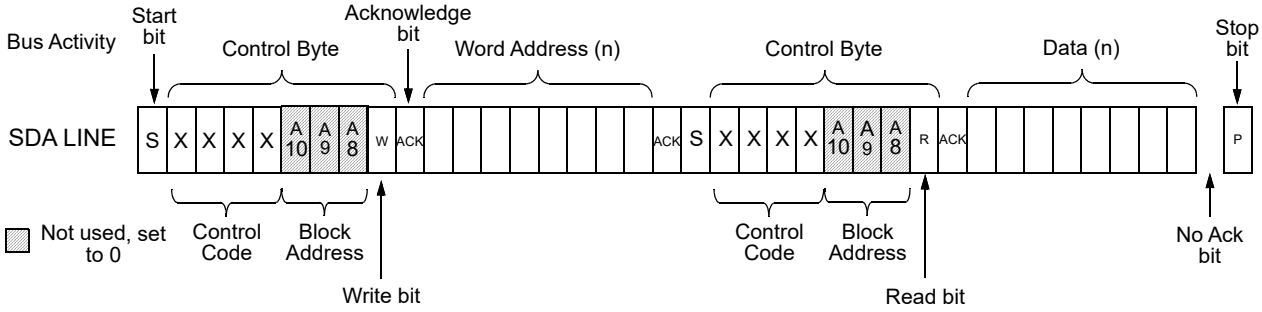


Figure 159. Random Read Command

21.4.5 Sequential Read Command

The Sequential Read Command is initiated in the same way as a Random Read Command, except that, once the SLG47115 transmits the first data byte, the Bus Master issues an Acknowledge bit as opposed to a Stop condition in a random read. The Bus Master can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

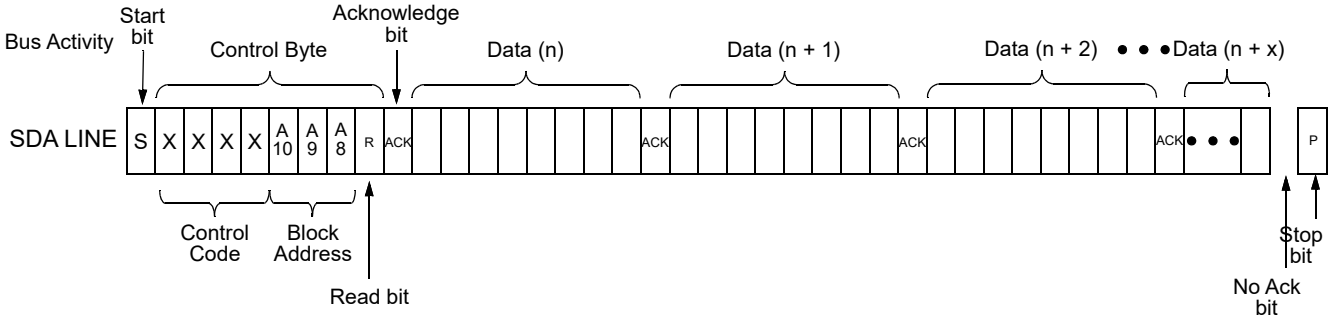


Figure 160. Sequential Read Command

21.5 I²C Serial Command Register Map

21.5.1 Register Read/Write Protection

There are seven read/write protect modes for the design sequence from being corrupted or copied. See Table 71 for details.

Table 71. Read/Write Protection Options

Configurations	Protection modes configuration							Data output from	Register address
	Unlocked	Partly Lock Read1	Partly Lock Read2	Partly Lock Read2/ Write	Lock Read	Lock Write	Lock Read/ Write		
	(Mode 0)	(Mode 1)	(Mode 2)	(Mode 3)	(Mode 4)	(Mode 5)	(Mode 6)		
I²C Byte Write Bit Masking (section 21.5.5 I2C Byte Write Bit Asking)	R/W	R/W	R/W	R/W	W	R	-	Memory	F6
I²C Serial Reset Command (section 21.5.2 I2C Serial Reset Command)	R/W	R/W	R/W	R/W	W	R	-	Memory	F5,b'0
Outputs LATCHing during I²C Write	R/W	R/W	R/W	R/W	W	R	-	Memory	F5,b'1
Connection Matrix Virtual Inputs (section 10.4 Connection Matrix Virtual Inputs)	R/W	R/W	R/W	R/W	W	R	-	Macrocell	4C
Configuration Bits for All Macrocells (IO Pins, ACMPs, Combination Function Macrocells, and others)	R/W	R/W	W	-	W	R	-	Memory	
Macrocells Inputs Configuration (Connection Matrix Outputs, section 10.3 Matrix Output Table)	R/W	W	W	-	W	R	-	Memory	0~47
Protection Mode Enable	R	R	R	R	R	R	R	Memory	F5,b'4
Protection Mode Selection	R/W	R	R	R	R	R	R	Memory	F5,b'7~5
Macrocells Output Values (Connection Matrix Inputs, section 10.2 Matrix Input Table)	R	R	R	R	-	R	-	Macrocell	48~4B; 4D~4F

Table 71. Read/Write Protection Options (Cont.)

Configurations	Protection modes configuration							Data output from	Register address
	Unlocked	Partly Lock Read1	Partly Lock Read2	Partly Lock Read2/ Write	Lock Read	Lock Write	Lock Read/ Write		
	(Mode 0)	(Mode 1)	(Mode 2)	(Mode 3)	(Mode 4)	(Mode 5)	(Mode 6)		
Counter Current Value (for 16-bit CNT)	R	R	R	R	-	R	-	Macrocell	89, 8A
Counter Current Value (for 8-bit CNT)	R	R	R	R	-	R	-	Macrocell	8B, A4, A5
I2C Control Code (section 21.2 I2C Serial Communications Device Addressing)	R	R	R	R	R	R	R	Memory	FD,b'3~0
Pin Slave Address Select	R	R	R	R	R	R	R	Memory	FD,b'7~4
I2C Disable/Enable	R	R	R	R	R	R	R	Memory	FE,b'0

R/W	Allow Read and Write Data
W	Allow Write Data Only
R	Allow Read Data Only
-	The Data is protected for Read and Write

It is possible to read some data from macrocells, such as counter current value, connection matrix, and connection matrix virtual inputs. The I2C write will not have any impact on data in case data comes from macrocell output, except Connection Matrix Virtual Inputs. The silicon identification service bits allows identifying silicon family, its revision, and others. See Section 23. Register Definitions for detailed information on all registers.

21.5.2 I2C Serial Reset Command

If I2C serial communication is established with the device, it is possible to reset the device to initial power-up conditions, including configuration of all macrocells, and all connections provided by the Connection matrix. This is implemented by setting register [1960] I2C reset bit to “1”, which causes the device to re-enable the Power-On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of register [1960] will be set to “0” automatically. Figure 161 illustrates the sequence of events for this reset function.

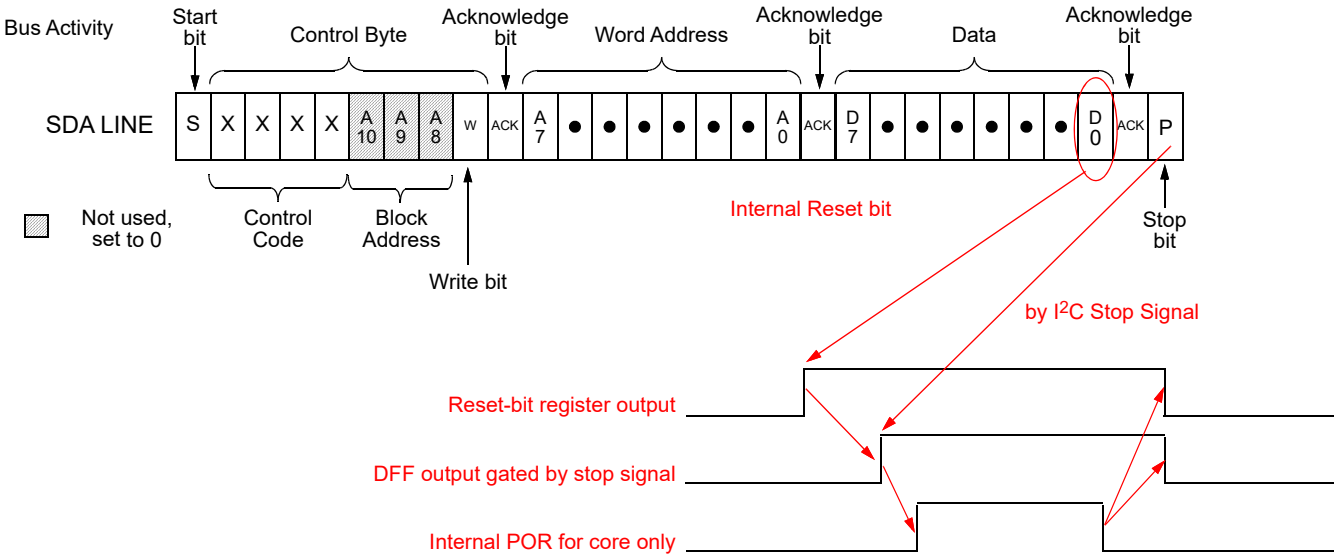


Figure 161. Reset Command Timing

21.5.3 I²C Additional Options

When output latching during I²C write, register [1961] = 1 allows all pins output value to be latched until I²C write is done. It will protect the output change due to configuration process during I²C write in case multiple register bytes are changed. Inputs and internal macrocells retain their status during I²C write.[Note]

If the user sets GPIO3 and GPIO2 function to a selection other than SDA and SCL, all access via I²C will be disabled.

Note: Any write commands that come to the device via I²C that are not blocked, based on the protection bits, will change the contents of the RAM register bits that mirror the NVM bits. These write commands will not change the NVM bits themselves, and a POR event will restore the register bits to original programmed contents of the NVM.

See Section 23. Register Definitions for detailed information on all registers.

21.5.4 Reading Current Counter Data via I²C

The current counter value in two counters in the device can be read via I²C. The counters that have this additional functionality are 16-bit CNT0 and 8-bit CNT4.

21.5.5 I²C Byte Write Bit Asking

The I²C macrocell inside SLG47115 supports masking of individual bits within a byte that is written to the RAM memory space. This function is supported across the entire RAM memory space. To implement this function, the user performs a Byte Write Command (see Section 21.4.1 Byte Write Command for details) on the I²C Byte Write Mask Register (address 0xF6) with the desired bit mask pattern. This sets a bit mask pattern for the target memory location that will take effect on the next Byte Write Command to this register byte. Any bit in the mask that is set to “1” in the I²C Byte Write Mask Register will mask the effect of changing that particular bit in the target register, during the next Byte Write Command. The contents of the I²C Byte Write Mask Register are reset (set to 00h) after valid Byte Write Command. If the next command received by the device is not a Byte Write Command, the effect of the bit masking function will be aborted, and the I²C Byte Write Mask Register will be reset with no effect. Figure 162 shows an example of this function.

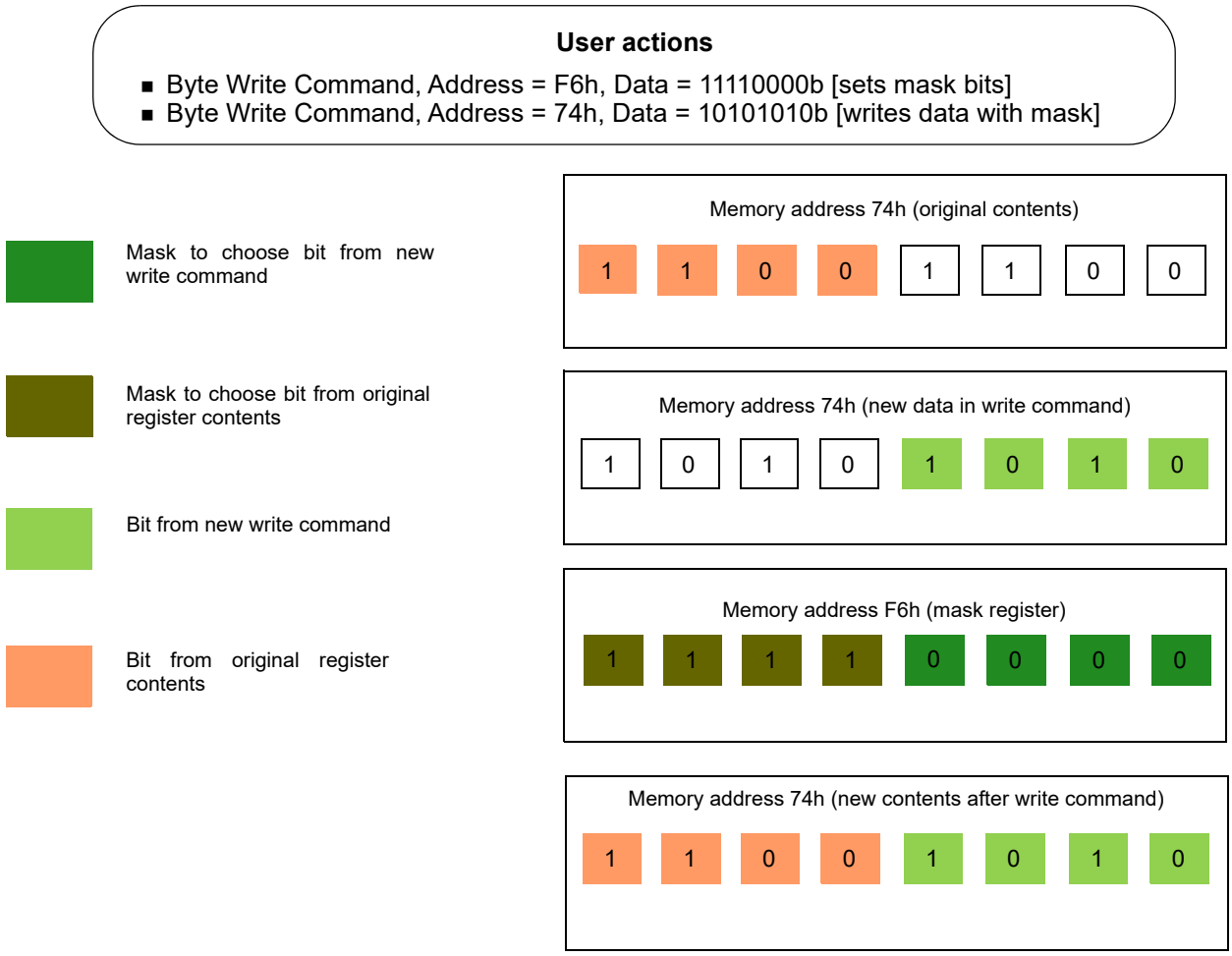


Figure 162. Example of I²C Byte Write Bit Masking

22. Analog Temperature Sensor

The SLG47115 has an Analog Temperature sensor (TS) with an output voltage linearly-proportional to the Centigrade temperature. The TS cell shares buffer with Vref1, so it is impossible to use both cells simultaneously, its output can be connected directly to the ACMP1_H positive input or to the GPIO0. For more details refer to Section 17.3 Mode Selection. The TS is rated to operate over a -40 °C to 150 °C junction temperature range. The error in the whole temperature range does not exceed ±2 %. For more details refer to Section 3.16 Analog Temperature Sensor Specifications.

The equation below calculates the typical analog voltage passed from the TS to the ACMPs' IN+ source input. It is important to note that there will be a chip to chip variation of about ±2 °C.

$$V_{TS1} = -2.4 \times T + 912.3$$

$$V_{TS2} = -2.9 \times T + 1101.3$$

where:

V_{TS1} (mV) - TS output voltage, range 1

V_{TS2} (mV) - TS output voltage, range 2

T (°C) - Temperature

Temperature hysteresis can be setup by enabling the GreenPAK's internal ACMP hysteresis.

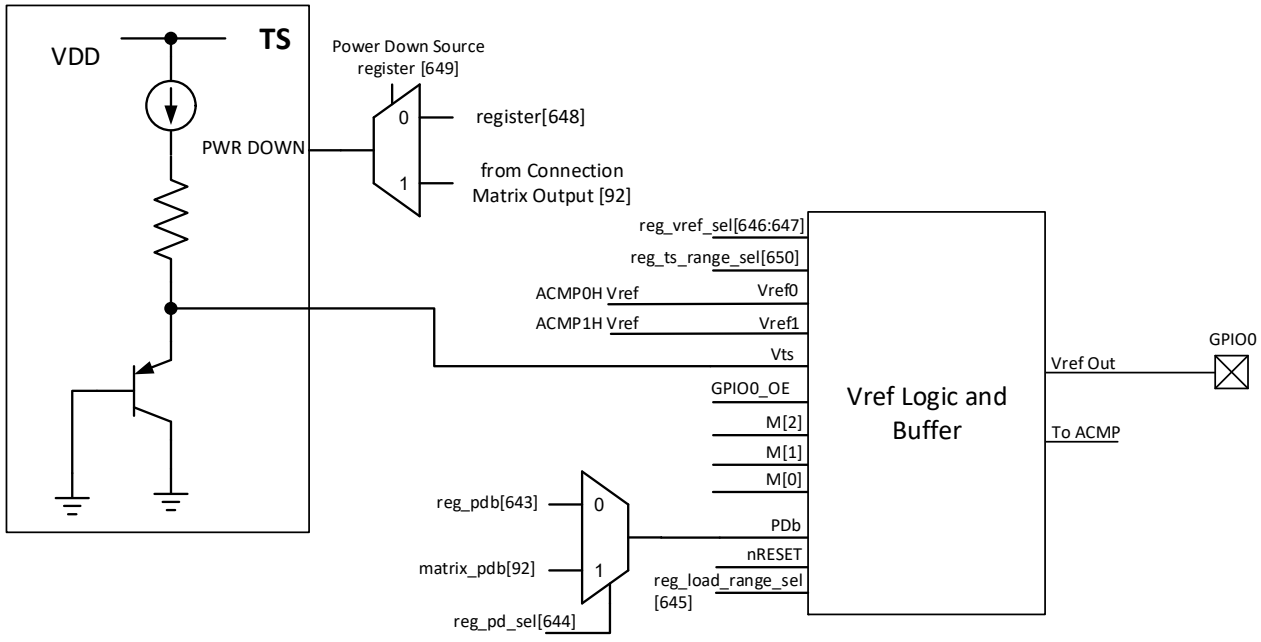


Figure 163. Analog Temperature Sensor Structure Diagram

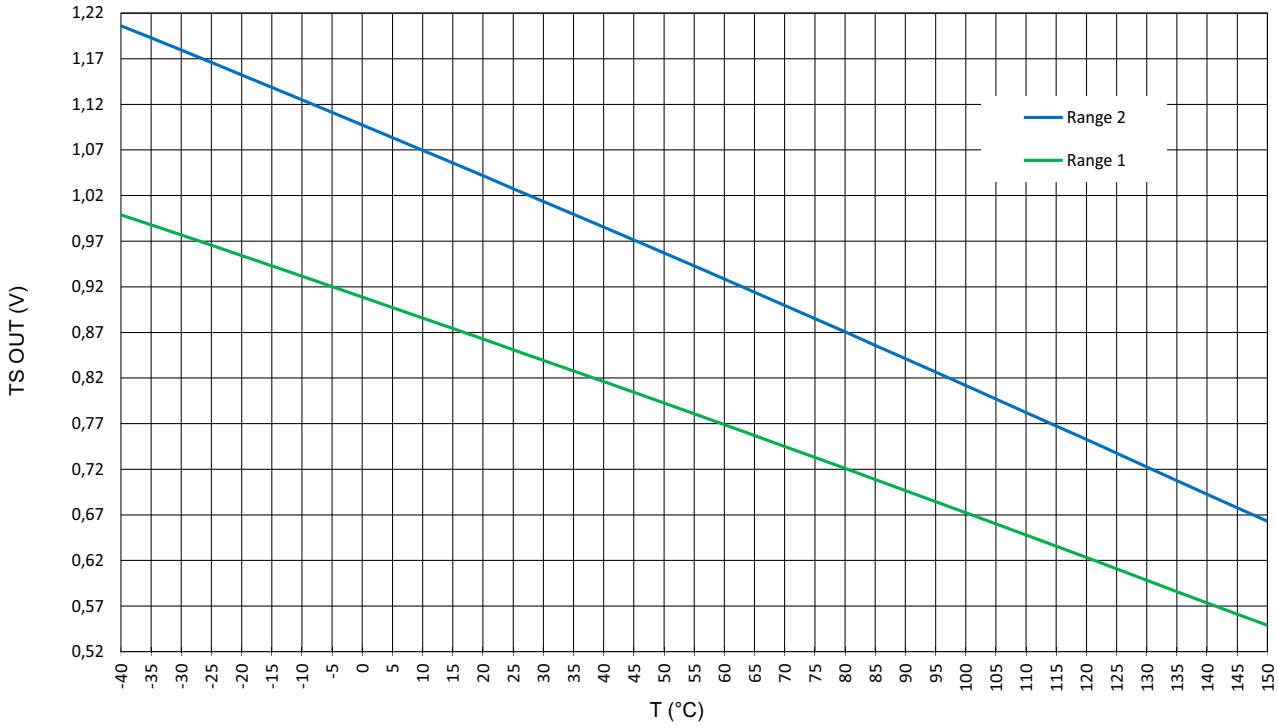


Figure 164. TS Output vs. Temperature, V_{DD} = 2.3 V to 5.5 V

23. Register Definitions

23.1 Register Map

Table 72. Register Map

Address		Signal function	Register Bit definition
Byte	Register Bit		
Matrix Output			
0	5:0	Matrix OUT0	GPIO0 Digital Output
0	11:6	Matrix OUT1	GPIO0 Digital Output OE
1			
1	17:12	Matrix OUT2	GPIO1 Digital Output
2			
2	23:18	Matrix OUT3	GPIO1 Digital Output OE
3	29:24	Matrix OUT4	GPIO2 Digital Output
3	35:30	Matrix OUT5	GPIO3 Digital Output
4			
4	41:36	Matrix OUT6	GPIO4 Digital Output
5			
5	47:42	Matrix OUT7	GPIO4 Digital Output OE
6	53:48	Matrix OUT8	GPIO5 Digital Output
6	59:54	Matrix OUT9	GPIO5 Digital Output OE
7			
7	65:60	Matrix OUT10	GPIO6 Digital Output
8			
8	71:66	Matrix OUT11	GPIO6 Digital Output OE
9	77:72	Matrix OUT12	HV GPO0 Digital Output
9	83:78	Matrix OUT13	HV GPO0 Digital Output OE
A			
A	89:84	Matrix OUT14	Unused
B			
B	95:90	Matrix OUT15	Unused
C	101:96	Matrix OUT16	HV GPO1 Digital Output
C	107:102	Matrix OUT17	HV GPO1 Digital Output OE
D			
D	113:108	Matrix OUT18	Unused
E			
E	119:114	Matrix OUT19	Unused
F	125:120	Matrix OUT20	Reserved

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
F	131:126	Matrix OUT21	Reserved
10			
10	137:132	Matrix OUT22	Reserved
11			
11	143:138	Matrix OUT23	HV GPO0 SLEEP or Power-up Current Sense Comparator
12	149:144	Matrix OUT24	Unused
12	155:150	Matrix OUT25	HV GPO1 SLEEP or Power-up Current Sense Comparator
13			
13	161:156	Matrix OUT26	Unused
14			
14	167:162	Matrix OUT27	IN0 of LUT2_0 or clock input of DFF0
15	173:168	Matrix OUT28	IN1 of LUT2_0 or data input of DFF0
15	179:174	Matrix OUT29	IN0 of LUT2_3 or clock input of PGen
16			
16	185:180	Matrix OUT30	IN1 of LUT2_3 or nRST of PGen
17			
17	191:186	Matrix OUT31	IN0 of LUT2_1 or clock input of DFF1
18	197:192	Matrix OUT32	IN1 of LUT2_1 or data input of DFF1
18	203:198	Matrix OUT33	IN0 of LUT2_2 or clock input of DFF2
19			
19	209:204	Matrix OUT34	IN1 of LUT2_2 or data input of DFF2
1A			
1A	215:210	Matrix OUT35	IN0 of LUT3_0 or clock input of DFF3
1B	221:216	Matrix OUT36	IN1 of LUT3_0 or data input of DFF3
1B	227:222	Matrix OUT37	IN2 of LUT3_0 or nRST(nSET) of DFF3
1C			
1C	233:228	Matrix OUT38	IN0 of LUT3_1 or clock input of DFF4 or Blanking of Chopper0
1D			
1D	239:234	Matrix OUT39	IN1 of LUT3_1 or data input of DFF4 or Chop of Chopper0
1E	245:240	Matrix OUT40	IN2 of LUT3_1 or nRST(nSET) of DFF4 of PWM of Chopper0
1E	251:246	Matrix OUT41	IN0 of LUT3_2 or clock input of DFF5 or Blanking of Chopper1
1F			

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
1F 20	257:252	Matrix OUT42	IN1 of LUT3_2 or data input of DFF5 or Chop of Chopper1
20	263:258	Matrix OUT43	IN2 of LUT3_2 or nRST(nSET) of DFF5 of PWM of Chopper1
21	269:264	Matrix OUT44	IN0 of LUT3_3 or clock input of DFF6
21 22	275:270	Matrix OUT45	IN1 of LUT3_3 or data input of DFF6
22 23	281:276	Matrix OUT46	IN2 of LUT3_3 or nRST(nSET) of DFF6
23	287:282	Matrix OUT47	IN0 of LUT3_4 or clock input of DFF7
24	293:288	Matrix OUT48	IN1 of LUT3_4 or data input of DFF7
24 25	299:294	Matrix OUT49	IN2 of LUT3_4 or nRST(nSET) of DFF7
25 26	305:300	Matrix OUT50	IN0 of LUT3_5 or clock input of DFF8
26	311:306	Matrix OUT51	IN1 of LUT3_5 or data input of DFF8
27	317:312	Matrix OUT52	IN2 of LUT3_5 or nRST(nSET) of DFF8
27 28	323:318	Matrix OUT53	IN0 of LUT3_6 or input of Pipe Delay or UP signal of RIPP CNT
28 29	329:324	Matrix OUT54	IN1 of LUT3_6 or nRST of Pipe Delay or nSET of RIPP CNT
29	335:330	Matrix OUT55	IN2 of LUT3_6 or clock of Pipe Delay/RIPP_CNT
2A	341:336	Matrix OUT56	IN0 of LUT4_0 or clock input of DFF9
2A 2B	347:342	Matrix OUT57	IN1 of LUT4_0 or data input of DFF9
2B 2C	353:348	Matrix OUT58	IN2 of LUT4_0 or nRST(nSET) of DFF9
2C	359:354	Matrix OUT59	IN3 of LUT4_0
2D	365:360	Matrix OUT60	MULTFUNC_8BIT_1: IN0 of LUT3_7 or clock input of DFF10; Delay1 Input (or Counter1 nRST input)
2D 2E	371:366	Matrix OUT61	MULTFUNC_8BIT_1: IN1 of LUT3_7 or nRST (nSET) of DFF10; Delay1 input (or Counter1 nRST Input) or Delay/Counter1 External Clock Source
2E 2F	377:372	Matrix OUT62	MULTFUNC_8BIT_1: IN2 of LUT3_7 or data input of DFF10; Delay1 input (or Counter1 nRST Input)

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
2F	383:378	Matrix OUT63	MULTFUNC_8BIT_2: IN0 of LUT3_8 or clock input of DFF11; Delay2 input (or Counter2 nRST Input)
30	389:384	Matrix OUT64	MULTFUNC_8BIT_2: IN1 of LUT3_8 or nRST (nSET) of DFF11; Delay2 input (or Counter2 nRST Input) or Delay/Counter2 External Clock Source
30	395:390	Matrix OUT65	MULTFUNC_8BIT_2: IN2 of LUT3_8 or data input of DFF11; Delay2 input (or Counter2 nRST input)
31			
31	401:396	Matrix OUT66	MULTFUNC_8BIT_3: IN0 of LUT3_9 or clock input of DFF12; Delay3 input (or Counter3 nRST input)
32	407:402	Matrix OUT67	MULTFUNC_8BIT_3: IN1 of LUT3_9 or nRST (nSET) of DFF12; Delay3 input (or Counter3 nRST input) or Delay/Counter3 External Clock Source
33	413:408	Matrix OUT68	MULTFUNC_8BIT_3: IN2 of LUT3_9 or data input of DFF12; Delay3 Input (or Counter3 nRST Input)
33	419:414	Matrix OUT69	MULTFUNC_8BIT_4: IN0 of LUT3_10 or clock input of DFF13; Delay4 Input (or Counter4 nRST Input)
34			
34	425:420	Matrix OUT70	MULTFUNC_8BIT_4: IN1 of LUT3_10 or nRST (nSET) of DFF13; Delay4 Input (or Counter4 nRST Input) or Delay/Counter4 External Clock Source
35			
35	431:426	Matrix OUT71	MULTFUNC_8BIT_4: IN2 of LUT3_10 or data input of DFF13; Delay4 Input (or Counter4 nRST Input)
36	437:432	Matrix OUT72	MULTFUNC_16BIT_0: IN0 of LUT4_1 or clock input of DFF14; Delay0 Input (or Counter0 RST/SET Input)
36	443:438	Matrix OUT73	MULTFUNC_16BIT_0: IN1 of LUT4_1 or nRST of DFF14; Delay0 Input (or Counter0 nRST Input) or Delay/Counter0 External Clock Source
37			
37	449:444	Matrix OUT74	MULTFUNC_16BIT_0: IN2 of LUT4_1 or nSET of DFF14 or KEEP Input of FSM0 or External clock input of Delay0 (or Counter0)
38			
38	455:450	Matrix OUT75	MULTFUNC_16BIT_0: IN3 of LUT4_1 or data input of DFF14; Delay0 Input (or Counter0 nRST Input) or UP Input of FSM0
39	461:456	Matrix OUT76	PWM0_UP/DOWN
39	467:462	Matrix OUT77	PWM0_KEEP/STOP
3A			

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
3A 3B	473:468	Matrix OUT78	PWM0_DUTY_CYCLE_CNT
3B	479:474	Matrix OUT79	PWM0_EXT_CLK
3C	485:480	Matrix OUT80	PWM0_Power-down
3C 3D	491:486	Matrix OUT81	PWM1_UP/DOWN
3D 3E	497:492	Matrix OUT82	PWM1_KEEP/STOP
3E	503:498	Matrix OUT83	PWM1_ DUTY_CYCLE_CNT
3F	509:504	Matrix OUT84	PWM1_EXT_CLK
3F 40	515:510	Matrix OUT85	PWM1_Power-down
40 41	521:516	Matrix OUT86	nPD of ACMP0H from the matrix
41	527:522	Matrix OUT87	nPD of ACMP1H from the matrix
42	533:528	Matrix OUT88	Filter/Edge detect input
42 43	539:534	Matrix OUT89	Programmable delay/edge detect input
43 44	545:540	Matrix OUT90	OSC0 Enable from matrix
44	551:546	Matrix OUT91	OSC1 Enable from matrix
45	557:552	Matrix OUT92	Vref Output and Temp sensor nPD from matrix
45 46	563:558	Matrix OUT93	BG Power-down from the matrix
46 47	569:564	Matrix OUT94	Diff_Amp_Integrator_En
47	575:570	Matrix OUT95	Reserved
Matrix Input			

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
48	576	Matrix Input 0	GND
	577	Matrix Input 1	LUT2_0/DFF0 output
	578	Matrix Input 2	LUT2_1/DFF1 output
	579	Matrix Input 3	LUT2_2/DFF2 output
	580	Matrix Input 4	LUT2_3/PGen output
	581	Matrix Input 5	LUT3_0/DFF3 output
	582	Matrix Input 6	LUT3_1/DFF4/Chopper0 output
	583	Matrix Input 7	LUT3_2/DFF5/Chopper1 output
49	584	Matrix Input 8	LUT3_3/DFF6 output
	585	Matrix Input 9	LUT3_4/DFF7 output
	586	Matrix Input 10	LUT3_5/DFF8 output
	587	Matrix Input 11	LUT4_0/DFF9 output
	588	Matrix Input 12	LUT3_6/PD/RIPP CNT output0
	589	Matrix Input 13	LUT3_6/PD/RIPP CNT output1
	590	Matrix Input 14	LUT3_6/PD/RIPP CNT output2
	591	Matrix Input 15	PROG_DLY_EDET_OUT
4A	592	Matrix Input 16	MULTFUNC_8BIT_1: DLY_CNT_OUT
	593	Matrix Input 17	MULTFUNC_8BIT_2: DLY_CNT_OUT
	594	Matrix Input 18	MULTFUNC_8BIT_3: DLY_CNT_OUT
	595	Matrix Input 19	MULTFUNC_8BIT_4: DLY_CNT_OUT
	596	Matrix Input 20	MULTFUNC_8BIT_1: LUT3_DFF_OUT
	597	Matrix Input 21	MULTFUNC_8BIT_2: LUT3_DFF_OUT
	598	Matrix Input 22	MULTFUNC_8BIT_3: LUT3_DFF_OUT
	599	Matrix Input 23	MULTFUNC_8BIT_4: LUT3_DFF_OUT
4B	600	Matrix Input 24	MULTFUNC_16BIT_0: DLY_CNT_OUT
	601	Matrix Input 25	MULTFUNC_16BIT_0: LUT4_DFF_OUT
	602	Matrix Input 26	GPIO0 Digital Input
	603	Matrix Input 27	GPI Digital Input
	604	Matrix Input 28	GPIO1 Digital Input
	605	Matrix Input 29	GPIO4 Digital Input
	606	Matrix Input 30	GPIO5 Digital Input
	607	Matrix Input 31	GPIO6 Digital Input

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
4C	608	Matrix Input 32	GPIO2 digital input or I^2C_virtual_0 Input
	609	Matrix Input 33	GPIO3 digital input or I^2C_virtual_1 Input
	610	Matrix Input 34	I^2C_virtual_2 Input
	611	Matrix Input 35	I^2C_virtual_3 Input
	612	Matrix Input 36	I^2C_virtual_4 Input
	613	Matrix Input 37	I^2C_virtual_5 Input
	614	Matrix Input 38	I^2C_virtual_6 Input
	615	Matrix Input 39	I^2C_virtual_7 Input
4D	616	Matrix Input 40	PWM0_OUT+
	617	Matrix Input 41	PWM0_OUT-
	618	Matrix Input 42	PWM1_OUT+
	619	Matrix Input 43	PWM1_OUT-
	620	Matrix Input 44	Diff. Amp +Integrator UPWARD
	621	Matrix Input 45	Diff. Amp +Integrator EQUAL
	622	Matrix Input 46	ACMP0H_OUT
	623	Matrix Input 47	ACMP1H_OUT
4E	624	Matrix Input 48	CurrentSenseComp_OUT
	625	Matrix Input 49	tieL
	626	Matrix Input 50	Fault
	627	Matrix Input 51	tieL
	628	Matrix Input 52	EDET_FILTER_OUT
	629	Matrix Input 53	Oscillator1(Ring_osc) output
	630	Matrix Input 54	Flex-Divider output
	631	Matrix Input 55	Oscillator0(LF_OSC) output 0
4F	632	Matrix Input 56	Oscillator0(LF_OSC) output 1
	633	Matrix Input 57	POR OUT
	634	Matrix Input 58	PWM0_PERIOD
	635	Matrix Input 59	PWM1_PERIOD
	636	Matrix Input 60	OCP_FAULT
	637	Matrix Input 61	tieL
	638	Matrix Input 62	TSD_FAULT
	639	Matrix Input 63	V_{DD}

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
ACMP Vref			
50	642:640	Vref OUT (to GPIO0) mode selection	1. With registers [756:755] ≠ 11 or GPIO0 OE = 1: 000: Analog Power-down 001: Analog Power-down 010: Vref_OUT to ACMP only by analog buffer 011: Vref_OUT to ACMP only by analog buffer 100: Analog Power-down 101: Vts_OUT to ACMP only by analog buffer 110: Vts_OUT to ACMP only by analog buffer 111: Analog Power-down. 2. With registers [756:755] = 11 and GPIO0 OE = 0: 000: Analog Power-down; 001: Vref_OUT to GPIO0 only by analog buffer 010: Vref_OUT to ACMP only by analog buffer 011: Vref_OUT to GPIO0 and ACMP by analog buffer 100: Vts_OUT to GPIO0 only by analog buffer 101: Vts_OUT to ACMP only by analog buffer 110: Vts_OUT to GPIO0 and ACMP by analog buffer 111: Vref_OUT to GPIO0 bypass analog buffer
	643	Vref OUT (to GPIO0) register Power-On/Off	1: On 0: Off
	644	Vref OUT (to GPIO0) Power-down selection	0: Come from register [643] 1: Come from Matrix OUT 92
	645	Vref OUT Buffer sink current selection	0: 2 uA 1: 12 uA
	646:647	Vref OUT (to GPIO0) input selection	00: None; 01: ACMP0_H Vref, 10: ACMP1_H Vref; 11: Temp sensor
51	648	Temp sensor register Power-down control	0: Power-down 1: Power-On
	649	Temp sensor register Power-down select	0: Come from register [648] 1: Come Matrix OUT 92
	650	Temp sensor range select	0: 0.62V ~ 0.99V (TYP), 1: 0.75V ~ 1.2V (TYP)
	652:651	ACMP0_H hysteresis	00: 0 mV 01: 32 mV 10: 64 mV 11: 192 mV
	653	Reserved	
	654	Reserved	
	655	ACMP0_H input tie to V_{DD} enable	0: Disable 1: Enable

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
52	656	ACMP1_H input come from Temp sensor output enable	0: Disable 1: Enable
	657	ACMP1_H positive input come from ACMP0_H's input mux output enable	0: Disable 1: Enable
	658	Reserved	
	659	Reserved	
	661:660	ACMP1_H hysteresis	00: 0 mV 01: 32 mV 10: 64 mV 11: 192 mV
	663:662	Reserved	
53	669:664	Integrator Vref select	Integrator Vref select: 000000: 32 mV ~ 111110: 2.016 V step = 32 mV 111111: External Vref
	671:670	Reserved	
54	672	ACMP0_H Wake/sleep enable	0: Disable 1: Enable
	673	ACMP1_H Wake/sleep enable	0: Disable 1: Enable
	674	ACMP wake/sleep time selection	0: Short time 1: Normal w/s
	675	Reserved	
	676	Reserved	
	679:677	Reserved	
55	681:680	ACMP0_H Gain divider select	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
	687:682	ACMP0_H Vref select	000000: 32 mV ~ 111110: 2.016 V/ step = 32 mV; 111111: External Vref
56	689:688	ACMP1_H Gain divider select	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
	695:690	ACMP1_H Vref select	000000: 32 mV ~ 111110: 2.016 V/ step = 32 mV; 111111: External Vref

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
57	701:696	Current Sense Vref select	000000: 32 mV ~ 111110: 2.016 V/ step = 32 mV; 111111: External Vref
	702	Current Sense Vref registers [5:0] source selection	0: Select static from current sense Vref registers [701:696] 1: Select dynamic from PWM0
	703	Reserved	
58	709:704	Reserved	
	710	Reserved	
	711	Reserved	
OSC1 (25 MHz)			
59	712	Turn on by register	When matrix output enable/PD control signal = 0: 0: Auto on by delay cells 1: Always on
	713	Matrix Power-down/on select	0: Matrix down 1: Matrix on
	716:714	Pre-divider ratio control	000: div 1 001: div 2 010: div 4 011: div 8 100: div 12
	719:717	Second stage divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
5A	720	External clock source enable	0: Internal OSC1 1: External clock from GPIO4
	721	Matrix OUT enable	0: Disable 1: Enable
	722	Startup delay with 100ns	0: Enable 1: Disable
OSC0 (2.048 kHz)			

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	**Register Bit**		
5A	723	Turn on by register	When matrix output enable/pd control signal = 0: 0: Auto on by delay cells 1: Always on
	724	Matrix Power-down/on select	0: Matrix down 1: Matrix on
	725	External clock source enable	0: Internal OSC0 1: External clock from GPIO1
	726	Matrix OUT enable	0: Disable 1: Enable
	727	Reserved	
5B	729:728	Pre-divider ratio control	00: div 1 01: div 2 10: div 4 11: div 8
	732:730	Second stage divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
	735:733	Reserved	
OSC0 second Output control			
5C	738:736	Matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
	739	Second output to matrix enable	0: Disable 1: Enable
OSC1 matrix OUT enable for flexible divider			
5C	740	OSC1 Matrix OUT enable for flexible divider	0: Disable 1: Enable
	741	OSC1 Enable for flexible divider	0: Disable 1: Enable
	743:742	Reserved	
Flexible divider for OSC1			
5D	751:744	Flexible divider for OSC1 (8-b counter)	Data[7:0] Equation: divider number = Data[7:0] + 1 (exclude Data[7:0] = 0000 0000)
HV_GPO_HD Common			

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	**Register Bit**		
5E	752	Reserved	
	753	Differential amplifier with integrator output duty cycle vs input duty cycle of Full Bridge drivers: invert_UPWARD	0: IN → OUT 1: IN → nOUT
IO Common			
5E	754	IO fast Pull-up/down enable at V_{DD} start	0: Disable 1: Enable
GPIO0			
5E	756:755	Input mode configuration	00: Digital without Schmitt trigger 01: Digital with Schmitt trigger 10: Low voltage digital in 11: Analog IO
	758:757	Output mode configuration	00: push-pull 1x 01: push-pull 2x 10: open-drain 1x 11: open-drain 2x
5E	760:759	Pull-up/down resistance selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
5F			
5F	761	Pull-up/down selection	0: Pull-down 1: Pull-up
	762	Reserved	
GPI			
5F	764:763	Input mode configuration	00: Digital without Schmitt trigger 01: Digital with Schmitt trigger 10: Low voltage digital in 11: Analog IO
	766:765	Pull-up/down resistance selection	00: Floating 01: 10 k 10: 100 k 11: 1 M.
	767	Pull-up/down selection	0: Pull-down 1: Pull-up
Reserved			
60	775:768	Reserved	
HV_GPO0_HD			

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
61	777:776	Output mode configuration	00: Hi-Z 01: NMOS open-drain Low-side on 10: NMOS High-side on 11: NMOS High-side and Low-side on
	780:778	Control delay of OCP0 retry	000: Delay 492 us 001: Delay 656 us 010: Delay 824 us 011: Delay 988 us 100: Delay 1152 us 101: Delay 1316 us 110: Delay 1480 us 111: Delay 1640 us
	781	HV_GPO0/HV_GPO1 slew rate control	0: Slow slew rate for motor driver 1: Fast slew rate for pre-driver mode
	782	HV_GPO0/HV_GPO1 Full Bridge/Half Bridge mode select	0: Half Bridge mode 1: Full Bridge.
	783	Reserved	
HV_GPO1_HD			
62	785:784	Output mode configuration	00: Hi-Z 01: NMOS open-drain Low-side on 10: NMOS High-side on 11: NMOS High-side and Low-side on
	788:786	Control delay of OCP1 retry	000: Delay 492 us 001: Delay 656 us 010: Delay 824 us 011: Delay 988 us 100: Delay 1152 us 101: Delay 1316 us 110: Delay 1480 us 111: Delay 1640 us
62	789	Reserved	
	790	Reserved	
	791	Reserved	
63	792	Reserved	
	793	Reserved	
	794	Reserved	
	795	Reserved	
	796	Reserved	
	797	Reserved	
	798	Reserved	
	799	Reserved	

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
64	800	Reserved	
	801	Reserved	
	802	OCP current limit 0	0: Enable, 1: disable
	803	OCP current limit 1	0: Enable, 1: disable
	804	Reserved	
	805	Integrator divide ratio	0: Divide by 8 (V_{DD2} > 12 V) 1: Divide by 4 (V_{DD2} <= 12 V)
	807:806	Connect integrator to outputs selection	00: Disconnects integrator from outputs when outputs in tri-state 01: Integrator always connects to outputs 10: Integrator always disconnect from outputs 11: No change state
65	808	Reserved	
	809	Reserved	
	810	Reserved	
	811	Reserved	
	812	Reserved	
	813	Reserved	
	814	Reserved	
	815	Reserved	

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
GPIO1 (LED)			
66	817:816	Input mode configuration	00: Digital without Schmitt trigger 01: Digital with Schmitt trigger 10: Low voltage digital in 11: Analog IO
	819:818	Output mode configuration	00: Push-pull 1x 01: Push-pull 2x 10: Open-drain 1x 11: Open-drain 2x
	821:820	Pull-up/down resistance selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
	822	Pull-up/down selection	0: Pull-down 1: Pull-up
	823	Reserved	
67	824	Reserved	
GPIO2/SCL			
67	826:825	Input mode configuration	00: Digital without Schmitt trigger 01: Digital with Schmitt trigger 10: Low voltage digital in 11: Reserved
	828:827	Pull-up/down resistance selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
	829	Pull-up/down selection	0: Pull-down 1: Pull-up
	830	I^2C mode selection (only GPIO3 SDA)	0: I^2C Fast Mode + 1: I^2C Standard/Fast Mode.
	831	Open-drain output enable (3.2x drivability)	0: Disable 1: Enable (3.2x)
GPIO3/SDA			
68	833:832	Input mode configuration	00: Digital without Schmitt trigger 01: Digital with Schmitt trigger 10: Low voltage digital in 11: Reserved
	835:834	Pull-up/down resistance selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
	836	Pull-up/down selection	0: Pull-down 1: Pull-up
	837	Open-drain output enable (3.2x drivability)	0: Disable 1: Enable (3.2x)
	838	Reserved	

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
68	839	Reserved	
GPIO4			
69	841:840	Input mode configuration	00: Digital without Schmitt trigger 01: Digital with Schmitt trigger 10: Low voltage digital in 11: Analog IO
	843:842	Output mode configuration	00: push-pull 1x 01: push-pull 2x 10: Open-drain 1x 11: Open-drain 2x
	845:844	Pull-up/down resistance selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
	846	Pull-up/down selection	0: Pull-down 1: Pull-up
	847	Reserved	
GPIO5 (LED)			
6A	849:848	Input mode configuration	00: Digital without Schmitt trigger 01: Digital with Schmitt trigger 10: Low voltage digital in 11: Analog IO
	851:850	Output mode configuration	00: Push-pull 1x 01: Push-pull 2x 10: Open-drain 1x 11: Open-drain 2x
	853:852	Pull-up/down resistance selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
	854	Pull-up/down selection	0: Pull-down 1: Pull-up
	855	Reserved	
GPIO6			
6B	857:856	Input mode configuration	00: Digital without Schmitt trigger 01: Digital with Schmitt trigger 10: Low voltage digital in 11: Analog IO
	859:858	Output mode configuration	00: push-pull 1x 01: push-pull 2x 10: Open-Drain 1x 11: Open-Drain 2x
	861:860	Pull-up/down selection	00: Floating 01: 10 k 10: 100 k 11: 1 M

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	**Register Bit**		
6B	862	Pull-up/down selection	0: Pull-down 1: Pull-up
	863	Reserved	
6C	864	V_{DD2} UVLO0 register enable/disable	0: Disable 1: Enable
	865	Reserved	
	866	Current sense amplifier gain selection	0: x8 1: x4
	867	Current sense comparator output polarity	0: OUT 1: Inverted OUT
	868	Reserved	
	869	Reserved	
	870	Current sense register enable/disable	0: Disable 1: Enable
	871	Reserved	
6D	872	Reserved	
Mode control for HV GPO0/1			
6D	873	OCP deglitch time enable for HV GPO0/1	0: Without deglitch time 1: With deglitch time
	874	Control selection for HV_GPO0/1	0: IN-IN mode 1: PH-EN mode
	875	Reserved	
	876	Reserved	
	877	Reserved	
Reserved			
6D	879:878	Reserved	
6E	887:880	Reserved	
6F	895:888	Reserved	

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
Multifunction0 (LUT4_DFF)			
70	902:896	Single 4-bit LUT	0000000: Matrix A - In3 Matrix B - In2 Matrix C - In1 Matrix D - In0 DLY_IN - LOW
		Single DFF nRST and SET	0010000: Matrix A - D Matrix B - nSET Matrix C - nRST Matrix D - CLK DLY_IN - LOW
		Single CNT/DLY	0000001: Matrix A - UP (CNT) Matrix B - KEEP (CNT) Matrix C - EXT_CLK (CNT) Matrix D - DLY_IN (CNT) DLY_OUT connected to LUT/DFF
		CNT/DLY → LUT	0000010: Matrix A - DLY_IN Matrix B - In2 Matrix C - In1 Matrix D - In0 DLY_OUT connected to In3
		CNT/DLY → DFF	0010010: Matrix A - DLY_IN Matrix B - nSET Matrix C - nRST Matrix D - CLK DLY_OUT connected to D

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
70	902:896	CNT/DLY → LUT	0100010: Matrix A - DLY_IN Matrix B - EXT_CLK (CNT) Matrix C - In1 Matrix D - In0 DLY_OUT connected to In3, In2 tied LOW
		CNT/DLY → DFF	0110010: Matrix A - DLY_IN Matrix B - EXT_CLK (CNT) Matrix C - nRST Matrix D - CLK DLY_OUT connected to D, nSET tied HIGH
		CNT/DLY → LUT	1000010: Matrix A - DLY_IN Matrix B - In2 Matrix C - EXT_CLK (CNT) Matrix D - In0 DLY_OUT connected to In3, In1 tied LOW
		CNT/DLY → DFF	1010010: Matrix A - DLY_IN Matrix B - nSET Matrix C - EXT_CLK (CNT) Matrix D - CLK DLY_OUT connected to D, nRST tied HIGH
		CNT/DLY → LUT	0000110: Matrix A - In3 Matrix B - DLY_IN Matrix C - In1 Matrix D - In0 DLY_OUT connected to In2

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
70	902:896	CNT/DLY → DFF	0010110: Matrix A - D Matrix B - DLY_IN Matrix C - nRST Matrix D - CLK DLY_OUT connected to nSET
		CNT/DLY → LUT	1000110: Matrix A - In3 Matrix B - DLY_IN Matrix C - EXT_CLK (CNT) Matrix D - In0 DLY_OUT connected to In2, In1 tied LOW
		CNT/DLY → DFF	1010110: Matrix A - D Matrix B - DLY_IN Matrix C - EXT_CLK (CNT) Matrix D - CLK DLY_OUT connected to nSET, nRST tied HIGH
		CNT/DLY → LUT	0001010: Matrix A - In3 Matrix B - In2 Matrix C - DLY_IN Matrix D - In0 DLY_OUT connected to In1
		CNT/DLY → DFF	0011010: Matrix A - D Matrix B - nSET Matrix C - DLY_IN Matrix D - CLK DLY_OUT connected to nRST
		CNT/DLY → LUT	0101010: Matrix A - In3 Matrix B - EXT_CLK (CNT) Matrix C - DLY_IN Matrix D - In0 DLY_OUT connected to In1, In2 tied LOW
		CNT/DLY → DFF	0111010: Matrix A - D Matrix B - EXT_CLK (CNT) Matrix C - DLY_IN Matrix D - CLK DLY_OUT connected to nRST, nSET tied HIGH

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
70	902:896	CNT/DLY → LUT	0001110: Matrix A - In3 Matrix B - In2 Matrix C - In1 Matrix D - DLY_IN DLY_OUT connected to In0
		CNT/DLY → DFF	0011110: Matrix A - D Matrix B - nSET Matrix C - nRST Matrix D - DLY_IN DLY_OUT connected to CLK
		CNT/DLY → LUT	0101110: Matrix A - In3 Matrix B - EXT_CLK (CNT) Matrix C - In1 Matrix D - DLY_IN DLY_OUT connected to In0, In2 tied LOW
		CNT/DLY → DFF	0111110: Matrix A - D Matrix B - EXT_CLK (CNT) Matrix C - nRST Matrix D - DLY_IN DLY_OUT connected to CLK, nSET tied HIGH
		CNT/DLY → LUT	1001110: Matrix A - In3 Matrix B - In2 Matrix C - EXT_CLK (CNT) Matrix D - DLY_IN DLY_OUT connected to In0, In1 tied LOW
		CNT/DLY → DFF	1011110: Matrix A - D Matrix B - nSET Matrix C - EXT_CLK (CNT) Matrix D - DLY_IN DLY_OUT connected to CLK, nRST tied HIGH
		LUT → CNT/DLY	0000011: Matrix A - In3 Matrix B - In2 Matrix C - In1 Matrix D - In0 LUT_OUT connected to DLY_IN

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
70	902:896	DFF → CNT/DLY	0010011: Matrix A - D Matrix B - nSET Matrix C - nRST Matrix D - CLK DFF_OUT connected to DLY_IN
		LUT → CNT/DLY	0100011: Matrix A - In3 Matrix B - EXT_CLK (CNT) Matrix C - In1 Matrix D - In0 LUT_OUT connected to DLY_IN, In2 tied LOW
		DFF → CNT/DLY	0110011: Matrix A - D Matrix B - EXT_CLK (CNT) Matrix C - nRST Matrix D - CLK DFF_OUT connected to DLY_IN, nSET tied LOW
		LUT → CNT/DLY	1000011: Matrix A - In3 Matrix B - In2 Matrix C - EXT_CLK (CNT) Matrix D - In0 LUT_OUT connected to DLY_IN, In1 tied LOW
		DFF → CNT/DLY	1010011: Matrix A - D Matrix B - nSET Matrix C - EXT_CLK (CNT) Matrix D - CLK DFF_OUT connected to DLY_IN, nRST tied HIGH
70	904:903	DLY/CNT0 Mode Selection	00: DLY 01: One Shoot 10: Frequency Detection 11: CNT register [912] = 0
71			

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
71	906:905	DLY/CNT0 Edge Mode Selection	00: Both edge 01: Falling edge 10: Rising edge; 11: HIGH Level Reset (only in CNT mode)
	910:907	DLY/CNT0 Clock Source Select	Clock source sel[3:0] 0000: 25 MHz(OSC1) 0001: 25 MHz/4 0010: Not used 0011: Not used 0100: Not used 0101: Not used 0110: 2.048 kHz(OSC0) 0111: 2.048 kHz/8 1000: 2.048 kHz/64 1001: 2.048 kHz/512 1010: 2.048 kHz/4096 1011: 2.048 kHz/32768 1100: 2.048 kHz/262144 1101: CNT4_END 1110: External 1111: Not used
	911	FSM0 SET/RST Selection	0: Reset to 0 1: Set to data
72	912	CNT0 DLY EDET FUNCTION Selection	0: Normal 1: DLY function edge detection (registers [904:903] = 00)
	913	UP signal SYNC selection	0: Bypass 1: After two DFF
	914	Keep signal SYNC selection	0: Bypass 1: After two DFF
	916:915	CNT0 initial value selection	00: Bypass the initial 01: Initial 0 10: Initial 1 11: Initial 1
	917	Wake/sleep Power-down state selection	0: LOW 1: HIGH
	918	Wake/sleep mode selection	0: Default Mode 1: Wake/Sleep Mode (registers [904:903] = 11)
	919	CNT0 output polarity selection	0: Default Output 1: Inverted Output
73	920	CNT0 CNT mode SYNC selection	0: Bypass 1: After two DFF
Multifunction1			

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
73	925:921	Single 3-bit LUT	00000: Matrix A - In2 Matrix B - In1 Matrix C - In0 DLY_IN - LOW
		Single DFF with nRST/nSET	10000: Matrix A - D Matrix B - nSET/nRST Matrix C - CLK DLY_IN - LOW
		Single CNT/DLY	00001: Matrix A - DLY_IN (CNT) Matrix B - EXT_CLK (CNT) Matrix C - NC DLY_OUT connected to LUT/DFF
		CNT/DLY → LUT	00010: Matrix A - DLY_IN Matrix B - In1 Matrix C - In0 DLY_OUT connected to In2
		CNT/DLY → DFF	10010: Matrix A - DLY_IN Matrix B - nSET/nRST Matrix C - CLK DLY_OUT connected to D
		CNT/DLY → LUT	00110: Matrix A - In2 Matrix B - DLY_IN Matrix C - In0 DLY_OUT connected to In1
		CNT/DLY → DFF	10110: Matrix A - D Matrix B - DLY_IN Matrix C - CLK DLY_OUT connected to nSET/nRST
		CNT/DLY → LUT	01010: Matrix A - In2 Matrix B - In1 Matrix C - DLY_IN DLY_OUT connected to In0

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
73	925:921	CNT/DLY → DFF	11010: Matrix A - D Matrix B - nSET/nRST Matrix C - DLY_IN DLY_OUT connected to CLK
		LUT → CNT/DLY	00011: Matrix A - In2 Matrix B - In1 Matrix C - In0 LUT_OUT connected to DLY_IN
		DFF → CNT/DLY	10011: Matrix A - D Matrix B - nSET/nRST Matrix C - CLK DLY_OUT connected to DLY_IN
73	929:926	CNT1 function and edge mode selection	0000: Both edge Delay 0001: Falling edge delay 0010: Rising edge delay 0011: Both edge One Shot 0100: Falling edge One Shot 0101: Rising edge One Shot 0110: Both edge freq detect 0111: Falling edge freq. detect 1000: Rising edge freq. detect 1001: Both edge detect 1010: Falling edge detect 1011: Rising edge detect 1100: Both edge reset CNT 1101: Falling edge reset CNT 1110: Rising edge reset CNT 1111: HIGH level reset CNT
74			
74	931:930	CNT1 initial value selection	00: Bypass the initial 01: Initial 0 10: Initial 1 11: Initial 1
74	935:932	DLY/CNT1 Clock Source Select	Clock source sel[3:0] 0000: 25 MHz(OSC1) 0001: 25 MHz/4 0010: Not used 0011: Not used 0100: Not used 0101: Not used 0110: 2.048 kHz(OSC0) 0111: 2.048 kHz/8 1000: 2.048 kHz/64 1001: 2.048 kHz/512 1010: 2.048 kHz/4096 1011: 2.048 kHz/32768 1100: 2.048 kHz/262144 1101: CNT0_END 1110: External 1111: Not used

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	**Register Bit**		
75	936	CNT1 output polarity selection	0: Default Output 1: Inverted Output
	937	CNT1 CNT mode SYNC selection	0: Bypass 1: After two DFF
	938	CNT1 DLY EDET FUNCTION Selection	0: Normal 1: DLY function edge detection (registers [929:926] = 0000/0001/0010)
Multifunction2			
75	943:939	Single 3-bit LUT	00000: Matrix A - In2 Matrix B - In1 Matrix C - In0 DLY_IN - LOW
		Single DFF w RST and SET	10000: Matrix A - D Matrix B - nSET/nRST Matrix C - CLK DLY_IN - LOW
		Single CNT/DLY	00001: Matrix A - DLY_IN (CNT) Matrix B - EXT_CLK (CNT) Matrix C - NC DLY_OUT connected to LUT/DFF
		CNT/DLY → LUT	00010: Matrix A - DLY_IN Matrix B - In1 Matrix C - In0 DLY_OUT connected to In2

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
75	943:939	CNT/DLY → DFF	10010: Matrix A - DLY_IN Matrix B - nSET/nRST Matrix C - CLK DLY_OUT connected to D
		CNT/DLY → LUT	00110: Matrix A - In2 Matrix B - DLY_IN Matrix C - In0 DLY_OUT connected to In1
		CNT/DLY → DFF	10110: Matrix A - D Matrix B - DLY_IN Matrix C - CLK DLY_OUT connected to nSET/nRST
		CNT/DLY → LUT	01010: Matrix A - In2 Matrix B - In1 Matrix C - DLY_IN DLY_OUT connected to In0
		CNT/DLY → DFF	11010: Matrix A - D Matrix B - nSET/nRST Matrix C - DLY_IN DLY_OUT connected to CLK
		LUT → CNT/DLY	00011: Matrix A - In2 Matrix B - In1 Matrix C - In0 LUT_OUT connected to DLY_IN
		DFF → CNT/DLY	10011: Matrix A - D Matrix B - nSET/nRST Matrix C - CLK DFF_OUT connected to DLY_IN
76	945:944	CNT2 initial value selection	00: Bypass the initial 01: Initial 0 10: Initial 1 11: Initial 1

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
76	949:946	CNT2 function and edge mode selection	0000: Both edge Delay 0001: Falling edge delay 0010: Rising edge delay 0011: Both edge One Shot 0100: Falling edge One Shot 0101: Rising edge One Shot 0110: Both edge freq detect 0111: Falling edge freq detect 1000: Rising edge freq detect 1001: Both edge detect 1010: Falling edge detect 1011: Rising edge detect 1100: Both edge reset CNT 1101: Falling edge reset CNT 1110: Rising edge reset CNT 1111: HIGH level reset CNT
76 77	953:950	DLY/CNT2 Clock Source Select	Clock source sel[3:0] 0000: 25 MHz(OSC1) 0001: 25 MHz/4 0010: Not used 0011: Not used 0100: Not used 0101: Not used 0110: 2.048 kHz(OSC0) 0111: 2.048 kHz/8 1000: 2.048 kHz/64 1001: 2.048 kHz/512 1010: 2.048 kHz/4096 1011: 2.048 kHz/32768 1100: 2.048 kHz/262144 1101: CNT1_END 1110: External 1111: Not used
	954	CNT2 output polarity selection	0: Default Output 1: Inverted Output
	955	CNT2 CNT mode SYNC selection	0: Bypass 1: After two DFF
	956	CNT2 DLY EDET Function Selection	0: Normal 1: DLY function edge detection (registers [949:946] = 0000/0001/0010)
Multifunction3			
77	958:957	CNT3 initial value selection	00: Bypass the initial 01: Initial 0 10: Initial 1 11: Initial 1
	959	Multi3 register configurartion	Refer table in register [967:964]

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
78	963:960	CNT3 function and edge mode selection	0000: Both edge Delay 0001: Falling edge delay 0010: Rising edge delay 0011: Both edge One Shot 0100: Falling edge One Shot 0101: Rising edge One Shot 0110: Both edge freq detect 0111: Falling edge freq detect 1000: Rising edge freq detect 1001: Both edge detect 1010: Falling edge detect 1011: Rising edge detect 1100: Both edge reset CNT 1101: Falling edge reset CNT 1110: Rising edge reset CNT 1111: HIGH level reset CNT
78	959 967:964	Single 3-bit LUT	00000: Matrix A - In2 Matrix B - In1 Matrix C - In0 DLY_IN - LOW
		Single DFF w RST and SET	10000: Matrix A - D Matrix B - nSET/nRST Matrix C - CLK DLY_IN - LOW
		Single CNT/DLY	00100: Matrix A - DLY_IN (CNT) Matrix B - EXT_CLK (CNT) Matrix C - NC DLY_OUT connected to LUT/DFF
		CNT/DLY → LUT	01000: Matrix A - DLY_IN Matrix B - In1 Matrix C - In0 DLY_OUT connected to In2
		CNT/DLY → DFF	11000: Matrix A - DLY_IN Matrix B - nSET/nRST Matrix C - CLK DLY_OUT connected to D

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
78	959 967:964	CNT/DLY → LUT	01001: Matrix A - In2 Matrix B - DLY_IN Matrix C - In0 DLY_OUT connected to In1
		CNT/DLY → DFF	11001: Matrix A - D Matrix B - DLY_IN Matrix C - CLK DLY_OUT connected to nSET/nRST
		CNT/DLY → LUT	01010: Matrix A - In2 Matrix B - In1 Matrix C - DLY_IN DLY_OUT connected to In0
		CNT/DLY → DFF	11010: Matrix A - D Matrix B - nSET/nRST Matrix C - DLY_IN DLY_OUT connected to CLK
		LUT → CNT/DLY	01100: Matrix A - In2 Matrix B - In1 Matrix C - In0 LUT_OUT connected to DLY_IN
		DFF → CNT/DLY	11100: Matrix A - D Matrix B - nSET/nRST Matrix C - CLK (DFF_OUT connected to DLY_IN)

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
79	971:968	DLY/CNT3 Clock Source Select	Clock source sel[3:0] 0000: 25 MHz(OSC1) 0001: 25 MHz/4 0010: Not used 0011: Not used 0100: Not used 0101: Not used 0110: 2.048 kHz(OSC0) 0111: 2.048 kHz/8 1000: 2.048 kHz/64 1001: 2.048 kHz/512 1010: 2.048 kHz/4096 1011: 2.048 kHz/32768 1100: 2.048 kHz/262144 1101: CNT2_END 1110: External 1111: Not used
	972	CNT3 output polarity selection	0: Default Output 1: Inverted Output
	973	CNT3 CNT mode SYNC selection	0: Bypass 1: After two DFF
	974	CNT3 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection (registers [963:960] = 0000/0001/0010)
Multifunction4			
79	975	CNT4 CNT mode SYNC selection	0: Bypass 1: After two DFF
7A	977:976	CNT4 initial value selection	00: bypass the initial 01: Initial 0 10: Initial 1 11: Initial 1
	978	CNT4 DLY EDET FUNCTION Selection	0: Normal 1: DLY function edge detection (registers [991:988] = 0000/0001/0010)
	979 983:980	Single 3-bit LUT	00000: Matrix A - In2 Matrix B - In1 Matrix C - In0 DLY_IN - LOW
		Single DFF with RST and SET	10000: Matrix A - D Matrix B - nSET/nRST Matrix C - CLK DLY_IN - LOW

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
7A	979 983:980	Single CNT/DLY	00001: Matrix A - DLY_IN (CNT) Matrix B - EXT_CLK (CNT) Matrix C - NC DLY_OUT connected to LUT/DFF
		CNT/DLY → LUT	00010: Matrix A - DLY_IN Matrix B - In1 Matrix C - In0 DLY_OUT connected to In2
		CNT/DLY → DFF	10010: Matrix A - DLY_IN Matrix B - nSET/nRST Matrix C - CLK DLY_OUT connected to D
		CNT/DLY → LUT	00110: Matrix A - In2 Matrix B - DLY_IN Matrix C - In0 DLY_OUT connected to In1
		CNT/DLY → DFF	10110: Matrix A - D Matrix B - DLY_IN Matrix C - CLK DLY_OUT connected to nSET/nRST
		CNT/DLY → LUT	01010: Matrix A - In2 Matrix B - In1 Matrix C - DLY_IN DLY_OUT connected to In0
		CNT/DLY → DFF	11010: Matrix A - D Matrix B - nSET/nRST Matrix C - DLY_IN DLY_OUT connected to CLK
		LUT → CNT/DLY	00011: Matrix A - In2 Matrix B - In1 Matrix C - In0 LUT_OUT connected to DLY_IN
		DFF → CNT/DLY	10011: Matrix A - D Matrix B - nSET/nRST Matrix C - CLK DFF_OUT connected to DLY_IN

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
7B	987:984	DLY/CNT4 Clock Source Select	Clock source sel[3:0] 0000: 25 MHz(OSC1) 0001: 25 MHz/4 0010: Not used 0011: Not used 0100: Not used 0101: Not used 0110: 2.048 kHz(OSC0) 0111: 2.048 kHz/8 1000: 2.048 kHz/64 1001: 2.048 kHz/512 1010: 2.048 kHz/4096 1011: 2.048 kHz/32768 1100: 2.048 kHz/262144 1101: CNT3_END 1110: External 1111: Not used
	991:988	CNT4 function and edge mode selection	0000: Both edge Delay 0001: Falling edge delay 0010: Rising edge delay: 0011: Both edge One Shot 0100: Falling edge One Shot 0101: Rising edge One Shot 0110: Both edge freq detect 0111: Falling edge freq detect 1000: Rising edge freq detect 1001: Both edge detect 1010: Falling edge detect 1011: Rising edge detect 1100: Both edge Reset CNT 1101: Falling edge Reset CNT 1110: Rising edge Reset CNT 1111: HIGH level Reset CNT
7C	992	CNT4 output polarity selection	0: Default Output 1: Inverted Output
	999:993	Reserved	
7D 7E	1015:1000	Multi0_LUT4_DFF setting	[15]:LUT4_1 [15]/DFF14 or LATCH Select 0: DFF function 1: LATCH function [14]:LUT4_1 [14]/DFF14 Output Select 0: Q output 1: nQ output [13]:LUT4_1 [13] /DFF14 Initial Polarity Select 0: LOW 1: HIGH [12:0]:LUT4_1 [12:0]

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
7F 80	1031:1016	REG_CNT0_D [15:0]	Data[15:0]
81	1039:1032	Multi1_LUT3_DFF setting	[7]:LUT3_7 [7]/DFF10 or LATCH Select 0: DFF function 1: LATCH function [6]:LUT3_7 [6]/DFF10 Output Select 0: Q output 1: nQ output [5]:LUT3_7 [5]/DFF10 0: nRST from Matrix Output 1: nSET from Matrix Output [4]:LUT3_7 [4]/DFF10 Initial Polarity Select 0: LOW 1: HIGH [3:0]:LUT3_7 [3:0]
82	1047:1040	REG_CNT1_D[7:0]	Data[7:0]
83	1055:1048	Multi2_LUT3_DFF setting	[7]:LUT3_8 [7]/DFF11 or LATCH Select 0: DFF function 1: LATCH function [6]:LUT3_8 [6]/DFF11 Output Select 0: Q output 1: nQ output [5]:LUT3_8 [5]/DFF11 0: nRST from Matrix Output 1: nSET from Matrix Output [4]:LUT3_8 [4]/DFF11 Initial Polarity Select 0: LOW 1: HIGH [3:0]:LUT3_8 [3:0]
84	1063:1056	REG_CNT2_D [7:0]	Data [7:0]
85	1071:1064	Multi3_LUT3_DFF setting	[7]:LUT3_9 [7]/DFF12 or LATCH Select 0: DFF function 1: LATCH function [6]:LUT3_9[6]/DFF12 Output Select 0: Q output 1: nQ output [5]:LUT3_9 [5]/DFF12 0: nRST from Matrix Output 1: nSET from Matrix Output [4]:LUT3_9 [4]/DFF12 Initial Polarity Select 0: LOW 1: HIGH [3:0]:LUT3_9 [3:0]
86	1079:1072	REG_CNT3_D [7:0]	Data[7:0]

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
87	1087:1080	Multi4_LUT3_DFF setting	[7]: LUT3_10 [7]/DFF13 or LATCH Select 0: DFF function 1: LATCH function [6]:LUT3_10[6]/DFF13 Output Select 0: Q output 1: nQ output [5]:LUT3_10 [5]/DFF13 0: nRST from Matrix Output 1: nSET from Matrix Output [4]:LUT3_10 [4]/DFF13 Initial Polarity Select 0: LOW 1: HIGH [3:0]:LUT3_10 [3:0]
88	1095:1088	REG_CNT4_D [7:0]	Data[7:0]
89	1111:1096	CNT0 (16bits) Counted Value	Virtual Input
8A			
8B	1119:1112	CNT4 (8bits) Counted Value	Virtual Input
8C	1127:1120	Reserved	
8D	1135:1128	Reserved	
Combinational Logic			
8E	1143:1136	LUT3_1_DFF4 or Chopper0 setting	[7]:LUT3_1 [7]/DFF4 or LATCH Select 0: DFF function 1: LATCH function [6]:LUT3_1 [6]/DFF4 Output Select 0: Q output 1: nQ output [5]:LUT3_1 [5]/DFF4 Initial Polarity Select 0: LOW 1: HIGH [4]:LUT3_1 [4]/DFF4 0: nRST from Matrix Output 1: nSET from Matrix Output [3]:LUT3_1 [3]/DFF4 Active level selection for RST/SET 0: Active Low-level reset/set 1: Active High-level reset/set [2:0]: LUT3_1 [2:0]

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
8F	1151:1144	LUT3_2_DFF5 or Chopper1 setting	[7]:LUT3_2 [7]/DFF5 or LATCH Select 0: DFF function 1: LATCH function [6]:LUT3_2 [6]/DFF5 Output Select 0: Q output 1: nQ output [5]:LUT3_2 [5]/DFF5 Initial Polarity Select 0: LOW 1: HIGH [4]:LUT3_2 [4]/DFF5 0: nRST from Matrix Output 1: nSET from Matrix Output [3]:LUT3_2 [3]/DFF5 Active level selection for RST/SET 0: Active Low-level reset/set 1: Active High-level reset/set [2:0]: LUT3_2 [2:0]
90	1159:1152	LUT3_3_DFF6 setting	[7]:LUT3_3 [7]/DFF6 or LATCH Select 0: DFF function 1: LATCH function [6]:LUT3_3 [6]/DFF6 Output Select 0: Q output 1: nQ output [5]:LUT3_3 [5]/DFF6 Initial Polarity Select 0: LOW 1: HIGH [4]:LUT3_3 [4]/DFF6 0: nRST from Matrix Output 1: nSET from Matrix Output [3]:LUT3_3 [3]/DFF6 Active level selection for RST/SET 0: Active Low-level reset/set 1: Active High-level reset/set [2:0]: LUT3_3 [2:0]
91	1167:1160	LUT3_4_DFF7 setting	[7]:LUT3_4 [7]/DFF7 or LATCH Select 0: DFF function 1: LATCH function [6]:LUT3_4 [6]/DFF7 Output Select 0: Q output 1: nQ output [5]:LUT3_4 [5]/DFF7 Initial Polarity Select 0: LOW 1: HIGH [4]:LUT3_4 [4]/DFF7 0: nRST from Matrix Output 1: nSET from Matrix Output [3]:LUT3_4 [3]/DFF7 Active level selection for RST/SET 0: Active Low-Level reset/set 1: Active High-Level reset/set [2:0]: LUT3_4 [2:0]

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
92	1171:1168	LUT2_3 value or PGen Size	LUT2_3[3:0] or PGen pattern size[3:0]
	1172	LUT3_1 or DFF4 Select or Chopper 0 registers [1265:1264]	0: LUT3_1 1: DFF4
	1173	LUT3_2 or DFF5 Select or Chopper 1 registers [1267:1266]	0: LUT3_2 1: DFF5
	1174	LUT3_3 or DFF6 Select	0: LUT3_3 1: DFF6
	1175	LUT3_4 or DFF7 Select	0: LUT3_4 1: DFF7
93	1191:1176	PGen data	PGen Data[15:0]
94			
95	1192	LUT2_3 or PGen Select	0: LUT2_3 1: PGen
	1193	LUT2_3 or PGen Active level selection for RST/SET	0: Active Low-level reset/set 1: Active High-level reset/set
	1194	LUT3_6 or Pipe Delay/RIPP CNT Active level selection for RST/SET	0: Active Low-level reset/set 1: Active High-level reset/set
	1195	OUT of LUT3_6 or Out0 of Pipe Delay/RIPP CNT Select	0: LUT3_6 1: OUT0 of Pipe Delay or RIPP CNT
	1196	Pipe Delay or RIPP CNT Selection	0: Pipe delay mode selection 1: Ripple Counter mode selection
	1197	Pipe Delay OUT1 Polarity Select	0: Non-inverted 1: Inverted
	1198	LUT4_0 or DFF9 Select	0: LUT4_0 1: DFF9
	1199	LUT3_0 or DFF3 Select	0: LUT3_0 1: DFF3
96	1207:1200	LUT value or Pipe Delay OUT sel or nSET/END value	[7:4]: LUT3_6 [7:4]/REG_S1[3:0] Pipe Delay OUT1 sel [3:0]: LUT3_6 [3:0]/REG_S0[3:0] Pipe Delay OUT0 sel at RIPP CNT mode: bits[1202:1200] is the nSET value. bits[1205:1203] is the END value. bit[1206] is the range control: 0: Full cycle 1: Range cycle bit[1207]: Not used

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
97 98	1223:1208	LUT4_0_DFF9 setting	[15]:LUT4_0 [15]/DFF9 or LATCH Select 0: DFF function 1: LATCH function [14]:LUT4_0 [14]/DFF9 Output Select 0: Q output 1: nQ output [13]:LUT4_0 [13]/DFF9 Initial Polarity Select 0: LOW 1: HIGH [12]:LUT4_0 [12]/DFF9 stage selection 0: Q of first DFF 1: Q of second DFF [11]:LUT4_0 [11]/DFF9 0: nRST from Matrix Output 1: nSET from Matrix Output [10]:LUT4_0 [10]/DFF9 Active level selection for RST/SET 0: Active Low-level reset/set 1: Active High-level reset/set [9:0]: LUT4_0 [9:0]
99	1231:1224	LUT3_0_DFF3 setting	[7]:LUT3_0 [7]/DFF3 or LATCH Select 0: DFF function 1: LATCH function [6]:LUT3_0 [6]/DFF3 Output Select 0: Q output 1: nQ output [5]:LUT3_0 [5]/DFF3 Initial Polarity Select 0: LOW 1: HIGH [4]:LUT3_0 [4]/DFF3stage selection 0: Q of first DFF 1: Q of second DFF [3]:LUT3_0 [3]/DFF3 0: nRST from Matrix Output 1: nSET from Matrix Output [2]:LUT3_0 [2]/DFF3 Active level selection for RST/SET 0: Active Low-level reset/set 1: Active High-level reset/set [1:0]: LUT3_0 [1:0]

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	**Register Bit**		
9A	1232	Filter or Edge Detector selection	0: Filter 1: Edge Det.
	1233	Filter or Edge Detector Output Polarity Select	0: Non-inverted output 1: Inverted output
	1235:1234	Filter or Edge Detector Select the edge mode	00: Rising Edges Det. 01: Falling Edge Det. 10: Both Edge Det. 11: Both Edge Delay
	1237:1236	Delay Value Select for Programmable Delay or Edge Detector	00: 125 ns 01: 250 ns 10: 375 ns 11: 500 ns
	1239:1238	Select the Edge Mode of Programmable Delay or Edge Detector	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
9B	1247:1240	LUT3_5_DFF8 setting	[7]:LUT3_5 [7]/DFF8 or LATCH Select 0: DFF function 1: LATCH function [6]:LUT3_5 [6]/DFF8 Output Select 0: Q output 1: nQ output [5]:LUT3_5 [5]/DFF8 Initial Polarity Select 0: LOW 1: HIGH [4]:LUT3_5 [4]/DFF8 0: nRST from Matrix Output 1: nSET from Matrix Output [3]:LUT3_5 [3]/DFF8 Active level selection for RST/SET 0: Active Low-level reset/set 1: Active High-level reset/set [2:0]: LUT3_5 [2:0]

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
9C	1251:1248	LUT2_0/DFF0 setting	[3]:LUT2_0 [3]/DFF0 or LATCH Select 0: DFF function 1: LATCH function [2]:LUT2_0 [2]/DFF0 Output Select 0: Q output 1: nQ output [1]:LUT2_0 [1]/DFF0 Initial Polarity Select 0: LOW 1: HIGH [0]:LUT2_0 [0]
	1255:1252	LUT2_1/DFF1 setting	[3]:LUT2_1 [3]/DFF1 or LATCH Select 0: DFF function 1: LATCH function [2]:LUT2_1 [2]/DFF1 Output Select 0: Q output 1: nQ output [1]:LUT2_1 [1]/DFF1 Initial Polarity Select 0: LOW 1: HIGH [0]:LUT2_1 [0]
9D	1259:1256	LUT2_2/DFF2 setting	[3]:LUT2_2 [3]/DFF2 or LATCH Select 0: DFF function 1: LATCH function [2]:LUT2_2 [2]/DFF2 Output Select 0: Q output 1: nQ output [1]:LUT2_2 [1]/DFF2 Initial Polarity Select 0: LOW 1: HIGH [0]:LUT2_2 [0]
	1260	LUT2_0 or DFF0 Select	0: LUT2_0 1: DFF0
	1261	LUT2_1 or DFF1 Select	0: LUT2_1 1: DFF1
	1262	LUT2_2 or DFF2 Select	0: LUT2_2 1: DFF2
	1263	LUT3_5 or DFF8 Select	0: LUT3_5 1: DFF8
9E	1264	LUT3_1/DFF4 or Chopper0 Select	0: LUT3_1/DFF_4 1: Chopper 0
	1265	Chopper0 polarity Select	0: Q 1: nQ
	1266	LUT3_2/DFF5 or Chopper1 Select	0: LUT3_2/DFF_5 1: Chopper 1
	1267	Chopper1 polarity Select	0: Q 1: nQ
	1271:1268	Reserved	

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
9F	1272	Reserved	
9F	1279:1273	Reserved	
PWM Macrocell			
A0	1287:1280	Reserved	
A1	1295:1288	Initial PWM0 Duty Cycle value	PWM0 Initial Duty Cycle value [7:0]
A2	1296	I^2C trigger for PWM0	0: Don't update duty cycle value 1: Update duty cycle value
	1297	I^2C trigger for PWM1	0: Don't update duty cycle value 1: Update duty cycle value
	1298	PWM0 8-bit or 7-bit resolution	0: 8-bit PWM0 1: 7-bit PWM0
	1299	PWM0 OUT+ output polarity selection	0: Non-Inverted Output 1: Inverted Output
	1300	PWM0 OUT- output polarity selection	0: Non-Inverted Output 1: Inverted Output
	1301	PWM0 SYNC On/Off for PWM0	0: Synchronous Power-Down 1: Asynchronous Power-Down
A2	1302	PWM0 Continuous/Autostop mode	0: Continuous mode 1: PWM Duty Cycle Counter Autostop at 0 % or 100 %
	1303	PWM0 Boundary OSC disable	0: OSC is always enabled at boundaries 1: Automatically Disable OSC
A3	1311:1304	Initial PWM1 Duty Cycle value	PWM1 Initial Duty Cycle value [7:0]
A4	1319:1312	Current PWM0 Duty Cycle value for I^2C read	PWM0 Current Duty Cycle value for I^2C read [7:0]
A5	1327:1320	Current PWM1 Duty Cycle value for I^2C read	PWM1 Current Duty Cycle value for I^2C read [7:0]
A6	1335:1328	PWM0 Preset 16 bytes Duty Cycle/CCMP Vref values → byte0	Byte0 [7:0]
A7	1343:1336	PWM0 Preset 16 bytes Duty Cycle/CCMP Vref values → byte1	Byte1 [15:8]
A8	1351:1344	PWM0 Preset 16 bytes Duty Cycle/CCMP Vref values → byte2	Byte2 [23:16]
A9	1359:1352	PWM0 Preset 16 bytes Duty Cycle/CCMP Vref values → byte3	Byte3 [31:24]
AA	1367:1360	PWM0 Preset 16 bytes Duty Cycle/CCMP Vref values → byte4	Byte4 [39:32]
AB	1375:1368	PWM0 Preset 16 bytes Duty Cycle/CCMP Vref values → byte5	Byte5 [47:40]
AC	1383:1376	PWM0 Preset 16 bytes Duty Cycle/CCMP Vref values → byte6	Byte6 [55:48]
AD	1391:1384	PWM0 Preset 16 bytes Duty Cycle/CCMP Vref values → byte7	Byte7 [63:56]
AE	1399:1392	PWM0 Preset 16 bytes Duty Cycle/CCMP Vref values → byte8	Byte8 [71:64]

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
AF	1407:1400	PWM0 Preset 16 bytes Duty Cycle/CCMP Vref values → byte9	Byte9 [79:72]
B0	1415:1408	PWM0 Preset 16 bytes Duty Cycle/CCMP Vref values → byte10	Byte10 [87:80]
B1	1423:1416	PWM0 Preset 16 bytes Duty Cycle/CCMP Vref values → byte11	Byte11 [95:88]
B2	1431:1424	PWM0 Preset 16 bytes Duty Cycle/CCMP Vref values→ byte12	Byte12 [103:96]
B3	1439:1432	PWM0 Preset 16 bytes Duty Cycle/CCMP Vref values → byte13	Byte13 [111:104]
B4	1447:1440	PWM0 Preset 16 bytes Duty Cycle/CCMP Vref values → byte14	Byte14 [119:112]
B5	1455:1448	PWM0 Preset 16 bytes Duty Cycle/CCMP Vref values → byte15	Byte15 [127:120]
B6	1459:1456	PWM0 Period Counter Clock Source selection	0000: CLK_OSC0 0001: CLK_OSC0/4 0010: CLK_OSC1 0011: CLK_OSC1/8 0100: CLK_OSC1/64 0101: CLK_OSC1/512 0110: CLK_OSC1/4096 0111: CLK_OSC1/32768 1000: CLK_OSC1/262144 1001: From Flexible Divider 1010: Reserved 1011: External clock through matrix (Matrix OUT [79])
	1460	PWM0 Phase Correct mode	0: Disable 1: Enable
	1461	PWM0 Keep/Stop selection	0: Keep 1: Stop
	1463:1462	Reserved	

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
B7	1465:1464	PWM0 Deadband selection	00: No Deadband 01: 1PWM0 clock cycles 10: 2PWM0 clock cycles 11: 3PWM0 clock cycles
	1467:1466	PWM0 Duty Cycle source	Regular Mode: 00: from PWM Duty Cycle CNT Preset Registers Modes: 01: 8-byte MSB of RegFile 10: 8-byte LSB of RegFile 11: 16-byte RegFile
	1469:1468	PWM0 Duty Cycle Counter Clock Source selection	00: Matrix output 01: PWM Period CNT overflow 10: Every 2nd pulse of PWM Period CNT overflow 11: Every 8th pulse of PWM Period CNT overflow
	1471:1470	Reserved	
B8	1472	PWM1 8-bit or 7-bit resolution	0: 8-bit PWM1 1: 7-bit PWM1
	1473	PWM1 OUT+ output polarity selection	0: Non-Inverted Output 1: Inverted Output
	1474	PWM1 OUT- output polarity selection	0: Non-Inverted Output 1: Inverted Output
	1475	PWM1 SYNC On/Off	0: Synchronous Power-Down 1: Asynchronous Power-Down
	1476	PWM1 Continuous/Autostop mode	0: Continuous mode 1: PWM Duty Cycle Counter Autostop at 0 % or 100 %
	1477	PWM1 Boundary OSC disable	0: OSC is always enabled at boundaries 1: Automatically Disable OSC
B8	1478	PWM1 Phase Correct mode	0: Disable 1: Enable
	1479	PWM1 Keep/Stop selection	0: Keep 1: Stop

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	**Register Bit**		
B9	1481:1480	PWM1 Deadband selection	00: No Deadband 01: 1PWM1 clock cycles 10: 2PWM1 clock cycles 11: 3PWM1 clock cycles
	1483:1482	PWM1 Duty Cycle source	Regular Mode: 00: from PWM Duty Cycle CNT Preset Registers Modes: 01: 8-byte MSB of RegFile 10: 8-byte LSB of RegFile 11: 16-byte RegFile
	1485:1484	PWM1 Duty Cycle Counter Clock Source selection	00: Matrix output 01: PWM Period CNT overflow 10: Every 2nd pulse of PWM Period CNT overflow 11: Every 8th pulse of PWM Period CNT overflow
	1487:1486	Reserved	
BA	1491:1488	PWM1 Period Counter Clock Source selection	0000: CLK_OSC0 0001: CLK_OSC0/4 0010: CLK_OSC1 0011: CLK_OSC1/8 0100: CLK_OSC1/64 0101: CLK_OSC1/512 0110: CLK_OSC1/4096 0111: CLK_OSC1/32768 1000: CLK_OSC1/262144 1001: From Flexible Divider 1010: Reserved 1011: External clock through matrix (Matrix OUT [84])
	1495:1492	Reserved	
BB	1503:1496	Reserved	
BC	1511:1504	Reserved	
BD	1519:1512	Reserved	
Reserved			
BE	1520	Reserved	
	1521	Reserved	
	1522	Reserved	
	1523	Reserved	
BE	1527:1524	Reserved	
BF	1531:1528	Reserved	
	1532	Reserved	
	1533	Reserved	
	1535:1534	Reserved	

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
C0	1539:1536	Reserved	
	1540	Reserved	
	1541	Reserved	
	1543:1542	Reserved	
C1	1547:1544	Reserved	
C1	1551:1548	Reserved	
C2	1559:1552	Reserved	
C3	1567:1560	Reserved	
C4	1575:1568	Reserved	
C5	1583:1576	Reserved	
C6	1591:1584	Reserved	
C7	1599:1592	Reserved	
C8	1607:1600	Reserved	
C9	1615:1608	Reserved	
CA	1623:1616	Reserved	
CB	1631:1624	Reserved	
CC	1639:1632	Reserved	
CD	1647:1640	Reserved	
CE	1655:1648	Reserved	
CF	1663:1656	Reserved	
D0	1671:1664	Reserved	
D1	1679:1672	Reserved	
D2	1687:1680	Reserved	
D3	1695:1688	Reserved	
D4	1703:1696	Reserved	
D5	1711:1704	Reserved	
D6	1719:1712	Reserved	
D7	1727:1720	Reserved	
D8	1735:1728	Reserved	
D9	1743:1736	Reserved	
DA	1751:1744	Reserved	
DB	1759:1752	Reserved	
DC	1767:1760	Reserved	
DD	1775:1768	Reserved	

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
Reserved			
DE	1776	Reserved	
	1777	Reserved	
	1778	Reserved	
	1779	Reserved	
	1780	Reserved	
DE	1781	Reserved	
	1782	Reserved	
	1783	Reserved	
DF	1784	Reserved	
	1785	Reserved	
	1786	Reserved	
	1787	Reserved	
	1788	Reserved	
	1789	Reserved	
	1790	Reserved	
	1791	Reserved	
E0	1792	Reserved	
	1793	Reserved	
	1794	Reserved	
	1795	Reserved	
	1796	Reserved	
	1797	Reserved	
	1798	Reserved	
	1799	Reserved	
E1	1800	Reserved	
	1801	Reserved	
	1802	Reserved	
	1803	Reserved	
	1804	Reserved	
	1805	Reserved	
	1806	Reserved	
	1807	Reserved	

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	**Register Bit**		
E2	1808	Reserved	
	1809	Reserved	
	1810	Reserved	
	1811	Reserved	
	1812	Reserved	
	1813	Reserved	
	1814	Reserved	
	1815	Reserved	
E3	1816	Reserved	
	1817	Reserved	
	1818	Reserved	
	1819	Reserved	
	1820	Reserved	
	1821	Reserved	
	1822	Reserved	
	1823	Reserved	
E4	1824	Reserved	
	1825	Reserved	
	1826	Reserved	
	1827	Reserved	
	1828	Reserved	
	1829	Reserved	
	1830	Reserved	
	1831	Reserved	

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
E5	1832	Reserved	
	1833	Reserved	
	1834	Reserved	
	1835	Reserved	
	1836	Reserved	
	1837	Reserved	
	1838	Reserved	
	1839	Reserved	
E6	1840	Reserved	
	1841	Reserved	
	1842	Reserved	
	1843	Reserved	
	1844	Reserved	
	1845	Reserved	
	1846	Reserved	
E6	1847	Reserved	
E7	1848	Reserved	
	1849	Reserved	
	1850	Reserved	
	1851	Reserved	
	1852	Reserved	
	1853	Reserved	
	1854	Reserved	
	1855	Reserved	
E8	1856	Reserved	
	1857	Reserved	
	1858	Reserved	
	1859	Reserved	
	1860	Reserved	
	1861	Reserved	
	1862	Reserved	
	1863	Reserved	

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
E9	1864	Reserved	
	1865	Reserved	
	1866	Reserved	
	1867	Reserved	
	1868	Reserved	
	1869	Reserved	
	1870	Reserved	
	1871	Reserved	
EA	1872	Reserved	
	1873	Reserved	
	1874	Reserved	
	1875	Reserved	
	1876	Reserved	
	1877	Reserved	
	1878	Reserved	
	1879	Reserved	
EB	1880	Reserved	
	1881	Reserved	
	1882	Reserved	
	1883	Reserved	
	1884	Reserved	
	1885	Reserved	
	1886	Reserved	
	1887	Reserved	
EC	1888	Reserved	
	1889	Reserved	
	1890	Reserved	
	1891	Reserved	
	1892	Reserved	
	1893	Reserved	
	1894	Reserved	
	1895	Reserved	

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	Register Bit		
ED	1896	Reserved	
	1897	Reserved	
	1898	Reserved	
	1899	Reserved	
	1900	Reserved	
	1901	Reserved	
	1902	Reserved	
	1903	Reserved	
EE	1904	Reserved	
	1905	Reserved	
	1906	Reserved	
	1907	Reserved	
	1910:1908	Reserved	
	1911	Reserved	
EF	1912	Reserved	
	1913	Reserved	
	1914	Reserved	
	1915	Reserved	
	1918:1916	Reserved	
	1919	Reserved	
F0	1920	Reserved	
	1921	Reserved	
	1922	Reserved	
	1923	Reserved	
	1926:1924	Reserved	
	1927	Reserved	
F1	1928	Reserved	
	1929	Reserved	
	1930	Reserved	
	1931	Reserved	
	1934:1932	Reserved	
	1935	Reserved	

Table 72. Register Map (Cont.)

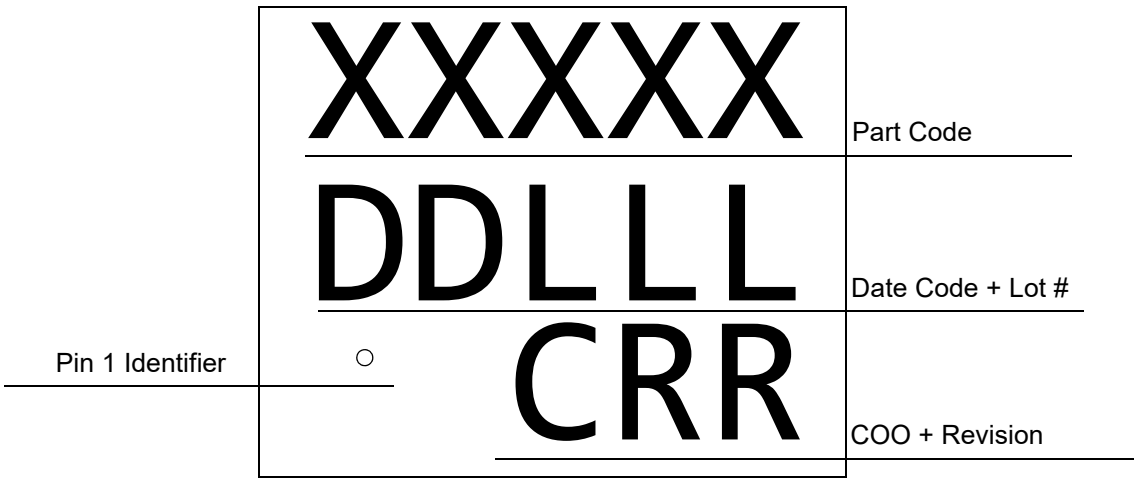
Address		Signal function	Register Bit definition
Byte	**Register Bit**		
F2	1936	Reserved	
	1937	Reserved	
	1938	Reserved	
	1939	Reserved	
	1940	Reserved	
	1941	Reserved	
	1942	Reserved	
	1943	Reserved	
F3	1947:1944	Reserved	
	1948	Reserved	
	1951:1949	Reserved	
F4	1952	Reserved	
	1953	Reserved	
	1954	Reserved	
	1955	Reserved	
	1958:1956	Reserved	
	1959	Reserved	
F5	1960	I^2C reset bit with reloading NVM into Data register (soft reset)	0: Keep existing condition 1: Reset execution
	1961	IO Latching Enable During I^2C Write Interface	0: Disable 1: Enable
	1963:1962	Reserved	
	1964	Protect mode enable	0: Disable 1: Enable
	1965	Register protection mode bit 0	000: All open read/write (mode 0) 001: Partly lock read (mode 1) 010: Partly lock read2 (mode 2) 011: Partly lock read2/write (mode 3) 100: All lock read (mode 4) 101: All lock write (mode 5) 110: All lock read/write (mode 6)
	1966	Register protection mode bit 1	
	1967	Register protection mode bit 2	
F6	1975:1968	I^2C write mask bits	1: Mask 0: Overwrite
F7	1983:1976	Reserved	
F8	1991:1984	Reserved	

Table 72. Register Map (Cont.)

Address		Signal function	Register Bit definition
Byte	**Register Bit**		
F9	1992	Reserved	
F9	1993	Reserved	
	1995:1994	Reserved	
	1999:1996	Reserved	
FA	2007:2000	8-bit Pattern ID Byte 0 (from NVM): ID[23:16]	
FB	2015:2008	Reserved	
FC	2023:2016	Reserved	
FD	2027:2024	I^2C slave address	
	2028	Slave address selection bit0	0: From register [2024] 1: From GPI
	2029	Slave address selection bit1	0: From register [2025] 1: From GPIO1
	2030	Slave address selection bit2	0: From register [2026] 1: From GPIO4
	2031	Slave address selection bit3	0: From register [2027] 1: From GPIO6
FE	2032	I^2C operation disable bit	0: I^2C operation enable; matrix in 32/33 select I^2C_virtual_0/1 Input 1: I^2C operation disable; matrix in 32/33 select GPIO2/3 digital input
	2033	Reserved	
	2034	Reserved	
	2039:2035	Reserved	
FF	2047:2040	Reserved	

24. Package Top Marking Definitions

24.1 STQFN 20L 2 mm x 3 mm 0.4P



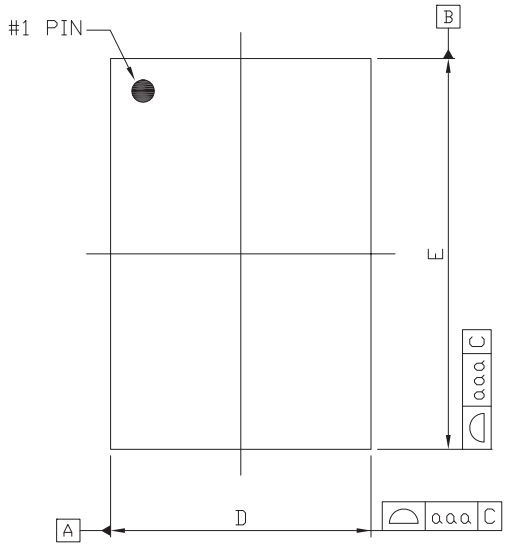
XXXXX - Part ID Field identifies the specific device configuration

25. Package Information

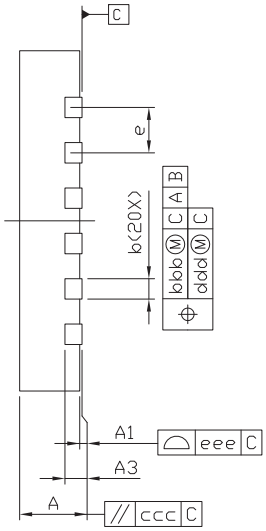
25.1 Package Outlines for STQFN 20L 2 mm x 3 mm 0.4P FCD Green Package

JEDEC MO-220

IC Net Weight: 0.008 g



Top view

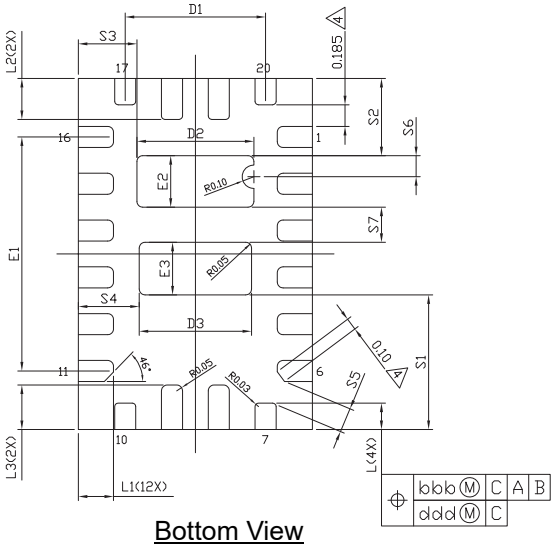


Side View

[1] All dimensions are in millimeters.

[2] Dimension “b” applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension “b” should not be measured in that radius area.

[3] Bilateral co-planarity zone applies to the exposed heat sink slug as well as the terminal.



Bottom View

Controlling Dimension: mm

Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.000	0.020	0.050	0.000	0.001	0.002
A3	0.10	0.15	0.20	0.004	0.006	0.008
D	1.95	2.00	2.05	0.077	0.079	0.081
E	2.95	3.00	3.05	0.116	0.118	0.120
D1	1.15	1.20	1.25	0.045	0.047	0.049
E1	1.95	2.00	2.05	0.077	0.079	0.081
D2	0.95	1.00	1.05	0.037	0.039	0.041
E2	0.39	0.44	0.49	0.015	0.017	0.019
D3	0.91	0.96	1.01	0.036	0.038	0.040
E3	0.40	0.45	0.50	0.016	0.018	0.020
S1	1.10	1.15	1.20	0.043	0.045	0.047
S2	0.61	0.66	0.71	0.024	0.026	0.028
S3	0.45	0.50	0.55	0.018	0.020	0.022
S4	0.47	0.52	0.57	0.018	0.020	0.022
S5	0.208 REF			0.008 REF		
S6	0.180 REF			0.007 REF		
S7	0.300 REF			0.012 REF		

“A1” max lead co-planarity 0.05 mm Standard tolerance: ±0.05

Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
e	0.40 BSC			0.016 BSC		
L	0.175	0.225	0.275	0.007	0.009	0.011
L1	0.250	0.300	0.350	0.010	0.012	0.014
L2	0.300	0.350	0.400	0.012	0.014	0.016
L3	0.330	0.380	0.430	0.013	0.015	0.017
b	0.130	0.180	0.230	0.005	0.007	0.009
aaa	0.07			0.003		
bbb	0.07			0.003		
ccc	0.1			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		

Figure 165. STQFN 20L 2x3mm 0.4P FCD Package

25.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 73.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The STQFN-20L package is qualified for MSL 1.

Table 73. MSL Classification

MSL level	Floor lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 60 % RH

25.3 STQFN Handling

Be sure to handle STQFN package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle STQFN package with fingers as this can contaminate the package pins and interface with solder reflow.

25.4 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

26. Thermal Guidelines

Actual thermal characteristics will depend on number and position of vias, PCB type, copper layers and other factors. Operating temperature range is from -40 °C to 85 °C. To guarantee reliable operation, the junction temperature of the SLG47115 must not exceed 150 °C.

To avoid overheating of the power MOSFETs (as shown in Figure 166), a good thermal design of the PCB layout must be implemented, especially when device operates near its maximum thermal limits. Refer to Section 3.4 Thermal Information to find max value of thermal resistance.

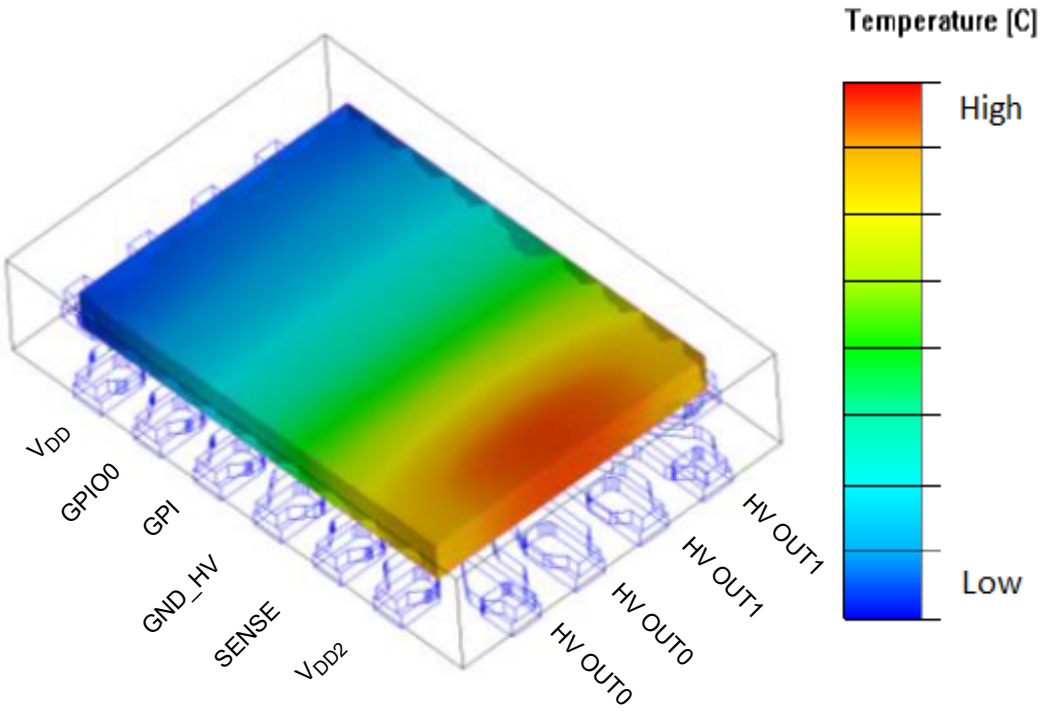


Figure 166. Die Temperature when HV OUTs are Active

27. Layout Consideration

PCB should have enough ground plane to dissipate heat. SLG47115 has two additional pads which provide enhanced thermal dissipation. Thermal vias are used to transfer heat from chip to other layers of the PCB.

The sense resistors and power capacitors should be placed as close as possible to the chip for reducing parasitic parameters.

Typical application circuit is shown in Figure 167.

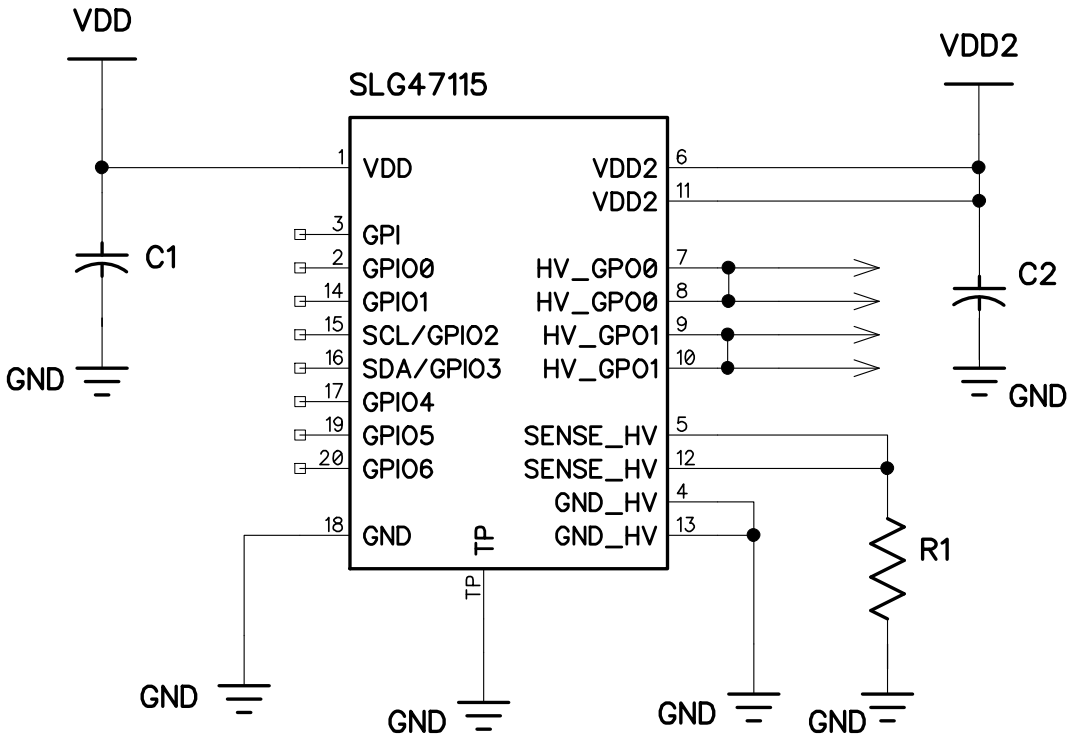


Figure 167. Typical Application Circuit

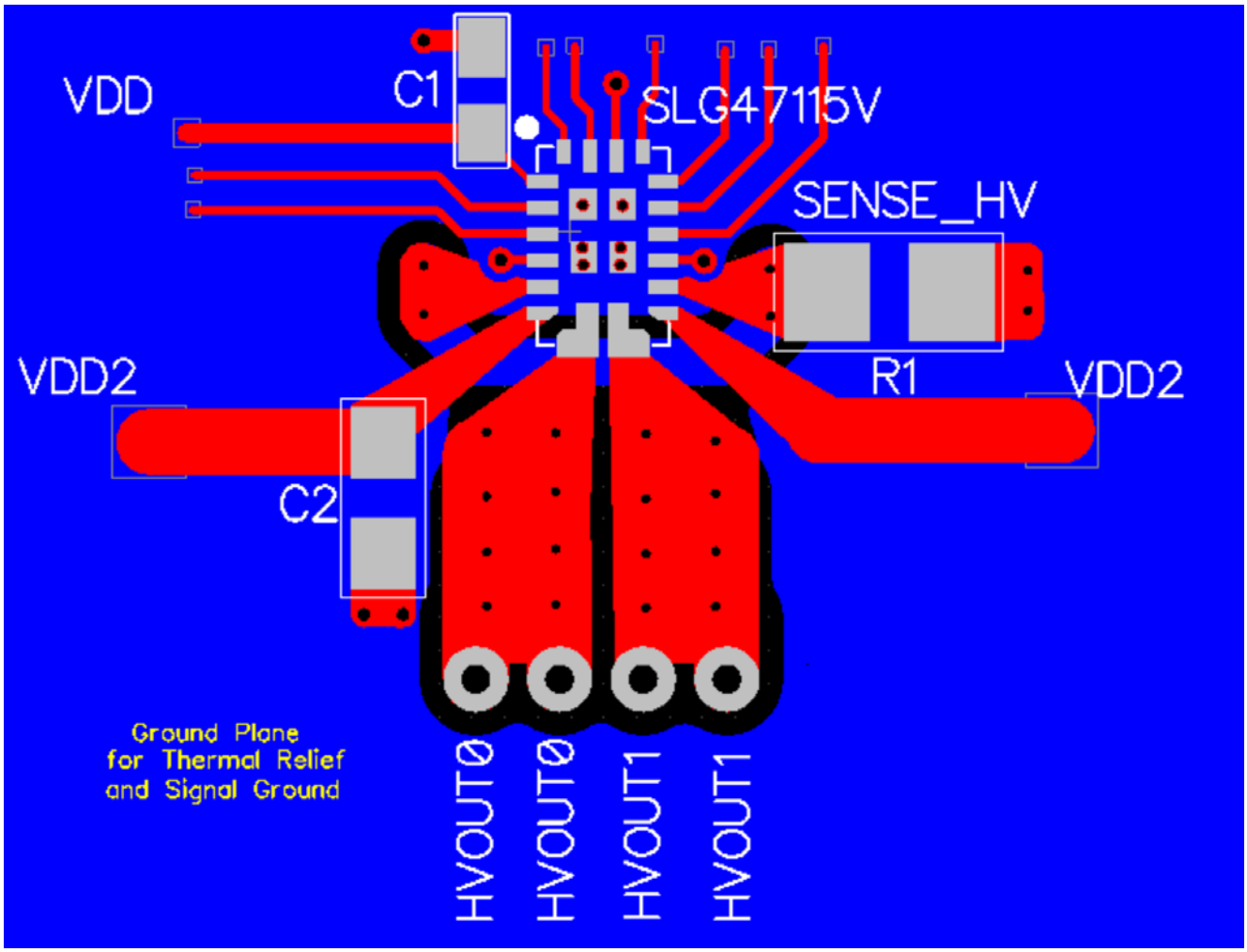


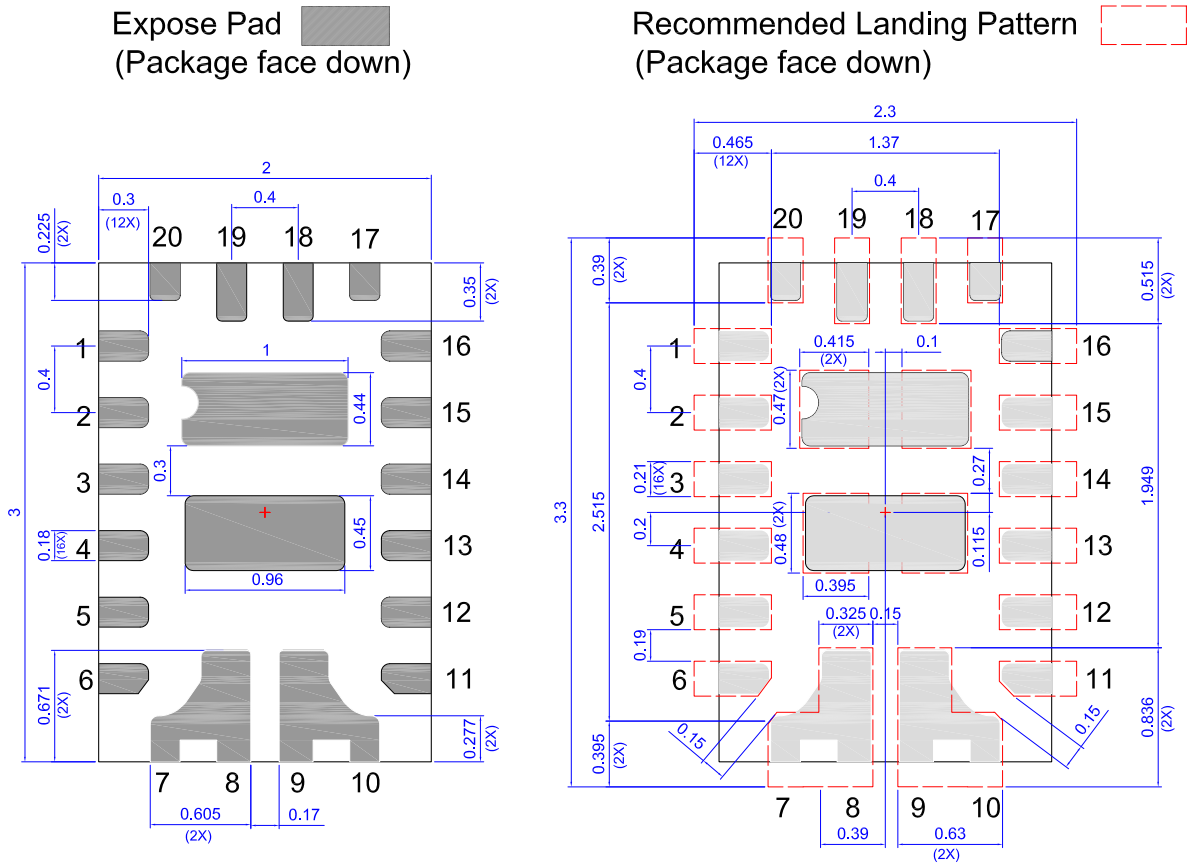
Figure 168. PCB Layout Example

28. Layout Guidelines

28.1 STQFN 20L 2 mm x 3 mm 0.4P FCD Package

It's highly recommended to place low-ESR capacitor between V_{DD2} and GND pin to keep input voltage stable and reduce ripple. This capacitor should be placed as close to the pins as possible. Also, the capacitor must have the low input impedance at the switching frequency. The recommended value of this capacitor is 1-10 µF for most applications. Motors with larger armature inductors require larger input capacitors.

Also, it's highly recommended to place 0.1 µF ceramic capacitor between V_{DD} and GND.



29. Ordering Information

Part number	Type
SLG47115	20-pin STQFN
SLG47115VTR	20-pin STQFN - Tape and Reel (3k units)

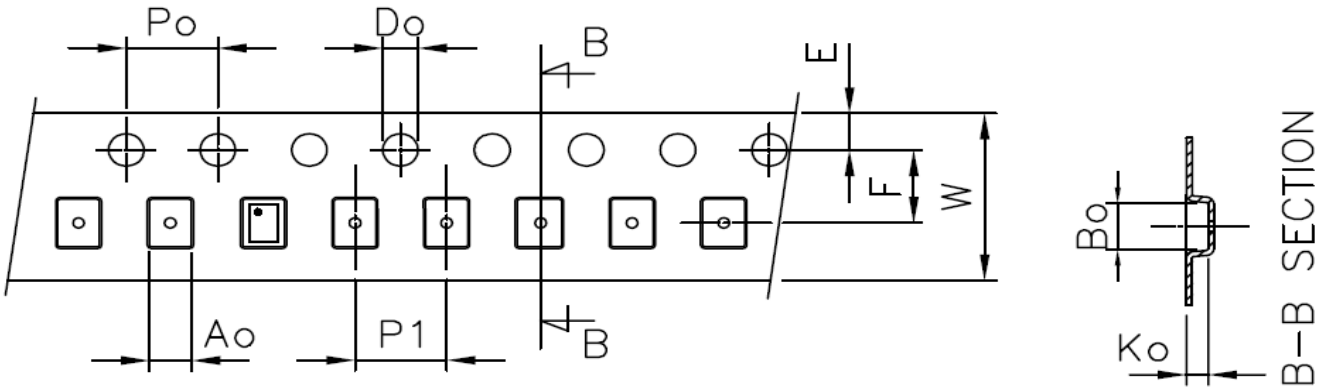
Note 1: Use SLG47115 to order. Shipments are automatically in Tape and Reel.
Note 2: “TR” suffix is no longer used. It is a legacy naming convention shown here only for informational purposes.

29.1 Tape and Reel Specifications

Package type	# of pins	Nominal Package size (mm)	Max units		Reel & Hub size (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
STQFN 20L 2 mm x 3 mm 0.4P FCD Green	20	2.0x3.0x0.55	3000	3000	178/60	100	400	100	400	8	4

29.2 Carrier Tape Drawing and Dimensions

Package type	Pocket BTM length (mm)	Pocket BTM width (mm)	Pocket depth (mm)	Index hole pitch (mm)	Pocket pitch (mm)	Index hole diameter (mm)	Index hole to tape edge (mm)	Index hole to pocket center (mm)	Tape width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2 mm x 3 mm 0.4P FCD Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8



Glossary

A

ACK	Acknowledge bit
ACMP	Analog Comparator
ACMPH	Analog Comparator High-speed
ACMPL	Analog Comparator Low Power

B

BG	Bandgap

C

CLK	Clock
CMO	Connection matrix output
CMP	Comparator
CNT	Counter

D

DFF	D Flip-Flop
Diff Amp	Differential Amplifier
DLY	Delay

E

ESD	Electrostatic discharge
EV	End Value
EXT	External

F

FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

H

HD	High Current Drive
HV	High Voltage

I

IN	Input
IO	Input/Output

L

LP_BG	Low Power Bandgap
LPF	Low-pass Filter
LS	Level Shifter
LSB	Least Significant Bit
LUT	Look Up Table

M

MSB	Most Significant Bit
MUX	Multiplexer

N

NPR	Non-Volatile Memory Read/Write/Erase Protection
nRST	Reset
NVM	Non-Volatile Memory

O

OCP	Overcurrent Protection
OD	Open-drain
OE	Output Enable
OSC	Oscillator
OTP	One Time Programmable
OUT	Output

P

PD	Power-Down
PGen	Pattern Generator
POR	Power-On Reset
PP	Push-pull
PWM	Pulse Width Modulator
PWR	Power
P DLY	Programmable Delay

R

R/W	Read/Write

S

SCL	I²C Clock Input
SDA	I²C Data Input/Output
SLA	Slave Address
SMT	With Schmitt trigger
SV	nSET Value

T

TSD	Thermal Shutdown
TS	Temperature Sensor
TS_OUT	Temperature Sensor Output

U

UVLO	Undervoltage-Lockout

V

Vref	Voltage Reference

W

WOSMT	Without Schmitt trigger
WS	Wake and Sleep Controller

Revision History

Revision	Date	Description
1.19	Sep 16, 2024	Fixed typos Corrected V_{UVLO} values in table Protection Circuits
1.18	Feb 7, 2024	Updated registers [2007:2000] Fixed typos
1.17	Dec 11, 2023	Changed table headings in section Specifications Fixed typos Corrected HV Output Modes section Updated Paragraph Styles
1.16	Jun 30, 2023	Fixed typos Corrected cross-reference in section Thermal Guidelines
1.15	Mar 1, 2023	Added notes to section Ordering Information
1.14	Feb 3, 2023	Updated section Analog Comparators
1.13	Jan 13, 2023	Added Note to Typical Current Estimated for Each Macrocell Table
1.12	Nov 9, 2022	Updated section Package Top Marking Definitions Updated section Analog Temperature Sensor
1.11	Sept 23, 2022	Updated section High Voltage Outputs Typical Performance Fixed typos
1.10	Sept 14, 2022	Updated section Specifications Updated section High Voltage Outputs Typical Performance
1.00	Jul 14, 2022	Initial release

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