SH74582

RENESAS MCU

R01DS0240EJ0111
Rev.1.11
Feb 18, 2015

1. Overview

The SH7458 Group is a single-chip RISC (reduced instruction set computer) microcontroller based on a Renesas original RISC CPU core.

Basically the SH7458 Group is the same as the SH7456 Group. Please refer to SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10 (Sep 22, 2011). Table 1.1 shows the differences between the SH7456 Group and the SH7458 Group.

* Henceforth, the bold letter portion (shaped portion) shows a difference from SH7456 Group.

Table 1.1 Products

Group	Product	Model	CPU Frequency	Memory Capacity	Package	FlexRay	Operating temperature (Ta)
SH7458	**SH74582**	**R5F74582KBG**	160MHz	ROM: 1Mbytes IL memory: 8 Kbytes, OL memory: 16 Kbytes, and SHwyRAM: **512** Kbytes	PRBG0176GA-A	**Yes**	-40 to +125°C
SH7455	SH74552	R5F74552KBG	160MHz	ROM: 1Mbyte IL memory: 8 Kbytes, OL memory: 16 Kbytes, and SHwyRAM: 256 Kbytes	PRBG0176GA-A	Yes	-40 to +125°C
SH7456	SH74562	R5F74562KBG	160MHz		PRBG0176GA-A	No	-40 to +125°C
SH7457	SH74572	R5F74572LBG	240MHz	ROM: 1Mbyte IL memory: 8 Kbytes, OL memory: 16 Kbytes, and SHwyRAM: 256 Kbytes	PRBG0176GA-A	Yes	-40 to +105°C
SH7459	SH74593	R5F74593LBG	240MHz	ROM: 1.5Mbytes IL memory: 8 Kbytes, OL memory: 16 Kbytes, and SHwyRAM: 512 Kbytes	PRBG0176GA-A	Yes	-40 to +105°C

2. Details

This section shows the details of the difference from SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10 (Sep 22, 2011). Table 2.1 shows the difference between the SH74562 and the SH74582.

Table 2.1 Difference between SH74562 and SH74582

Page	Description
1-1	• 1.1 Features Product — SuperHyway RAM (SHwyRAM) Capacity SH74562 — 256 Kbytes SH74582 — **512** Kbytes
1-4	• Table 1.1 Specifications Overview: Descriptions of RAM Product — RAM Capacity SH74562 — 256-Kbyte SH74582 — **512**-Kbyte

Page	Description
1-6	• Table 1.1 Specifications Overview: Descriptions of FlexRay Product — Channels of FlexRay SH74562 — None: SH7456 Group SH74582 — **Two channels**: **SH7458** Group
1-7	• Table 1.2 Products Product — Model — SHwyRAM Capacity — FlexRay SH74562 — R5F74562KBG — 256 Kbytes — No SH74582 — **R5F74582KBG** — **512** Kbytes — **Yes** Please refer to Appendix A.
1-8	• Figure 1.1 Block Diagram Product — SHwyRAM Capacity SH74562 — SHwyRAM (256 Kbytes) SH74582 — SHwyRAM (**512** Kbytes)
11-2	• Figure 11.2 Address Space (P0/U0 Area): Descriptions of 29-bit physical address space (Single chip) Product — SHwyRAM Capacity (Start address – Last address) SH74562 — 256 Kbytes (H'1800 0000 – H'1803 FFFF) SH74582 — **512** Kbytes (H'1800 0000 – **H'1807 FFFF**) Please refer to Appendix B.1.
11-3	• Figure 11.3 Address Space (P1 Area): Descriptions of 29-bit physical address space (Single chip) Product — SHwyRAM Capacity (Start address – Last address) SH74562 — 256 Kbytes (H'9800 0000 – H'9803 FFFF) SH74582 — **512** Kbytes (H'9800 0000 – **H'9807 FFFF**) Please refer to Appendix B.2.
11-4	• Figure 11.4 Address Space (P2 Area): Descriptions of 29-bit physical address space (Single chip) Product — SHwyRAM Capacity (Start address – Last address) SH74562 — 256 Kbytes (H'B800 0000 – H'B803 FFFF) SH74582 — **512** Kbytes (H'B800 0000 – **H'B807 FFFF**) Please refer to Appendix B.3.
11-5	• Figure 11.5 Address Space (P3 Area): Descriptions of 29-bit physical address space (Single chip) Product — SHwyRAM Capacity (Start address – Last address) SH74562 — 256 Kbytes (H'D800 0000 – H'D803 FFFF) SH74582 — **512** Kbytes (H'D800 0000 – **H'D807 FFFF**) Please refer to Appendix B.4.
13-1	• 13.1 Overview Product — Page structure SH74562 — 64-Kbyte units (pages 0 to 3) SH74582 — 64-Kbyte units (pages **0 to 7**) • Figure 13.1 Block Diagram of SHwyRAM : Descriptions of Memory block Product — Page number [Capacity] SH74562 — Page 3 [64 KB] SH74582 — **Page 7** [64 KB]

Page	Description
13-1 13-2	• 13.1 Overview Product SHwyRAM allocation SH74562 the upper 256 Kbytes of area 6 (H'1800 0000 to H'1803 FFFF in the 29-bit physical address space) SH74582 the upper **512** Kbytes of area 6 (H'1800 0000 to **H'1807 FFFF** in the 29-bit physical address space) • Figure 13.2 Address Space : Descriptions of 29-bit physical address space (area 6) Product SHwyRAM Capacity (Start address – Last address) SH74562 256 Kbytes (H'1800 0000 – H'1803 FFFF) SH74582 **512** Kbytes (H'1800 0000 – **H'1807 FFFF**) Added the following pages Page Address (29-bit physical address) **Page 4** **H'1804 0000 – H'1804 FFFF** **Page 5** **H'1805 0000 – H'1805 FFFF** **Page 6** **H'1806 0000 – H'1806 FFFF** **Page 7** **H'1807 0000 – H'1807 FFFF** Please refer to Appendix C.
28-1	• Table 28.1 DRIi Overview Product Access areas SH74562 All SHwyRAM areas (up to 256 Kbytes) SH74582 All SHwyRAM areas (up to **512** Kbytes) Please refer to Appendix D.1.
28-46	• 28.3.23 DRIi Address Reload Registers 0 and 1 (DRIiADR0RLD and DRIiADR1RLD) : Description of DRIADmRLD bit Product Description SH74562 Address Bits 18 to 2 Reload Value (256-Kbyte area) SH74582 Address Bits 18 to 2 Reload Value (**512**-Kbyte area) Please refer to Appendix D.2.
28-47	• 28.3.24 DRIi Address Counters 0 and 1 (DRIiADR0CT and DRIiADR1CT) : Description of DRIADn bit Product Description SH74562 Destination Address Bits 18 to 2 (256-Kbyte area) SH74582 Destination Address Bits 18 to 2 (**512**-Kbyte area) Please refer to Appendix D.3.
29-1	• Table 29.1 DRO Module Overview Product Access area SH74562 SHwyRAM area (256 Kbytes) SH74582 SHwyRAM area (**512** Kbytes) Please refer to Appendix E.

Appendix A

Section 1 Overview

1.2 Product Line Overview

Table 1.2 lists the products.

Table 1.2 Products

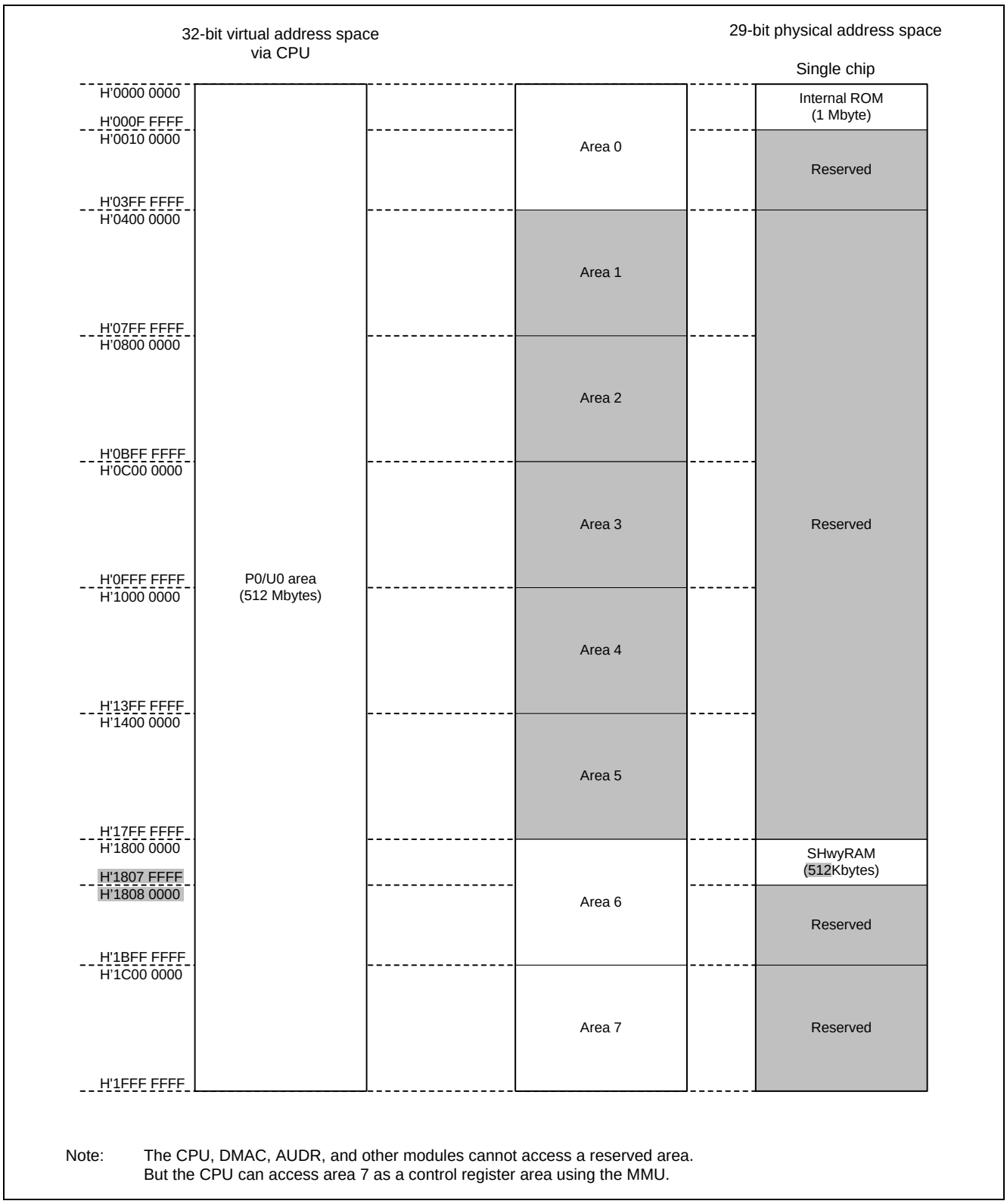
Product	Model	ROM Capacity	RAM Capacity	Package	FlexRay
SH74552	R5F74552KBG	1 Mbyte	IL memory: 8 Kbytes, OL memory: 16 Kbytes, and SHwyRAM: 256 Kbytes	PRBG0176GA-A	Yes
SH74562	R5F74562KBG				No
SH74572	R5F74572LBG				Yes
SH74582	**R5F74582KBG**		IL memory: 8 Kbytes, OL memory: 16 Kbytes, and SHwyRAM: **512** Kbytes		**Yes**
SH74593	R5F74593LBG	1.5 Mbytes	IL memory: 8 Kbytes, OL memory: 16 Kbytes, and SHwyRAM: 512 Kbytes		Yes

Appendix B

Appendix B.1

Section 11 Address Space

For details on the P0/U0 area to the P4 area, see figures 11.2 to 11.6.

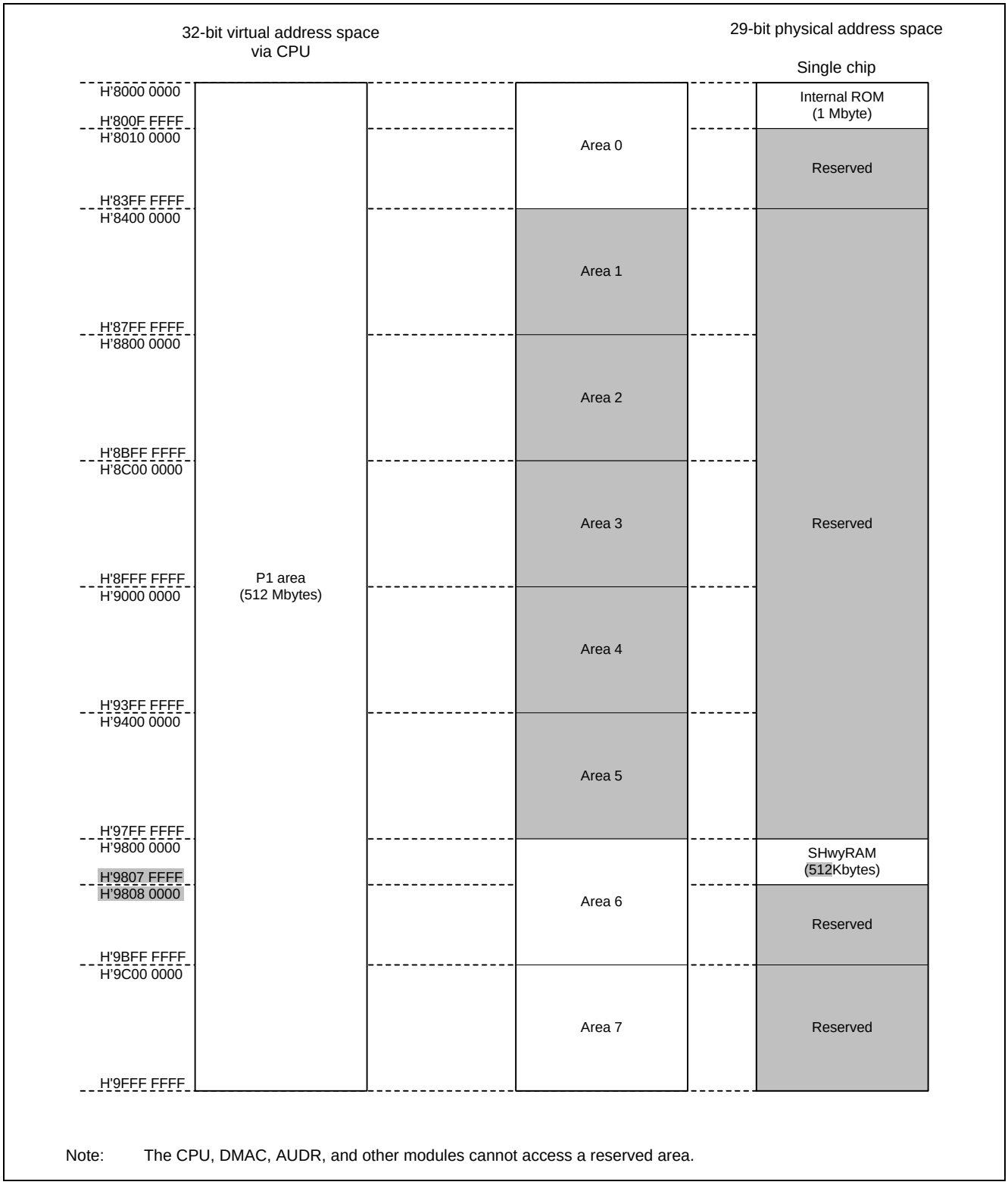


Note: The CPU, DMAC, AUDR, and other modules cannot access a reserved area.
But the CPU can access area 7 as a control register area using the MMU.

Figure 11.2 Address Space (P0/U0 Area)

Appendix B.2

Section 11 Address Space

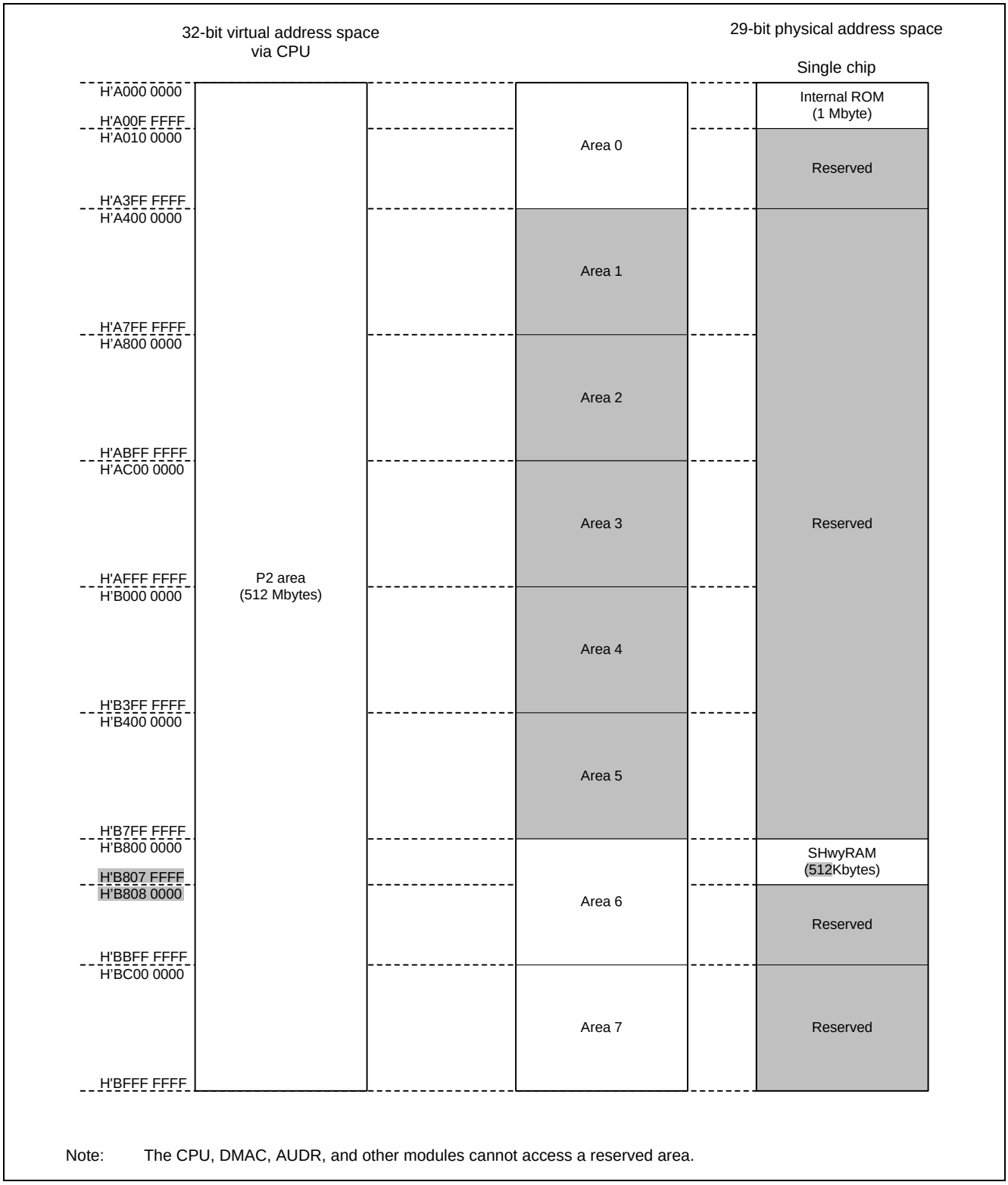


Note: The CPU, DMAC, AUDR, and other modules cannot access a reserved area.

Figure 11.3 Address Space (P1 Area)

Appendix B.3

Section 11 Address Space

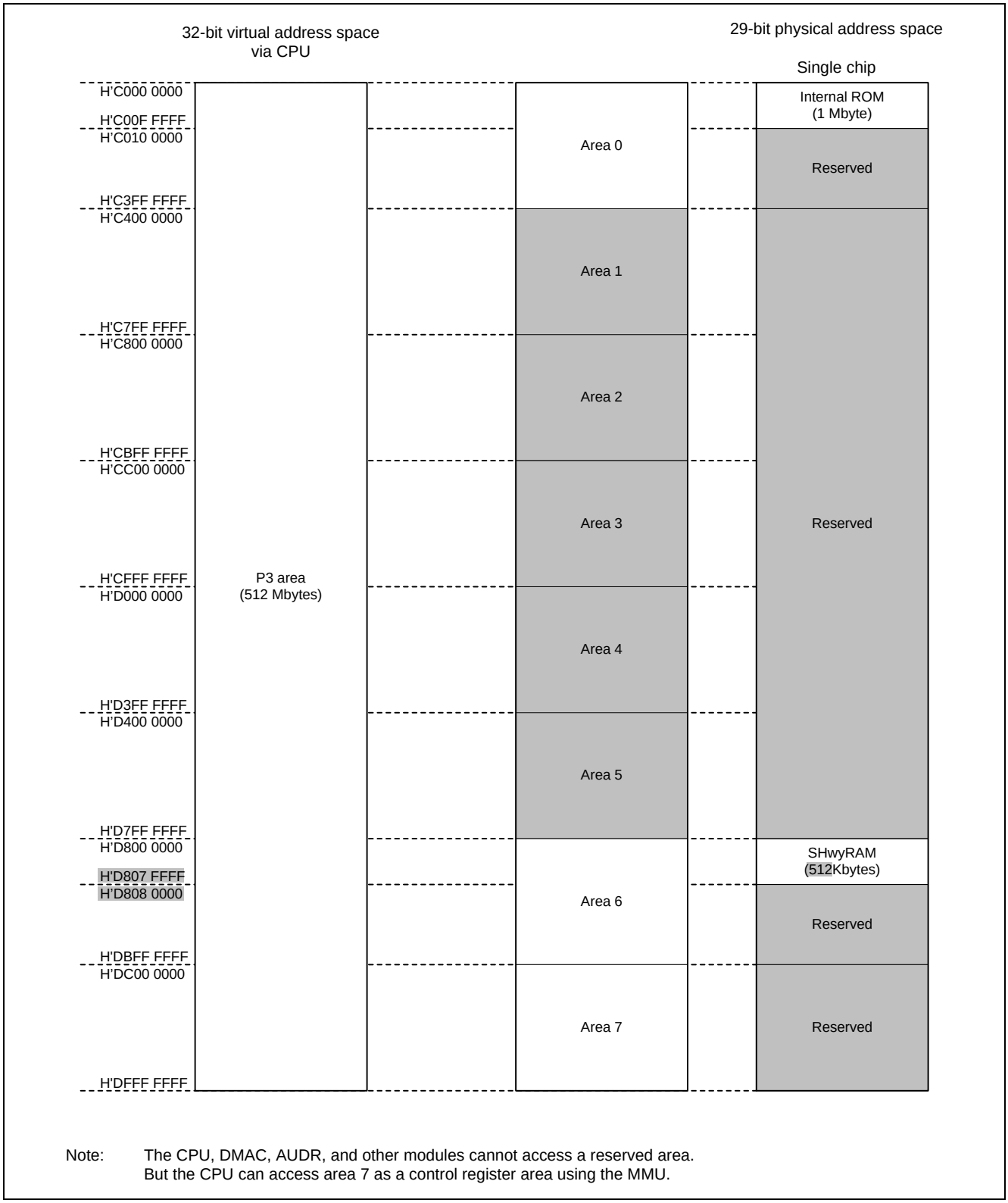


Note: The CPU, DMAC, AUDR, and other modules cannot access a reserved area.

Figure 11.4 Address Space (P2 Area)

Appendix B.4

Section 11 Address Space



Note: The CPU, DMAC, AUDR, and other modules cannot access a reserved area.
But the CPU can access area 7 as a control register area using the MMU.

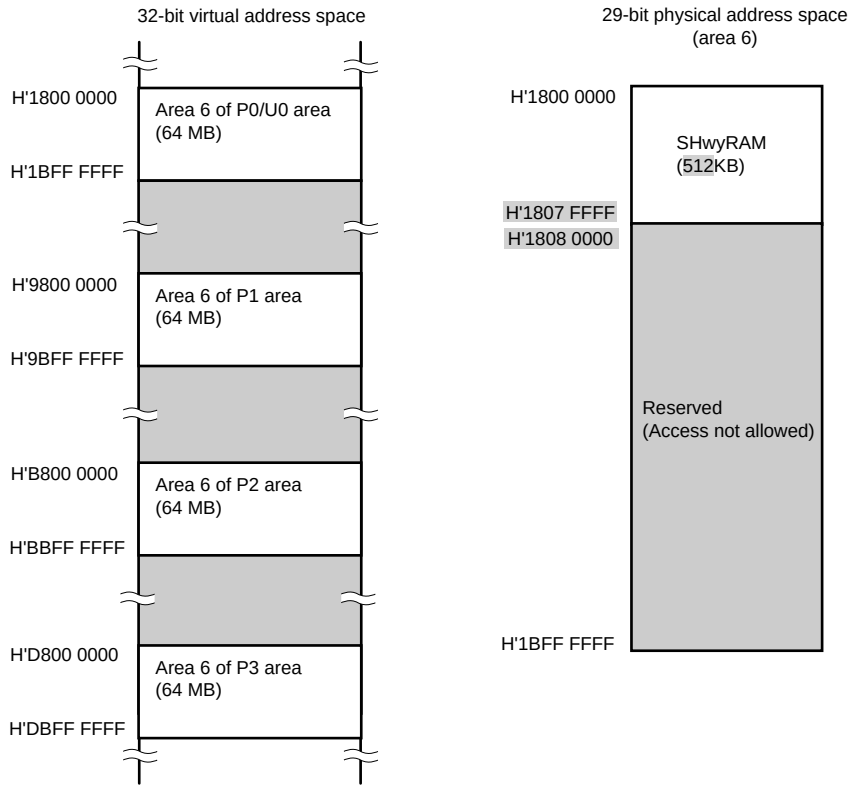
Figure 11.5 Address Space (P3 Area)

Appendix C

Section 13 SuperHyway RAM (SHwyRAM)

13.1 Overview

As shown in figure 13.2, the SHwyRAM is allocated to the upper **512** Kbytes of area 6 (H'1800 0000 to **H'1807 FFFF** in the 29-bit physical address space).



Page	Address (29-bit physical address)
Page 0	H'1800 0000 to H'1800 FFFF
Page 1	H'1801 0000 to H'1801 FFFF
Page 2	H'1802 0000 to H'1802 FFFF
Page 3	H'1803 0000 to H'1803 FFFF
Page 4	H'1804 0000 to H'1804 FFFF
Page 5	H'1805 0000 to H'1805 FFFF
Page 6	H'1806 0000 to H'1806 FFFF
Page 7	H'1807 0000 to H'1807 FFFF

Figure 13.2 Address Space

Appendix D

Section 28 Direct RAM Input Interface (DRI)

Appendix D.1

28.1 Overview

Table 28.1 lists the overview of the DRIi modules.

Table 28.1 DRIi Overview

Item	Description
Number of channels	3 channels
Operating frequency	80 MHz (when PAck = 80 MHz)
Transfer method	Clock synchronous parallel input
Access areas	All SHwyRAM areas (up to **512** Kbytes)
Maximum transfer rate	80 Mbytes/second (when the DRIi operating frequency is 80 MHz)
Minimum data acquisition period	The following are the minimum periods when the DRIi operating frequency is 80 MHz. 43.75 ns (special mode disabled and the input data bus width is 8 or 16 bits) 25 ns (special mode enabled)
Data acquisition bus width	8 or 16 bits
Event counter	16 bits × 6 counters (DEC5 to DEC0)
Bank switching function	Two banks can be specified as the data storage destination in SHwyRAM
Data acquisition edges	Either rising edges, falling edges, or both edges can be selected
Acquisition timing adjustment function	Sets the time between detection of the data acquisition edge and the acquisition operation
Decimation control function	Data can be acquired selectively using an event counter (DEC5 to DEC0)

Appendix D.2

28.3.23 DRIi Address Reload Registers 0 and 1 (DRIiADR0RLD and DRIiADR1RLD)

DRIiADR0CT and DRIiADR1CT are registers that hold counter reload values. When reload mode is selected with the DRIi transfer control register (DRIiTRMCNT) ADMD (address counter operating mode selection) bit, the corresponding DRIi address counters are reloaded with the values set in these registers when the DRIi data acquisition control register (DRIiDCAPCNT) DCPEN (acquisition enable) bit changes from "0" to "1".

Note: • These registers may only be rewritten when the DRIi data acquisition control register (DRIiDCAPCNT) DCPEN (acquisition enable) bit is in the "0" state.

DRI0 Address Reload Register 0 (DRI0ADR0RLD) <P4 address: location H'FFBF C024>
DRI1 Address Reload Register 0 (DRI1ADR0RLD) <P4 address: location H'FFBF D024>
DRI2 Address Reload Register 0 (DRI2ADR0RLD) <P4 address: location H'FFBF E024>

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	DRIAD0RLD		
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRIAD0RLD														—	—
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DRI0 Address Reload Register 1 (DRI0ADR1RLD) <P4 address: location H'FFBF C02C>
DRI1 Address Reload Register 1 (DRI1ADR1RLD) <P4 address: location H'FFBF D02C>
DRI2 Address Reload Register 1 (DRI2ADR1RLD) <P4 address: location H'FFBF E02C>

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	DRIAD1RLD		
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRIAD1RLD														—	—
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<After Reset: H'0000 0000>

Bit	Abbreviation	After Reset	R	W	Description
31 to 19	—	All 0	0	0	Reserved Bits These bits are always read as "0". The write value should always be "0".
18 to 2	DRIADmRLD	All 0	R	W	Address Bits 18 to 2 Reload Value (**512**-Kbyte area)
1, 0	—	All 0	0	0	Reserved Bits These bits are always read as "0". The write value should always be "0".

Legend: m = 0 or 1

Appendix D.3

28.3.24 DRIi Address Counters 0 and 1 (DRIiADR0CT and DRIiADR1CT)

The DRIiADR0CT and DRIiADR1CT counters are provided to specify bits A18 to A2 of the address in SHwyRAM that is the DRIi module transfer destination. Bits A31 to A19 are fixed at "0". These counters are incremented by "4" each time a DRIi transfer completes. There are two DRIi address counter operating modes, and applications can select the mode with the DRIi transfer control register (DRIiTRMCNT) ADMD bit. See the documentation of the DRIi transfer control register (DRIiTRMCNT) for details.

Notes:
- If a DRIi address counter value is a value other than an area in which SHwyRAM is located, the DRIi module will behave as though the DRIi transfers complete, but no writes of the acquired data will be performed whatsoever.
- A DRIi address counter is incremented by "4" when a DRIi transfer completed. This is performed for the one that is active at that time according to the setting of the DRIi transfer control register (DRIiTRMCNT) ADSL (address counter selection) bit.
- These registers must only be rewritten in the state where a DRIi transfer counter (DRIiTRMCT) underflow has occurred (the counter is stopped at the value H'0000 0000).

DRI0 Address Counters 0 (DRI0ADR0CT) <P4 address: location H'FFBF C028>
DRI1 Address Counters 0 (DRI1ADR0CT) <P4 address: location H'FFBF D028>
DRI2 Address Counters 0 (DRI2ADR0CT) <P4 address: location H'FFBF E028>

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	DRIAD0		
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRIAD0														—	—
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DRI0 Address Counters 1 (DRI0ADR1CT) <P4 address: location H'FFBF C030>
DRI1 Address Counters 1 (DRI1ADR1CT) <P4 address: location H'FFBF D030>
DRI2 Address Counters 1 (DRI2ADR1CT) <P4 address: location H'FFBF E030>

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	DRIAD1		
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRIAD1														—	—
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<After Reset: H'0000 0000>

Bit	Abbreviation	After Reset	R	W	Description
31 to 19	—	All 0	0	0	Reserved Bits These bits are always read as "0". The write value should always be "0".
18 to 2	DRIADn	All 0	R	W	Destination Address Bits 18 to 2 (**512**-Kbyte area)
1, 0	—	All 0	0	0	Reserved Bits These bits are always read as "0". The write value should always be "0".

Legend: n = 0 or 1

Appendix E

Section 29 Direct RAM Output Interface (DRO)

29.1 Overview

Table 29.1 lists the overview of the DRO module.

Table 29.1 DRO Module Overview

Item	Description
Transfer method	Parallel strobed output
Access area	SHwyRAM area (**512** Kbytes)
Output data width	Either 8-bits or 16-bits
Maximum transfer clock	10 MHz
Maximum transfer rate	20 Mbytes/s (when 16 bits is selected, Pck = 40MHz)
Strobe polarity	Either "H" active or "L" active may be selected.
Timing adjustment function	The setup and hold times can be programmed in 1Pck units relative to the strobe signal edge.
Interrupt request	An interrupt request is generated after a prespecified number of data items have been output.

REVISION HISTORY	SH74582 Datasheet

Rev.	Date	Description	
		Page	Summary
1.10	Oct 20, 2014	-	First edition issued
1.11	Feb 18, 2015	1	Corrected SHwyRAM capacity of R5F74572LBG. (Error) 512K -> (Correct) 256K