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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A826A/E	Rev.	1.00
Title	SH7450 Group, SH7451 Group User's Manual Hardware Errata Rev.A		Information Category	Technical Notification		
Applicable Product	SH7450 Group, SH7451 Group	Lot No.	Reference Document	SH7450 Group, SH7451 Group User's Manual: Hardware Rev.1.10 (R01UH0286EJ0110)		

Since we changed the following contents of "SH7450 Group, SH7451 Group User's Manual: Hardware Rev.1.10(Published on September 27, 2011)", we announce you.

Please use attached errata in the case of use of SH7450 Group, SH7451 Group User's Manual: Hardware Rev.1.10.

Appending Document:" SH7450 Group, SH7451 Group User's Manual: Hardware Rev.1.10" errata REV.A – 3 sheets

* In the following, the portion of net credit ( ) or an underline is a portion with an addition/change.

Rev.	Page	Part	Contents
Adds by REV.A	Revision History - xiii	26.3.14 CANi Status Register	Revision History: Description of CAN added -Page of Previous Edition: 26-49 -Description: Description of the bit 1 (SDST bit) in the CANi Status Register (CiSTR) (i=0 to 4) corrected Error: The SDST bit is set to "1" when at least one SENTDATA bit in the CiMCTLj register is "1" regardless of the value of the CiMIER register. Correct: The SDST bit is set to "1" when at least one SENTDATA bit in the CiMCTLj (j = 32 to 63) register is "1" regardless of the value of the CiMIER register. -Page of Previous Edition: 26-49 -Description: Description of the bit 0 (NDST bit) in the CANi Status Register (CiSTR) (i=0 to 4) corrected Error: The NDST bit is set to "1" when at least one NEWDATA bit in the CiMCTLj register is "1" regardless of the value of the CiMIER register. Correct: The NDST bit is set to "1" when at least one NEWDATA bit in the CiMCTLj (j = 0 to 63) register is "1" regardless of the value of the CiMIER register.
Adds by REV.A	Revision History - xv	32.5.1 FlexRay Error Interrupt Register	Revision History: Description of FlexRay added -Page of Previous Edition: 32-17 -Description: Description of the bit 24 (EDB bit) in the FlexRay Error Interrupt Register (FREIR) corrected Error: 0: No error detected on channel B RW Correct: 0: No error detected on channel B -Page of Previous Edition: 32-18 -Description: Description of the bit 9 (IIBA bit) in the FlexRay Error Interrupt Register (FREIR) corrected Error: 0: No illegal CPU access to Output Buffer occurred 1: Illegal CPU access to Output Buffer occurred Correct: 0: No illegal CPU access to Input Buffer occurred 1: Illegal CPU access to Input Buffer occurred
Adds by REV.A	Revision History - xvi	Appendix A CPU Operation Mode Register	Revision History: Description of Appendix A added -Page of Previous Edition: A-1 -Description: Value after reset of the bit 5 (RABD bit) in the CPU Operation Mode Register (CPUOPM) revised Error: Value after reset of the RABD bit is "1" Correct: Value after reset of the RABD bit is " 0"
Adds by REV.A	32-76	32.7.1 FlexRay CC Status Vector Register	Description of the bit 29 to 24 (PSL5 to PSL0 bit) in the FlexRay CC Status Vector Register (FRCCSV) corrected Error: Set to B'000100 when leaving HALT state. Correct: Set to B'000000 when leaving HALT state.

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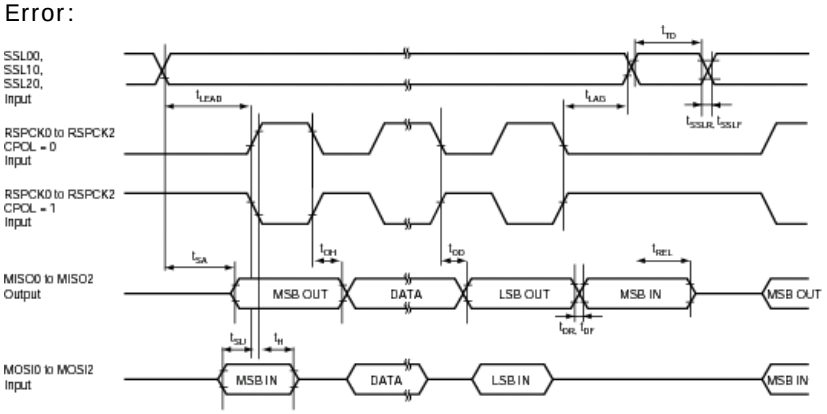
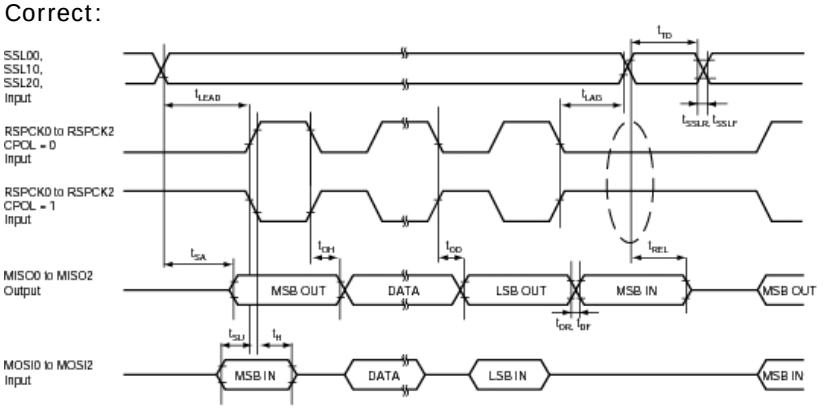
<tr><td>Adds by REV.A</td><td>38-33</td><td>Table 38.26 RSPI Timing</td><td>
Table 38.26 RSPI Timing : Incorrect description corrected.
Error:
<table>
<tr><th colspan="2">Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
<tr><td>Data input setup time</td><td>Slave</td><td>t_{SU}</td><td>25 + 2 x t_{cyc}</td><td>-</td><td>ns</td><td>38.28 to 38.31</td></tr>
</table>
Correct:
<table>
<tr><th colspan="2">Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
<tr><td>Data input setup time</td><td>Slave</td><td>t_{SU}</td><td>25 - 2 x t_{cyc}</td><td>-</td><td>ns</td><td>38.28 to 38.31</td></tr>
</table>
</td></tr>
<tr><td>Adds by REV.A</td><td>38-35</td><td>Figure 38.30 RSPI Timing (Slave, CPHA = "0")</td><td>
Figure 38.30 RSPI Timing (Slave, CPHA = "0") : Incorrect description corrected. O in a figure shows the added part.
Error:


Correct:


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Error:
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<tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
<tr><td>DIN2 to DIN4 sampling edge undefined time before DIN1 initialization level release (when direct reset is selected)</td><td>tar</td><td>8</td><td>-</td><td>ns</td><td rowspan="2">38.33 to 38.36</td></tr>
<tr><td>DIN2 to DIN4 sampling edge undefined time before DIN1 initialization level release</td><td>tbr</td><td>12</td><td>-</td><td>ns</td></tr>
</table>
Correct:
<table>
<tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
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Error:
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<tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
<tr><td>AUDRD output delay time before AUDRCLK</td><td>td(AUDRCLKH-AUDRD)</td><td>-</td><td>35</td><td>ns</td><td>38.46</td></tr>
</table>
Correct:
<table>
<tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
<tr><td>AUDRD output delay time after AUDRCLK</td><td>td(AUDRCLKH-AUDRD)</td><td>-</td><td>35</td><td>ns</td><td>38.46</td></tr>
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<tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
<tr><td>AUDRD output delay time before AUDRCLK</td><td>td(AUDRCLKH-AUDRD)</td><td>-</td><td>40</td><td>ns</td><td>38.46</td></tr>
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Correct:
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<tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
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