Section 1 Overview

1.1 Features

This LSI includes 1.8 GHz Quad Arm® Cortex®-A55 on-chip FPU, Neon™, L1-caches and L3-cache, 800 MHz Dual Arm® Cortex®-R8 on-chip FPU, TCM, and L1-cache, 200MHz Arm® Cortex®-M33 on-chip FPU and DSP-extension, DRP-AI, Mali™-G31 (GE3D), Mali™-C55 (ISP), 6 MB of on-chip SRAM, 2ch GbEthernet MAC, USB2.0, USB3.2 Gen 2x1, 4-MIPI® CSI-2® camera input interface, 1-MIPI® DSI® video output interface, PCIe® Gen3 4Lane or 2-2Lane (EP/RC), various communication interfaces such as xSPI, eMMC™, I2S (TDM), I3C®, PDM, and security functions.

■ CPU

- On-chip Quad 64-bit Arm® Cortex®-A55 Core processors

  Application processing (up to 1.8 GHz)
- On-chip Dual 32-bit Arm® Cortex®-R8 (MPCore™) processors

  Real-time processing (up to 800 MHz)
- 32-bit Arm® Cortex®-M33 processor

  System management (up to 200 MHz)

■ Accelerator engines

- AI accelerator (dynamically reconfigurable processor for AI (DRP-AI))
- Dynamically reconfigurable processor (DRP)
- 3D graphics engine (GE3D) (option)
- Image signal processor (ISP) (option)
- Image scaling unit (ISU)
- Video codec unit (VCD)

■ On-chip SRAM and external memory interfaces

- On-chip shared SRAM (6-Mbyte on-chip SRAM with ECC)
- External DDR memory interface

  2-channel memory controller for LPDDR4-3200 or LPDDR4X-3200 with a 32-bit bus width
- xSPI interface
- SDHI (eMMC/SD (1-, 4-, 8-bit bus width) supported)

■ Boot

- Selectable boot CPU from Cortex®-M33 or Cortex®-A55

■ Extended-function timers

- 32-bit general-purpose timer (16 ch.)
- 32-bit CMTW (8 ch.)

■ Various communication/storage/network interfaces

- Ethernet (2 ch.: 10/100/1000 BASE)
- USB2.0 (1 ch.: Host/Function, 1 ch.: Host-only)
- USB3.2 Gen2 × 1 (2 ch.: Host-only)
- PCIe Gen3 (1, 2, or 4 lanes × 1 pair or 1 or 2 lanes × 2 pairs)
- MIPI CSI-2 (4 ch.: 1, 2, or 4 lanes)
- MIPI DSI (1 ch.: 1, 2, or 4 lanes)
- CAN/CANFD (compliant with ISO11898-1) (6 ch.)
- SCI (10 ch.: UART/SPI/I2C-host)
- SPI (3 ch.)
- I2C (9 ch.)
- I3C (1 ch.)

■ Audio

- Asynchronous sampling rate converter unit (SCU) (up to 192 kHz)
- DMAC for Audio (ADMAC) is available to transfer audio formats of I2S with SCU.
- Flexible audio clock generator (ADG) for audio functions.
- I2S (TDM) input/output interfaces (half-duplex 10 ch.; full-duplex 5 ch.)
- SPDIF input/output interfaces (3 ch.)
- Pulse density modulation (PDM) input interfaces (6 ch.)

■ Analog/Digital converter (ADC) and sensors

- 2.5 Msps 12-bit ADC (8 ch.)
- Internal temperature sensors (2 ch.)

■ Security

- Hardware cryptographic engine (option)

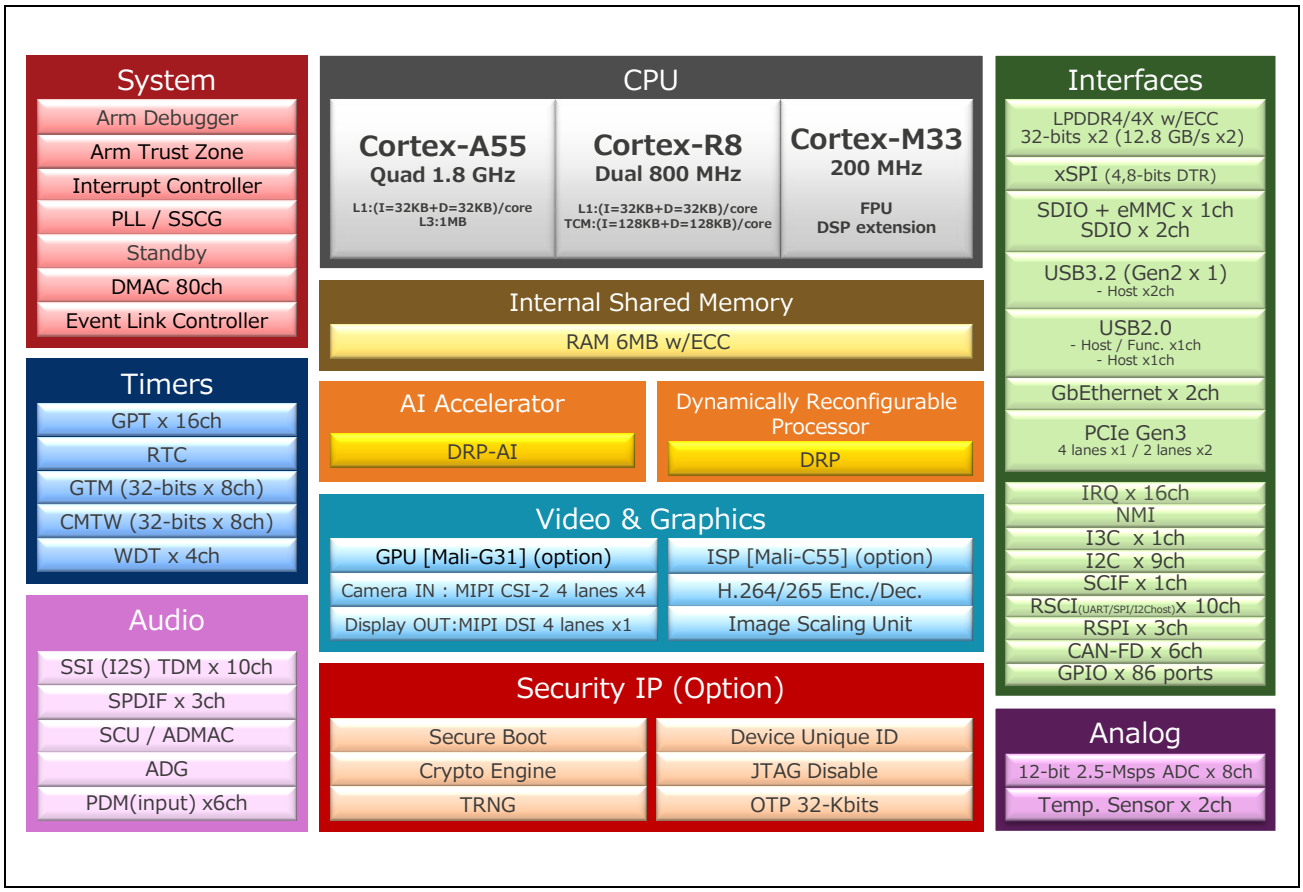


Figure 1.1-1 Diagram of Functional Overview

1.2 Product Lineup

Table 1.2-1 Product Lineup

Group	Name	Part Number	GE3D	Security	ISP
RZ/V2H	RZ/V2H	R9A09G057H41GBG	N/A	N/A	N/A
		R9A09G057H42GBG	Available (Mali-G31)		
		R9A09G057H45GBG	N/A	Available	
		R9A09G057H46GBG	Available (Mali-G31)		
	RZ/V2HP	R9A09G057H44GBG	Available (Mali-G31)	N/A	Available (Mali-C55)
		R9A09G057H48GBG	Available (Mali-G31)	Available	

1.3 Functions

The following tables list the functions of this LSI.

Table 1.3-1 CPU

Item	Description
Application Processor Cortex-A55 (CA55)	• Arm Cortex-A55 Quad Core 1.8 GHz with 0.9 V, 1.1 GHz with 0.8 V • L1 I-cache 32 Kbytes (with parity) and D-cache 32 Kbytes (with ECC) per core • L2 cache: 0 Kbytes • L3 cache: 1 Mbyte (with ECC)*1 • MMU supported • Neon™ and FPU supported • Cryptographic extension supported (for security-supported products only) • Armv8-A architecture
Realtime Processor Cortex-R8 (CR8)	• Arm Cortex-R8 Dual MPCore 800 MHz • L1 I-cache 32 Kbytes (with ECC) and D-cache 32 Kbytes (with ECC) pre core • I-TCM 128 Kbytes (with ECC) and D-TCM 128 Kbytes (with ECC) pre core • VFPv3, double precision • Armv7-R architecture • No support for dual-link lock-step technology
System Manager Cortex-M33 (CM33)	• Arm Cortex-M33 processor 200 MHz • FPU supported • DSP extension supported • Security extension supported • Armv8-M architecture
Debug Interface	• Arm® CoreSight® architecture • JTAG and SWD interfaces supported • ETF: Total of 60 Kbytes for program flow tracing • JTAG disabling supported (option)
Boundary Scan	• Boundary scan based on IEEE 1149.1 via the JTAG interface is supported. • Note that some module pins are not available on this boundary scan.

Note 1. The maximum operating frequency of the L3 cache is 1.26 GHz.

Table 1.3-2 Accelerator Engines

Item	Description
Dynamically reconfigurable processor (DRP)	• DRP (DRP1)
AI accelerator (DRP-AI)	• DRP-AI (AI-MAC + DRP0) • Up to 8 dense TOPS • Up to 80 sparse TOPS
3D Graphics Engine (GE3D) (option)	• Arm Mali-G31 • One single-pixel shader core • 8-Kbyte L2 cache • OpenGL ES™ 1.1, 2.0, and 3.2 supported • OpenCL 2.0 full profile supported
Image Signal Processor Unit (ISP) (option*) *RZ/V2HP only	• Arm Mali-C55 • 1 unit, supporting 4K • Maximum pixel rate: 630 Mpixels/s • Supports the functions below: – Black level correction – WB gain – Defect pixel correction – Color correction – Gamma correction – Edge enhancement and sharpness filter – Down-scaling and cropping – Dynamic range correction – 2-exprosure HDR – Shading correction • Supports input formats: RAW8, 10, 12, 14, 16, 20 • Supports output formats: YUV422, YUV420, RGB
Image Scaling Unit (ISU)	• Scaling down function with bilinear interpolation • Input image size (max): 4096 × 4096 • Output image size (max): 4096 × 4096 • Supports color format conversion (YCbCr422, YcbCr420, RGB)
Video Codec Unit (VCD)	• H.264/H.265 codec module • Support for encoding and decoding – H.264/AVC (High Profile, level 4.2; Main Profile, level 4.2; Baseline Profile, level 4.2) – H.265/HEVC (Main Profile, level 5) • Maximum size – (H.264) 1920 × 1080 × 60 fps*1 – (H.265) 3840 × 2160p × 30 fps*1

Note 1. Maximum frame rate for this size. The number of streams can be defined within this specification by software.

Table 1.3-3 On-chip SRAM and External Memory Interfaces

Item	Description
System RAM	• 6 Mbytes (with ECC)
External Bus Controller for LPDDR4/4X SDRAM (DDR)	• 2 channels • Support for LPDDR4-3200 and LPDDR4X-3200 • Bus width: 32-bits • In line ECC (16 ECC regions) supported (support for error detection interrupts) • Memory size: Up to 16 Gbytes (8 Gbytes per channel) • Auto-refresh, self-refresh, and IO retention supported • Memory access protection for secure regions using TZC-400 (Arm® TrustZone® supported)
xSPI Controller (xSPI)	• 1 channel (2 chip select signals) • Compliant with the xSPI protocol • Protocol mode 1, 4, or 8 pins with SDR or DDR (1S-1S-1S, 4S-4D-4D, 8D-8D-8D) 2 or 4 pins with SDR (1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S) • Support for XiP mode • Support for up to 256-Mbyte address space (support for up to 128M bytes per channel address space in boot sequence)
SD Card Host Interface/ Multimedia Card Interface (SD/MMC)	• 3 channels • Channel 0 supports SDHI and e-MMC. • Channels 1 and 2 support SDHI. • SD memory I/O card interface (1-bit or 4-bit SD bus) • SD, SDHC and SDXC SD memory card access supported • Compliant with SD specification version 3.01 • Default, high-speed, UHS-I/SDR50, SDR104 and DDR50 transfer modes supported • Error check function: CRC7 (command), CRC16 (data) • Support for card detection and write protection • MMC interface (1-bit, 4-bit, or 8-bit MMC bus) • e-MMC device access supported • Compliant with eMMC 4.51 • High-speed, HS200 and HS-DDR transfer modes supported

Table 1.3-4 Boot

Item	Description
Boot	• Boot CPU selectable as CA55 and CM33 • CM33 boot – Boot mode 2: Booting from a serial flash memory connected to the xSPI bus space – Boot mode 3: Booting from SCIF download • CA55 boot – Boot mode 0: Booting from SD – Boot mode 1: Booting from eMMC – Boot mode 2: Booting from a serial flash memory connected to the xSPI bus space – Boot mode 3: Booting from SCIF download *Note:* 1.8 V or 3.3 V selectable for eMMC and xSPI interfaces.

Table 1.3-5 System, Data Transfer, Enhanced Interrupt Controller Unit, Clock Functions

Item	Description
Direct Memory Access Controller (DMAC)	• 80 channels • Transfer modes: Single transfer mode and block transfer mode • LINK mode (DMA transfer under descriptor control) supported • Transfer size: 1, 2, 4, 8, 16, 32, 64, or 128 bytes • Transfer request: Software trigger, external DMA requests (DREQ) and interrupt requests from peripheral functions • A specific DMA transfer interval can be specified to adjust the bus occupancy.
Clock Pulse Generator (CPG)	• Generates the clocks from an external clock or external resonator (24 MHz). – Maximum CA55 clock: 1.8 GHz (0.9 V), 1.1GHz (0.8 V) – Maximum CR8 clock: 800 MHz – Maximum CM33 clock: 200 MHz – Maximum DDR clock: 800 MHz (LPDDR4/4X-3200) – Maximum GE3D clock: 630 MHz – Maximum ISP clock: 630 MHz – Maximum H.264/H.265 clock: 400 MHz – Maximum system bus clock: 400 MHz • SSC (spread spectrum clock) supported
Interrupt Controller (GIC)	• Arm® CoreLink® generic interrupt controller (GIC-600) for CA55 • 32 priority levels available • Nested vectored interrupt controller (NVIC) for CM33 • Integrated interrupt controller (NVIC) for CR8 • External Interrupt pins (NMI, IRQ0 to IRQ15, and TINT0 to TINT31) • On-chip peripheral Interrupts: Priority level set for each module
Event Link Controller (ELC)	• Up to 455 event signals can be interlinked with the operation of modules. • In particular, the operation of timer modules can be started by input event signals. • Event-linked operation of signals of 16 port pins,P60 to 67 and P80 to 87, is to be possible.
Error Controller	• Error events from CPU and peripherals are captured and merged to interrupt with mask for CA55 and CM33 respectively. • System reset can be generated by error events.
Message Handling Unit (MHU)	• Message handling function between each core of CA55, CR8 and CM33 • Assert interrupts to inform messages and responses from/to every core

Table 1.3-6 Various Communication/Storage/Network Interfaces (1/3)

Item	Description
USB3.2 Host (USB3)	• 2 channels • Compliant with USB3.2 Gen2 × 1 • Maximum rate: 10 Gbps • Support for control, bulk, interrupt, and isochronous transfer • Internal dedicated DMA
USB2.0 Host/Function (USB2)	• 2 channels (ch. 0: Host/Function; ch. 1: Host-only) • Compliant with USB2.0 • Support for On-The-Go (OTG) functionality (ch. 0 only) • Support for control, bulk, interrupt, and isochronous transfer • Internal dedicated DMA
PCIe Express® 3.0 (PCIE)	• PCIe Gen3 • Root complex or Endpoint selectable • Lane configuration selectable from below: – 1, 2, or 4 lanes × 1 channel – 1 or 2 lanes × 2 channels
MIPI CSI-2 Interface with camera image processing (CRU)	• 4 channels • Number of lanes: 1, 2, or 4 lanes per channel • Maximum bandwidth: 2.1 Gbps per lane • Support for the throughput up to 4K RAW12 60 fps • Support for 4 virtual channels selected from VC0 to VC15 • Support for input data formats: – YUV422 8 bits or 10 bits – RGB444, RGB555, RGB565, RGB666, RGB888 – RAW6, RAW7, RAW8, RAW10, RAW12, RAW14, RAW16, RAW20 – YUV420 8-bits or 10-bits (image processing not supported) – Legacy YUV420 8-bits (image processing not supported) – YUV420 8-bits or 10-bits (chroma shifted pixel sampling) (image processing not supported) – User defined byte-based data • The other formats from the MIPI CSI-2 interface can also be output without image processing. • Generic long packet data types 1 to 4 • User defined 8-bit data types 1 to 8
MIPI DSI Interface with LCD controller (LCDC)	• 1 channel • Number of lanes: 1, 2, or 4 lanes • Support for the throughput up to 1920 × 1200 RGB888 60 fps • Support for the throughput up to 1280 × 1024 RGB888 120 fps • Maximum bandwidth: 1.5 Gbps per lane • Support for 2-plane blending (with the ability to blend 2 differently sized images) • Support for image processing: – Dither processing (RGB666) – Clipping – RGB gamma correction LUT • Support for input data formats: – RGB565, RGB666, RGB888 – ARGB1555, ARGB4444, ARGB8888 – YUV (YcbCr) 444 8-bits, YUV (YcbCr) 422 8-bits, YUV (YcbCr) 420 8-bits • Support for output data formats: – RGB666, RGB888

Table 1.3-6 Various Communication/Storage/Network Interfaces (2/3)

Item	Description
Gigabit Ethernet Interface (GBETH)	• 2 channels • Compliant with IEEE802.3 • Compliant with IEEE802.1Qav, IEEE802.1Qat, and IEEE802.1AS • Compliant with IEEE1588-2008 with nano second timer in ch. 0 (main) and ch. 1 (sub) • Support for 10BASE, 100BASE, and 1000BASE • Support for full duplex and half duplex • Support for RGMII and MII Interfaces
CANFD Interface (CANFD)	• 6 channels • CAN-FD ISO 11898-1 (2015) compliant • Support for up to 8 MHz with payload transfer • Message buffer – 64 transmit message buffers per channel – 256 shared buffers for RXMB and FIFO buffers per channel
I3C Bus Interface (I3C)	• 1 channel • Support for 1.2 V and 1.8 V • Master or Slave mode selectable • Support for the multi-master • Compliant with MIPI I3C v1.0 and I3C Basic v1.0 The following functions are not supported: – Bridge device (I3C v1.0 and I3C Basic v1.0) – Asynchronous timing control async mode 2 & 3 (I3C v1.0) • Support for DMAC and event linking
I2C Bus Interface (RIIC)	• 9 channels • Master or Slave mode selectable • Support for the multi-master • Support for Standard mode (100 kHz), Fast mode (400 kHz), and Fast mode+ (1 MHz) • Support for DMAC and event linking
Renesas Serial Communication Interface (RSCI)	• 10 channels • 6 communication modes – Asynchronous interfaces – 8-bit clock synchronous interface – Simple IIC (host-only) – Simple SPI (with one chip select signal) – Smart card interface – Simple LIN (expanded SCIX mode) • 32-stage FIFO registers for transmission and reception • Clock source selectable from among four internal clock signals • Bit rate specifiable with the on-chip baud rate generator • Full-duplex and half-duplex communications • Data length: 7 to 9 bits • Bit-rate modulation • Double speed mode • Loopback function to enable self-diagnosis • Support for DMAC and event linking • Support for CRC calculation by the CRC unit

Table 1.3-6 Various Communication/Storage/Network Interfaces (3/3)

Item	Description
Renesas Serial Peripheral Interface (RSPI)	• 3 channels • SPI transfer facility The MOSI (master out slave in), MISO (master in slave out), SSL (slave select, 4 channels available), and RSPCK (SPI clock) signals enable serial transfer through SPI operation (four lines). The MOSI, MISO, and RSPCK signals enable clock-synchronous operation (three lines). Capable of handling serial transfer as a master or slave. • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or 20, 24, or 32 bits. 32-bit × 16-stage buffers for transmission and reception. Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits). • Buffered structure Independent 16 stages and channels for MOSI and MISO Double buffers for both transmission and reception • RSPCK can be stopped automatically with the reception buffer full for master reception. • Support for DMAC and event link • Support for CRC calculation by the CRC unit
CRC Calculator (CRC)	• 1 channel • CRC code generation for arbitrary amounts of data in 8-, 16-, or 32-bit units • Select any of four generating polynomials: – X32+X26+X23+X22+X16+X12+X11+X10+X8+X7+X5+X4+X2+X+1 (CRC-32) – X32+X28+X27+X26+X25+X23+X22 +X20+X19+X18+X14+X13+X11+X10+X9+X8+X6+1 (CRC-32C) – X16+X15+X2+1(CRC-16) – X16+X12+X5+1 (CRC-CCITT) – X8+X2+X+1 (CRC-8) • Support for RSCI and RSPI interfaces
Serial Communication Interface with FIFO (SCIF)	• 1 channel • Asynchronous mode • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud-rate generator • Separate 16-byte FIFO registers for transmission and reception

Table 1.3-7 Extended-Function Timers

Item	Description
General-Purpose Timer (GPT)	• 32 bits × 16 channels • Counting up or down (sawtooth-wave), counting up and down (triangle-wave) selectable for all channels • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Enabling synchronized operation of the several counters between 2 units • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Automatic generation of three-phase PWM waveforms incorporating dead times through the combination of three counters • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: Software and compare-match • Generation of triggers for A/D converter conversion • Digital noise filter functions for signals on the input capture and external trigger pins • Event linking by the ELC • Support for phase counting mode
Port Output Enable for GPT (POEG)	• Controlling the output disable for GPT waveform output • Initiation by input level detection of GTETRG pins • Initiation by an output disable request from GPT • Initiation by detection of oscillation stopping or by software
Compare Match Timer W (CMTW)	• 32 bits x 8 channels • Compare-match, input-capture input, and output-comparison output are available (ch. 0 to ch. 3) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events
Watchdog Timer (WDT)	• 4 channels • A counter underflow can reset the LSI.
General Timer (GTM)	• 32 bits x 8 channels • Two operating modes: – Interval timer mode – Free-running comparison mode
Real Time Clock (RTC)	• A 100-year calendar from 2000 to 2099 • BCD code display • Clock source is an oscillator dedicated to RTC (32.768-kHz) • Automatic adjustment function for leap years • Alarm function

Table 1.3-8 Audio

Item	Description
Sampling Rate Converter Unit (SCU)	• 10 channels • Sampling rate: Up to192 kHz • Asynchronous/synchronous sampling rate conversions are available. • Support for resolutions of up to 24 bits • High-sound-quality type (THD + N*1 is −132 dB) and general-sound-quality type (THD + N*1 is −96 dB) • Automatically generates antialiasing filter coefficients • Four modules support one, two, four, six, or eight channels, and six modules support one or two channels. *Note 1.* Total harmonic distortion plus noise
Audio Clock Generator Unit (ADG)	• Supplies clock signals to the SSIU, SCU and SPDIF module.
Direct Access Memory Controller for Audio (ADMAC)	• Allows transfer of L/R data via I2S • 29 channels • Controls data transfer between the audio modules (SSIU, SCU)
Serial Sound Interface Unit (SSIU)	• 10 channels for half-duplex communication with transmit or receive function • 5 channels for full-duplex communication (full-duplex paring: ch. 0 & 9, ch.1 & 2, ch. 3 & 4, ch. 5 & 6, ch. 7 & 8) • Support for I2S, monaural, and TDM audio formats • Support for master and slave functions • Generation of programmable word clocks and bit clocks • Multi-channel formats • Support for 8, 16, 18, 20, 22, 24, and 32-bit data formats • Support for WS (word select) signal continuation with which the WS signal is not stopped • Support for DMAC
SPDIF Interface (SPDIF)	• 3 channels • Support for the IEC 60958 standard (stereo and consumer use modes only) • Sampling frequencies of 32 kHz, 44.1 kHz, and 48 kHz • Audio word sizes of 16 to 24 bits per sample • Bi-phase mark encoding • Double buffered data • Parity encoded serial data • Support for DMAC
Pulse Density Modulation (PDM)	• 6 channels • Direction: Input • Sampling rate: 8, 10, 12, 15, 16, 20, 24, 25, 30, 40, or 48 kHz • Capable of filtering 1-bit digital input data and converting them into 20-bit or 16-bit digital data • Support for the stereo microphone (L/R sampling by rising/falling clock edge) • Support for the sound activity detector to wake up CPU from WFI • Support for DMAC

Table 1.3-9 12-bit Analog to Digital Converter

Item	Description
A/D Converter (ADC0)	• 8 channels • Resolution: 12 bits • Input range: 0 V to 1.8 V • Conversion rate: 2.5 Msps, 2.0 Msps, 1.0 Msps, 0.5 Msps, 0.25 Msps • Operation mode: Single scan, continuous scan, group scan • Condition for starting A/D conversion – Software trigger – Asynchronous trigger: External ADTRG trigger supported – Synchronous trigger: ELC and GPT timers • Interrupt sources: A/D scan end, window compare match, compare match/mismatch, data register overwrite

Table 1.3-10 Internal Sensors

Item	Description
Temperature Sensor Unit (TSU)	• 2 channels for internal temperature • Includes a 12-bit A/D convertor per unit • Resolution: 0.0625°C/code • Rang: −40°C to 125°C • Precision: ±5°C • Conversion rate: 14.9 ksps • Operation mode: Single scan • Condition for starting measurement – Software trigger – Synchronous trigger: ELC • Interrupt sources: Conversion end, window compare match

Table 1.3-11 Security

Item	Description
Trusted Secure IP (option)	• Security algorism – Common key encryption: AES – Non-common key encryption: RSA, ECC • Other features – TRNG (true-random number generator) – Hash value generation: SHA-1, SHA-224, SHA-256, GHASH – Support for unique ID

Table 1.3-12 General-Purpose I/O Pins

Item	Description
General-purpose I/O ports (GPIO)	• Multiple I/O pins: 86 pins • Selectable: Pulling up or down by register settings • Selectable: N-ch. open-drain mode, Schmitt mode • 3.3-V tolerant pins available for use: 75 • 1.8-V tolerant pins available for use: 2 • Selectable IO-voltages for eight power blocks (7 blocks: 1.8 V or 3.3 V; 1 block: 1.2 V or 1.8 V)

Table 1.3-13 Power Supply Voltage

Item	Description
Power supply voltage	• VDD (core): 0.8 V • VDD (CA55): 0.8 V or 0.9 V • VDD (ADC, TSU, OTP): 1.8 V • VDD (DDR IO): 1.1 V, 0.6 V (only 0.6 V: for LPDDR4X) • VDD (MIPI DPHY): 1.2 V, 1.8 V (only 1.8 V: for MIPI CSI-2) • VDD (others): 1.8 V, 3.3 V

Table 1.3-14 Temperature Range

Item	Description
Junction temperature (Tj)	• −40°C to +125°C

Table 1.3-15 Quality Level

Item	Description
Quality level	• Industrial usage, etc.

1.4 Block Diagram

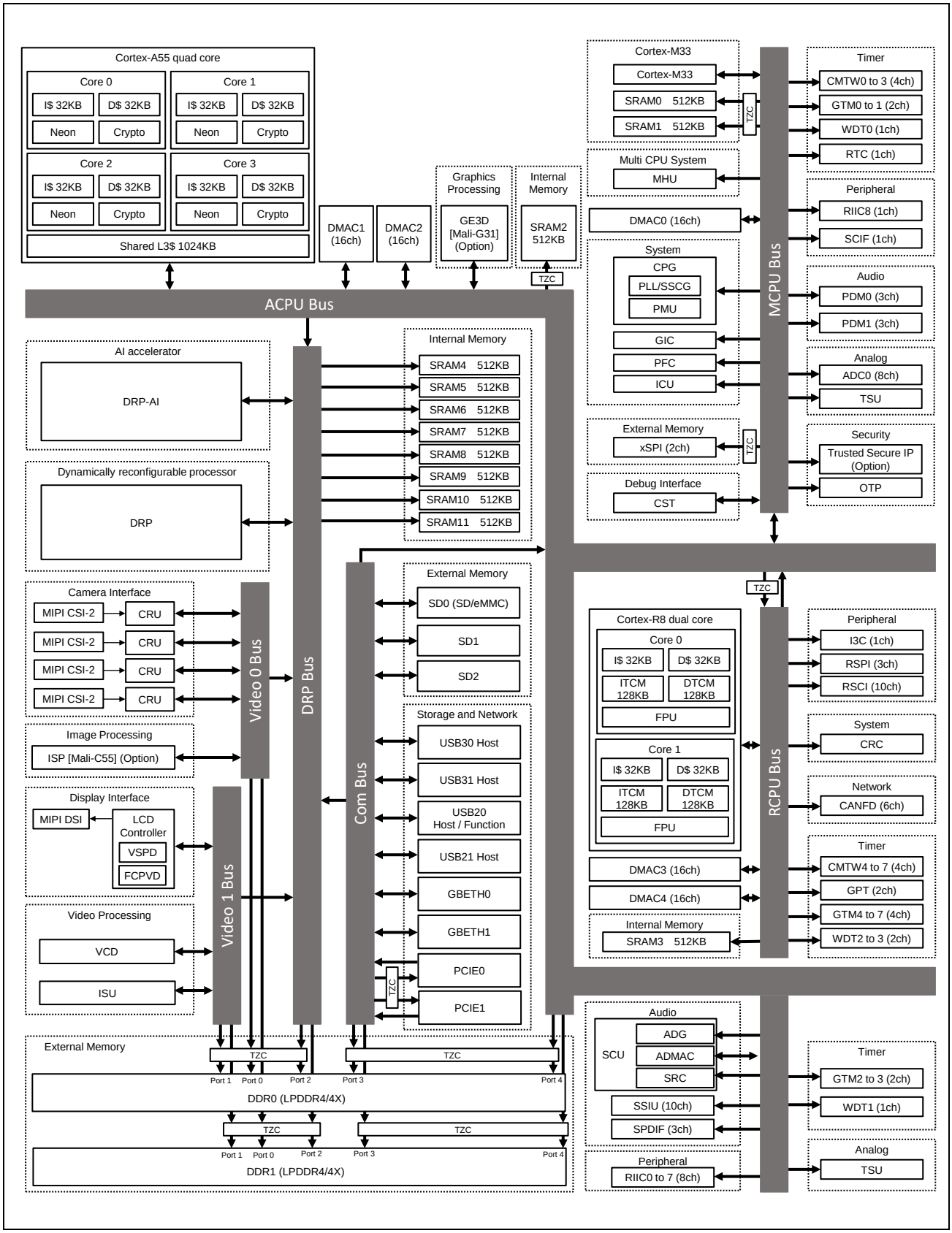


Figure 1.4-1 Block Diagram

Table 1.4-1 List of Units (1/2)

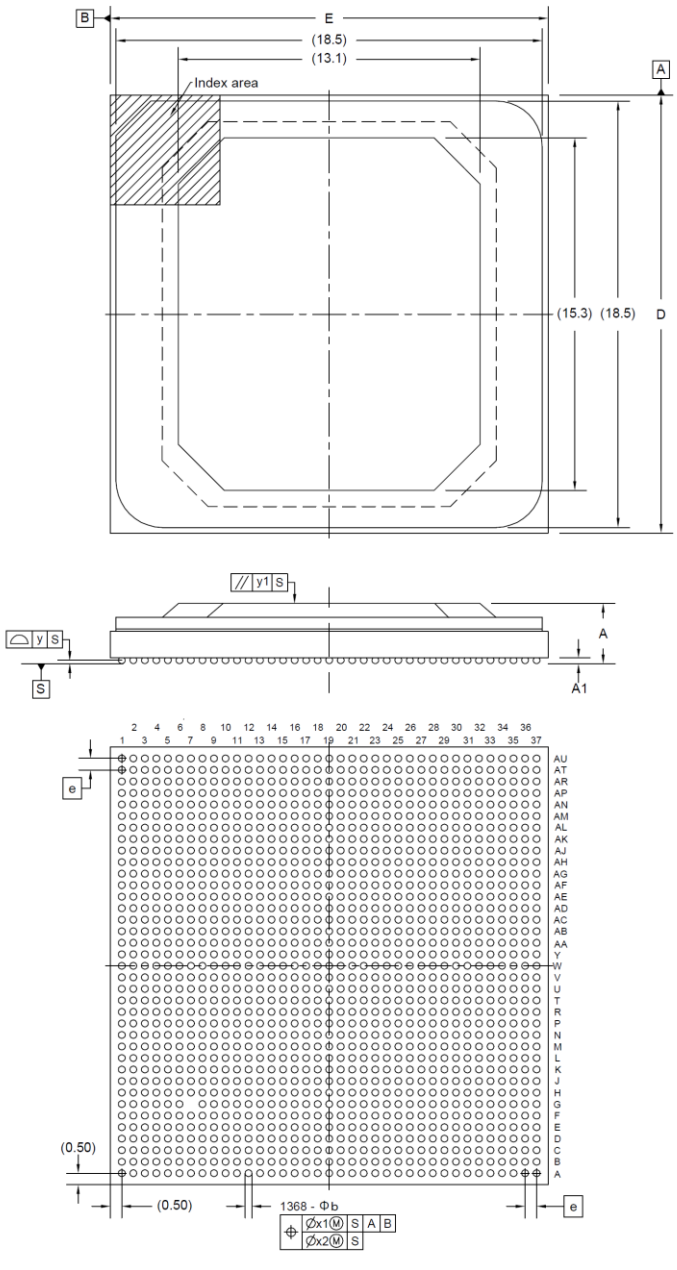
Unit Name	Unit number	Function
ADC	ADC0	A/D converter
ADG	—	Audio clock generator
ADMAC	—	DMAC for audio
CA55	—	Arm Cortex-A55
CANFD	CANFD0	CAN-FD interface
CM33	—	Arm Cortex-M33
CMTW	CMTW0 to CMTW7	Compare match timer
CPG	—	Clock pulse generator
CR8	—	Arm Cortex-R8
CRC	—	CRC operation unit
CRU	CRU0 to CRU3	Camera data receive unit (MIPI CSI-2 interface)
CST	—	Debug interface (Arm CoreSight)
DDR	DDR0, DDR1	LPDDR4/4X controller
DMAC	DMAC0 to DMAC4 (each 16 ch.)	Direct memory access (DMA) controller
DRP	DRP1	Dynamically reconfigurable processor
DRP-AI	DRP0 and AI-MAC	AI accelerator
ELC	—	Event link controller
GBETH	GBETH0, GBETH1	Gigabit Ethernet interface
GE3D	—	3D graphics engine
GIC	—	Generic interrupt controller
GPT	GPT0, GPT1 (each 16 ch.)	General purpose timer
GTM	GTM0 to GTM7	General timer
GPV	—	Global programmers view
I3C	I3C0	I3C bus interface
ICU	—	Interrupt control unit
ISP	—	Image signal processor
ISU	—	Image scale unit
LCDC	—	LCD controller
MHU	—	Message handling unit
OTP	—	One time programmable memory
PCIE	PCIE0, PCIE1	PCIe Express 3.0 interface
PCU	—	Power control unit
PDM	PDM0, PDM1	Pulse density modulation (PDM) interface
PFC	—	Pin function controller
POEG	POEG0, POEG1	Port output enable for GPT
PMU	—	Power management unit
PWC	—	Power sequence controller
RIIC	RIIC0 to RIIC8	I2C bus interface
RSCI	RSCI0 to RSCI9	Serial communication interface
RSPI	RSPI0 to RSPI2	Serial peripheral interface
RTC	—	Real time clock
SCIF	SCIF0	Serial communication interface with FIFO
SD	SD0 to SD2	SD/MMC host interface
Secure IP	—	Trusted secure IP

Table 1.4-2 List of Units (2/2)

Unit Name	Unit number	Functional Overview
SRAM	SRAM0 to SRAM11	SRAM
SRC	—	Sampling rate controller
SSIU	—	Serial sound interface unit
SYC	—	System counter
SYS	—	System controller
SYSTEM BUS	—	Internal bus
ACPU Bus	—	A bus connected to Cortex-A55, DDR memory controllers, SRAM, and its peripheral units
RCPU Bus	—	A bus connected to Cortex-R8, SRAM, and its peripheral units
MCPU Bus	—	A bus connected to Cortex-M33, SRAM, its peripheral units, and the system control units
DRP Bus	—	A bus connected to DRP, DRP-AI, SRAM, and DDR memory controllers
Video 0 Bus Video 1 Bus	—	A bus connected to image processing units and DDR memory controllers
COM Bus	—	A bus connected to communication interface units and DDR memory controllers
TSU	TSU0, TSU1	Temperature sensor unit
TZC	—	CoreLink™ TrustZone Address Space Controller
USB2	USB20, USB21	USB2.0 host / function interface
USB3	USB30, USB31	USB3.2 host interface
VCD	—	H.265/H.264 multi codec
WDT	WDT0 to WDT3	Watchdog timer
xSPI	xSPI0	xSPI controller

Section 2 Package Dimensions

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HFBGA1368-19x19-0.50	PRBG1368KA-A	2.9



Reference Symbol	Dimension in Millimeters		
	MIN.	NOM.	MAX.
D	18.85	19.00	19.15
E	18.85	19.00	19.15
e	—	0.50	—
A	(2.45)	(2.65)	2.85
A1	0.15	(0.25)	—
b	0.25	0.30	0.35
x1	—	—	0.20
x2	—	—	0.05
y	—	—	0.12
y1	—	—	0.35

Figure 2-1 Package Dimensions

REVISION HISTORY	RZ/V2H Group Datasheet

Rev.	Date	Description	
		Page	Summary
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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