

RQJ0306FQDQA

Silicon P Channel MOS FET Power Switching

R07DS0298EJ0300 Rev.3.00 Jan 10, 2014

Features

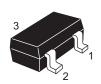
• Low gate drive

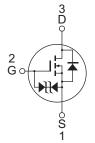
V_{DSS}: -30 V and 2.5 V gate drive

- Low drive current
- High speed switching
- Small traditional package (MPAK)

Outline

RENESAS Package code: PLSP0003ZB-A (Package name: MPAK)





1. Source

2. Gate

3. Drain

Notes: Marking is "FQ".

Absolute Maximum Ratings

 $(Ta = 25^{\circ}C)$

			(/
Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	-30	V
Gate to source voltage	V _{GSS}	+8 / –12	V
Drain current	I _D	-3	А
Drain peak current	I _{D(pulse)} Note1	-12	А
Body - drain diode reverse drain current	I _{DR}	3	А
Channel dissipation	Pch Note2	0.8	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Notes: 1. PW \leq 10 μ s, Duty cycle \leq 1%

2. When using the glass epoxy board (FR-4 $40 \times 40 \times 1$ mm)

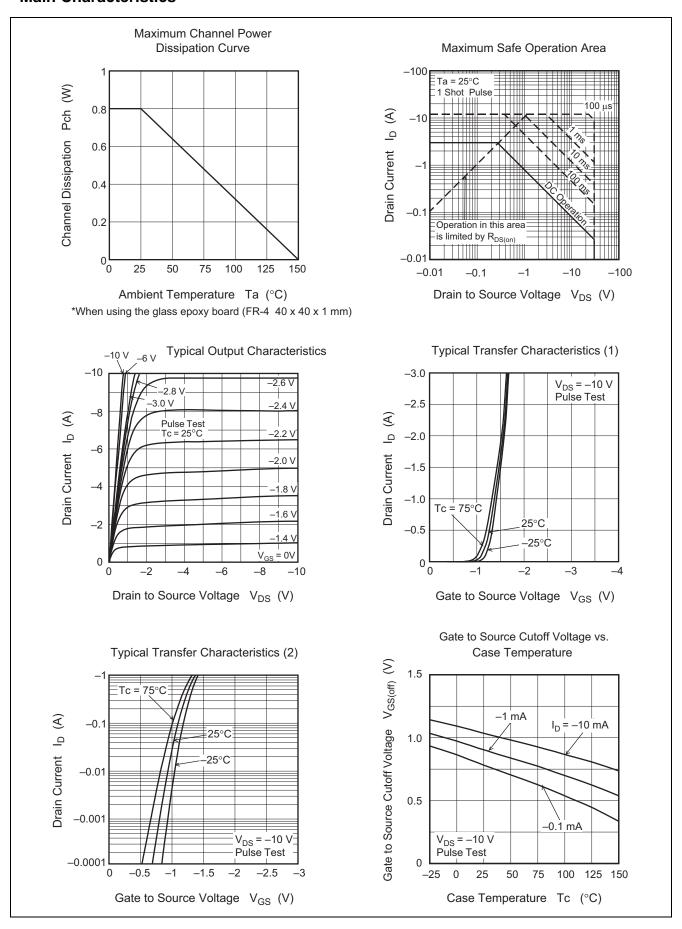
Electrical Characteristics

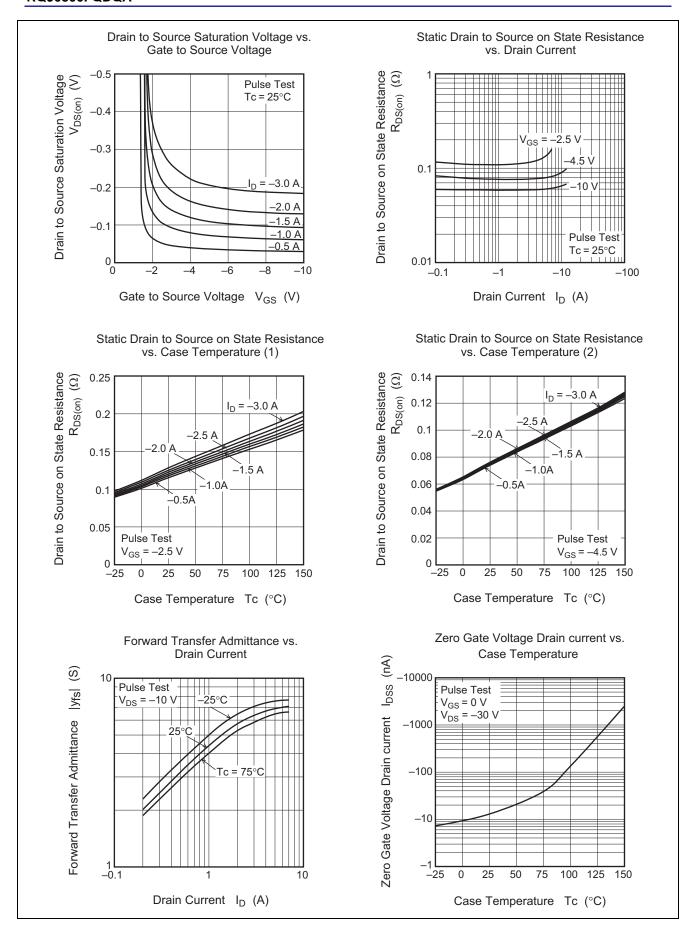
 $(Ta = 25^{\circ}C)$

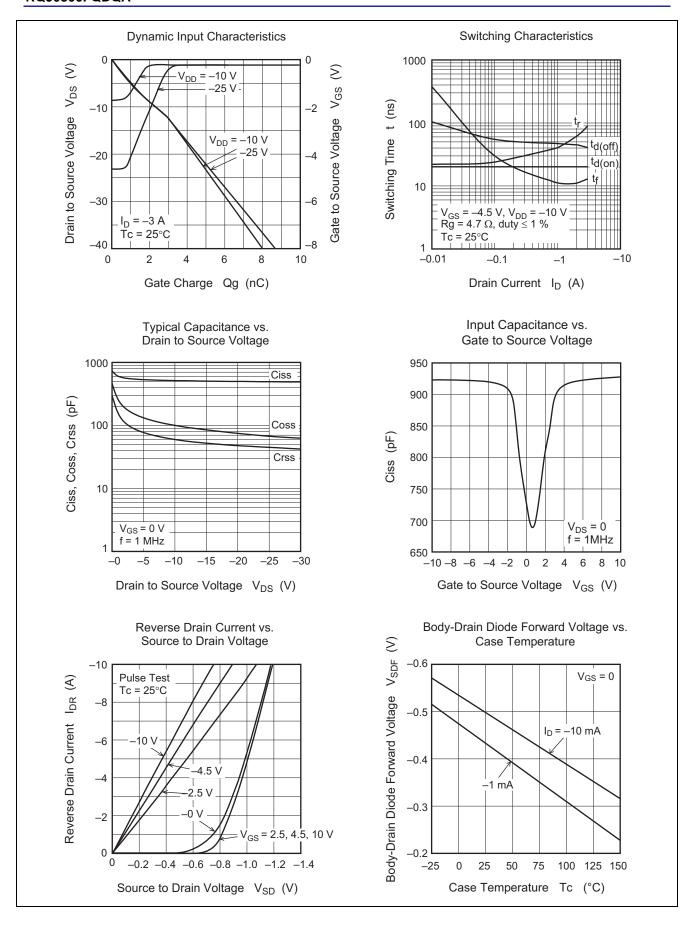
Item	Symbol	Min	Тур	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	_		>	$I_D = -10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	+8			>	$I_G = +100 \mu\text{A}, V_{DS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	-12	_		>	$I_G = -100 \mu\text{A}, V_{DS} = 0$
Gate to source leak current	I _{GSS}		_	+10	μΑ	$V_{GS} = +6 \text{ V}, V_{DS} = 0$
Gate to source leak current	I _{GSS}		_	-10	μΑ	$V_{GS} = -10 \text{ V}, V_{DS} = 0$
Drain to source leak current	I _{DSS}		_	-1	μΑ	$V_{DS} = -30 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.4	_	-1.4	V	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$
Drain to source on state resistance	R _{DS(on)}	_	75	95	mΩ	$I_D = -1.5 \text{ A}, V_{GS} = -4.5 \text{ V}^{\text{Note3}}$
Drain to source on state resistance	R _{DS(on)}	_	120	165	mΩ	$I_D = -1.5 \text{ A}, V_{GS} = -2.5 \text{ V}^{\text{Note3}}$
Forward transfer admittance	y _{fs}	3.5	5.2	_	S	$I_D = -1.5 \text{ A}, V_{DS} = -10 \text{ V}^{\text{Note3}}$
Input capacitance	Ciss	_	510	_	pF	$V_{DS} = -10 \text{ V}, V_{GS} = 0,$
Output capacitance	Coss	_	100	_	pF	f = 1 MHz
Reverse transfer capacitance	Crss	_	58	_	pF	
Turn - on delay time	t _{d(on)}	_	18	_	ns	$I_D = -1.5 \text{ A}$
Rise time	t _r	_	48	_	ns	$V_{GS} = -4.5 \text{ V}$
Turn - off delay time	t _{d(off)}	_	47	_	ns	$R_L = 6.7 \Omega$
Fall time	t _f	_	13	_	ns	$R_g = 4.7 \Omega$
Total gate charge	Qg	_	4.8	_	nC	V _{DD} = -10 V
Gate to Source charge	Qgs	_	0.8	_	nC	$V_{GS} = -4.5 \text{ V}$
Gate to drain charge	Qgd	_	1.8	_	nC	$I_D = -3.0 \text{ A}$
Body - drain diode forward voltage	V_{DF}	_	-0.8	-1.2	V	$I_F = -3.0 \text{ A}, V_{GS} = 0^{\text{Note3}}$

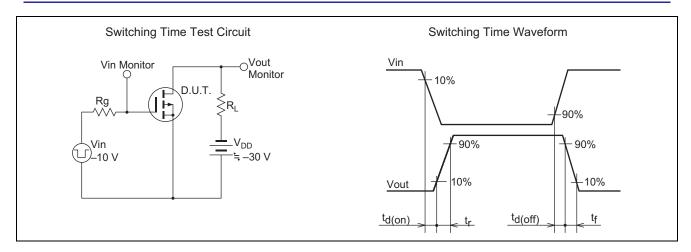
Notes: 3. Pulse test

Main Characteristics



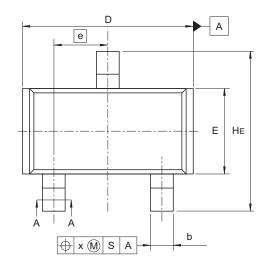


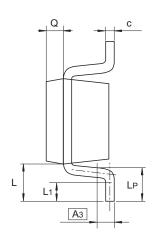


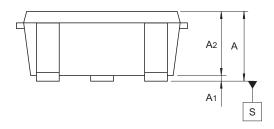


Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
SC-59A	PLSP0003ZB-A	MPAK(T) / MPAK(T)V	0.011









Reference	Dimensions in millimeters		
Symbol	Min	Nom	Max
Α	1.0	_	1.3
A ₁	0	_	0.1
A ₂	1.0	1.1	1.2
A_3		0.25	_
b	0.35	0.4	0.5
С	0.1	0.16	0.26
D	2.7	_	3.1
E	1.35	1.5	1.65
е	_	0.95	_
HE	2.2	2.8	3.0
L	0.35	_	0.75
L ₁	0.15	_	0.55
Lp	0.25	_	0.65
Х	_	_	0.05
Q		0.3	

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Ordering Information

Orderable Part Number	Quantity	Shipping Container
RQJ0306FQDQATL-H	3000 pcs.	φ178 mm reel, 8 mm Emboss taping

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