1. OUTLINE

1.1 Features

Ultra-Low Power Technology
- 2.7 V to 5.5 V operation from a single supply
- Stop (RAM retained): 0.23 µA, (LVD enabled): 0.31 µA
- Halt (RTC + LVD): 0.60 µA
- Operating: 156.25 µA/Mhz

16-bit RL78 CPU Core
- Delivers 41 DMIPS at maximum operating frequency of 32 MHz
- Instruction execution: 86% of instructions can be executed in 1 to 2 clock cycles
- CISC architecture (Harvard) with 3-stage pipeline
- Multiply signed & unsigned: 16 x 16 to 32-bit result in 1 clock cycle
- MAC: 16 x 16 to 32-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 1 clock cycle
- 1-wire on-chip debug function

Main Flash Memory
- Density: 32 KB to 64 KB
- Block size: 1 KB
- On-chip single voltage flash memory with protection from block erase/writing
- Self-programming with secure boot swap function and flash shield window function

Data Flash Memory
- Data flash with background operation
- Data flash size: 4 KB
- Erase cycles: 1 million (typ.)
- Erase/programming voltage: 2.7 V to 5.5 V

RAM
- 2 KB to 4 KB size options
- Supports operands or instructions
- Back-up retention in all modes

High-speed On-chip Oscillator
- 32 MHz with +/- 1% accuracy over voltage (2.7 V to 5.5 V) and temperature (−20°C to 85°C)
- Pre-configured settings: 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz & 1 MHz

Reset and Supply Management
- Power-on reset (POR) monitor/generator
- Low voltage detection (LVD) with 6 setting options (Interrupt and/or reset function)

Data Memory Access (DMA) Controller
- Up to 2 fully programmable channels
- Transfer unit: 8- or 16-bit

16-bit timers KB0 to KB2, and KC0 for PWM output
- 16-bit timers KB0 to KB2: maximum 6 outputs (3 channels × 2)
- Smooth start function, dithering function, forced output stop function (unsynchronized with comparator or external interrupt) enables over-voltage protection, over-current protection and peak current control, and single/interleave PFC function
- Average resolution < 0.98 nsec output, 64 MHz (when using PLL) + dithering option

Extended-Function Timers
- Multi-function 16-bit timers: Up to 8 channels
- Real-time clock (RTC): 1 channel (full calendar and alarm function with watch correction function)
- Interval timer: 12-bit, 1 channel
- 15 kHz watchdog timer: 1 channel (window function)

Multiple Communication Interfaces
- Up to 1 channel x I2C multi-master (SMBus/PMBus support)
- Up to 1 channel x Simplified SPI (CSI1Note1)/SPI (7-, 8-bit)
- Up to 3 channels x UART (7-, 8-, 9-bit), DALI support 1 channel (8-, 16-, 17-, 24-bit, master and slave)
- Up to 1 channel x LIN

Rich Analog
- ADC: Up to 11 channels, 8/10-bit resolution, 2.125 µs conversion time
- Supports 2.7 V
- Internal voltage reference (1.45 V)
- Comparator: High response time 70 ns (typ.), up to 6 channels, internal DAC 3 channels 8-bit resolution, window comparator mode
- PGA (×4 to ×32): 6 input channels
- On-chip temperature sensor

Safety Features (IEC or UL 60730 compliance)
- Flash memory CRC calculation
- RAM parity error check
- RAM/SFR write protection
- Illegal memory access detection
- Clock stop/frequency detection
- ADC self-test

General Purpose I/O
- 5-V tolerant, high-current (up to 8.5 mA per pin)
- Open-drain, internal pull-up support

Operating Ambient Temperature
- Standard: −40°C to +105°C
- Extend: −40°C to +125°C

Package Type and Pin Count
- SSOP: 20, 30, 38
Notes 1. Although the CSI function is generally called SPI, it is also called CSI in this product, so it is referred to as such in this manual.

- ROM, RAM capacities

<table>
<thead>
<tr>
<th>Flash ROM</th>
<th>Data flash</th>
<th>RAM</th>
<th>RL78/I1A</th>
</tr>
</thead>
<tbody>
<tr>
<td>64 KB</td>
<td>4 KB</td>
<td>4 KB</td>
<td>–</td>
</tr>
<tr>
<td>32 KB</td>
<td>4 KB</td>
<td>2 KB</td>
<td>R5F1076C</td>
</tr>
</tbody>
</table>

Note: This is about 3 KB when the self-programming function and data flash function are used.
1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/I1A

<table>
<thead>
<tr>
<th>Pin count</th>
<th>Package</th>
<th>Operating Ambient Temperature</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 pins</td>
<td>20-pin plastic LSSOP (4.4 x 6.5)</td>
<td>( T_a = -40 , ^\circ C ) to ( +105 , ^\circ C )</td>
<td>R5F1076CGSP#V0, R5F1076CGSP#X0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_a = -40 , ^\circ C ) to ( +125 , ^\circ C )</td>
<td>R5F1076CMSP#V0, R5F1076CMSP#X0</td>
</tr>
<tr>
<td>30 pins</td>
<td>30-pin plastic LSSOP (7.62 mm (300))</td>
<td>( T_a = -40 , ^\circ C ) to ( +105 , ^\circ C )</td>
<td>R5F107ACGSP#V0, R5F107ACGSP#X0, R5F107ACGSP#V0, R5F107ACGSP#X0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_a = -40 , ^\circ C ) to ( +125 , ^\circ C )</td>
<td>R5F107ACMSP#V0, R5F107ACMSP#X0, R5F107ACMSP#V0, R5F107ACMSP#X0</td>
</tr>
<tr>
<td>38 pins</td>
<td>38-pin plastic SSOP (7.62 mm (300))</td>
<td>( T_a = -40 , ^\circ C ) to ( +105 , ^\circ C )</td>
<td>R5F107DEGSP#V0, R5F107DEGSP#X0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_a = -40 , ^\circ C ) to ( +125 , ^\circ C )</td>
<td>R5F107DEMSP#V0, R5F107DEMSP#X0</td>
</tr>
</tbody>
</table>

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.
1.3 Pin Configuration (Top View)

1.3.1 20-pin products

- 20-pin plastic LSSOP (4.4 x 6.5)

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 \( \mu \)F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See Figure 4-8 Format of Peripheral I/O redirection register (PIOR1) and Figure 15-20 Format of Input Switch Control Register (ISC) in the RL78/I1A User's Manual.

3. The shared function CMP3P can be assigned to P147 by setting the CMPSEL0 bit in the comparator input switch control register (CMPSEL).
1.3.2 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300))

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR1) and Figure 15-20 Format of Input Switch Control Register (ISC) in the RL78/I1A User’s Manual.
1.3.3 38-pin products

- 38-pin plastic SSOP (7.62 mm (300))

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see 1.4 Pin Identification.
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR1) and Figure 15-20 Format of Input Switch Control Register (ISC) in the RL78/I1A User’s Manual.
1.4 Pin Identification

<table>
<thead>
<tr>
<th>Pin Identifier</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19</td>
<td>Analog Input</td>
</tr>
<tr>
<td>AVREFM, AVREFP</td>
<td>Analog Reference Voltage Minus, Plus</td>
</tr>
<tr>
<td>CMP0P to CMP5P</td>
<td>Comparator Analog Input</td>
</tr>
<tr>
<td>CMPCOM</td>
<td>Comparator External Reference Voltage</td>
</tr>
<tr>
<td>EXCLK</td>
<td>External Clock Input (Main System Clock)</td>
</tr>
<tr>
<td>EXCLKS</td>
<td>External Clock Input (Subsystem Clock)</td>
</tr>
<tr>
<td>INTP0, INTP3, INTP4, INTP9, INTP10, INTP11, INTP20 to INTP23</td>
<td>Interrupt Request from Peripheral</td>
</tr>
<tr>
<td>P02, P03, P05, P06</td>
<td>Port 0</td>
</tr>
<tr>
<td>P10 to P12</td>
<td>Port 1</td>
</tr>
<tr>
<td>P20 to P22</td>
<td>Port 2</td>
</tr>
<tr>
<td>P24 to P27</td>
<td>Port 3</td>
</tr>
<tr>
<td>P30, P31</td>
<td>Port 4</td>
</tr>
<tr>
<td>P40</td>
<td>Port 7</td>
</tr>
<tr>
<td>P75 to P77</td>
<td>Port 12</td>
</tr>
<tr>
<td>P120 to P124</td>
<td>Port 13</td>
</tr>
<tr>
<td>P137</td>
<td>Port 14</td>
</tr>
<tr>
<td>P147</td>
<td>Port 20</td>
</tr>
<tr>
<td>REGC</td>
<td>Regulator Capacitance</td>
</tr>
<tr>
<td>RESET</td>
<td>Reset</td>
</tr>
<tr>
<td>RTC1HZ</td>
<td>Real-time Clock Correction Clock (1 Hz) Output</td>
</tr>
<tr>
<td>RxD0, RxD1, DALIRxD4, SCK00, SCLA0, SDAA0, SIO0</td>
<td>Receive Data, Serial Clock Input/Output, Serial Data Input/Output</td>
</tr>
<tr>
<td>SIO0:</td>
<td>Serial Data Input</td>
</tr>
<tr>
<td>TI03, TI05, TI06, TI07:</td>
<td>Timer Input</td>
</tr>
<tr>
<td>TO03, TO05, TO06, TOOL0:</td>
<td>Data Input/Output for Tool</td>
</tr>
<tr>
<td>TxD0, TxD1, TxCx4:</td>
<td>Serial Data Input/Output for Single Wired UART</td>
</tr>
<tr>
<td>VDD, VSS:</td>
<td>Power Supply, Ground</td>
</tr>
<tr>
<td>X1, X2:</td>
<td>Crystal Oscillator (Main System Clock)</td>
</tr>
<tr>
<td>XT1, XT2:</td>
<td>Crystal Oscillator (Subsystem Clock)</td>
</tr>
</tbody>
</table>
1.5 Block Diagram

1.5.1 20-pin products

Remarks 1. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR1) and Figure 15-20 Format of Input Switch Control Register (ISC) in the RL78/I1A User’s Manual.

2. The shared function CMP3P can be assigned to P147 by setting the CMPSEL0 bit in the comparator input switch control register (CMPSEL).
1.5.2 30-pin products

Remark  Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See Figure 4-8  Format of Peripheral I/O Redirection Register (PIOR1) and Figure 15-20  Format of Input Switch Control Register (ISC) in the RL78/I1A User's Manual.
1.5.3 38-pin products

Remark  Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR1) and Figure 15-20 Format of Input Switch Control Register (ISC) in the RL78/I1A User’s Manual.
1.6 Outline of Functions

**Caution** This outline describes the functions at the time when Peripheral I/O redirection register (PIOR1) is set to 00H.

<table>
<thead>
<tr>
<th>Item</th>
<th>20-pin</th>
<th>30-pin</th>
<th>38-pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code flash memory (KB)</td>
<td>32</td>
<td>32</td>
<td>64</td>
</tr>
<tr>
<td>Data flash memory (KB)</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>RAM (KB)</td>
<td>2</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>Address space</td>
<td>1 MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Main system clock</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High-speed system clock</td>
<td>X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>HS (High-speed main) mode: 1 to 20 MHz (VDD = 2.7 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (VDD = 2.7 to 5.5 V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>High-speed on-chip oscillator</td>
<td>HS (High-speed main) mode: 1 to 32 MHz (VDD = 2.7 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (VDD = 2.7 to 5.5 V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock for 16-bit timers KB0 to KB2, and KC0</td>
<td>64 MHz (TYP.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Subsystem clock (38-pin products only)</td>
<td>XT1 (crystal) oscillation, external subsystem clock input (EXCLKS)</td>
<td>32.768 kHz</td>
<td></td>
</tr>
<tr>
<td>Low-speed on-chip oscillator</td>
<td>15 kHz (TYP.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>General-purpose register</td>
<td>(8-bit register (\times 8)) (\times 4) banks</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum instruction execution time</td>
<td>0.03125 (\mu)s (High-speed on-chip oscillator: (f_OH = 32) MHz operation)</td>
<td>0.05 (\mu)s (High-speed system clock: (f_{SW} = 20) MHz operation)</td>
<td>30.5 (\mu)s (Subsystem clock: (f_{SUB} = 32.768) kHz operation) (38-pin products only)</td>
</tr>
<tr>
<td>Instruction set</td>
<td>• 8-bit operation, 16-bit operation</td>
<td>• Multiplication (8 bits (\times) 8 bits)</td>
<td>• Bit manipulation (Set, reset, test, and Boolean operation), etc.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>I/O port</th>
<th>Total</th>
<th>26</th>
<th>34</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS I/O</td>
<td>13</td>
<td>23</td>
<td>29</td>
</tr>
<tr>
<td>CMOS input</td>
<td>3</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>CMOS output</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Timer 16-bit timer TAU</td>
<td>8 channels (no timer output)</td>
<td>8 channels (timer output: 1, PWM output: 1(\text{Note 2}))</td>
<td>8 channels (timer outputs: 3, PWM outputs: 3(\text{Note 2}))</td>
</tr>
<tr>
<td>16-bit timer KB</td>
<td>2 channels (PWM outputs: 4)</td>
<td>3 channels (PWM outputs: 6)</td>
<td></td>
</tr>
<tr>
<td>16-bit timer KC</td>
<td>1 channel (PWM outputs: 3)</td>
<td>1 channel (PWM outputs: 6)</td>
<td></td>
</tr>
</tbody>
</table>

**Notes**
1. This is about 3 KB when the self-programming function and data flash function are used. (For details, see CHAPTER 3 in the RL78/I1A User’s Manual.)
2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see 6.9.3 Operation as multiple PWM output function in the RL78/I1A User’s Manual).
### 1. OUTLINE

<table>
<thead>
<tr>
<th>Item</th>
<th>20-pin</th>
<th>30-pin</th>
<th>38-pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>Watchdog timer</td>
<td>1 channel</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Real-time clock (RTC)</td>
<td>1 channel&lt;sup&gt;Note 1, 2&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td></td>
<td>12-bit interval timer (IT)</td>
<td></td>
<td>1 channel</td>
</tr>
<tr>
<td>RTC output</td>
<td>–</td>
<td></td>
<td>1 Hz (subsystem clock: f&lt;sub&gt;SUB&lt;/sub&gt; = 32.768 kHz)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>6 channels</th>
<th>11 channels</th>
<th>11 channels</th>
</tr>
</thead>
<tbody>
<tr>
<td>8/10-bit resolution A/D converter</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>4 channels</th>
<th>6 channels</th>
<th>6 channels</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comparator</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>1 channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Programmable gain amplifier</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>4 channels</th>
<th>6 channels</th>
<th>6 channels</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial interface</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- UART (Supporting LIN-bus and DMX512): 1 channel
- UART (Supporting DALI communication): 1 channel

<table>
<thead>
<tr>
<th></th>
<th>16 bits x 16 bits = 32 bits (Unsigned or signed)</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiplier and divider/multiply-accumulator</td>
<td>32 bits x 32 bits = 32 bits (Unsigned)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16 bits x 16 bits + 32 bits = 32 bits (Unsigned or signed)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>2 channels</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMA controller</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>27</th>
<th>30</th>
<th>30</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vectored interrupt sources</td>
<td>Internal</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>7</th>
<th>10</th>
<th>11</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Reset by RESET pin
- Internal reset by watchdog timer
- Internal reset by power-on-reset
- Internal reset by voltage detector
- Internal reset by illegal instruction execution<sup>Note 4</sup>
- Internal reset by RAM parity error
- Internal reset by illegal-memory access

**Notes**

1. The subsystem clock (f<sub>SUB</sub>) can be selected as the operating clock only for 38-pin products.
2. The 20- and 30-pin products can only be used as the constant-period interrupt function.
3. The comparator input is alternatively used with analog input pin (ANI pin).
4. The illegal instruction is generated when instruction code FFH is executed.
   - Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.
5. The 20 pin products can only be used 1 UART simultaneously due to sharing of the same I/O pins.
<table>
<thead>
<tr>
<th>Item</th>
<th>20-pin</th>
<th>30-pin</th>
<th>38-pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-on-reset circuit</td>
<td>R5F1076C</td>
<td>R5F107AC, R5F107AE</td>
<td>R5F107DE</td>
</tr>
<tr>
<td>• Power-on-reset:</td>
<td>1.51 V (TYP.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Power-down-reset:</td>
<td>1.50 V (TYP.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage detector</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Rising edge:</td>
<td>2.81 V to 4.06 V (6 stages)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Falling edge:</td>
<td>2.75 V to 3.98 V (6 stages)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>On-chip debug function</td>
<td>Provided</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>$V_{DD} = 2.7$ to $5.5$ V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating ambient temperature</td>
<td>$T_A = -40$ to $+105^\circ C$ (G: Industrial applications), $T_A = -40$ to $+125^\circ C$ (M: Industrial applications)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
2. ELECTRICAL SPECIFICATIONS
(G: Industrial applications, $T_A = -40$ to $+105^\circ C$)

In this chapter, shows the electrical specifications of the target products.
Target products (G: Industrial applications): $T_A = -40$ to $+105^\circ C$
R5F107xxGxx

Cautions
1. The RL78/I1A has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
2. The pins mounted depend on the product. See 2.1 Port Function to 2.2.1 Functions for each product in the RL78/I1A User’s Manual.
## 2.1 Absolute Maximum Ratings

### Absolute Maximum Ratings (TA = 25°C) (1/2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbols</th>
<th>Conditions</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>VDD</td>
<td></td>
<td>–0.5 to +6.5</td>
<td>V</td>
</tr>
<tr>
<td>REGC pin input voltage</td>
<td>VREGC</td>
<td>REGC</td>
<td>–0.3 to +2.8</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>and –0.3 to VDD +0.3 Note 1</td>
<td></td>
</tr>
<tr>
<td>Input voltage</td>
<td>VI1</td>
<td>P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P200 to P206, EXCLK, EXCLKS, RESET</td>
<td>–0.3 to VDD +0.3 Note 2</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>VO1</td>
<td>P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120, P147, P200 to P206</td>
<td>–0.3 to VDD +0.3 Note 2</td>
<td>V</td>
</tr>
<tr>
<td>Analog input voltage</td>
<td>VAI1</td>
<td>ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19</td>
<td>–0.3 to VDD +0.3 and –0.3 to AVREF (+) + 0.3 Notes 2, 3</td>
<td>V</td>
</tr>
</tbody>
</table>

**Notes**

1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
2. Must be 6.5 V or lower.
3. Do not exceed AVREF(+) + 0.3 V in case of A/D conversion target pin.

**Caution**

Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks**

1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
2. AVREF(+) : + side reference voltage of the A/D converter.
3. VSS: Reference voltage
### Absolute Maximum Ratings (TA = 25°C) (2/2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbols</th>
<th>Conditions</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output current, high</td>
<td>$I_{OH1}$</td>
<td>Per pin P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206</td>
<td>−40 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of all pins −170 mA P02, P03, P40, P120</td>
<td>−70 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206</td>
<td>−100 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{OH2}$</td>
<td>Per pin P20 to P22, P24 to P27</td>
<td>−0.5 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of all pins −2 mA</td>
<td>−2 mA</td>
<td></td>
</tr>
<tr>
<td>Output current, low</td>
<td>$I_{OL1}$</td>
<td>Per pin P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206</td>
<td>40 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of all pins 170 mA P02, P03, P40, P120</td>
<td>70 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206</td>
<td>100 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{OL2}$</td>
<td>Per pin P20 to P22, P24 to P27</td>
<td>1 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of all pins 5 mA</td>
<td>5 mA</td>
<td></td>
</tr>
<tr>
<td>Operating ambient temperature</td>
<td>$T_A$</td>
<td>In normal operation mode</td>
<td>−40 to +105 °C</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>In flash memory programming mode</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{stg}$</td>
<td></td>
<td>−65 to +150 °C</td>
<td></td>
</tr>
</tbody>
</table>

**Caution**  Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark**  Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

\((T_A = -40 \text{ to } +105^\circ\text{C}, 2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}, V_{SS} = 0\text{ V})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Resonator</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1 clock oscillation frequency (f_X)(^{\text{Note}})</td>
<td>Ceramic resonator/crystal resonator</td>
<td></td>
<td>1.0</td>
<td>20.0</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>XT1 clock oscillation frequency (f_{XT})(^{\text{Note}})</td>
<td>Crystal resonator</td>
<td></td>
<td>32</td>
<td>32.768</td>
<td>35</td>
<td>kHz</td>
</tr>
</tbody>
</table>

**Note** Indicates only permissible oscillator frequency ranges. See **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution** Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

**Remark** When using the X1 oscillator and XT1 oscillator, see **5.4 System Clock Oscillator** in the RL78/I1A User's Manual.
2.2.2 On-chip oscillator characteristics

\((T_A = -40 \text{ to } +105^\circ C, 2.7 \text{ V } \leq V_{DD} \leq 5.5 \text{ V}, V_{SS} = 0 \text{ V})\)

<table>
<thead>
<tr>
<th>Oscillators</th>
<th>Parameters</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-speed on-chip oscillator clock frequency (^{\text{Note 1}})</td>
<td>(f_{IH})</td>
<td>(T_A = -20 \text{ to } 85^\circ C)</td>
<td>-1</td>
<td>+1</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(T_A = -40 \text{ to } 105^\circ C)</td>
<td>-1.5</td>
<td>+1.5</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Low-speed on-chip oscillator clock frequency</td>
<td>(f_{IL})</td>
<td>15</td>
<td></td>
<td></td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Low-speed on-chip oscillator clock frequency accuracy</td>
<td></td>
<td>-15</td>
<td></td>
<td></td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

\(^{\text{Note 1}}\) Frequency can be selected in a high-speed on-chip oscillator. Selected by bits 0 to 3 of option byte (000C2H/010C2H).

\(^{\text{Note 2}}\) This indicates the oscillator characteristics only. See AC Characteristics for instruction execution time.

2.2.3 PLL characteristics

\((T_A = -40 \text{ to } +105^\circ C, 2.7 \text{ V } \leq V_{DD} \leq 5.5 \text{ V}, V_{SS} = 0 \text{ V})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL input clock frequency (^{\text{Note}})</td>
<td>(f_{PLLIN})</td>
<td>High-speed system clock is selected ((f_{MX} = 4 \text{ MHz}))</td>
<td>3.94</td>
<td>4.00</td>
<td>4.06</td>
<td>MHz</td>
</tr>
<tr>
<td>PLL output clock frequency (^{\text{Note}})</td>
<td>(f_{PLL})</td>
<td>High-speed on-chip oscillator clock is selected ((f_{IH} = 4 \text{ MHz}))</td>
<td>3.94</td>
<td>4.00</td>
<td>4.06</td>
<td>MHz</td>
</tr>
<tr>
<td>PLL output clock frequency (^{\text{Note}})</td>
<td></td>
<td>(f_{PLLIN} \times 16)</td>
<td></td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
</tbody>
</table>

\(^{\text{Note}}\) This only indicates the oscillator characteristics. See AC Characteristics for instruction execution time.
2.3 DC Characteristics

2.3.1 Pin characteristics

\((T_A = -40 \text{ to } +105 \degree C, \ 2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, \ V_{SS} = 0 \text{ V})\)

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN. (V_{DD})</th>
<th>TYP. (V_{DD})</th>
<th>MAX. (V_{DD})</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output current, high (^1)</td>
<td>(I_{OH1})</td>
<td>Per pin for P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206</td>
<td>(-3.0) (^2) mA</td>
<td>(-1.0) mA</td>
<td>(-12.0) mA</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of P02, P03, P40, P120</td>
<td>(-4.0) mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(When duty (\leq 70%) (^3))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206</td>
<td>(-30.0) mA</td>
<td>(-10.0) mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(When duty (\leq 70%) (^3))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of all pins</td>
<td>(-30.0) mA</td>
<td>(-14.0) mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(When duty (\leq 70%) (^3))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(I_{OH2})</td>
<td>Per pin for P20 to P22, P24 to P27</td>
<td>(-0.1) (^2) mA</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of all pins</td>
<td>(-0.7) mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(When duty (\leq 70%) (^3))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

1. Value of current at which the device operation is guaranteed even if the current flows from the \(V_{DD}\) pin to an output pin.
2. However, do not exceed the total current value.
3. Specification under conditions where the duty factor \(\leq 70\%\).

The output current value that has changed to the duty factor \(> 70\%\) the duty ratio can be calculated with the following expression (when changing the duty factor from \(70\%\) to \(n\%\)).

- Total output current of pins \(= (I_{OH} \times 0.7)/(n \times 0.01)\)

**Example**

\[\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) = -8.7 \text{ mA}\]

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Caution**
P02, P10 to P12 do not output high level in N-ch open-drain mode.

**Remark**
Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
### 2. ELECTRICAL SPECIFICATIONS (G: Industrial applications, TA = −40 to +105°C)

(TA = −40 to +105°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output current, low&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td>I&lt;sub&gt;O1&lt;/sub&gt;</td>
<td>Per pin for P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206</td>
<td>4.0 V ≤ VDD ≤ 5.5 V</td>
<td>8.5&lt;sup&gt;Note 2&lt;/sup&gt;mA</td>
<td>1.5&lt;sup&gt;Note 2&lt;/sup&gt;mA</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of P02, P03, P40, P120 (When duty ≤ 70%&lt;sup&gt;Note 3&lt;/sup&gt;)</td>
<td>4.0 V ≤ VDD ≤ 5.5 V</td>
<td>40.0 mA</td>
<td>7.5 mA</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 (When duty ≤ 70%&lt;sup&gt;Note 3&lt;/sup&gt;)</td>
<td>4.0 V ≤ VDD ≤ 5.5 V</td>
<td>40.0 mA</td>
<td>7.5 mA</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of all pins (When duty ≤ 70%&lt;sup&gt;Note 3&lt;/sup&gt;)</td>
<td>4.0 V ≤ VDD ≤ 5.5 V</td>
<td>80.0 mA</td>
<td>25.0 mA</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>I&lt;sub&gt;O2&lt;/sub&gt;</td>
<td>Per pin for P20 to P22, P24 to P27</td>
<td>2.7 V ≤ VDD ≤ 5.5 V</td>
<td>0.4&lt;sup&gt;Note 2&lt;/sup&gt;mA</td>
<td>2.8 mA</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of all pins (When duty ≤ 70%&lt;sup&gt;Note 3&lt;/sup&gt;)</td>
<td>2.7 V ≤ VDD ≤ 5.5 V</td>
<td>2.8 mA</td>
<td>2.8 mA</td>
<td>mA</td>
</tr>
</tbody>
</table>

**Notes**

1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the VSS pin.
2. However, do not exceed the total current value.
3. Specification under conditions where the duty factor ≤ 70%.
   - The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
     - Total output current of pins = (I<sub>O1</sub> \times 0.7)/(n \times 0.01)
   
   **Example**
   - Where n = 80% and I<sub>O1</sub> = −10.0 mA
     - Total output current of pins = (−10.0 \times 0.7)/(80 \times 0.01) ≈ −8.7 mA
   - However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Remark**

Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
(TA = −40 to +105°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage, high</td>
<td>VIH1</td>
<td>P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, RESET</td>
<td>0.8VDD</td>
<td>VDD</td>
<td>VDD</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Normal input buffer</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VIL2</td>
<td>P03, P10, P11</td>
<td>2.1</td>
<td>VDD</td>
<td>VDD</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TTL input buffer 4.0 V ≤ VDD ≤ 5.5 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>TTL input buffer 3.3 V ≤ VDD &lt; 4.0 V</td>
<td>2.0</td>
<td>VDD</td>
<td>VDD</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TTL input buffer 2.7 V ≤ VDD &lt; 3.3 V</td>
<td>1.5</td>
<td>VDD</td>
<td>VDD</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage, low</td>
<td>VIL1</td>
<td>P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, RESET</td>
<td>0</td>
<td>0.2VDD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Normal input buffer</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VIL2</td>
<td>P03, P10, P11</td>
<td>0</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>TTL input buffer 4.0 V ≤ VDD ≤ 5.5 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>TTL input buffer 3.3 V ≤ VDD &lt; 4.0 V</td>
<td>0</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>TTL input buffer 2.7 V ≤ VDD &lt; 3.3 V</td>
<td>0</td>
<td>0.32</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

**Caution**  The maximum value of VIH of pins P02, P10 to P12 is VDD, even in the N-ch open-drain mode.

**Remark**  Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
(TA = −40 to +105°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage, high</td>
<td>VOH1</td>
<td>P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206</td>
<td>4.0 V ≤ VDD ≤ 5.5 V, IOH1 = −3.0 mA</td>
<td>VDD – 0.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V ≤ VDD ≤ 5.5 V, IOH1 = −1.0 mA</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VOH2</td>
<td>P20 to P22, P24 to P27</td>
<td>2.7 V ≤ VDD ≤ 5.5 V, IOH2 = −100 μA</td>
<td>VDD – 0.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output voltage, low</td>
<td>VIL1</td>
<td>P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206</td>
<td>4.0 V ≤ VDD ≤ 5.5 V, IOL1 = 8.5 mA</td>
<td>0.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.0 V ≤ VDD ≤ 5.5 V, IOL1 = 4.0 mA</td>
<td></td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 1.5 mA</td>
<td></td>
<td>0.4</td>
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<td>V</td>
</tr>
<tr>
<td></td>
<td>VIL2</td>
<td>P20 to P22, P24 to P27</td>
<td>2.7 V ≤ VDD ≤ 5.5 V, IOL2 = 400 μA</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

**Caution** P02, P10 to P12 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
### Electrical Specifications (G: Industrial applications, TA = −40 to +105°C)

(TA = −40 to +105°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input leakage current, high</td>
<td>ILIH1</td>
<td>P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120, P137, P147, P200 to P206, RESET</td>
<td>V_i = VDD</td>
<td></td>
<td>1 μA</td>
<td></td>
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</tr>
<tr>
<td></td>
<td>ILIH2</td>
<td>P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)</td>
<td>V_i = VDD</td>
<td></td>
<td>1 μA</td>
<td></td>
<td></td>
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<tr>
<td>Input leakage current, low</td>
<td>ILIL1</td>
<td>P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120, P137, P147, P200 to P206, RESET</td>
<td>V_i = VSS</td>
<td></td>
<td>−1 μA</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>ILIL2</td>
<td>P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)</td>
<td>V_i = VSS</td>
<td></td>
<td>−1 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>On-chip pull-up resistance</td>
<td>RU</td>
<td>P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206</td>
<td>V_i = VSS, In input port</td>
<td>10</td>
<td>20</td>
<td>100</td>
<td>kΩ</td>
</tr>
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</table>

**Remark**  Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
2.3.2 Supply current characteristics

\((T_A = -40 \text{ to } +105^\circ C, 2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, V_{SS} = 0 \text{ V}) (1/2)\)

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<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Operating mode</th>
<th>Conditions</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>Unit</th>
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<tr>
<td>Supply current</td>
<td>IDD</td>
<td>Note 1</td>
<td>HS (high-speed main mode)</td>
<td>Note 3</td>
<td>5.0</td>
<td>7.5</td>
<td>mA</td>
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<td>fIH = 32 MHz</td>
<td>VDD = 5.0 V</td>
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<td>VDD = 3.0 V</td>
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<td>7.5</td>
<td>mA</td>
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<td>LS (low-speed main mode)</td>
<td>Note 5</td>
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<td>fIH = 8 MHz</td>
<td>VDD = 3.0 V</td>
<td>1.3</td>
<td>2.0</td>
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<tr>
<td>Subsystem clock operation</td>
<td>fSUB</td>
<td>Note 4</td>
<td>HS (high-speed main mode)</td>
<td>Note 5</td>
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<td>fIH = 4 MHz</td>
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<td>VDD = 3.0 V</td>
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<td>8.5</td>
<td>mA</td>
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<td></td>
<td>fIH = 4 MHz</td>
<td>VDD = 3.0 V</td>
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<td>4.4</td>
<td>6.2</td>
<td>mA</td>
</tr>
</tbody>
</table>

(Notes and Remarks are listed on the next page.)
Notes 1. Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The following points apply in the HS (high-speed main), and LS (low-speed main) modes

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

2. When high-speed on-chip oscillator and subsystem clock are stopped.
3. When high-speed system clock and subsystem clock are stopped.
4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).
5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
   - HS (high-speed main) mode: 2.7 V ≤ VDD ≤ 5.5 V at 1 MHz to 32 MHz
   - LS (low-speed main) mode: 2.7 V ≤ VDD ≤ 5.5 V at 1 MHz to 8 MHz

Remarks 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. fSH: High-speed on-chip oscillator clock frequency
3. fSUB: Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C
### ELECTRICAL SPECIFICATIONS (G: Industrial applications, T<sub>A</sub> = −40 to +105°C)

#### (T<sub>A</sub> = −40 to +105°C, 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V) (2/2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply current</td>
<td>I&lt;sub&gt;DD2&lt;/sub&gt;</td>
<td>Note 2</td>
<td>f&lt;sub&gt;H&lt;/sub&gt; = 32 MHz&lt;sup&gt;Note 4&lt;/sup&gt;</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5.0 V</td>
<td>0.72</td>
<td>2.9</td>
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<td>HALT mode</td>
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<td></td>
<td>f&lt;sub&gt;H&lt;/sub&gt; = 32 MHz&lt;sup&gt;Note 4&lt;/sup&gt;</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 3.0 V</td>
<td>0.72</td>
<td>2.9</td>
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<td>f&lt;sub&gt;H&lt;/sub&gt; = 24 MHz&lt;sup&gt;Note 4&lt;/sup&gt;</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5.0 V</td>
<td>0.57</td>
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<td>f&lt;sub&gt;H&lt;/sub&gt; = 24 MHz&lt;sup&gt;Note 4&lt;/sup&gt;</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 3.0 V</td>
<td>0.57</td>
<td>2.3</td>
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<td>f&lt;sub&gt;H&lt;/sub&gt; = 16 MHz&lt;sup&gt;Note 4&lt;/sup&gt;</td>
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<td>f&lt;sub&gt;H&lt;/sub&gt; = 16 MHz&lt;sup&gt;Note 4&lt;/sup&gt;</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 3.0 V</td>
<td>0.50</td>
<td>1.7</td>
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<td>f&lt;sub&gt;L&lt;/sub&gt; = 8 MHz&lt;sup&gt;Note 4&lt;/sup&gt;, T&lt;sub&gt;A&lt;/sub&gt; = −40 to +105°C</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 3.0 V</td>
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<td>910</td>
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<td>LS (low-speed main) mode&lt;sup&gt;Note 6&lt;/sup&gt;</td>
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<td>f&lt;sub&gt;MX&lt;/sub&gt; = 20 MHz&lt;sup&gt;Note 3&lt;/sup&gt;, V&lt;sub&gt;DD&lt;/sub&gt; = 5.0 V</td>
<td>Square wave input</td>
<td>0.40</td>
<td>1.9</td>
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<td>Resonator connection</td>
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<td>0.50</td>
<td>2.0</td>
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<td>f&lt;sub&gt;MX&lt;/sub&gt; = 10 MHz&lt;sup&gt;Note 3&lt;/sup&gt;, V&lt;sub&gt;DD&lt;/sub&gt; = 5.0 V</td>
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<td>f&lt;sub&gt;L&lt;/sub&gt; = 8 MHz&lt;sup&gt;Note 3&lt;/sup&gt;, T&lt;sub&gt;A&lt;/sub&gt; = −40 to +85°C</td>
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<td>f&lt;sub&gt;H&lt;/sub&gt; = 4 MHz&lt;sup&gt;Note 4&lt;/sup&gt;, f&lt;sub&gt;L&lt;/sub&gt; = 64 MHz, f&lt;sub&gt;SL&lt;/sub&gt; = 32 MHz</td>
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<td>V&lt;sub&gt;DD&lt;/sub&gt; = 3.0 V</td>
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<td>f&lt;sub&gt;H&lt;/sub&gt; = 4 MHz&lt;sup&gt;Note 4&lt;/sup&gt;, f&lt;sub&gt;L&lt;/sub&gt; = 64 MHz, f&lt;sub&gt;SL&lt;/sub&gt; = 32 MHz</td>
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<td>f&lt;sub&gt;H&lt;/sub&gt; = 4 MHz&lt;sup&gt;Note 4&lt;/sup&gt;, f&lt;sub&gt;L&lt;/sub&gt; = 64 MHz, f&lt;sub&gt;SL&lt;/sub&gt; = 16 MHz</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 3.0 V</td>
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<td>Subsystem clock operation</td>
<td>f&lt;sub&gt;sub&lt;/sub&gt;</td>
<td>Note 5</td>
<td>f&lt;sub&gt;sub&lt;/sub&gt; = 32.768 kHz&lt;sup&gt;Note 5&lt;/sup&gt;, T&lt;sub&gt;A&lt;/sub&gt; = −40°C</td>
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<td></td>
<td></td>
<td>f&lt;sub&gt;sub&lt;/sub&gt; = 32.768 kHz&lt;sup&gt;Note 5&lt;/sup&gt;, T&lt;sub&gt;A&lt;/sub&gt; = +50°C</td>
<td>Square wave input</td>
<td>0.41</td>
<td>1.90</td>
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<td></td>
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<td>Resonator connection</td>
<td></td>
<td>0.60</td>
<td>2.09</td>
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<td>f&lt;sub&gt;sub&lt;/sub&gt; = 32.768 kHz&lt;sup&gt;Note 5&lt;/sup&gt;, T&lt;sub&gt;A&lt;/sub&gt; = +70°C</td>
<td>Square wave input</td>
<td>0.54</td>
<td>2.80</td>
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<td>Resonator connection</td>
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<td>0.73</td>
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<td>f&lt;sub&gt;sub&lt;/sub&gt; = 32.768 kHz&lt;sup&gt;Note 5&lt;/sup&gt;, T&lt;sub&gt;A&lt;/sub&gt; = +85°C</td>
<td>Square wave input</td>
<td>1.27</td>
<td>6.10</td>
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<td>Resonator connection</td>
<td></td>
<td>1.46</td>
<td>6.29</td>
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<td>f&lt;sub&gt;sub&lt;/sub&gt; = 32.768 kHz&lt;sup&gt;Note 5&lt;/sup&gt;, T&lt;sub&gt;A&lt;/sub&gt; = +105°C</td>
<td>Square wave input</td>
<td>3.04</td>
<td>15.5</td>
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<td></td>
<td></td>
<td>Resonator connection</td>
<td></td>
<td>3.23</td>
<td>15.7</td>
</tr>
</tbody>
</table>

(Notes and Remarks are listed on the next page.)
Notes 1. Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The following points apply in the HS (high-speed main) and LS (low-speed main) modes.
   • The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
   • The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.
   In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.
   In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

2. During HALT instruction execution by flash memory.
3. When high-speed on-chip oscillator and subsystem clock are stopped.
4. When high-speed system clock and subsystem clock are stopped.
5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).
6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
   HS (high-speed main) mode: 2.7 V ≤ VDD ≤ 5.5 V@1 MHz to 32 MHz
   LS (low-speed main) mode: 2.7 V ≤ VDD ≤ 5.5 V@1 MHz to 8 MHz
7. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. \( f_{\text{MX}} \): High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. \( f_{\text{OH}} \): High-speed on-chip oscillator clock frequency
3. \( f_{\text{SUB}} \): Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is \( T_A = 25^\circ C \)
\[ \text{(TA} = -40 \text{ to } +105^\circ \text{C, } 2.7 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V, VSS} = 0 \text{ V)} \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low-speed on-chip oscillator operating current</td>
<td>[I_{FIL}]</td>
<td>Note 1</td>
<td>0.20</td>
<td></td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>RTC operating current</td>
<td>[I_{RTC}]</td>
<td>Notes 1, 2, 3</td>
<td>0.02</td>
<td></td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>12-bit interval timer operating current</td>
<td>[I_{IT}]</td>
<td>Notes 1, 2, 4</td>
<td>0.02</td>
<td></td>
<td></td>
<td>(\mu\text{A})</td>
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<tr>
<td>Watchdog timer operating current</td>
<td>[I_{WD}]</td>
<td>Notes 1, 2, 3, (f_L = 15 \text{ kHz})</td>
<td>0.22</td>
<td></td>
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<td>(\mu\text{A})</td>
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<tr>
<td>A/D converter operating current</td>
<td>[I_{ADC}]</td>
<td>When conversion at maximum speed Normal mode, (AV_{REFP} = \text{VDD} = 5.0 \text{ V})</td>
<td>1.3</td>
<td>1.7</td>
<td></td>
<td>mA</td>
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<tr>
<td>A/D converter reference voltage current</td>
<td>[I_{ADREF}]</td>
<td>Note 1</td>
<td>75.0</td>
<td></td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>Temperature sensor operating current</td>
<td>[I_{TEMP}]</td>
<td>Note 1</td>
<td>75.0</td>
<td></td>
<td></td>
<td>(\mu\text{A})</td>
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<tr>
<td>LVD operating current</td>
<td>[I_{LVD}]</td>
<td>Notes 1, 7</td>
<td>0.08</td>
<td></td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>Self-programming operating current</td>
<td>[I_{SP}]</td>
<td>Notes 1, 8</td>
<td>2.50</td>
<td>12.2</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Programmable gain amplifier operating current</td>
<td>[I_{PG}]</td>
<td>Note 5, (AV_{REFP} = \text{VDD} = 5.0 \text{ V})</td>
<td>0.21</td>
<td>0.31</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(AV_{REFP} = \text{VDD} = 3.0 \text{ V})</td>
<td>0.18</td>
<td>0.29</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Comparator operating current</td>
<td>[I_{REF}]</td>
<td>Note 10, When one comparator channel is operating</td>
<td>41.4</td>
<td>62</td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(AV_{REFP} = \text{VDD} = 3.0 \text{ V})</td>
<td>37.2</td>
<td>59</td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>Programmable gain amplifier/comparator reference current source</td>
<td>[I_{IREF}]</td>
<td>Note 11, When one internal reference voltage circuit is operating</td>
<td>14.8</td>
<td>26</td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(AV_{REFP} = \text{VDD} = 5.0 \text{ V})</td>
<td>8.9</td>
<td>20</td>
<td></td>
<td>(\mu\text{A})</td>
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<tr>
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<td></td>
<td>(AV_{REFP} = \text{VDD} = 3.0 \text{ V})</td>
<td>3.2</td>
<td>5.1</td>
<td></td>
<td>(\mu\text{A})</td>
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<tr>
<td></td>
<td></td>
<td>(AV_{REFP} = \text{VDD} = 3.0 \text{ V})</td>
<td>2.9</td>
<td>4.9</td>
<td></td>
<td>(\mu\text{A})</td>
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<tr>
<td>BGO operating current</td>
<td>[I_{BGO}]</td>
<td>Note 12</td>
<td>2.50</td>
<td>12.2</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>SNOOZE operating current</td>
<td>[I_{SNOE}]</td>
<td>Note 1, ADC operation The mode is performed (^{\text{Note 13}})</td>
<td>0.50</td>
<td>1.1</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The A/D conversion operations are performed, Standard mode, (AV_{REFP} = \text{VDD} = 5.0 \text{ V})</td>
<td>2.0</td>
<td>3.04</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Simplified SPI (CSI)/UART operation</td>
<td>0.70</td>
<td>1.54</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

\(<R>\)

(Notes and Remarks are listed on the next page.)
Notes 1. Current flowing to the $V_{DD}$.
2. When the high-speed on-chip oscillator and high-speed system clock are stopped.
3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{RTC}$, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FL}$ should be added. $I_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.
4. Current flowing only to the 12-bit interval timer (excluding the operating current of the XT1 oscillator and $f_{FL}$ operating current). The current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode.
5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$, and $I_{WDT}$ when the watchdog timer is in operation.
6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.
7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit is in operation.
9. Current flowing only to the programmable gain amplifier. The supply current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$, and $I_{PGA}$, when the programmable gain amplifier is operating in operation mode or in HALT mode.
10. Current flowing only to the comparator. The supply current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$, and $I_{CMP}$, when the comparator is operating.
11. This is the current required to flow to $V_{DD}$ pin of the current circuit that is used as the programmable gain amplifier and the comparator.
12. Current flowing only during data flash rewrite.
13. See 21.3.3 SNOOZE mode in the RL78/I1A User’s Manual for shift time to the SNOOZE mode.

Remarks 1. $f_{FL}$: Low-speed on-chip oscillator clock frequency
2. $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
3. $f_{CLK}$: CPU/peripheral hardware clock frequency
4. Temperature condition of the TYP. value is $T_{A} = 25^\circ C$
5. Example of calculating current value when using programmable gain amplifier and comparator.

Examples 1) TYP. operating current value when three comparator channels, one internal reference voltage generator, and PGA are operating (when $AV_{REFP} = V_{DD} = 5.0 \text{ V}$)

$$I_{CMP} \times 3 + I_{REF} + I_{PGA} + I_{IREF}$$

$$= 41.4 \times 3 + 14.8 \times 1 + 210 \times 3.2 \times [\mu A]$$

$$= 352.2 [\mu A]$$

Examples 2) TYP. operating current value when using two comparator channels, without using internal reference voltage generator (when $AV_{REFP} = V_{DD} = 5.0 \text{ V}$)

$$I_{CMP} \times 2 + I_{IREF}$$

$$= 41.4 \times 2 + 3.2 [\mu A]$$

$$= 86.0 [\mu A]$$
### 2.4 AC Characteristics

**Conditions:**
- \( T_A = -40 \) to +105°C
- 2.7 V ≤ \( V_{DD} \) ≤ 5.5 V, \( V_{SS} = 0 \) V

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction cycle (minimum instruction execution time)</td>
<td>TCY</td>
<td>Main system clock (( f_{MCK} )) operation</td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td></td>
<td></td>
<td>HS (high-speed main) mode</td>
<td>0.03125</td>
<td>1</td>
<td></td>
<td>( \mu s )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LS (low-speed main) mode</td>
<td>0.125</td>
<td>1</td>
<td></td>
<td>( \mu s )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_A = -40 ) to +85°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Subsystem clock (( f_{SUB} )) operation</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>In the self programming mode</td>
<td>28.5</td>
<td>30.5</td>
<td>31.3</td>
<td>( \mu s )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LS (high-speed main) mode, ( T_A = -40 ) to +85°C</td>
<td>0.03125</td>
<td>1</td>
<td></td>
<td>( \mu s )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LS (low-speed main) mode, ( T_A = -40 ) to +85°C</td>
<td>0.125</td>
<td>1</td>
<td></td>
<td>( \mu s )</td>
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<tr>
<td>External system clock frequency</td>
<td>( f_{EX} )</td>
<td></td>
<td></td>
<td>1.0</td>
<td>20.0</td>
<td>MHz</td>
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<td></td>
<td></td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>External system clock input high-level width, low-level width</td>
<td>( t_{EXH}, t_{EXL} )</td>
<td></td>
<td>24</td>
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<td></td>
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<tr>
<td>TI03, TI05, TI06, TI07 input high-level width, low-level width</td>
<td>( t_{TIH}, t_{TIL} )</td>
<td></td>
<td>13.7</td>
<td></td>
<td></td>
<td>( \mu s )</td>
</tr>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TO03, TO05, TO06, TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21, TKCO00 to TKCO05 output frequency (When duty = 50%)</td>
<td>( f_{TO} )</td>
<td>HS (high-speed main) mode</td>
<td>4.0 V ≤ ( V_{DD} ) ≤ 5.5 V</td>
<td>8</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.7 V ≤ ( V_{DD} ) &lt; 4.0 V</td>
<td>4</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LS (low-speed main) mode, ( T_A = -40 ) to +85°C</td>
<td>4.0 V ≤ ( V_{DD} ) ≤ 5.5 V</td>
<td>4</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.7 V ≤ ( V_{DD} ) &lt; 4.0 V</td>
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<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Interrupt input high-level width, low-level width</td>
<td>( t_{INTH}, t_{INTL} )</td>
<td>INTP0, INTP3, INTP4, INTP9 to INTP11, INTP20 to INTP23</td>
<td>1</td>
<td></td>
<td></td>
<td>( \mu s )</td>
</tr>
<tr>
<td>RESET low-level width</td>
<td>( t_{RSL} )</td>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td>( \mu s )</td>
</tr>
</tbody>
</table>

**Remark**

- \( f_{MCK} \): Timer array unit operation clock frequency
- (Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). \( n \): Channel number (\( n = 0 \) to 7))
Minimum Instruction Execution Time during Main System Clock Operation

**TCY vs VDD (HS (high-speed main) mode)**

- **Cycle time TCY [µs]**
- **Supply voltage VDD [V]**

- When the high-speed on-chip oscillator clock is selected
- During self programming
- When high-speed system clock is selected

**TCY vs VDD (LS (low-speed main) mode)**

- **Cycle time TCY [µs]**
- **Supply voltage VDD [V]**

- When the high-speed on-chip oscillator clock is selected
- During self programming
- When high-speed system clock is selected
AC Timing Test Points

External System Clock Timing

TI/TO Timing

Interrupt Request Input Timing

RESET Input Timing
2.5 Peripheral Functions Characteristics

**AC Timing Test Points**

- VIH/VOH
- VIL/VOL

2.5.1 Serial array unit 0, 4 (UART0, UART1, CSI00, DALI/UART4)

(1) During communication at the same potential (UART mode)

(T\textsubscript{A} = \textendash40 to +105°C, 2.7 V \leq V\textsubscript{DD} \leq 5.5 V, V\textsubscript{SS} = 0 V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main) Mode</th>
<th>LS (low-speed main) Mode</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer rate\textsuperscript{Note 1}</td>
<td></td>
<td>2.7 V \leq V\textsubscript{DD} \leq 5.5 V</td>
<td>f\textsubscript{MCK}/6</td>
<td>f\textsubscript{MCK}/6</td>
<td>bps</td>
</tr>
</tbody>
</table>

\textsuperscript{Note 1} Theoretical value of the maximum transfer rate f\textsubscript{MCK} = f\textsubscript{CLK} \textsuperscript{Note 2}

**Notes**

1. Transfer rate in the SNOOZE mode is 4800 bps only.
2. The maximum operating frequencies of the CPU/peripheral hardware clock (f\textsubscript{CLK}) are:
   - HS (high-speed main) mode: 32 MHz (2.7 V \leq V\textsubscript{DD} \leq 5.5 V)
   - LS (low-speed main) mode: 8 MHz (2.7 V \leq V\textsubscript{DD} \leq 5.5 V), T\textsubscript{A} = \textendash40 to +85°C

**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**UART mode connection diagram (during communication at the same potential)**

**UART mode bit width (during communication at the same potential) (reference)**

**Remarks**

1. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)
2. f\textsubscript{MCK}: Serial array unit operation clock frequency
   
   (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))
During communication at same potential (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output)

\( T_A = -40 \) to \(+105^\circ \text{C} \)
\( 2.7 \, \text{V} \leq \text{VDD} \leq 5.5 \, \text{V}, \text{VSS} = 0 \, \text{V} \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main) Mode</th>
<th>LS (low-speed main) Mode</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCKp cycle time</td>
<td>#KCY1</td>
<td>( t_{KCY1} \geq 4/f_{CLK} )</td>
<td>MIN. 125</td>
<td>MIN. 44</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MAX. 500</td>
<td>MAX. 110</td>
<td></td>
</tr>
<tr>
<td>SCKp high-/low-level width</td>
<td>#KH1,</td>
<td>4.0 V \leq \text{VDD} \leq 5.5 V</td>
<td>#KCY2/2 – 12</td>
<td>#KCY2/2 – 50</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>#KL1</td>
<td>2.7 V \leq \text{VDD} \leq 5.5 V</td>
<td>#KCY2/2 – 18</td>
<td>#KCY2/2 – 50</td>
<td></td>
</tr>
<tr>
<td>SCKp setup time (to SCKp( ^\uparrow )) Note 1</td>
<td>#SK1</td>
<td>4.0 V \leq \text{VDD} \leq 5.5 V</td>
<td>44</td>
<td>110</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V \leq \text{VDD} \leq 5.5 V</td>
<td>44</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td>SCKp hold time (from SCKp( ^\downarrow )) Note 2</td>
<td>#KSI1</td>
<td>19</td>
<td>19</td>
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<td>ns</td>
</tr>
<tr>
<td>Delay time from SCKp( ^\downarrow ) to SOp output Note 3</td>
<td>#SDT1</td>
<td>( C = 30 , \text{pF} ) Note 4</td>
<td>25</td>
<td>25</td>
<td></td>
</tr>
</tbody>
</table>

**Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp\( ^\downarrow \)” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp\( ^\downarrow \)” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp\( ^\downarrow \)” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
4. C is the load capacitance of the SCKp and SOp output lines.
5. Operating conditions of LS (low-speed main) mode is \( T_A = -40 \) to \(+85^\circ \text{C} \).

**Caution** Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMG) and port output mode register g (POMG).

**Remarks**
1. \( p \): CSI number \( (p = 00) \), \( m \): Unit number \( (m = 0) \), \( n \): Channel number \( (n = 0) \),
\( g \): PIM and POM number \( (g = 1) \)
2. \( f_{MCK} \): Serial array unit operation clock frequency
   (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRMn). \( m \): Unit number,
   \( n \): Channel number \( (mn = 00) \))
(3) **During communication at same potential (Simplified SPI (CSI) mode) (slave mode, SCKp... external clock input)**

\(\text{T_A = -40 to +105^\circ C}\)\(^6\), \(2.7 \text{ V} \leq \text{V}_{DD} \leq 5.5 \text{ V}, \text{V}_{SS} = 0 \text{ V}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main) Mode</th>
<th>LS (low-speed main) Mode</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN.</td>
<td>MAX.</td>
<td>MIN.</td>
</tr>
<tr>
<td>SCKp cycle time</td>
<td>(t_{KCY})</td>
<td>(4.0 \text{ V} \leq \text{V}_{DD} \leq 5.5 \text{ V})</td>
<td>(20 \text{ MHz} &lt; f_{MCK})</td>
<td>(8/f_{MCK})</td>
<td>--</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(f_{MCK} \leq 20 \text{ MHz})</td>
<td>(6/f_{MCK})</td>
<td>(6/f_{MCK})</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(2.7 \text{ V} \leq \text{V}_{DD} \leq 5.5 \text{ V})</td>
<td>(16 \text{ MHz} &lt; f_{MCK})</td>
<td>(8/f_{MCK})</td>
<td>--</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(f_{MCK} \leq 16 \text{ MHz})</td>
<td>(6/f_{MCK})</td>
<td>(6/f_{MCK})</td>
<td>ns</td>
</tr>
<tr>
<td>SCKp high-/low-level width</td>
<td>(t_{KH}, t_{KL})</td>
<td>(2.7 \text{ V} \leq \text{V}_{DD} \leq 5.5 \text{ V})</td>
<td>(16 \text{ MHz} &lt; f_{MCK})</td>
<td>(2/f_{MCK}+44)</td>
<td>ns</td>
</tr>
<tr>
<td>Slp setup time (to SCKp)(^1)</td>
<td>(t_{SIK})</td>
<td>(1/f_{MCK}+20)</td>
<td>(1/f_{MCK}+30)</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(1/f_{MCK}+31)</td>
<td>(1/f_{MCK}+31)</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Delay time from SCKp to SOp output(^3)</td>
<td>(t_{KSO})</td>
<td>(C = 30 \text{ pF})(^4)</td>
<td>(2/f_{MCK}+110)</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

1. When \(DAP_{mn} = 0\) and \(CKP_{mn} = 0\), or \(DAP_{mn} = 1\) and \(CKP_{mn} = 1\). The Slp setup time becomes “to SCKp” when \(DAP_{mn} = 0\) and \(CKP_{mn} = 1\), or \(DAP_{mn} = 1\) and \(CKP_{mn} = 0\).
2. When \(DAP_{mn} = 0\) and \(CKP_{mn} = 0\), or \(DAP_{mn} = 1\) and \(CKP_{mn} = 1\). The Slp hold time becomes “from SCKp” when \(DAP_{mn} = 0\) and \(CKP_{mn} = 1\), or \(DAP_{mn} = 1\) and \(CKP_{mn} = 0\).
3. When \(DAP_{mn} = 0\) and \(CKP_{mn} = 0\), or \(DAP_{mn} = 1\) and \(CKP_{mn} = 1\). The delay time to SOp output becomes “from SCKp” when \(DAP_{mn} = 0\) and \(CKP_{mn} = 1\), or \(DAP_{mn} = 1\) and \(CKP_{mn} = 0\).
4. \(C\) is the load capacitance of the SOp output lines.
5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps
6. Operating conditions of LS (low-speed main) mode is \(\text{T_A = -40 to +85^\circ C}\).

**Caution**
Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register \(g\) (PIMg) and port output mode register \(g\) (POMg).

**Remarks**

1. \(p\): CSI number \((p = 00)\), \(m\): Unit number \((m = 0)\), \(n\): Channel number \((n = 0)\),
\(g\): PIM and POM number \((g = 1)\)
2. \(f_{MCK}\): Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register \(mn\) (SMRmn). \(m\): Unit number, \(n\): Channel number \((mn = 00)\))
Simplified SPI (CSI) mode connection diagram (during communication at same potential)

- **RL78 microcontroller**
- **SCKp**
- **Slp**
- **SOp**
- **SCK**
- **SO**
- **SI**
- **User’s device**

Simplified SPI (CSI) mode serial transfer timing (during communication at same potential)

(When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$.)

![Timing Diagram 1](image1)

- **SIp**: Input data
- **SOp**: Output data
- **tKCY1, 2**
- **tKL1, 2**
- **tKH1, 2**
- **tSIK1, 2**
- **tKSI1, 2**
- **tKSO1, 2**
- **SCKp**
- **Slp**
- **SOp**

Simplified SPI (CSI) mode serial transfer timing (during communication at same potential)

(When $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.)

![Timing Diagram 2](image2)

- **SIp**: Input data
- **SOp**: Output data
- **tKCY1, 2**
- **tKL1, 2**
- **tKH1, 2**
- **tSIK1, 2**
- **tKSI1, 2**
- **tKSO1, 2**
- **SCKp**
- **Slp**
- **SOp**

**Remarks**

1. **p**: CSI number ($p = 00$)
2. **m**: Unit number, **n**: Channel number ($mn = 00$)
(4) Communication at different potential (2.5 V, 3 V) (UART mode) (1/2)

\((T_A = -40 \text{ to } +105^\circ C, 2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, V_{SS} = 0 \text{ V})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main) Mode</th>
<th>LS (low-speed main) Mode</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN.</td>
<td>MAX.</td>
<td>MIN.</td>
</tr>
<tr>
<td>Transfer rate</td>
<td>Reception</td>
<td>4.0 V \leq V_{DD} \leq 5.5 V, 2.7 V \leq V_{b} \leq 4.0 V</td>
<td>f_{MCK}/6^{\text{Note 1}}</td>
<td>f_{MCK}/6^{\text{Note 1}}</td>
<td>bps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK}^{\text{Note 2}}</td>
<td>5.3</td>
<td>1.3</td>
<td>Mbps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V \leq V_{DD} &lt; 4.0 V, 2.3 V \leq V_{b} \leq 2.7 V</td>
<td>f_{MCK}/6^{\text{Note 1}}</td>
<td>f_{MCK}/6^{\text{Note 1}}</td>
<td>bps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK}^{\text{Note 2}}</td>
<td>5.3</td>
<td>1.3</td>
<td>Mbps</td>
</tr>
</tbody>
</table>

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.
2. The maximum operating frequencies of the CPU/peripheral hardware clock \(f_{CLK}\) are:
   - HS (high-speed main) mode: 32 MHz (2.7 V \leq V_{DD} \leq 5.5 V)
   - LS (low-speed main) mode: 8 MHz (2.7 V \leq V_{DD} \leq 5.5 V), \(T_A = -40 \text{ to } +85^\circ C\).

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output \(V_{DD}\) tolerance mode for the TxDq pin by using port input mode register \(g\) (PIMg) and port output mode register \(g\) (POMg). For \(V_{IH}\) and \(V_{IL}\), see the DC characteristics with TTL input buffer selected.

Remarks 1. \(V_b[V]\): Communication line voltage
2. \(q\): UART number \((q = 0, 1)\), \(g\): PIM and POM number \((g = 0, 1)\)
3. \(f_{MCK}\): Serial array unit operation clock frequency
   - (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). \(m\): Unit number, \(n\): Channel number \((mn = 00 \text{ to } 03)\)
(4) Communication at different potential (2.5 V, 3 V) (UART mode) (2/2)

\( T_A = -40 \text{ to } +105^\circ C \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main) Mode</th>
<th>LS (low-speed main) Mode</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer rate</td>
<td>Transmission</td>
<td>( 4.0 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}, 2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V} )</td>
<td>Note 1</td>
<td>Note 1</td>
<td>bps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Theoretical value of the maximum transfer rate ( C_b = 50 \text{ pF}, R_b = 1.4 \text{ k\Omega}, V_b = 2.7 \text{ V} )</td>
<td>2.8Note 2</td>
<td>2.8Note 2</td>
<td>Mbps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 2.7 \text{ V} \leq \text{VDD} &lt; 4.0 \text{ V}, 2.3 \text{ V} \leq \text{Vb} \leq 2.7 \text{ V} )</td>
<td>Note 3</td>
<td>Note 3</td>
<td>bps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Theoretical value of the maximum transfer rate ( C_b = 50 \text{ pF}, R_b = 2.7 \text{ k\Omega}, V_b = 2.3 \text{ V} )</td>
<td>1.2Note 4</td>
<td>1.2Note 4</td>
<td>Mbps</td>
</tr>
</tbody>
</table>

Notes

1. The smaller maximum transfer rate derived by using \( f_{MCK}/6 \) or the following expression is valid maximum transfer rate.

Expression for calculating the transfer rate when \( 4.0 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V} \) and \( 2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V} \)

\[
\text{Maximum transfer rate} = \frac{1}{\left( -C_b \times R_b \times \ln \left( 1 - \frac{2.2}{V_b} \right) \right) \times 3}
\]

Baud rate error (theoretical value) = \( \frac{1}{\text{Transfer rate}} \times \frac{\left( \frac{1}{2} \times \text{Transfer rate} \right)}{\left( \frac{1}{2} \times \text{Transfer rate} \right) \times \text{Number of transferred bits}} \times 100 \%
\]

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. See Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using \( f_{MCK}/6 \) or the following expression is valid maximum transfer rate.

Expression for calculating the transfer rate when \( 2.7 \text{ V} \leq \text{VDD} < 4.0 \text{ V} \) and \( 2.3 \text{ V} \leq \text{Vb} \leq 2.7 \text{ V} \)

\[
\text{Maximum transfer rate} = \frac{1}{\left( -C_b \times R_b \times \ln \left( 1 - \frac{2.0}{V_b} \right) \right) \times 3}
\]

Baud rate error (theoretical value) = \( \frac{1}{\text{Transfer rate}} \times \frac{\left( \frac{1}{2} \times \text{Transfer rate} \right)}{\left( \frac{1}{2} \times \text{Transfer rate} \right) \times \text{Number of transferred bits}} \times 100 \%
\]

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. See Note 3 above to calculate the maximum transfer rate under conditions of the customer.

5. Operating conditions of LS (low-speed main) mode is \( T_A = -40 \text{ to } +85^\circ C \).

Caution

Select the TTL input buffer for the Rxdq pin and the N-ch open drain output (Vdd tolerance) mode for the Txdq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For \( V_H \) and \( V_L \), see the DC characteristics with TTL input buffer selected.

Remarks

1. \( R_b[q] \): Communication line (Txdq) pull-up resistance,
   \( C_b[f] \): Communication line (Txdq) load capacitance, \( V_b[v] \): Communication line voltage
2. \( q \): UART number (\( q = 0, 1 \)), \( g \): PIM and POM number (\( g = 0, 1 \))
3. \( f_{MCK} \): Serial array unit operation clock frequency
   (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn)).
   \( m \): Unit number, \( n \): Channel number (\( mn = 00 \text{ to } 03 \))
UART mode connection diagram (during communication at different potential)

UART mode bit width (during communication at different potential) (reference)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. Rs[Ω]: Communication line (TxDq) pull-up resistance, Vb[V]: Communication line voltage
2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)
(5) Communication at different potential (2.5 V, 3 V) (Simplified SPI (CSI) mode) (master mode, SCKp...
internal clock output)
(TA = –40 to +105°C Note 3, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main) Mode</th>
<th>LS (low-speed main) Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN.</td>
<td>MAX.</td>
</tr>
<tr>
<td>SCKp cycle time</td>
<td>bCKV</td>
<td>4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ</td>
<td>200</td>
<td>1150</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V ≤ VDD &lt; 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ</td>
<td>bCKV/2 – 50</td>
<td>bCKV/2 – 75</td>
</tr>
<tr>
<td>SCKp high-level width</td>
<td>bCKH</td>
<td>4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ</td>
<td>bCKV/2 – 7</td>
<td>bCKV/2 – 50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V ≤ VDD &lt; 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ</td>
<td>81</td>
<td>479</td>
</tr>
<tr>
<td>SCKp low-level width</td>
<td>bCKL</td>
<td>4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ</td>
<td>10</td>
<td>19</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V ≤ VDD &lt; 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ</td>
<td>60</td>
<td>100</td>
</tr>
<tr>
<td>SCKp setup time</td>
<td>bSIK</td>
<td>4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ</td>
<td>44</td>
<td>110</td>
</tr>
<tr>
<td>(to SCKp↑)</td>
<td></td>
<td>2.7 V ≤ VDD &lt; 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ</td>
<td>10</td>
<td>19</td>
</tr>
<tr>
<td>SCKp hold time</td>
<td>bSIH</td>
<td>4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ</td>
<td>10</td>
<td>25</td>
</tr>
<tr>
<td>(from SCKp↑)</td>
<td></td>
<td>2.7 V ≤ VDD &lt; 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ</td>
<td>4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ</td>
<td>10</td>
</tr>
</tbody>
</table>

Notes
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. Operating conditions of LS (low-speed main) mode is TA = –40 to +85°C.

Caution
Select the TTL input buffer for the Slop pin and the N-ch open drain output (VDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For Vih and Vil, see the DC characteristics with TTL input buffer selected.

Remarks
1. Rs[Ω]: Communication line (SCKp, SOp) pull-up resistance, Cs[F]: Communication line (SCKp, SOp) load capacitance, VDD[V]: Communication line voltage
2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)
2. ELECTRICAL SPECIFICATIONS (G: Industrial applications, \(T_A = -40 \text{ to } +105^\circ\text{C}\))

(6) Communication at different potential (2.5 V, 3 V) (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output)

\(T_A = -40 \text{ to } +105^\circ\text{C}\)\(^{\text{Note 2}}\), \(2.7 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}, \text{VSS} = 0 \text{ V}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>(\text{HS (high-speed main) Mode})</th>
<th>(\text{LS (low-speed main) Mode})</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCKp cycle time</td>
<td>bcy1</td>
<td>(b_{cy1} \geq 4/f_{CL\max}) (4.0 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}, 2.7 \text{ V} \leq \text{Vt} \leq 4.0 \text{ V}, C_o = 30 \text{ pF}, R_o = 1.4 \text{ k})</td>
<td>300</td>
<td>1150</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2.7 \text{ V} \leq \text{VDD} &lt; 4.0 \text{ V}, 2.3 \text{ V} \leq \text{Vt} \leq 2.7 \text{ V}, C_o = 30 \text{ pF}, R_o = 2.7 \text{ k})</td>
<td>500</td>
<td>1150</td>
</tr>
<tr>
<td>SCKp high-level width</td>
<td>bo1</td>
<td>(4.0 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}, 2.7 \text{ V} \leq \text{Vt} \leq 4.0 \text{ V}, C_o = 30 \text{ pF}, R_o = 1.4 \text{ k})</td>
<td>(b_{cy1}/2 - 75)</td>
<td>(b_{cy1}/2 - 75)</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2.7 \text{ V} \leq \text{VDD} &lt; 4.0 \text{ V}, 2.3 \text{ V} \leq \text{Vt} \leq 2.7 \text{ V}, C_o = 30 \text{ pF}, R_o = 2.7 \text{ k})</td>
<td>(b_{cy1}/2 - 170)</td>
<td>(b_{cy1}/2 - 170)</td>
</tr>
<tr>
<td>SCKp low-level width</td>
<td>b1</td>
<td>(4.0 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}, 2.7 \text{ V} \leq \text{Vt} \leq 4.0 \text{ V}, C_o = 30 \text{ pF}, R_o = 1.4 \text{ k})</td>
<td>(b_{cy1}/2 - 12)</td>
<td>(b_{cy1}/2 - 50)</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2.7 \text{ V} \leq \text{VDD} &lt; 4.0 \text{ V}, 2.3 \text{ V} \leq \text{Vt} \leq 2.7 \text{ V}, C_o = 30 \text{ pF}, R_o = 2.7 \text{ k})</td>
<td>(b_{cy1}/2 - 18)</td>
<td>(b_{cy1}/2 - 50)</td>
</tr>
<tr>
<td>Stp setup time (to SCKp(^+)) (\text{Note 1})</td>
<td>bsk1</td>
<td>(4.0 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}, 2.7 \text{ V} \leq \text{Vt} \leq 4.0 \text{ V}, C_o = 30 \text{ pF}, R_o = 1.4 \text{ k})</td>
<td>81</td>
<td>479</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2.7 \text{ V} \leq \text{VDD} &lt; 4.0 \text{ V}, 2.3 \text{ V} \leq \text{Vt} \leq 2.7 \text{ V}, C_o = 30 \text{ pF}, R_o = 2.7 \text{ k})</td>
<td>177</td>
<td>479</td>
</tr>
<tr>
<td>Stp hold time (from SCKp(^-)) (\text{Note 1})</td>
<td>b3s1</td>
<td>(4.0 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}, 2.7 \text{ V} \leq \text{Vt} \leq 4.0 \text{ V}, C_o = 30 \text{ pF}, R_o = 1.4 \text{ k})</td>
<td>19</td>
<td>19</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2.7 \text{ V} \leq \text{VDD} &lt; 4.0 \text{ V}, 2.3 \text{ V} \leq \text{Vt} \leq 2.7 \text{ V}, C_o = 30 \text{ pF}, R_o = 2.7 \text{ k})</td>
<td>19</td>
<td>19</td>
</tr>
<tr>
<td>Delay time from SCKp(^+) to SOp output (\text{Note 1})</td>
<td>bsk01</td>
<td>(4.0 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}, 2.7 \text{ V} \leq \text{Vt} \leq 4.0 \text{ V}, C_o = 30 \text{ pF}, R_o = 1.4 \text{ k})</td>
<td>100</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2.7 \text{ V} \leq \text{VDD} &lt; 4.0 \text{ V}, 2.3 \text{ V} \leq \text{Vt} \leq 2.7 \text{ V}, C_o = 30 \text{ pF}, R_o = 2.7 \text{ k})</td>
<td>195</td>
<td>195</td>
</tr>
<tr>
<td>Stp setup time (to SCKp(^-)) (\text{Note 2})</td>
<td>bsk1</td>
<td>(4.0 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}, 2.7 \text{ V} \leq \text{Vt} \leq 4.0 \text{ V}, C_o = 30 \text{ pF}, R_o = 1.4 \text{ k})</td>
<td>44</td>
<td>110</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2.7 \text{ V} \leq \text{VDD} &lt; 4.0 \text{ V}, 2.3 \text{ V} \leq \text{Vt} \leq 2.7 \text{ V}, C_o = 30 \text{ pF}, R_o = 2.7 \text{ k})</td>
<td>44</td>
<td>110</td>
</tr>
<tr>
<td>Stp hold time (from SCKp(^+)) (\text{Note 2})</td>
<td>b3s1</td>
<td>(4.0 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}, 2.7 \text{ V} \leq \text{Vt} \leq 4.0 \text{ V}, C_b = 30 \text{ pF}, R_b = 1.4 \text{ k})</td>
<td>19</td>
<td>19</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2.7 \text{ V} \leq \text{VDD} &lt; 4.0 \text{ V}, 2.3 \text{ V} \leq \text{Vt} \leq 2.7 \text{ V}, C_b = 30 \text{ pF}, R_b = 2.7 \text{ k})</td>
<td>19</td>
<td>19</td>
</tr>
<tr>
<td>Delay time from SCKp(^+) to SOp output (\text{Note 2})</td>
<td>bsk01</td>
<td>(4.0 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}, 2.7 \text{ V} \leq \text{Vt} \leq 4.0 \text{ V}, C_b = 30 \text{ pF}, R_b = 1.4 \text{ k})</td>
<td>25</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2.7 \text{ V} \leq \text{VDD} &lt; 4.0 \text{ V}, 2.3 \text{ V} \leq \text{Vt} \leq 2.7 \text{ V}, C_b = 30 \text{ pF}, R_b = 2.7 \text{ k})</td>
<td>25</td>
<td>25</td>
</tr>
</tbody>
</table>

**Notes**

1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. Operating conditions of LS (low-speed main) mode is \(T_A = -40 \text{ to } +85^\circ\text{C}\).

(Caution and Remarks are listed on the next page.)
Caution  Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For \( V_{IH} \) and \( V_{IL} \), see the DC characteristics with TTL input buffer selected.

Simplified SPI (CSI) mode connection diagram (during communication at different potential)

\[
\begin{align*}
&\text{<Master>} \\
&\quad \begin{array}{c}
\text{SCKp} \\
\text{Slp} \\
\text{SOp}
\end{array} \\
&\quad \begin{array}{c}
R_b \quad V_b \\
R_b \quad V_b
\end{array}
\end{align*}
\]

RL78 microcontroller

User's device

Remarks 1. \( R_b [\Omega] \): Communication line (SCKp, SOp) pull-up resistance, \( C_b [F] \): Communication line (SCKp, SOp) load capacitance, \( V_b [V] \): Communication line voltage

2. \( p \): CSI number (\( p = 00 \)), \( m \): Unit number (\( m = 0 \)), \( n \): Channel number (\( n = 0 \)), \( g \): PIM and POM number (\( g = 1 \))
Simplified SPI (CSI) mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)
### (7) DALI/UART4 mode

(T_A = -40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main) Mode</th>
<th>LS (low-speed main) Mode</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer rate</td>
<td></td>
<td>Maximum transfer rate theoretical value</td>
<td>f_{MCK}/12</td>
<td>f_{MCK}/12</td>
<td>bps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HS: f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>LS: f_{CLK} = 8 MHz, f_{MCK} = f_{CLK}</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Remark**  
f_{MCK}: Operation clock frequency of DALI/UART.  
(Operation clock to be set by the serial clock select register mn (SPS4).)

**Caution**  
Operating conditions of LS (low-speed main) mode is T_A = -40 to +85°C.
2.5.2 Serial interface IICA

(1) I^2C standard mode

\(T_A = -40\) to \(+105^\circ C\) Note 3, \(2.7\) V \(\leq V_{DD} \leq 5.5\) V, \(V_{SS} = 0\) V

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main) Mode</th>
<th>LS (low-speed main) Mode</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCLA0 clock frequency</td>
<td>(f_{SCL})</td>
<td>Standard mode: (f_{CLK} \geq 1) MHz</td>
<td>0</td>
<td>100</td>
<td>0</td>
</tr>
<tr>
<td>Setup time of restart condition</td>
<td>(t_{SU:STA})</td>
<td></td>
<td>4.7</td>
<td>4.7</td>
<td>(\mu s)</td>
</tr>
<tr>
<td>Hold time(^{Note 1})</td>
<td>(t_{H:STA})</td>
<td></td>
<td>4.0</td>
<td>4.0</td>
<td>(\mu s)</td>
</tr>
<tr>
<td>Hold time when SCLA0 = &quot;L&quot;</td>
<td>(t_{LOW})</td>
<td></td>
<td>4.7</td>
<td>4.7</td>
<td>(\mu s)</td>
</tr>
<tr>
<td>Hold time when SCLA0 = &quot;H&quot;</td>
<td>(t_{HIGH})</td>
<td></td>
<td>4.0</td>
<td>4.0</td>
<td>(\mu s)</td>
</tr>
<tr>
<td>Data setup time (reception)</td>
<td>(t_{SU:DAT})</td>
<td></td>
<td>250</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td>Data hold time (transmission)(^{Note 2})</td>
<td>(t_{H:DAT})</td>
<td></td>
<td>0</td>
<td>3.45</td>
<td>(\mu s)</td>
</tr>
<tr>
<td>Setup time of stop condition</td>
<td>(t_{SU:STO})</td>
<td></td>
<td>4.0</td>
<td>4.0</td>
<td>(\mu s)</td>
</tr>
<tr>
<td>Bus-free time</td>
<td>(t_{BUF})</td>
<td></td>
<td>4.7</td>
<td>4.7</td>
<td>(\mu s)</td>
</tr>
</tbody>
</table>

Notes
1. The first clock pulse is generated after this period when the start/restart condition is detected.
2. The maximum value (MAX.) of \(t_{H:DAT}\) is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.
3. Operating conditions of LS (low-speed main) mode is \(T_A = -40\) to \(+85^\circ C\).

Remark
The maximum value of \(C_b\) (communication line capacitance) and the value of \(R_b\) (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: \(C_b = 400\) pF, \(R_b = 2.7\) k\(\Omega\)
(2) **I²C fast mode**

**(T_A = −40 to +105°C Note 3, 2.7 V ≤ V_DD ≤ 5.5 V, V_SS = 0 V)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main) Mode</th>
<th>LS (low-speed main) Mode</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCLA0 clock frequency</td>
<td>f_SCL</td>
<td>fast mode: f_CLK ≥ 3.5 MHz</td>
<td>0</td>
<td>400</td>
<td>kHz</td>
</tr>
<tr>
<td>Setup time of restart condition</td>
<td>t_SU:STA</td>
<td></td>
<td>0.6</td>
<td>0.6</td>
<td>μs</td>
</tr>
<tr>
<td>Hold time<strong>Note 1</strong></td>
<td>t_LOW</td>
<td></td>
<td>1.3</td>
<td>1.3</td>
<td>μs</td>
</tr>
<tr>
<td>Hold time when SCLA0 = “L”</td>
<td>t_LOW</td>
<td></td>
<td>1.3</td>
<td>1.3</td>
<td>μs</td>
</tr>
<tr>
<td>Hold time when SCLA0 = “H”</td>
<td>t_HIGH</td>
<td></td>
<td>0.6</td>
<td>0.6</td>
<td>μs</td>
</tr>
<tr>
<td>Data setup time (reception)</td>
<td>t_SU:DAT</td>
<td></td>
<td>100</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>Data hold time (transmission)<strong>Note 2</strong></td>
<td>t_HD:DAT</td>
<td></td>
<td>0</td>
<td>0.9</td>
<td>μs</td>
</tr>
<tr>
<td>Setup time of stop condition</td>
<td>t_SU:STO</td>
<td></td>
<td>0.6</td>
<td>0.6</td>
<td>μs</td>
</tr>
<tr>
<td>Bus-free time</td>
<td>t_BUF</td>
<td></td>
<td>1.3</td>
<td>1.3</td>
<td>μs</td>
</tr>
</tbody>
</table>

**Notes**

1. The first clock pulse is generated after this period when the start/restart condition is detected.
2. The maximum value (MAX.) of t_HD:DAT is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.
3. Operating conditions of LS (low-speed main) mode is T_A = −40 to +85°C.

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: Cb = 320 pF, Rb = 1.1 kΩ

**I²C serial transfer timing**
## 2.6 Analog Characteristics

### 2.6.1 A/D converter characteristics

**Classification of A/D converter characteristics**

<table>
<thead>
<tr>
<th>Input channel</th>
<th>Reference Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Reference voltage (+) = AVREFP</td>
</tr>
<tr>
<td></td>
<td>Reference voltage (−) = AVREFM</td>
</tr>
<tr>
<td></td>
<td>Reference voltage (+) = VDD</td>
</tr>
<tr>
<td></td>
<td>Reference voltage (−) = VSS</td>
</tr>
<tr>
<td></td>
<td>Reference voltage (+) = VBGR</td>
</tr>
<tr>
<td></td>
<td>Reference voltage (−) = AVREFM</td>
</tr>
</tbody>
</table>

| ANI0 to ANI2, ANI4 to ANI7 | See 2.6.1 (1). | See 2.6.1 (3). | See 2.6.1 (4). |
| ANI16 to ANI19 | See 2.6.1 (2). | | |
| Internal reference voltage Temperature sensor output voltage | See 2.6.1 (1). | | – |
(1) When reference voltage (+)= AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-)= AVREFM/ANI1 (ADREFM = 1), target pin: ANI2, ANI4 to ANI7, internal reference voltage, and temperature sensor output voltage

\[(T_A = -40 \text{ to } +105^\circ \text{C}, \ 2.7 \text{ V} \leq AVREFP \leq V_DD \leq 5.5 \text{ V}, \ V_SS = 0 \text{ V}, \ \text{Reference voltage (+)} = AVREFP, \ \text{Reference voltage (-)} = AVREFM = 0 \text{ V}\]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>RES</td>
<td>10-bit resolution</td>
<td>8</td>
<td>10</td>
<td>bit</td>
<td></td>
</tr>
<tr>
<td>Overall error</td>
<td>AINL</td>
<td>10-bit resolution AVREFP = VDD</td>
<td>1.2</td>
<td>±3.5</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>Conversion time</td>
<td>ICONV</td>
<td>10-bit resolution Target pin: ANI2, ANI4 to ANI7</td>
<td>3.6 V ≤ VDD ≤ 5.5 V</td>
<td>2.125</td>
<td>39</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)</td>
<td>2.7 V ≤ VDD ≤ 5.5 V</td>
<td>3.1875</td>
<td>39</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.6 V ≤ VDD ≤ 5.5 V</td>
<td>2.375</td>
<td>39</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V ≤ VDD ≤ 5.5 V</td>
<td>3.5625</td>
<td>39</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>Zero-scale error</td>
<td>E_ZS</td>
<td>10-bit resolution AVREFP = VDD</td>
<td>±0.25</td>
<td>%FSR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full-scale error</td>
<td>E_FS</td>
<td>10-bit resolution AVREFP = VDD</td>
<td>±0.25</td>
<td>%FSR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Integral linearity error</td>
<td>ILE</td>
<td>10-bit resolution AVREFP = VDD</td>
<td>±2.5</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential linearity error</td>
<td>DLE</td>
<td>10-bit resolution AVREFP = VDD</td>
<td>±1.5</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog input voltage</td>
<td>V_IN</td>
<td>ANI2, ANI4 to ANI7</td>
<td>0</td>
<td>AVREFP</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Internal reference voltage (HS (high-speed main) mode)</td>
<td>V_IN</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Temperature sensor output voltage (HS (high-speed main) mode)</td>
<td>V_TMP</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes
1. Excludes quantization error (±1/2 LSB).
2. This value is indicated as a ratio (%FSR) to the full-scale value.
3. When AVREFP < VDD, the MAX. values are as follows.
   - Overall error: Add ±1.0 LSB to the MAX. value when AVREFP = VDD.
   - Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AVREFP = VDD.
   - Integral linearity error/Differential linearity error: Add ±0.5 LSB to the MAX. value when AVREFP = VDD.
4. See 2.6.2 Temperature sensor/internal reference voltage characteristics.
(2) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI16 to ANI19

(TA = −40 to +105°C, 2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (−) = AVREFM = 0 V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>RES</td>
<td>8-bit resolution</td>
<td>8</td>
<td>10</td>
<td>bit</td>
<td></td>
</tr>
<tr>
<td>Overall error</td>
<td>AINL</td>
<td>10-bit resolution AVREFP = VDD</td>
<td>1.2</td>
<td>±5.0</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>Conversion time</td>
<td>tCONV</td>
<td>10-bit resolution AVREFP = VDD</td>
<td>3.6 V ≤ VDD ≤ 5.5 V</td>
<td>2.125</td>
<td>39</td>
<td>µs</td>
</tr>
<tr>
<td>Zero-scale error</td>
<td>EFS</td>
<td>10-bit resolution AVREFP = VDD</td>
<td>±0.35</td>
<td>%FSR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full-scale error</td>
<td>EFS</td>
<td>10-bit resolution AVREFP = VDD</td>
<td>±0.35</td>
<td>%FSR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Integral linearity error</td>
<td>ILE</td>
<td>10-bit resolution AVREFP = VDD</td>
<td>±3.5</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential linearity error</td>
<td>DLE</td>
<td>10-bit resolution AVREFP = VDD</td>
<td>±2.0</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog input voltage</td>
<td>VAIN</td>
<td>ANI16 to ANI19</td>
<td>0</td>
<td>AVREFP and VDD</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AVREFP < VDD, the MAX. values are as follows.
   - Overall error: Add ±1.0 LSB to the MAX. value when AVREFP = VDD.
   - Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AVREFP = VDD.
   - Integral linearity error/Differential linearity error: Add ±0.5 LSB to the MAX. value when AVREFP = VDD.
(3) When reference voltage (⁺) = Vdd (ADREFP1 = 0, ADREFP0 = 0), reference voltage (⁻) = Vss (ADREFM = 0), target pin: ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19, internal reference voltage, and temperature sensor output voltage

\(T_A = -40 \text{ to } +105^\circ\text{C}, 2.7 \text{ V} \leq \text{Vdd} \leq 5.5 \text{ V}, \text{Vss} = 0 \text{ V}, \text{Reference voltage (⁺)} = \text{Vdd}, \text{Reference voltage (⁻)} = \text{Vss}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>RES</td>
<td>10-bit resolution</td>
<td>8</td>
<td>10</td>
<td></td>
<td>bit</td>
</tr>
<tr>
<td>Overall error^Note 1</td>
<td>AINL</td>
<td>10-bit resolution</td>
<td>1.2</td>
<td></td>
<td>±7.0</td>
<td>LSB</td>
</tr>
<tr>
<td>Conversion time^Note 1</td>
<td>t_{CONV}</td>
<td>10-bit resolution, Target pin: ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19</td>
<td>3.6 V ≤ Vdd ≤ 5.5 V</td>
<td>2.125</td>
<td>39</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V ≤ Vdd ≤ 5.5 V</td>
<td>3.1875</td>
<td>39</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>Conversion time^Note 1</td>
<td>t_{CONV}</td>
<td>10-bit resolution, Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)</td>
<td>3.6 V ≤ Vdd ≤ 5.5 V</td>
<td>2.375</td>
<td>39</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V ≤ Vdd ≤ 5.5 V</td>
<td>3.5625</td>
<td>39</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>Zero-scale error^Note 1, 2</td>
<td>E_{ZS}</td>
<td>10-bit resolution</td>
<td>±0.60</td>
<td>%FSR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full-scale error^Note 1, 2</td>
<td>E_{FS}</td>
<td>10-bit resolution</td>
<td>±0.60</td>
<td>%FSR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Integral linearity error^Note 1</td>
<td>ILE</td>
<td>10-bit resolution</td>
<td>±4.0</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential linearity error^Note 1</td>
<td>DLE</td>
<td>10-bit resolution</td>
<td>±2.0</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog input voltage</td>
<td>V_{AIN}</td>
<td>ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19</td>
<td>0</td>
<td>Vdd</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Internal reference voltage (HS (high-speed main) mode)</td>
<td></td>
<td>Vdd</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Temperature sensor output voltage (HS (high-speed main) mode)</td>
<td></td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes 1. Excludes quantization error (±1/2 LSB).
2. This value is indicated as a ratio (%FSR) to the full-scale value.
3. See 2.6.2 Temperature sensor/internal reference voltage characteristics.
(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage 
(−) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI0, ANI2, ANI4 to ANI7, ANI16 to ANI19

(TA = −40 to +105°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = VBORefNote 3, Reference voltage (−) = 
AVREFM = 0 VNote 4, HS (high-speed main) mode)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>RES</td>
<td>8-bit resolution</td>
<td></td>
<td></td>
<td></td>
<td>bit</td>
</tr>
<tr>
<td>Conversion time</td>
<td>tCONV</td>
<td>8-bit resolution</td>
<td>17</td>
<td>39</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>Zero-scale errorNote 1, 2</td>
<td>EZS</td>
<td>8-bit resolution</td>
<td>±0.60</td>
<td>%FSR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Integral linearity errorNote 1</td>
<td>ILE</td>
<td>8-bit resolution</td>
<td>±2.0</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential linearity errorNote 1</td>
<td>DLE</td>
<td>8-bit resolution</td>
<td>±1.0</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog input voltage</td>
<td>VAIN</td>
<td>0</td>
<td></td>
<td></td>
<td>VSS</td>
<td>V</td>
</tr>
</tbody>
</table>

Notes 1. Excludes quantization error (±1/2 LSB).
2. This value is indicated as a ratio (%FSR) to the full-scale value.
3. See 2.6.2 Temperature sensor/internal reference voltage characteristics.
4. When reference voltage (−) = VSS, the MAX. values are as follows.
   Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (−) = AVREFM.
   Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (−) = AVREFM.
   Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (−) = AVREFM.
2.6.2 Temperature sensor/internal reference voltage characteristics

(TA = -40 to +105°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V, HS (high-speed main) mode)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature sensor output voltage</td>
<td>V_TMPS25</td>
<td>Setting ADS register = 80H, TA = +25°C</td>
<td>1.05</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Internal reference voltage</td>
<td>V_BGRT</td>
<td>Setting ADS register = 81H</td>
<td>1.38</td>
<td>1.45</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>Temperature coefficient</td>
<td>F_VTMPS</td>
<td>Temperature sensor that depends on the temperature</td>
<td>-3.6</td>
<td></td>
<td></td>
<td>mV/C</td>
</tr>
<tr>
<td>Operation stabilization wait time</td>
<td>t_AMP</td>
<td></td>
<td>5</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
</tbody>
</table>
2.6.3 Programmable gain amplifier

\((T_A = -40\text{ to } +105^\circ \text{C}, 2.7 \text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5 \text{ V}, V_{SS} = AV_{REFM} = 0 \text{ V})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input offset voltage</td>
<td>(V_{IOPGA})</td>
<td>(\pm 5 \text{ mV})</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input voltage range</td>
<td>(V_{IPGA})</td>
<td>0 (0.9V_{DD})</td>
<td>(\pm 1 %)</td>
<td>(\pm 1.5 %)</td>
<td>(\pm 2 %)</td>
<td>(V)</td>
</tr>
<tr>
<td>Gain error(^1)</td>
<td></td>
<td>4, 8 times</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>16 times</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>32 times</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slew rate(^1)</td>
<td>(SR_{RPGA})</td>
<td>4.0 (\text{ V} \leq V_{DD} \leq 5.5 \text{ V})</td>
<td>4, 8 times</td>
<td>4 (\text{ V/\mu s})</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>16, 32 times</td>
<td>1.4 (\text{ V/\mu s})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(SR_{FPGA})</td>
<td>2.7 (\text{ V} \leq V_{DD} &lt; 4.0 \text{ V})</td>
<td>4, 8 times</td>
<td>1.8 (\text{ V/\mu s})</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>16, 32 times</td>
<td>0.5 (\text{ V/\mu s})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(SR_{FPGA})</td>
<td>4.0 (\text{ V} \leq V_{DD} \leq 5.5 \text{ V})</td>
<td>4, 8 times</td>
<td>3.2 (\text{ V/\mu s})</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>16, 32 times</td>
<td>1.4 (\text{ V/\mu s})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(SR_{FPGA})</td>
<td>2.7 (\text{ V} \leq V_{DD} &lt; 4.0 \text{ V})</td>
<td>4, 8 times</td>
<td>1.2 (\text{ V/\mu s})</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>16, 32 times</td>
<td>0.5 (\text{ V/\mu s})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operation stabilization wait time(^2)</td>
<td>(t_{PGA})</td>
<td>4, 8 times</td>
<td>5 (\mu s)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>16, 32 times</td>
<td>10 (\mu s)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

1. When \(V_{IPGA} = 0.1V_{DD}/\text{gain\text{ to }0.9V_{DD}/\text{gain}}\).
2. Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

**Remark** These characteristics apply when \(AV_{REFM}\) is selected as GND of the PGA by using the CVRVS1 bit.
2.6.4 Comparator

\((T_A = \text{-}40 \text{ to } +105^\circ\text{C}, 2.7 \text{ V} \leq AV_{\text{REFP}} = V_{\text{DD}} \leq 5.5 \text{ V}, V_{\text{SS}} = AV_{\text{REFM}} = 0 \text{ V})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input offset voltage</td>
<td>(V_{\text{ICMP}})</td>
<td>CMP0P to CMP5P</td>
<td>(\pm 5)</td>
<td>(\pm 40) mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CMPCOM</td>
<td>0.045</td>
<td>0.9V_{\text{DD}} V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input voltage range</td>
<td>(V_{\text{CMP}})</td>
<td>CMP0P to CMP5P</td>
<td>(0)</td>
<td>(V_{\text{DD}}) V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CMPCOM</td>
<td>0.045</td>
<td>0.9V_{\text{DD}} V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal reference voltage deviation</td>
<td>(\Delta V_{\text{RE}})</td>
<td>CmRVM register values: 7FH to 80H ((m = 0) to 2)</td>
<td>(\pm 2)</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Other than above</td>
<td>(\pm 1)</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Response time</td>
<td>(t_{\text{CR}}, t_{\text{CF}})</td>
<td>Input amplitude = (\pm 100) mV</td>
<td>70</td>
<td>150 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operation stabilization wait time(^{\text{Note 1}})</td>
<td>(t_{\text{CMP}})</td>
<td>3.3 V (\leq V_{\text{DD}} \leq 5.5) V</td>
<td>1</td>
<td>(\mu)s</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V (\leq V_{\text{DD}} &lt; 3.3) V</td>
<td>3</td>
<td>(\mu)s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference voltage stabilization wait</td>
<td>(t_{\text{VR}})</td>
<td>CVRE: 0 to (^{\text{Note 2}})</td>
<td>10</td>
<td>(\mu)s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>time(^{\text{Note 2}})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

1. Time required until a state is entered where the DC and AC specifications of the comparator are satisfied after the operation of the comparator has been enabled (CMPnEN bit = 1; \(n = 0\) to 5)
2. Enable comparator output (CnOE bit = 1; \(n = 0\) to 5) after enabling operation of the internal reference voltage generator (by setting the CVREm bit to 1; \(m = 0\) to 2) and waiting for the operation stabilization time to elapse.

**Remark** These characteristics apply when \(AV_{\text{REFP}}\) is selected as the power supply source of the internal reference voltage by using the CVRVS0 bit, and when \(AV_{\text{REFM}}\) is selected as GND of the internal reference voltage by using the CVRVS1 bit.
2.6.5 POR circuit characteristics

\[(T_A = -40 \text{ to } +105^\circ C, \ V_{SS} = 0 \ V)\]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detection voltage</td>
<td>(V_{POR})</td>
<td>Power supply rise time</td>
<td>1.45</td>
<td>1.51</td>
<td>1.57</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{POR})</td>
<td>Power supply fall time</td>
<td>1.44</td>
<td>1.50</td>
<td>1.56</td>
<td>V</td>
</tr>
<tr>
<td>Minimum pulse width[Note]</td>
<td>(T_{PW})</td>
<td></td>
<td>300</td>
<td></td>
<td></td>
<td>(\mu)s</td>
</tr>
</tbody>
</table>

**Note** Minimum time required for a POR reset when \(V_{DD}\) exceeds below \(V_{POR}\). This is also the minimum time required for a POR reset from when \(V_{DD}\) exceeds below 0.7 V to when \(V_{DD}\) exceeds \(V_{POR}\) while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).

![POR Circuit Diagram](attachment:POR_diagram.png)
2.6.6 LVD circuit characteristics

**LVD Detection Voltage of Reset Mode and Interrupt Mode**

(TA = -40 to +105°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detection voltage level</td>
<td>VLD0</td>
<td>Power supply rise time</td>
<td>3.97</td>
<td>4.06</td>
<td>4.14</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power supply fall time</td>
<td>3.89</td>
<td>3.98</td>
<td>4.06</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VLD1</td>
<td>Power supply rise time</td>
<td>3.67</td>
<td>3.75</td>
<td>3.82</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power supply fall time</td>
<td>3.59</td>
<td>3.67</td>
<td>3.74</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VLD2</td>
<td>Power supply rise time</td>
<td>3.06</td>
<td>3.13</td>
<td>3.19</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power supply fall time</td>
<td>2.99</td>
<td>3.06</td>
<td>3.12</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VLD3</td>
<td>Power supply rise time</td>
<td>2.95</td>
<td>3.02</td>
<td>3.08</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power supply fall time</td>
<td>2.89</td>
<td>2.96</td>
<td>3.02</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VLD4</td>
<td>Power supply rise time</td>
<td>2.85</td>
<td>2.92</td>
<td>2.97</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power supply fall time</td>
<td>2.79</td>
<td>2.86</td>
<td>2.91</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VLD5</td>
<td>Power supply rise time</td>
<td>2.75</td>
<td>2.81</td>
<td>2.87</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power supply fall time</td>
<td>2.70</td>
<td>2.75</td>
<td>2.81</td>
<td>V</td>
</tr>
</tbody>
</table>

| Minimum pulse width | t_LW | 300 | µs |
| Detection delay time |      | 300 | µs |

**LVD Detection Voltage of Interrupt & Reset Mode**

(TA = -40 to +105°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupt and reset mode</td>
<td>VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage: 2.7 V</td>
<td>Rising release reset voltage</td>
<td>2.70</td>
<td>2.75</td>
<td>2.81</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>LVIS1, LVIS0 = 1, 0</td>
<td>Falling interrupt voltage</td>
<td>2.85</td>
<td>2.92</td>
<td>2.97</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>LVIS1, LVIS0 = 0, 1</td>
<td>Rising release reset voltage</td>
<td>2.95</td>
<td>3.02</td>
<td>3.08</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>LVIS1, LVIS0 = 0, 0</td>
<td>Falling interrupt voltage</td>
<td>2.89</td>
<td>2.96</td>
<td>3.02</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>LVIS1, LVIS0 = 0, 0</td>
<td>Rising release reset voltage</td>
<td>3.97</td>
<td>4.06</td>
<td>4.14</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>LVIS1, LVIS0 = 0, 0</td>
<td>Falling interrupt voltage</td>
<td>3.89</td>
<td>3.98</td>
<td>4.06</td>
<td>V</td>
</tr>
</tbody>
</table>

2.6.7 Supply voltage rise inclination characteristics

(TA = -40 to +105°C, VSS = 0 V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage rise</td>
<td>SVDD</td>
<td></td>
<td>54</td>
<td>V/ms</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Caution: Keep the internal reset status by using the LVD circuit or an external reset signal until VDD rises to within the operating voltage range shown in 32.4 AC Characteristics.
2.7 RAM Data Retention Characteristics

\((T_A = -40 \text{ to } +105 ^\circ C, V_{SS} = 0 \text{ V})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data retention supply voltage</td>
<td>(V_{DDR})</td>
<td>Note 2</td>
<td>1.44</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

**Note** The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

**Caution** When CPU is operated at the voltage of out of the operation voltage range, RAM data is not retained. Therefore, set STOP mode before the supplied voltage is below the operation voltage range.

---

![Diagram of RAM Data Retention Characteristics](attachment:image.png)
2.8 Flash Memory Programming Characteristics

\( (T_A = -40 \text{ to } +105^\circ\text{C}, 2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, V_{SS} = 0 \text{ V}) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU/peripheral hardware clock frequency</td>
<td>fCLK</td>
<td>(2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V})</td>
<td>1</td>
<td>32</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Number of code flash rewrites(^{a, b, c})</td>
<td>Cer,w</td>
<td>Retained for 20 years, (T_A = 85^\circ\text{C})(^{c})</td>
<td>1,000</td>
<td></td>
<td></td>
<td>Times</td>
</tr>
<tr>
<td>Number of data flash rewrites(^{a, b, c})</td>
<td>Cer,d</td>
<td>Retained for 1 year, (T_A = 25^\circ\text{C})(^{c})</td>
<td></td>
<td>1,000,000</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Retained for 5 years, (T_A = 85^\circ\text{C})(^{c})</td>
<td>100,000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Retained for 20 years, (T_A = 85^\circ\text{C})(^{c})</td>
<td>10,000</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes
1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
2. When using flash memory programmer and Renesas Electronics self programming library
3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

\( (T_A = -40 \text{ to } +105^\circ\text{C}, 2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, V_{SS} = 0 \text{ V}) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer rate</td>
<td></td>
<td>During serial programming</td>
<td>115.2 k</td>
<td>1 M</td>
<td></td>
<td>bps</td>
</tr>
</tbody>
</table>
2.10 Timing of Entry to Flash Memory Programming Modes

\( (T_A = -40 \text{ to } +105^\circ C, 2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, V_{SS} = 0 \text{ V}) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>How long from when an external reset ends until the initial communication settings are specified</td>
<td>( t_{SUINIT} )</td>
<td>POR and LVD reset must end before the external reset ends.</td>
<td>100</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>How long from when the TOOL0 pin is placed at the low level until an external reset ends</td>
<td>( t_{SU} )</td>
<td>POR and LVD reset must end before the external reset ends.</td>
<td>10</td>
<td></td>
<td></td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>How long the TOOL0 pin must be kept at the low level after a reset ends (except soft processing time)</td>
<td>( t_{HD} )</td>
<td>POR and LVD reset must end before the external reset ends.</td>
<td>1</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

\[
\begin{align*}
<1> & \quad \text{The low level is input to the TOOL0 pin.} \\
<2> & \quad \text{The external reset ends (POR and LVD reset must end before the pin reset ends.).} \\
<3> & \quad \text{The TOOL0 pin is set to the high level.} \\
<4> & \quad \text{Complete the baud rate setting by UART reception.}
\end{align*}
\]

**Remark** \( t_{SUINIT} \): The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

\( t_{SU} \): How long from when the TOOL0 pin is placed at the low level until an external reset ends

\( t_{HD} \): How long to keep the TOOL0 pin at the low level from when the external and internal resets end (except soft processing time)
3. ELECTRICAL SPECIFICATIONS
(M: Industrial applications, $T_A = -40$ to $+125^\circ$C)

In this chapter, shows the electrical specifications of the target products.

**Target products (M: Industrial applications):** $T_A = -40$ to $+125^\circ$C

**R5F107xxMxx**

**Cautions**

1. The RL78/I1A has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. See 2.1 Port Function to 2.2.1 Functions for each product in the RL78/I1A User’s Manual.

3. When any of these products are used at $105^\circ$C or lower, see 2. ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+105^\circ$C).
3.1 Absolute Maximum Ratings

**Absolute Maximum Ratings (TA = 25°C) (1/2)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbols</th>
<th>Conditions</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>VDD</td>
<td></td>
<td>−0.5 to +6.5</td>
<td>V</td>
</tr>
<tr>
<td>REGC pin input voltage</td>
<td>VREGC</td>
<td>REGC</td>
<td>−0.3 to +2.8 and −0.3 to VDD +0.3</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage</td>
<td>VIL</td>
<td>P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P20 to P206, EXCLK, EXCLKS, RESET</td>
<td>−0.3 to VDD +0.3 Note 2</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>VOH</td>
<td>P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120, P147, P200 to P206</td>
<td>−0.3 to VDD +0.3 Note 2</td>
<td>V</td>
</tr>
<tr>
<td>Analog input voltage</td>
<td>VIN</td>
<td>ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19</td>
<td>−0.3 to VDD +0.3 and −0.3 to AVREF(+), +0.3 Note 2, 3</td>
<td>V</td>
</tr>
</tbody>
</table>

**Notes**

1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
2. Must be 6.5 V or lower.
3. Do not exceed AVREF(+) + 0.3 V in case of A/D conversion target pin.

**Caution**

Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks**

1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
3. VSS: Reference voltage
### Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) (2/2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbols</th>
<th>Conditions</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output current, high</td>
<td>$I_{OH1}$</td>
<td>Per pin P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206</td>
<td>–40</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of all pins P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206</td>
<td>–70</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>$I_{OH2}$</td>
<td>Per pin P20 to P22, P24 to P27</td>
<td>–0.5</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of all pins</td>
<td>–2</td>
<td>mA</td>
</tr>
<tr>
<td>Output current, low</td>
<td>$I_{OL1}$</td>
<td>Per pin P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206</td>
<td>40</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of all pins 170 mA</td>
<td>70</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>$I_{OL2}$</td>
<td>Per pin P20 to P22, P24 to P27</td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of all pins</td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td>Operating ambient temperature</td>
<td>$T_A$</td>
<td>In normal operation mode</td>
<td>–40 to +125</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In flash memory programming mode</td>
<td>–40 to +105</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{ST}$</td>
<td></td>
<td>–65 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Caution**  Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark**  Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
3.2 Oscillator Characteristics

3.2.1 X1, XT1 oscillator characteristics

\((T_A = -40 \text{ to } +125^\circ \text{C}, 2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, V_{SS} = 0 \text{ V})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Resonator</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1 clock frequency ((f_X))(\text{Note})</td>
<td>Ceramic resonator/crystal resonator</td>
<td></td>
<td>1.0</td>
<td></td>
<td>20.0</td>
<td>MHz</td>
</tr>
<tr>
<td>XT1 clock frequency ((f_{XT}))(\text{Note})</td>
<td>Crystal resonator</td>
<td></td>
<td>32</td>
<td>32.768</td>
<td>35</td>
<td>kHz</td>
</tr>
</tbody>
</table>

**Note** Indicates only permissible oscillator frequency ranges. See **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution** Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

**Remark** When using the X1 oscillator and XT1 oscillator, see 5.4 System Clock Oscillator in the RL78/I1A User’s Manual.
### 3.2.2 On-chip oscillator characteristics

\( (TA = -40 \text{ to } +125^\circ C, 2.7 \text{ V} \leq VDD \leq 5.5 \text{ V}, VSS = 0 \text{ V}) \)

<table>
<thead>
<tr>
<th>Oscillators</th>
<th>Parameters</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-speed on-chip oscillator clock frequency(\text{Note 1})</td>
<td>(f_{\text{IH}})</td>
<td>TA = -20 to 85(^\circ)C</td>
<td>-1</td>
<td>+1</td>
<td>%</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TA = -40 to 105(^\circ)C</td>
<td>-1.5</td>
<td>+1.5</td>
<td>%</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TA = -40 to 125(^\circ)C</td>
<td>-2</td>
<td>+2</td>
<td>%</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>When 16 MHz selected</td>
<td></td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>High-speed on-chip oscillator clock frequency accuracy(\text{Note 2})</td>
<td>(f_{\text{IH}})</td>
<td>TA = -20 to 85(^\circ)C</td>
<td>-1</td>
<td>+1</td>
<td>%</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TA = -40 to 105(^\circ)C</td>
<td>-1.5</td>
<td>+1.5</td>
<td>%</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TA = -40 to 125(^\circ)C</td>
<td>-2</td>
<td>+2</td>
<td>%</td>
<td>kHz</td>
</tr>
<tr>
<td>Low-speed on-chip oscillator clock frequency</td>
<td>(f_{\text{IL}})</td>
<td>15</td>
<td>kHz</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>Low-speed on-chip oscillator clock frequency accuracy</td>
<td>(f_{\text{IL}})</td>
<td>-15</td>
<td>%</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
</tbody>
</table>

**Notes 1.** Frequency can be selected in a high-speed on-chip oscillator. Selected by bits 0 to 3 of option byte (000C2H/010C2H).

2. This indicates the oscillator characteristics only. See AC Characteristics for instruction execution time.

**Remark** When using the device at an ambient temperature that exceeds \(TA = 105^\circ\)C, the selectable oscillation frequency is 16 MHz max.

### 3.2.3 PLL characteristics

\( (TA = -40 \text{ to } +125^\circ C, 2.7 \text{ V} \leq VDD \leq 5.5 \text{ V}, VSS = 0 \text{ V}) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL input clock frequency(\text{Note})</td>
<td>(f_{\text{PLL}})</td>
<td>High-speed system clock is selected (f_{\text{MAX}} = 4 \text{ MHz})</td>
<td>3.92</td>
<td>4.00</td>
<td>4.08</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-speed on-chip oscillator clock is selected (f_{\text{IH}} = 4 \text{ MHz})</td>
<td>3.92</td>
<td>4.00</td>
<td>4.08</td>
<td>MHz</td>
</tr>
<tr>
<td>PLL output clock frequency(\text{Note})</td>
<td>(f_{\text{PLL}})</td>
<td>(f_{\text{PLL}} \times 16)</td>
<td></td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
</tbody>
</table>

**Note** This only indicates the oscillator characteristics. See AC Characteristics for instruction execution time.

**Remark** When using the device at an ambient temperature that exceeds \(TA = 105^\circ\)C, only 16 MHz \((f_{\text{PLL}} \times 1/4)\) can be selected as the CPU operating frequency.
3.3 DC Characteristics

3.3.1 Pin characteristics

\( (T_A = -40 \text{ to } +125^\circ \text{C}, 2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, V_{SS} = 0 \text{ V}) \)

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output current, high(^{\text{Note 1}})</td>
<td>(I_{OH1})</td>
<td>Per pin for P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206</td>
<td>4.0 V \leq V_{DD} \leq 5.5 V</td>
<td>(-3.0)(^{\text{Note 2}}) mA</td>
<td>-1.0 mA</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of P02, P03, P40, P120 (When duty (\leq 70%)(^{\text{Note 3}}))</td>
<td>4.0 V \leq V_{DD} \leq 5.5 V</td>
<td>-9.0 mA</td>
<td>-3.0 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 (When duty (\leq 70%)(^{\text{Note 3}}))</td>
<td>4.0 V \leq V_{DD} \leq 5.5 V</td>
<td>-21.0 mA</td>
<td>-6.0 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of all pins (When duty (\leq 70%)(^{\text{Note 3}}))</td>
<td>4.0 V \leq V_{DD} \leq 5.5 V</td>
<td>-21.0 mA</td>
<td>-9.0 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(I_{OH2})</td>
<td>Per pin for P20 to P22, P24 to P27</td>
<td>2.7 V \leq V_{DD} \leq 5.5 V</td>
<td>(-0.1)(^{\text{Note 2}}) mA</td>
<td>-0.4 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of all pins (When duty (\leq 70%)(^{\text{Note 3}}))</td>
<td>2.7 V \leq V_{DD} \leq 5.5 V</td>
<td>(-0.1)(^{\text{Note 2}}) mA</td>
<td>-0.4 mA</td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

1. Value of current at which the device operation is guaranteed even if the current flows from the \(V_{DD}\) pin to an output pin.
2. However, do not exceed the total current value.
3. Specification under conditions where the duty factor \(\leq 70\%\).
   The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
   - Total output current of pins = \((I_{OH} \times 0.7)/(n \times 0.01)\)
     <Example> Where \(n = 80\%\) and \(I_{OH} = -10.0 \text{ mA}\)
     Total output current of pins = \((-10.0 \times 0.7)/(80 \times 0.01)\) \(\approx -8.7 \text{ mA}\)
   However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

**Caution** P02, P10 to P12 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
(TA = −40 to +125°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output current, low Note 1</td>
<td>IOL1</td>
<td>Per pin for P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206</td>
<td>4.0 V ≤ VDD ≤ 5.5 V</td>
<td>8.5 Note 2 mA</td>
<td>15 Note 2 mA</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of P02, P03, P40, P120 (When duty ≤ 70% Note 3)</td>
<td>2.7 V ≤ VDD &lt; 4.0 V</td>
<td>20.0 mA</td>
<td>5.0 mA</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 (When duty ≤ 70% Note 3)</td>
<td>4.0 V ≤ VDD ≤ 5.5 V</td>
<td>20.0 mA</td>
<td>10.0 mA</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of all pins (When duty ≤ 70% Note 3)</td>
<td>2.7 V ≤ VDD &lt; 4.0 V</td>
<td>40.0 mA</td>
<td>15.0 mA</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>IOL2</td>
<td>Per pin for P20 to P22, P24 to P27</td>
<td>2.7 V ≤ VDD ≤ 5.5 V</td>
<td>0.4 Note 2 mA</td>
<td>1.6 mA</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total of all pins (When duty ≤ 70% Note 3)</td>
<td>2.7 V ≤ VDD ≤ 5.5 V</td>
<td>1.6 mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the VSS pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

   The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

   - Total output current of pins = (IOL × 0.7)/(n × 0.01)

   *Example* Where n = 80% and IOL = −10.0 mA

   Total output current of pins = (−10.0 × 0.7)/(80 × 0.01) ≈ −8.7 mA

   However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Remark**

Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
(TA = −40 to +125°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage, high</td>
<td>V&lt;sub&gt;H&lt;/sub&gt;</td>
<td>P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, RESET</td>
<td>0.8V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;HI&lt;/sub&gt;</td>
<td>P03, P10, P11</td>
<td>TTL input buffer 4.0 V ≤ VDD ≤ 5.5 V</td>
<td>2.1</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TTL input buffer 3.3 V ≤ VDD &lt; 4.0 V</td>
<td>2.0</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, RESET</td>
<td>Normal input buffer</td>
<td>0</td>
<td>0.2V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;L&lt;/sub&gt;</td>
<td>P03, P10, P11</td>
<td>TTL input buffer 4.0 V ≤ VDD ≤ 5.5 V</td>
<td>0</td>
<td>0.8</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TTL input buffer 3.3 V ≤ VDD &lt; 4.0 V</td>
<td>0</td>
<td>0.5</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TTL input buffer 2.7 V ≤ VDD &lt; 3.3 V</td>
<td>0</td>
<td>0.32</td>
<td>V</td>
</tr>
</tbody>
</table>

Caution  The maximum value of V<sub>H</sub> of pins P02, P10 to P12 is V<sub>DD</sub>, even in the N-ch open-drain mode.

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
### 3. ELECTRICAL SPECIFICATIONS (M: Industrial applications, $T_A = -40$ to $+125^\circ C$)

($T_A = -40$ to $+125^\circ C$, $2.7 \, \text{V} \leq V_{DD} \leq 5.5 \, \text{V}$, $V_{SS} = 0 \, \text{V}$)

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage, high</td>
<td>$V_{OH1}$</td>
<td>P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206</td>
<td>$4.0 , \text{V} \leq V_{DD} \leq 5.5 , \text{V}$, $I_{OH1} = -3.0 , \text{mA}$</td>
<td>$V_{DD} = 0.7$</td>
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<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$2.7 , \text{V} \leq V_{DD} \leq 5.5 , \text{V}$, $I_{OH1} = -1.0 , \text{mA}$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{OH2}$</td>
<td>P20 to P22, P24 to P27</td>
<td>$2.7 , \text{V} \leq V_{DD} \leq 5.5 , \text{V}$, $I_{OH2} = -100 , \mu\text{A}$</td>
<td>$V_{DD} = 0.5$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output voltage, low</td>
<td>$V_{OL1}$</td>
<td>P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206</td>
<td>$4.0 , \text{V} \leq V_{DD} \leq 5.5 , \text{V}$, $I_{OL1} = 8.5 , \text{mA}$</td>
<td>0.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$4.0 , \text{V} \leq V_{DD} \leq 5.5 , \text{V}$, $I_{OL1} = 4.0 , \text{mA}$</td>
<td></td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$2.7 , \text{V} \leq V_{DD} \leq 5.5 , \text{V}$, $I_{OL1} = 1.5 , \text{mA}$</td>
<td></td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{OL2}$</td>
<td>P20 to P22, P24 to P27</td>
<td>$2.7 , \text{V} \leq V_{DD} \leq 5.5 , \text{V}$, $I_{OL2} = 400 , \mu\text{A}$</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

**Caution** P02, P10 to P12 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
3. ELECTRICAL SPECIFICATIONS (M: Industrial applications, $T_A = -40 \text{ to } +125\degree C$)

$(-40 \text{ to } +125\degree C, \ 2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, \ V_{SS} = 0 \text{ V})$

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input leakage</td>
<td>$I_{IH1}$</td>
<td>$P02, P03, P05, P06, P10 \text{ to } P12,$</td>
<td>$V_I = V_{DD}$</td>
<td>1</td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td>current, high</td>
<td></td>
<td>$P20 \text{ to } P22,$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$P24 \text{ to } P27,$</td>
<td></td>
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<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$P30,$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$P31,$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$P40,$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$P75 \text{ to } P77,$</td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td>$P120,$</td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td>$P137,$</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td>$P147,$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$P200 \text{ to } P206,$</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\text{RESET}$</td>
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</tr>
<tr>
<td>Input leakage</td>
<td>$I_{IH2}$</td>
<td>$P121 \text{ to } P124$</td>
<td>$V_I = V_{DD}$</td>
<td>1</td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td>current, low</td>
<td></td>
<td>$(X1, X2, XT1, XT2, EXCLK, EXCLKS)$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>In input port or $V_I = V_{SS}$</td>
<td>$I_{IL1}$</td>
<td>$V_I = V_{SS}$</td>
<td>$-1$</td>
<td>$\mu$A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>external clock input</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>In resonator connection</td>
<td>10</td>
<td></td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td></td>
<td>$I_{IL2}$</td>
<td>$P121 \text{ to } P124$</td>
<td>$V_I = V_{SS}$</td>
<td>$-1$</td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$(X1, X2, XT1, XT2, EXCLK, EXCLKS)$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>In input port or external clock</td>
<td>$-10$</td>
<td></td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>input</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>In resonator connection</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>On-chip pull-up</td>
<td>$R_U$</td>
<td>$P02, P03, P05, P06,$</td>
<td>$V_I = V_{SS}, \text{ in input port}$</td>
<td>10</td>
<td>20</td>
<td>100</td>
</tr>
<tr>
<td>resistance</td>
<td></td>
<td>$P10 \text{ to } P12,$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$P30,$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$P31,$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$P40,$</td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td>$P75 \text{ to } P77,$</td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td>$P120,$</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>$P137,$</td>
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<tr>
<td></td>
<td></td>
<td>$P147,$</td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td>$P200 \text{ to } P206$</td>
<td></td>
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</tr>
</tbody>
</table>

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
3.3.2 Supply current characteristics

\( (T_A = -40\text{ to } +125^\circ\text{C}, 2.7 \, \text{V} \leq V_{DD} \leq 5.5 \, \text{V}, V_{SS} = 0 \, \text{V}) \) (1/2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply current ( \text{Note 1} )</td>
<td>( \text{IDD1} )</td>
<td>Operating mode</td>
<td>f( \text{IH} = 16 , \text{MHz} )( \text{Note 3} )</td>
<td>( V_{DD} = 5.0 , \text{V} )</td>
<td>2.9</td>
<td>4.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{DD} = 3.0 , \text{V} )</td>
<td>2.9</td>
<td>4.8</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>f( \text{IH} = 4 , \text{MHz} )( \text{Note 3} )</td>
<td>( V_{DD} = 5.0 , \text{V} )</td>
<td>3.3</td>
<td>6.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{DD} = 3.0 , \text{V} )</td>
<td>3.3</td>
<td>6.5</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>f( \text{IH} = 4 , \text{MHz} )( \text{Note 3} )</td>
<td>( V_{DD} = 5.0 , \text{V} )</td>
<td>4.2</td>
<td>6.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{DD} = 3.0 , \text{V} )</td>
<td>4.4</td>
<td>6.2</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>f( \text{IH} = 4 , \text{MHz} )( \text{Note 3} )</td>
<td>( V_{DD} = 5.0 , \text{V} )</td>
<td>4.3</td>
<td>7.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{DD} = 3.0 , \text{V} )</td>
<td>4.5</td>
<td>7.4</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>f( \text{IH} = 4 , \text{MHz} )( \text{Note 3} )</td>
<td>( V_{DD} = 5.0 , \text{V} )</td>
<td>4.4</td>
<td>8.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{DD} = 3.0 , \text{V} )</td>
<td>4.6</td>
<td>8.3</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>f( \text{IH} = 4 , \text{MHz} )( \text{Note 3} )</td>
<td>( V_{DD} = 5.0 , \text{V} )</td>
<td>5.2</td>
<td>11.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{DD} = 3.0 , \text{V} )</td>
<td>5.4</td>
<td>11.6</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>f( \text{IH} = 4 , \text{MHz} )( \text{Note 3} )</td>
<td>( V_{DD} = 5.0 , \text{V} )</td>
<td>6.9</td>
<td>20.8</td>
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<td>( V_{DD} = 3.0 , \text{V} )</td>
<td>7.1</td>
<td>21.0</td>
<td>( \mu \text{A} )</td>
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<td>f( \text{IH} = 4 , \text{MHz} )( \text{Note 3} )</td>
<td>( V_{DD} = 5.0 , \text{V} )</td>
<td>11.1</td>
<td>51.2</td>
</tr>
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<td></td>
<td></td>
<td></td>
<td>( V_{DD} = 3.0 , \text{V} )</td>
<td>11.3</td>
<td>51.4</td>
<td>( \mu \text{A} )</td>
</tr>
</tbody>
</table>

(Notes and Remarks are listed on the next page.)
Notes 1. Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The following points apply in the HS (high-speed main) modes.
   • The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
   • The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.
   In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

2. When high-speed on-chip oscillator and subsystem clock are stopped.
3. When high-speed system clock and subsystem clock are stopped.
4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).
5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
   HS (high-speed main) mode: 2.7 V ≤ VDD ≤ 5.5 V @ 1 MHz to 20 MHz

Remarks 1. \( f_{MX} \): High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. \( f_{OH} \): High-speed on-chip oscillator clock frequency
3. \( f_{SUB} \): Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation, temperature condition of the TYP. value is \( T_A = 25^\circ C \)
### 3. ELECTRICAL SPECIFICATIONS (M: Industrial applications, \( T_A = -40 \) to \(+125^\circ C\))

\((T_A = -40 \text{ to } +125^\circ C, \ 2.7 \ V \leq \ V_{DD} \leq 5.5 \ V, \ V_{SS} = 0 \ V\) (2/2))

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply current</td>
<td>( I_{CC} )</td>
<td>HALT mode</td>
<td>( f_{IH} = 16 \text{ MHz} )</td>
<td>( V_{DD} = 5.0 \ V )</td>
<td>0.50</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{DD} = 3.0 \ V )</td>
<td>0.50</td>
<td>2.0</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HS (high-speed main) mode</td>
<td>( V_{CC} = 5.0 \ V )</td>
<td>0.40</td>
<td>2.2</td>
<td>mA</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>Resonator connection</td>
<td>0.50</td>
<td>2.3</td>
<td>mA</td>
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<td></td>
<td></td>
<td>HS (high-speed main) mode</td>
<td>( V_{CC} = 3.0 \ V )</td>
<td>0.40</td>
<td>2.2</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Resonator connection</td>
<td>0.50</td>
<td>2.3</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HS (high-speed main) mode</td>
<td>( V_{CC} = 5.0 \ V )</td>
<td>0.24</td>
<td>1.22</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Resonator connection</td>
<td>0.30</td>
<td>1.28</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HS (high-speed main) mode</td>
<td>( V_{CC} = 3.0 \ V )</td>
<td>0.24</td>
<td>1.22</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Resonator connection</td>
<td>0.30</td>
<td>1.28</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Subsystem clock operation</td>
<td>( f_{SUB} = 32.768 \text{ kHz} )</td>
<td>( T_A = -40^\circ C )</td>
<td>0.28</td>
<td>0.70</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Resonator connection</td>
<td>0.47</td>
<td>0.89</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_A = +25^\circ C )</td>
<td>0.33</td>
<td>0.70</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Resonator connection</td>
<td>0.52</td>
<td>0.89</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_A = +50^\circ C )</td>
<td>0.41</td>
<td>1.90</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Resonator connection</td>
<td>0.60</td>
<td>2.09</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_A = +70^\circ C )</td>
<td>0.54</td>
<td>2.80</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>Resonator connection</td>
<td>0.73</td>
<td>2.99</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_A = +85^\circ C )</td>
<td>1.27</td>
<td>6.10</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Resonator connection</td>
<td>1.46</td>
<td>6.29</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_A = +105^\circ C )</td>
<td>3.04</td>
<td>15.5</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Resonator connection</td>
<td>3.23</td>
<td>15.7</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_A = +125^\circ C )</td>
<td>7.20</td>
<td>45.2</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Resonator connection</td>
<td>7.53</td>
<td>45.5</td>
<td>( \mu A )</td>
</tr>
</tbody>
</table>

\(<R>\)

### STOP mode

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Conditions</th>
<th>( T_A )</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{CC} )</td>
<td></td>
<td>( T_A = -40^\circ C )</td>
<td>0.18</td>
<td>0.50</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_A = +25^\circ C )</td>
<td>0.23</td>
<td>0.50</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_A = +50^\circ C )</td>
<td>0.27</td>
<td>1.70</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_A = +70^\circ C )</td>
<td>0.44</td>
<td>2.60</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_A = +85^\circ C )</td>
<td>1.17</td>
<td>5.90</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_A = +105^\circ C )</td>
<td>2.94</td>
<td>15.3</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_A = +125^\circ C )</td>
<td>7.14</td>
<td>45.1</td>
<td>( \mu A )</td>
<td></td>
</tr>
</tbody>
</table>

\(<R>\)

(Notes and Remarks are listed on the next page.)
Notes 1. Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The following points apply in the HS (high-speed main) modes.
   • The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
   • The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.
   In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.
   In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

2. During HALT instruction execution by flash memory.
3. When high-speed on-chip oscillator and subsystem clock are stopped.
4. When high-speed system clock and subsystem clock are stopped.
5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).
6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
   HS (high-speed main) mode: 2.7 V ≤ VDD ≤ 5.5 V@1 MHz to 20 MHz
7. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. \( f_{MX} \): High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. \( f_{SH} \): High-speed on-chip oscillator clock frequency
3. \( f_{SUB} \): Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is \( T_A = 25^\circ C \)
### Electrical Specifications (M: Industrial applications, TA = −40 to +125°C)

(TA = −40 to +125°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low-speed on-chip oscillator operating current</td>
<td>IFIL Note 1</td>
<td></td>
<td></td>
<td></td>
<td>0.20</td>
<td>μA</td>
</tr>
<tr>
<td>RTC operating current</td>
<td>IRTC Notes 1, 2, 3</td>
<td></td>
<td></td>
<td></td>
<td>0.02</td>
<td>μA</td>
</tr>
<tr>
<td>12-bit interval timer operating current</td>
<td>IT Notes 1, 2, 4</td>
<td>fL = 15 kHz</td>
<td></td>
<td></td>
<td>0.02</td>
<td>μA</td>
</tr>
<tr>
<td>Watchdog timer operating current</td>
<td>IWDT Notes 1, 2, 5</td>
<td></td>
<td></td>
<td></td>
<td>0.22</td>
<td>μA</td>
</tr>
<tr>
<td>A/D converter operating current</td>
<td>IADC Notes 1, 6</td>
<td>When conversion at maximum speed</td>
<td>1.3</td>
<td>1.7</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>A/D converter reference voltage current</td>
<td>IADREF Note 1</td>
<td></td>
<td></td>
<td></td>
<td>75.0</td>
<td>μA</td>
</tr>
<tr>
<td>Temperature sensor operating current</td>
<td>ITMPS Note 1</td>
<td></td>
<td></td>
<td></td>
<td>75.0</td>
<td>μA</td>
</tr>
<tr>
<td>LVD operating current</td>
<td>IVD Notes 1, 7</td>
<td></td>
<td></td>
<td></td>
<td>0.08</td>
<td>μA</td>
</tr>
<tr>
<td>Self-programming operating current</td>
<td>IFSP Notes 1, 8</td>
<td></td>
<td></td>
<td></td>
<td>2.5 12.2</td>
<td>mA</td>
</tr>
<tr>
<td>Programmable gain amplifier operating current</td>
<td>IPGA Note 9</td>
<td>AVREFP = VDD = 5.0 V</td>
<td>0.21</td>
<td>0.37</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Comparator operating current</td>
<td>ICMP Note 10</td>
<td>When one comparator channel is operating</td>
<td>41.4 74</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Programmable gain amplifier/comparator reference current source</td>
<td>IIREF Note 11</td>
<td>AVREFP = VDD = 5.0 V</td>
<td>3.2 6.1</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BGO operating current</td>
<td>IBGO Note 12</td>
<td></td>
<td></td>
<td></td>
<td>2.50 12.2</td>
<td>mA</td>
</tr>
<tr>
<td>SNOOZE operating current</td>
<td>ISNOZ Note 1</td>
<td>A/D converter operation</td>
<td>0.50 1.10</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(Notes and Remarks are listed on the next page.)
Notes 1. Current flowing to the VDD.
2. When the high-speed on-chip oscillator and high-speed system clock are stopped.
3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{RTC}$, when the real-time clock is operating in operating mode or in HALT mode. When the low-speed on-chip oscillator is selected, $I_{SS}$ should be added. $I_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.
4. Current flowing only to the 12-bit interval timer (excluding the operating current of the XT1 oscillator and $f_{IL}$ operating current). The current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{IL}$ should be added.
5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$, and $I_{WDT}$, when the watchdog timer is operating.
6. Current flowing only to the A/D converter. The supply current value of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$, when the A/D converter is operating in operating mode or in HALT mode.
7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit is in operation.
9. Current flowing only to the programmable gain amplifier. The supply current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$, and $I_{PGA}$, when the programmable gain amplifier is operating in operating mode or in HALT mode.
10. Current flowing only to the comparator. The supply current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$, and $I_{ICMP}$, when the comparator is operating.
11. This is the current required to flow to VDD pin of the current circuit that is used as the programmable gain amplifier and the comparator.
12. Current flowing only during data flash rewrite.
13. See 21.3.3 SNOOZE mode in the RL78/I1A User's Manual for shift time to the SNOOZE mode.

Remarks 1. $f_{IL}$: Low-speed on-chip oscillator clock frequency
2. $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
3. $f_{CLK}$: CPU/peripheral hardware clock frequency
4. Temperature condition of the TYP. value is $T_A = 25^\circ C$
5. Example of calculating current value when using programmable gain amplifier and comparator.

Examples 1) TYP. operating current value when three comparator channels, one internal reference voltage generator, and PGA are operating (when $AV_{REFP} = VDD = 5.0 \, V$)

\[
I_{CMP} \times 3 + I_{REF} + I_{PGA} + I_{REF} \\
= 41.4 \, [\mu A] \times 3 + 14.8 \, [\mu A] \times 1 + 210 \, [\mu A] + 3.2 \, [\mu A] \\
= 352.2 \, [\mu A]
\]

Examples 2) TYP. operating current value when using two comparator channels, without using internal reference voltage generator (when $AV_{REFP} = VDD = 5.0 \, V$)

\[
I_{CMP} \times 2 + I_{REF} \\
= 41.4 \, [\mu A] \times 2 + 3.2 \, [\mu A] \\
= 86.0 \, [\mu A]
\]
### 3.4 AC Characteristics

\((T_A = -40 \text{ to } +125^\circ C, 2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, V_{SS} = 0 \text{ V})\)

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction cycle (minimum instruction execution time)</td>
<td>(T_{CY})</td>
<td>Main system clock ((f_{MAIN})) operation</td>
<td>HS (high-speed main) mode</td>
<td>0.05</td>
<td>1</td>
<td>(\mu s)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Subsystem clock ((f_{SUB})) operation</td>
<td></td>
<td>28.5</td>
<td>30.5</td>
<td>31.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In the self programming mode</td>
<td>HS (high-speed main) mode (T_A = -40 \text{ to } +105^\circ C)</td>
<td>0.05</td>
<td>1</td>
<td>(\mu s)</td>
</tr>
<tr>
<td>External system clock frequency</td>
<td>(f_{EX})</td>
<td></td>
<td></td>
<td>1.0</td>
<td>20.0</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>(f_{EXS})</td>
<td></td>
<td></td>
<td>32</td>
<td>35</td>
<td>kHz</td>
</tr>
<tr>
<td>External system clock input high-level width, low-level width</td>
<td>(t_{EXH}, t_{EXL})</td>
<td></td>
<td></td>
<td>24</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(t_{EXHS}, t_{EXLS})</td>
<td></td>
<td></td>
<td>13.7</td>
<td>(\mu s)</td>
<td></td>
</tr>
<tr>
<td>TI03, TI05, TI06, TI07 input high-level width, low-level width</td>
<td>(t_{TIH}, t_{TIL})</td>
<td>(2/f_{MCK}+10)</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TO03, TO05, TO06, TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21, TKCO00 to TKCO05 output frequency (When duty = 50%)</td>
<td>(f_{TO})</td>
<td>HS (high-speed main) mode</td>
<td></td>
<td>4.0 V (\leq V_{DD} \leq 5.5) V</td>
<td>5</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.7 V (\leq V_{DD} &lt; 4.0) V</td>
<td>4</td>
<td>MHz</td>
</tr>
<tr>
<td>Interrupt input high-level width, low-level width</td>
<td>(t_{INTH}, t_{INTL})</td>
<td>INTP0, INTP3, INTP4, INTP9 to INTP11, INTP20 to INTP23</td>
<td></td>
<td>2.7 V (\leq V_{DD} \leq 5.5) V</td>
<td>1</td>
<td>(\mu s)</td>
</tr>
<tr>
<td>RESET low-level width</td>
<td>(t_{RSL})</td>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td>(\mu s)</td>
</tr>
</tbody>
</table>

**Remark**  \(f_{MCK}\): Timer array unit operation clock frequency  
(\(f_{MCK}\) is set by the CKS0n bit of timer mode register 0n (TMR0n). \(n\): Channel number (\(n = 0 \text{ to } 7\))
Minimum Instruction Execution Time during Main System Clock Operation

The graph shows the relationship between cycle time $T_{CY}$ and supply voltage $V_{DD}$ in HS (high-speed main) mode. The graph includes three lines:

- The solid line indicates when the high-speed on-chip oscillator clock is selected.
- The dashed line indicates during self programming.
- The dotted line indicates when the high-speed system clock is selected.

**AC Timing Test Points**

- $V_{IH}/V_{OH}$
- $V_{IL}/V_{OL}$

**External System Clock Timing**

- EXCLK/EXCLKS
- $t_{EXL}$
- $t_{EXHS}$
- $1/f_{EX}$
- $1/f_{EXS}$
3. ELECTRICAL SPECIFICATIONS (M: Industrial applications, $T_A = -40$ to $+125^\circ C$)

**TI/TO Timing**

- TI03, TI05, TI06, TI07

- TO03, TO05, TO06, TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21, TKCO00 to TKCO05

**Interrupt Request Input Timing**

- INTP0, INTP3, INTP4, INTP9 to INTP11, INTP20 to INTP23

**RESET Input Timing**

- RESET
3.5 Peripheral Functions Characteristics

AC Timing Test Points

3.5.1 Serial array unit 0, 4 (UART0, UART1, CSI00, DALI/UART4)

(1) During communication at same potential (UART mode)

\( T_A = -40 \text{ to } +125^\circ C, \ 2.7 \leq V_{DD} \leq 5.5 \text{ V}, \ V_{SS} = 0 \text{ V} \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main) Mode</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer rate</td>
<td>Note 1</td>
<td>Theoretical value of the maximum transfer rate ( f_{MCK} = f_{CLK} )</td>
<td>MIN.</td>
<td>MAX.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>fMCK/6 bps</td>
<td>3.3 Mbps</td>
</tr>
</tbody>
</table>

Notes

1. Transfer rate in the SNOOZE mode is 4800 bps only.
2. The operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
   - HS (high-speed main) mode: 20 MHz (2.7 \leq V_{DD} \leq 5.5 \text{ V})

UART mode connection diagram (during communication at same potential)

UART mode bit width (during communication at same potential) (reference)

Caution
Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register \( g \) (PIMg) and port output mode register \( g \) (POMg).

Remarks

1. \( q \): UART number (\( q = 0, 1 \)), \( g \): PIM and POM number (\( g = 0, 1 \))
2. \( f_{MCK} \): Serial array unit operation clock frequency
   
   \( f_{MCK} \) is set by the CKSmn bit of serial mode register mn (SMRmn). \( m \): Unit number, \( n \): Channel number (mn = 00 to 03)
(2) During communication at same potential (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output)

\( (T_A = -40 \text{ to } +125^\circ C, 2.7 \text{ V } \leq V_{DD} \leq 5.5 \text{ V}, V_{SS} = 0 \text{ V}) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCKp cycle time</td>
<td>t_{CY1}</td>
<td>t_{CY1} \geq 4/f_{CLK}</td>
<td>4.0 \text{ V } \leq V_{DD} \leq 5.5 \text{ V}</td>
<td>250 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.7 \text{ V } \leq V_{DD} \leq 5.5 \text{ V}</td>
<td>500 ns</td>
</tr>
<tr>
<td>SCKp high-/low-level width</td>
<td>t_{KH1}, t_{KL1}</td>
<td>4.0 \text{ V } \leq V_{DD} \leq 5.5 \text{ V}</td>
<td>b_{CY1}/2 – 20 ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.7 \text{ V } \leq V_{DD} \leq 5.5 \text{ V}</td>
<td>b_{CY1}/2 – 40 ns</td>
</tr>
<tr>
<td>SIp setup time (to SCKp( \uparrow )) (^{\text{Note 1}})</td>
<td>t_{SIK1}</td>
<td>4.0 \text{ V } \leq V_{DD} \leq 5.5 \text{ V}</td>
<td>80 ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.7 \text{ V } \leq V_{DD} \leq 5.5 \text{ V}</td>
<td>80 ns</td>
</tr>
<tr>
<td>SIp hold time (from SCKp( \uparrow )) (^{\text{Note 2}})</td>
<td>t_{SIK1}</td>
<td>40 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Delay time from SCKp( \uparrow ) to SOp output (^{\text{Note 3}})</td>
<td>t_{SO1}</td>
<td>C = 30 pF (^{\text{Note 4}})</td>
<td>80 ns</td>
<td></td>
</tr>
</tbody>
</table>

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp\( \uparrow \)” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp\( \uparrow \)” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp\( \uparrow \)” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. \( p \): CSI number \( (p = 00) \), \( m \): Unit number \( (m = 0) \), \( n \): Channel number \( (n = 0) \), \( g \): PIM and POM number \( (g = 1) \)

2. \( f_{MCK} \): Serial array unit operation clock frequency

\( (\text{Operation clock to be set by the CKS mn bit of serial mode register mn} (\text{SMRmn}). \ m: \text{Unit number}, \ n: \text{Channel number (mn } = 00)) \)
### Electrical Specifications (M: Industrial applications, $T_A = -40$ to $+125^\circ$C)

(3) During communication at same potential (Simplified SPI (CSI) mode) (slave mode, SCKp... external clock input)  
($T_A = -40$ to $+125^\circ$C, $2.7 \, \text{V} \leq V_{DD} \leq 5.5 \, \text{V}, V_{SS} = 0 \, \text{V}$)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main) Mode</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCKp cycle time$^{Note 5}$</td>
<td>$t_{KCY2}$</td>
<td>$4.0 , \text{V} \leq V_{DD} \leq 5.5 , \text{V}$</td>
<td>$6/f_{MCK}$</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$2.7 , \text{V} \leq V_{DD} \leq 5.5 , \text{V}$</td>
<td>$8/f_{MCK}$</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{MCK} \leq 20 , \text{MHz}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{MCK} \leq 16 , \text{MHz}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCKp high-/low-level width</td>
<td>$t_{KH2}$, $t_{KL2}$</td>
<td>$2.7 , \text{V} \leq V_{DD} \leq 5.5 , \text{V}$</td>
<td>$6/f_{MCK}$</td>
<td>ns</td>
</tr>
<tr>
<td>Sckp setup time (to SCKp$^\uparrow_{Note 1}$)</td>
<td>$t_{SIK2}$</td>
<td></td>
<td>$1/f_{MCK}+40$</td>
<td>ns</td>
</tr>
<tr>
<td>Sckp hold time (from SCKp$^\uparrow_{Note 2}$)</td>
<td>$t_{SIK2}$</td>
<td></td>
<td>$1/f_{MCK}+60$</td>
<td>ns</td>
</tr>
<tr>
<td>Delay time from SCKp$^\downarrow$ to SOp output$^{Note 3}$</td>
<td>$t_{KSO2}$</td>
<td>C = 30 pF$^{Note 4}$</td>
<td>$2/f_{MCK}+80$</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Notes**

1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp$^\downarrow$” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp$^\uparrow$” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp$^\uparrow$” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
4. C is the load capacitance of the SOp output lines.
5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Caution**

Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remarks**

1. p: CSI number ($p = 00$), m: Unit number ($m = 0$), n: Channel number ($n = 0$),  
g: PIM and POM number ($g = 1$)
2. $f_{MCK}$: Serial array unit operation clock frequency  
   (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,  
n: Channel number ($mn = 00$))
Simplified SPI (CSI) mode connection diagram (during communication at same potential)

Simplified SPI (CSI) mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

Simplified SPI (CSI) mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

Remarks
1. p: CSI number (p = 00)
2. m: Unit number, n: Channel number (mn = 00)
### Communication at different potential (2.5 V, 3 V) (UART mode) (1/2)

\( (T_A = -40 \text{ to } +125^\circ C, 2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, V_{SS} = 0 \text{ V}) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main) Mode</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer rate</td>
<td>Reception</td>
<td>( 4.0 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, ) ( 2.7 \text{ V} \leq V_b \leq 4.0 \text{ V} )</td>
<td>( f_{MCK}/6 ) Note 1</td>
<td>bps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[ \text{Theoretical value of the maximum transfer rate} ] ( f_{MCK} = f_{CLK} ) Note 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 2.7 \text{ V} &lt; V_{DD} &lt; 4.0 \text{ V}, ) ( 2.3 \text{ V} &lt; V_b &lt; 2.7 \text{ V} )</td>
<td>( f_{MCK}/6 ) Note 1</td>
<td>bps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[ \text{Theoretical value of the maximum transfer rate} ] ( f_{MCK} = f_{CLK} ) Note 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

1. Transfer rate in the SNOOZE mode is 4800 bps only.
2. The operating frequencies of the CPU/peripheral hardware clock (f\(_{CLK}\)) are:
   - **HS (high-speed main) mode:** 20 MHz (2.7 V \( \leq V_{DD} \leq 5.5 \text{ V} \))

**Caution**

Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V\(_{DD}\) tolerance) mode for the TxDq pin by using port input mode register g (PIM\(_g\)) and port output mode register g (POM\(_g\)).

**Remarks**

1. \( V_b [\text{V}]: \) Communication line voltage
2. \( q: \) UART number (\( q = 0, 1 \)), \( g: \) PIM and POM number (\( g = 0, 1 \))
3. \( f_{MCK}: \) Serial array unit operation clock frequency

   (Operation clock to be set by the CKSmn bit of serial mode register \( mn \) (SMR\(_mn\)). \( m: \) Unit number,
   \( n: \) Channel number (\( mn = 00 \text{ to } 03 \))
### 3. ELECTRICAL SPECIFICATIONS

**M: Industrial applications, \( T_A = -40 \text{ to } +125^\circ \text{C} \)**

**RL78/I1A 3. ELECTRICAL SPECIFICATIONS**

#### (4) Communication at different potential (2.5 V, 3 V) (UART mode) (2/2)

\( (T_A = -40 \text{ to } +125^\circ \text{C}, 2.7 \text{ V} \leq \text{V}_{\text{DD}} \leq 5.5 \text{ V}, \text{V}_{\text{SS}} = 0 \text{ V}) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main) Mode</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer rate</td>
<td>Transmission</td>
<td>4.0 V \leq \text{V}<em>{\text{DD}} \leq 5.5 V, 2.7 \text{ V} \leq \text{V}</em>{\text{b}} \leq 4.0 V</td>
<td>Note 1</td>
<td>bps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Theoretical value of the maximum transfer rate ( C_b = 50 \text{ pF}, R_b = 1.4 \text{ k}\Omega, \text{V}_{\text{b}} = 2.7 \text{ V} )</td>
<td>Note 2</td>
<td>Mbps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 \text{ V} \leq \text{V}<em>{\text{DD}} &lt; 4.0 V, 2.3 \text{ V} \leq \text{V}</em>{\text{b}} \leq 2.7 \text{ V}</td>
<td>Note 3</td>
<td>bps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Theoretical value of the maximum transfer rate ( C_b = 50 \text{ pF}, R_b = 2.7 \text{ k}\Omega, \text{V}_{\text{b}} = 2.3 \text{ V} )</td>
<td>Note 4</td>
<td>Mbps</td>
</tr>
</tbody>
</table>

**Notes**

1. The smaller maximum transfer rate derived by using \( f_{MCK}/6 \) or the following expression is the valid maximum transfer rate.

   Expression for calculating the transfer rate when \( 4.0 \text{ V} \leq \text{V}_{\text{DD}} \leq 5.5 \text{ V} \) and \( 2.7 \text{ V} \leq \text{V}_{\text{b}} \leq 4.0 \text{ V} \)

   \[
   \text{Maximum transfer rate} = \frac{1}{(-C_b \times R_b \times \ln (1 - \frac{2.2}{V_b}))} \times 3 \text{ [bps]}
   \]

   Baud rate error (theoretical value) = \[
   \frac{1}{\text{Transfer rate} \times 2 - (-C_b \times R_b \times \ln (1 - \frac{2.2}{V_b}))} \times 100 \% \]

   \[
   \left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}
   \]

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the "Conditions" column are met. See Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using \( f_{MCK}/6 \) or the following expression is the valid maximum transfer rate.

   Expression for calculating the transfer rate when \( 2.7 \text{ V} \leq \text{V}_{\text{DD}} < 4.0 \text{ V} \) and \( 2.3 \text{ V} \leq \text{V}_{\text{b}} \leq 2.7 \text{ V} \)

   \[
   \text{Maximum transfer rate} = \frac{1}{(-C_b \times R_b \times \ln (1 - \frac{2.0}{V_b}))} \times 3 \text{ [bps]}
   \]

   Baud rate error (theoretical value) = \[
   \frac{1}{\text{Transfer rate} \times 2 - (-C_b \times R_b \times \ln (1 - \frac{2.0}{V_b}))} \times 100 \% \]

   \[
   \left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}
   \]

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the "Conditions" column are met. See Note 3 above to calculate the maximum transfer rate under conditions of the customer.

**Caution**

Select the TTL input buffer for the \( \text{RxDq} \) pin and the N-ch open drain output (\( \text{V}_{\text{DD}} \) tolerance) mode for the \( \text{TxDq} \) pin by using port input mode register \( \text{g} \) (\( \text{PIMg} \)) and port output mode register \( \text{g} \) (\( \text{POMg} \)).

**Remarks**

1. \( R_b[\Omega] \): Communication line (\( \text{TxDq} \)) pull-up resistance,
   \( C_b[F] \): Communication line (\( \text{TxDq} \)) load capacitance, \( \text{V}_b[V] \): Communication line voltage
2. \( q \): UART number \( (q = 0, 1) \), \( g \): PIM and POM number \( (g = 0, 1) \)
3. \( f_{MCK} \): Serial array unit operation clock frequency

   (Operation clock to be set by the \( \text{CKS}\text{mn} \) bit of serial mode register \( \text{mn} \) (\( \text{SMRmn} \)).

   \( m \): Unit number, \( n \): Channel number \( (mn = 00 \text{ to } 03) \)
3. ELECTRICAL SPECIFICATIONS (M: Industrial applications, $T_A = -40 \text{ to } +125^\circ\text{C}$)

UART mode connection diagram (during communication at different potential)

UART mode bit width (during communication at different potential) (reference)

Caution  Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V$_{DD}$ tolerance) mode for the TxDq pin by using port input mode register $g$ (PIM$g$) and port output mode register $g$ (POM$g$).

Remarks  1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $V_b[V]$: Communication line voltage
   2. $q$: UART number ($q = 0, 1$), $g$: PIM and POM number ($g = 0, 1$)
(5) Communication at different potential (2.5 V, 3 V) (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output)

(TA = −40 to +125°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main)</th>
<th>Mode</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCKp cycle time</td>
<td>bCY1</td>
<td>bCY1 ≥ 4/fCLK</td>
<td>MIN.</td>
<td>MAX.</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ</td>
<td>600</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V ≤ VDD &lt; 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ</td>
<td>1000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCKp high-level width</td>
<td>bH1</td>
<td>4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ</td>
<td>bCY1/2 – 80</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V ≤ VDD &lt; 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ</td>
<td>bCY1/2 – 170</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCKp low-level width</td>
<td>bL1</td>
<td>4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ</td>
<td>bCY1/2 – 28</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V ≤ VDD &lt; 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ</td>
<td>bCY1/2 – 40</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCKp setup time (to SCKp↑)</td>
<td>tSIK1</td>
<td>4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ</td>
<td>160</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V ≤ VDD &lt; 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ</td>
<td>250</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCKp hold time (from SCKp↑)</td>
<td>tKSI1</td>
<td>4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V ≤ VDD &lt; 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ</td>
<td>40</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Delay time from SCKp↓ to SOp output↑</td>
<td>tSO1</td>
<td>4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ</td>
<td>160</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V ≤ VDD &lt; 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ</td>
<td>250</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCKp setup time (to SCKp↓)</td>
<td>tSIK1</td>
<td>4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ</td>
<td>80</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V ≤ VDD &lt; 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ</td>
<td>80</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCKp hold time (from SCKp↓)</td>
<td>tKSI1</td>
<td>4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V ≤ VDD &lt; 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ</td>
<td>40</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

(Caution and Remarks are listed on the next page.)
Caution  Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Simplified SPI (CSI) mode connection diagram (during communication at different potential)

Remarks 1. R_b[\Omega]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage
2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)
Simplified SPI (CSI) mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

Simplified SPI (CSI) mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

Caution  Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance) mode for
the SOP pin and SCKp pin by using port input mode register g (PIMg) and port output mode
register g (POMg).

Remark  p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)
(6) DALI/UART4 mode  
(T<sub>A</sub> = −40 to +125°C, 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main) Mode</th>
<th>Unit</th>
</tr>
</thead>
</table>
| Transfer rate     |        | Maximum transfer rate theoretical value 
|                   |        | f<sub>CLK</sub> = 20 MHz, f<sub>MCK</sub> = f<sub>CLK</sub>                | f<sub>MCK</sub>/12       | bps  |

**Remark**  

f<sub>MCK</sub>: Operation clock frequency of DALI/UART.  
(Operation clock to be set by the serial clock select register 4 (SPS4).)

f<sub>MCK</sub>: Operation clock frequency of DALI/UART.
### 3.5.2 Serial interface I2C

#### (1) I2C standard mode

(T<sub>A</sub> = −40 to +125°C, 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main) Mode</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCLA0 clock frequency</td>
<td>f&lt;sub&gt;SCL&lt;/sub&gt;</td>
<td>Standard mode: f&lt;sub&gt;CLK&lt;/sub&gt; ≥ 1 MHz</td>
<td>MIN.</td>
<td>MAX.</td>
</tr>
<tr>
<td>Setup time of restart condition</td>
<td>t&lt;sub&gt;SU:STA&lt;/sub&gt;</td>
<td></td>
<td>0</td>
<td>100 kHz</td>
</tr>
<tr>
<td>Hold time&lt;sup&gt;1&lt;/sup&gt;</td>
<td>t&lt;sub&gt;HD:STA&lt;/sub&gt;</td>
<td></td>
<td>4.0</td>
<td>µs</td>
</tr>
<tr>
<td>Hold time when SCLA0 = &quot;L&quot;</td>
<td>t&lt;sub&gt;LOW&lt;/sub&gt;</td>
<td></td>
<td>4.7</td>
<td>µs</td>
</tr>
<tr>
<td>Hold time when SCLA0 = &quot;H&quot;</td>
<td>t&lt;sub&gt;HIGH&lt;/sub&gt;</td>
<td></td>
<td>4.0</td>
<td>µs</td>
</tr>
<tr>
<td>Data setup time (reception)</td>
<td>t&lt;sub&gt;LSU:DAT&lt;/sub&gt;</td>
<td></td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td>Data hold time (transmission)&lt;sup&gt;2&lt;/sup&gt;</td>
<td>t&lt;sub&gt;HDS:DAT&lt;/sub&gt;</td>
<td></td>
<td>0</td>
<td>3.45 µs</td>
</tr>
<tr>
<td>Setup time of stop condition</td>
<td>t&lt;sub&gt;SU:STO&lt;/sub&gt;</td>
<td></td>
<td>4.0</td>
<td>µs</td>
</tr>
<tr>
<td>Bus-free time</td>
<td>t&lt;sub&gt;BUF&lt;/sub&gt;</td>
<td></td>
<td>4.7</td>
<td>µs</td>
</tr>
</tbody>
</table>

#### Notes
1. The first clock pulse is generated after this period when the start/restart condition is detected.
2. The maximum value (MAX.) of t<sub>HDS:DAT</sub> is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

#### Remark
The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.

| Standard mode: | C<sub>b</sub> = 400 pF, R<sub>b</sub> = 2.7 kΩ |
### 2. I²C fast mode

(T<sub>A</sub> = −40 to +125°C, 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>HS (high-speed main) Mode</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCLA0 clock frequency</td>
<td>f&lt;sub&gt;SCL&lt;/sub&gt;</td>
<td>fast mode: f&lt;sub&gt;CLK&lt;/sub&gt; ≥ 3.5 MHz</td>
<td>MIN. 0 MAX. 400 kHz</td>
<td>kHz</td>
</tr>
<tr>
<td>Setup time of restart condition</td>
<td>t&lt;sub&gt;SU:STA&lt;/sub&gt;</td>
<td></td>
<td>MIN. 0.6 MAX. 1.3 µs</td>
<td>µs</td>
</tr>
<tr>
<td>Hold time&lt;sup&gt;1&lt;/sup&gt;</td>
<td>t&lt;sub&gt;HD:STA&lt;/sub&gt;</td>
<td></td>
<td>MIN. 0.6 MAX. 1.3 µs</td>
<td>µs</td>
</tr>
<tr>
<td>Hold time when SCLA0 = “L”</td>
<td>t&lt;sub&gt;LOW&lt;/sub&gt;</td>
<td></td>
<td>MIN. 1.3 µs</td>
<td>µs</td>
</tr>
<tr>
<td>Hold time when SCLA0 = “H”</td>
<td>t&lt;sub&gt;HIGH&lt;/sub&gt;</td>
<td></td>
<td>MIN. 0.6 µs</td>
<td>µs</td>
</tr>
<tr>
<td>Data setup time (reception)</td>
<td>t&lt;sub&gt;SU:DAT&lt;/sub&gt;</td>
<td></td>
<td>MIN. 100 ns</td>
<td>ns</td>
</tr>
<tr>
<td>Data hold time (transmission)&lt;sup&gt;2&lt;/sup&gt;</td>
<td>t&lt;sub&gt;HD:DAT&lt;/sub&gt;</td>
<td></td>
<td>MIN. 0 µs MAX. 0.9 µs</td>
<td>µs</td>
</tr>
<tr>
<td>Setup time of stop condition</td>
<td>t&lt;sub&gt;SU:STO&lt;/sub&gt;</td>
<td></td>
<td>MIN. 0.6 µs</td>
<td>µs</td>
</tr>
<tr>
<td>Bus-free time</td>
<td>t&lt;sub&gt;BUF&lt;/sub&gt;</td>
<td></td>
<td>MIN. 1.3 µs</td>
<td>µs</td>
</tr>
</tbody>
</table>

#### Notes
1. The first clock pulse is generated after this period when the start/restart condition is detected.
2. The maximum value (MAX.) of t<sub>HD:DAT</sub> is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

#### Remark
The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.

- **fast mode:** C<sub>b</sub> = 320 pF, R<sub>b</sub> = 1.1 kΩ

#### IIC serial transfer timing

![IIC serial transfer timing diagram](image-url)
3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

<table>
<thead>
<tr>
<th>Input channel</th>
<th>Reference Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ani0 to Ani2, Ani4 to Ani7</td>
<td>Reference voltage (+) = AVREFP</td>
</tr>
<tr>
<td></td>
<td>Reference voltage (-) = AVREFM</td>
</tr>
<tr>
<td></td>
<td>Reference voltage (-) = AVREFM</td>
</tr>
<tr>
<td>ANI16 to ANI19</td>
<td>See 3.6.1 (1).</td>
</tr>
<tr>
<td>Internal reference voltage</td>
<td>See 3.6.1 (1).</td>
</tr>
<tr>
<td>Temperature sensor output</td>
<td></td>
</tr>
<tr>
<td>voltage</td>
<td></td>
</tr>
</tbody>
</table>
(1) When reference voltage (+) = $AV_{REFP}/ANI0$ (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}/ANI1$ (ADREFM = 1), target ANI pin: ANI2, ANI4 to ANI7, internal reference voltage, and temperature sensor output voltage

($TA = -40 \text{ to } +125^\circ C$, $2.7 \text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM} = 0 \text{ V}$)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>RES</td>
<td></td>
<td>8</td>
<td>10</td>
<td></td>
<td>bit</td>
</tr>
<tr>
<td>Overall error Note 1</td>
<td>AINL</td>
<td>10-bit resolution $AV_{REFP} = V_{DD}$ Note 3</td>
<td></td>
<td>1.2</td>
<td>±3.5</td>
<td>LSB</td>
</tr>
<tr>
<td>Conversion time</td>
<td>$t_{CONV}$</td>
<td>10-bit resolution $AV_{REFP} = V_{DD}$ Note 3</td>
<td>3.6</td>
<td>2.125</td>
<td>39</td>
<td>$\mu$s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Target pin: ANI2, ANI4 to ANI7</td>
<td>2.7</td>
<td>3.4</td>
<td>39</td>
<td>$\mu$s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10-bit resolution $AV_{REFP} = V_{DD}$ Note 3</td>
<td>3.6</td>
<td>2.375</td>
<td>39</td>
<td>$\mu$s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)</td>
<td>2.7</td>
<td>3.8</td>
<td>39</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Zero-scale error Note 1, 2</td>
<td>$E_{ZS}$</td>
<td>10-bit resolution $AV_{REFP} = V_{DD}$ Note 3</td>
<td>±0.25</td>
<td>%FSR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full-scale error Note 1, 2</td>
<td>$E_{FS}$</td>
<td>10-bit resolution $AV_{REFP} = V_{DD}$ Note 3</td>
<td>±0.25</td>
<td>%FSR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Integral linearity error Note 1</td>
<td>ILE</td>
<td>10-bit resolution $AV_{REFP} = V_{DD}$ Note 3</td>
<td>±2.5</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential linearity error Note 1</td>
<td>DLE</td>
<td>10-bit resolution $AV_{REFP} = V_{DD}$ Note 3</td>
<td>±1.5</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog input voltage</td>
<td>$V_{AN}$</td>
<td>ANI2, ANI4 to ANI7</td>
<td>0</td>
<td>$AV_{REFP}$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Internal reference voltage (HS (high-speed main) mode)</td>
<td></td>
<td>$V_{BGR}$ Note 4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Temperature sensor output voltage (HS (high-speed main) mode)</td>
<td></td>
<td>$V_{TMPS25}$ Note 4</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

**Notes**

1. Excludes quantization error ($\pm 1/2$ LSB).
2. This value is indicated as a ratio (%FSR) to the full-scale value.
3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
   - Overall error: Add $\pm 1.0$ LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
   - Zero-scale error/Full-scale error: Add $\pm 0.05\%$FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
   - Integral linearity error/Differential linearity error: Add $\pm 0.5$ LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
4. See 3.6.2 Temperature sensor/internal reference voltage characteristics.
(2) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI16 to ANI19

(TA = −40 to +125°C, 2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (−) = AVREFM = 0 V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>RES</td>
<td>10-bit resolution</td>
<td>8</td>
<td>10</td>
<td></td>
<td>bit</td>
</tr>
<tr>
<td>Overall error Note 1</td>
<td>AINL</td>
<td>10-bit resolution VREFP = VDD Note 3</td>
<td></td>
<td>1.2</td>
<td>±5.0</td>
<td>LSB</td>
</tr>
<tr>
<td>Conversion time</td>
<td>tCONV</td>
<td>10-bit resolution Target ANI pin: ANI16 to ANI19</td>
<td>3.6 V ≤ VDD ≤ 5.5 V</td>
<td>2.125</td>
<td>39</td>
<td>μs</td>
</tr>
<tr>
<td>Full-scale error Notes 1, 2</td>
<td>EFS</td>
<td>10-bit resolution VREFP = VDD Note 3</td>
<td></td>
<td>±0.35</td>
<td>%FSR</td>
<td></td>
</tr>
<tr>
<td>Integral linearity error Note 1</td>
<td>ILE</td>
<td>10-bit resolution VREFP = VDD Note 3</td>
<td></td>
<td>±3.5</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>Differential linearity error Note 1</td>
<td>DLE</td>
<td>10-bit resolution VREFP = VDD Note 3</td>
<td></td>
<td>±2.0</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>Analog input voltage</td>
<td>VAIN</td>
<td>ANI16 to ANI19</td>
<td>0</td>
<td>AVREFP and VDD</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

Notes
1. Excludes quantization error (±1/2 LSB).
2. This value is indicated as a ratio (%FSR) to the full-scale value.
3. When AVREFP < VDD, the MAX. values are as follows.
   Overall error: Add ±4.0 LSB to the MAX. value when AVREFP = VDD.
   Zero-scale error/Full-scale error: Add ±0.2%FSR to the MAX. value when AVREFP = VDD.
   Integral linearity error/Differential linearity error: Add ±2.0 LSB to the MAX. value when AVREFP = VDD.
(3) When reference voltage (+) = VDD (ADREFP1 = 0, ADREFP0 = 0), reference voltage (−) = VSS (ADREFM = 0),
target pin: ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19, internal reference voltage, and temperature
sensor output voltage

\( (T_A = -40 \text{ to } +125^\circ C, 2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, V_{SS} = 0 \text{ V})\)
Reference voltage (+) = VDD, Reference voltage (−) = VSS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>RES</td>
<td>8</td>
<td>10</td>
<td>bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overall error(^{Note 1})</td>
<td>AINL</td>
<td>10-bit resolution</td>
<td>1.2</td>
<td>±7.0</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>Conversion time</td>
<td>(t_{CONV})</td>
<td>10-bit resolution</td>
<td>Min.</td>
<td>TYP.</td>
<td>Max.</td>
<td>Unit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V})</td>
<td>3.4</td>
<td>39</td>
<td>(\mu s)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Target pin: ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(3.6 \text{ V} \leq V_{DD} \leq 5.5 \text{ V})</td>
<td>2.125</td>
<td>39</td>
<td>(\mu s)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V})</td>
<td>3.4</td>
<td>39</td>
<td>(\mu s)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V})</td>
<td>2.375</td>
<td>39</td>
<td>(\mu s)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(3.6 \text{ V} \leq V_{DD} \leq 5.5 \text{ V})</td>
<td>3.8</td>
<td>39</td>
<td>(\mu s)</td>
<td></td>
</tr>
<tr>
<td>Zero-scale error(^{Notes 1, 2})</td>
<td>(E_{ZS})</td>
<td>10-bit resolution</td>
<td>±0.60</td>
<td>%FSR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full-scale error(^{Notes 1, 2})</td>
<td>(E_{FS})</td>
<td>10-bit resolution</td>
<td>±0.60</td>
<td>%FSR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Integral linearity error(^{Note 1})</td>
<td>ILE</td>
<td>10-bit resolution</td>
<td>±2.0</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential linearity error</td>
<td>DLE</td>
<td>10-bit resolution</td>
<td>±2.0</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog input voltage</td>
<td>(V_{AIN})</td>
<td>ANI0 to ANI2, ANI4 to ANI7</td>
<td>0</td>
<td>VDD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ANI16 to ANI19</td>
<td>0</td>
<td>VDD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Internal reference voltage (HS (high-speed main) mode)</td>
<td>(V_{BAIR})(^{Note 3})</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Temperature sensor output voltage (HS (high-speed main) mode)</td>
<td>(V_{TEMP})(^{Note 3})</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes**
1. Excludes quantization error (±1/2 LSB).
2. This value is indicated as a ratio (%FSR) to the full-scale value.
3. See 3.6.2 Temperature sensor/internal reference voltage characteristics.
(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage
(−) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI0, ANI2, ANI4 to ANI7, ANI16 to ANI19

(TA = −40 to +125°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = VBG, Reference voltage (−) =
AVREFM = 0 V, HS (high-speed main) mode)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>RES</td>
<td>8-bit resolution</td>
<td>8</td>
<td>17</td>
<td>39</td>
<td>μs</td>
</tr>
<tr>
<td>Conversion time</td>
<td>tCONV</td>
<td>8-bit resolution</td>
<td>17</td>
<td>39</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>Zero-scale error</td>
<td>EZS</td>
<td>8-bit resolution</td>
<td>±0.60</td>
<td></td>
<td>%FSR</td>
<td></td>
</tr>
<tr>
<td>Integral linearity error</td>
<td>ILE</td>
<td>8-bit resolution</td>
<td>±2.0</td>
<td></td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>Differential linearity error</td>
<td>DLE</td>
<td>8-bit resolution</td>
<td>±1.0</td>
<td></td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>Analog input voltage</td>
<td>VAIN</td>
<td></td>
<td>0</td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

Notes 1. Excludes quantization error (±1/2 LSB).
2. This value is indicated as a ratio (%FSR) to the full-scale value.
3. See 3.6.2 Temperature sensor/internal reference voltage characteristics.
4. When reference voltage (−) = VSS, the MAX. values are as follows.
   Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (−) = AVREFM.
   Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (−) = AVREFM.
   Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (−) = AVREFM.

3.6.2 Temperature sensor/internal reference voltage characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature sensor output voltage</td>
<td>VTMPS25</td>
<td>Setting ADS register = 80H, TA = +25°C</td>
<td>1.05</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Internal reference voltage</td>
<td>VBG</td>
<td>Setting ADS register = 81H</td>
<td>1.45</td>
<td>1.38</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>Temperature coefficient</td>
<td>FVTMP5</td>
<td>Temperature sensor that depends on the temperature</td>
<td>−3.6</td>
<td></td>
<td></td>
<td>mV/C</td>
</tr>
<tr>
<td>Operation stabilization wait time</td>
<td>tAMP</td>
<td></td>
<td>5</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
</tbody>
</table>
### 3.6.3 Programmable gain amplifier

\((T_A = -40 \text{ to } +125^\circ C, 2.7 \text{ V} \leq AVREFP = V_{DD} \leq 5.5 \text{ V}, V_{SS} = AVREFM = 0 \text{ V})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input offset voltage</td>
<td>(V_{IOPGA})</td>
<td>(\pm 5) (\pm 10) mV</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Input voltage range</td>
<td>(V_{IPGA})</td>
<td>0</td>
<td></td>
<td></td>
<td>(0.9V_{DD}/\text{gain})</td>
<td>V</td>
</tr>
<tr>
<td>Gain error(^1)</td>
<td></td>
<td>4, 8 times</td>
<td>(\pm 1)</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16 times</td>
<td>(\pm 1.5)</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>32 times</td>
<td>(\pm 2)</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Slew rate(^1)</td>
<td>(SR_{RPGA})</td>
<td>Rising edge 4.0 V (\leq V_{DD} \leq 5.5) V</td>
<td>4, 8 times</td>
<td>4</td>
<td></td>
<td>V/(\mu)s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16, 32 times</td>
<td>1.4</td>
<td></td>
<td></td>
<td>V/(\mu)s</td>
</tr>
<tr>
<td></td>
<td>(SR_{FPGA})</td>
<td>Falling edge 2.7 V (\leq V_{DD} &lt; 4.0) V</td>
<td>4, 8 times</td>
<td>1.8</td>
<td></td>
<td>V/(\mu)s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16, 32 times</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V/(\mu)s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V (\leq V_{DD} &lt; 4.0) V</td>
<td>4, 8 times</td>
<td>1.2</td>
<td></td>
<td>V/(\mu)s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16, 32 times</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V/(\mu)s</td>
</tr>
<tr>
<td>Operation stabilization wait time(^2)</td>
<td>(t_{PGA})</td>
<td>4, 8 times</td>
<td>5</td>
<td></td>
<td></td>
<td>(\mu)s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16, 32 times</td>
<td>10</td>
<td></td>
<td></td>
<td>(\mu)s</td>
</tr>
</tbody>
</table>

\(^1\) When \(V_{IPGA} = 0.1V_{DD}/\text{gain} \) to \(0.9V_{DD}/\text{gain}\).

\(^2\) Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

**Remark** These characteristics apply when \(AVREFM\) is selected as GND of the PGA by using the CVRVS1 bit.
### 3.6.4 Comparator

**Conditions:**
- $-40 \degree C \leq T_A \leq +125 \degree C$
- $2.7 \, V \leq AV_{REFP} = V_{DD} \leq 5.5 \, V$
- $V_{SS} = AV_{REFM} = 0 \, V$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input offset voltage</td>
<td>$V_{IOCMP}$</td>
<td>CMP0P to CMP5P</td>
<td>$\pm 5$</td>
<td>$\pm 40$</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Input voltage range</td>
<td>$V_{ICMP}$</td>
<td>CMP0P to CMP5P</td>
<td>0</td>
<td>$V_{DD}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Internal reference voltage deviation</td>
<td>$\Delta V_{REF}$</td>
<td>CmRVM register values: 7FH to 80H ($m = 0$ to 2)</td>
<td>$\pm 2$</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Other than above</td>
<td>$\pm 1$</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Response time</td>
<td>$t_{CR}, t_{CF}$</td>
<td>Input amplitude = $\pm 100 , mV$</td>
<td>70</td>
<td>150</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Operation stabilization wait time</td>
<td>$t_{CMP}$</td>
<td>$3.3 , V \leq V_{DD} \leq 5.5 , V$</td>
<td>1</td>
<td>$\mu s$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$2.7 , V \leq V_{DD} &lt; 3.3 , V$</td>
<td>3</td>
<td>$\mu s$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference voltage stabilization wait time</td>
<td>$t_{VR}$</td>
<td>CVRE: 0 to 1</td>
<td>10</td>
<td>$\mu s$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:***
1. Time required until a state is entered where the DC and AC specifications of the comparator are satisfied after the operation of the comparator has been enabled (CMPnEN bit = 1; $n = 0$ to 5)
2. Enable comparator output (CnOE bit = 1; $n = 0$ to 5) after enabling operation of the internal reference voltage generator (by setting the CVREm bit to 1; $m = 0$ to 2) and waiting for the operation stabilization time to elapse.

**Remark:** These characteristics apply when $AV_{REFP}$ is selected as the power supply source of the internal reference voltage by using the CVRVS0 bit, and when $AV_{REFM}$ is selected as GND of the internal reference voltage by using the CVRVS1 bit.

![Comparator Waveform](image_url)
3.6.5 POR circuit characteristics

\((T_A = -40 \text{ to } +125^\circ C, \ V_{SS} = 0 \ V)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detection voltage</td>
<td>(V_{POR})</td>
<td>Power supply rise time</td>
<td>1.45</td>
<td>1.51</td>
<td>1.62</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{POR})</td>
<td>Power supply fall time</td>
<td>1.44</td>
<td>1.50</td>
<td>1.61</td>
<td>V</td>
</tr>
<tr>
<td>Minimum pulse widthNote</td>
<td>(T_{PW})</td>
<td></td>
<td>300</td>
<td></td>
<td></td>
<td>(\mu s)</td>
</tr>
</tbody>
</table>

Note: Minimum time required for a POR reset when \(V_{DD}\) exceeds below \(V_{PDR}\). This is also the minimum time required for a POR reset from when \(V_{DD}\) exceeds below 0.7 \(V\) to when \(V_{DD}\) exceeds \(V_{POR}\) while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).

Supply voltage \((V_{DD})\)

\(V_{PDR}\) or 0.7 \(V\)

3.6.6 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

\((T_A = -40 \text{ to } +125^\circ C, \ V_{PDR} \leq \ V_{DD} \leq 5.5 \ V, \ V_{SS} = 0 \ V)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detection voltage</td>
<td>(V_{LVD0})</td>
<td>Power supply rise time</td>
<td>3.97</td>
<td>4.06</td>
<td>4.25</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{LVD0})</td>
<td>Power supply fall time</td>
<td>3.89</td>
<td>3.98</td>
<td>4.15</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{LVD1})</td>
<td>Power supply rise time</td>
<td>3.67</td>
<td>3.75</td>
<td>3.93</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{LVD1})</td>
<td>Power supply fall time</td>
<td>3.59</td>
<td>3.67</td>
<td>3.83</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{LVD2})</td>
<td>Power supply rise time</td>
<td>3.06</td>
<td>3.13</td>
<td>3.28</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{LVD2})</td>
<td>Power supply fall time</td>
<td>2.99</td>
<td>3.06</td>
<td>3.20</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{LVD3})</td>
<td>Power supply rise time</td>
<td>2.95</td>
<td>3.02</td>
<td>3.17</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{LVD3})</td>
<td>Power supply fall time</td>
<td>2.89</td>
<td>2.96</td>
<td>3.09</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{LVD4})</td>
<td>Power supply rise time</td>
<td>2.85</td>
<td>2.92</td>
<td>3.07</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{LVD4})</td>
<td>Power supply fall time</td>
<td>2.79</td>
<td>2.86</td>
<td>2.99</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{LVD5})</td>
<td>Power supply rise time</td>
<td>2.75</td>
<td>2.81</td>
<td>2.95</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{LVD5})</td>
<td>Power supply fall time</td>
<td>2.70</td>
<td>2.75</td>
<td>2.88</td>
<td>V</td>
</tr>
<tr>
<td>Minimum pulse width</td>
<td>(t_{LW})</td>
<td></td>
<td>300</td>
<td></td>
<td></td>
<td>(\mu s)</td>
</tr>
<tr>
<td>Detection delay time</td>
<td></td>
<td></td>
<td>300</td>
<td></td>
<td></td>
<td>(\mu s)</td>
</tr>
</tbody>
</table>
LVD Detection Voltage of Interrupt & Reset Mode

\((T_A = -40 \text{ to } +125^\circ C, \ V_{POR} \leq V_{DD} \leq 5.5 \ V, V_{SS} = 0 \ V)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupt and reset mode</td>
<td>(V_{LVO0})</td>
<td>(V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, ) falling reset voltage: 2.7 V</td>
<td>2.70</td>
<td>2.75</td>
<td>2.88</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{LVO1})</td>
<td>(LVIS1, LVIS0 = 1, 0) Rising release reset voltage</td>
<td>2.85</td>
<td>2.92</td>
<td>3.07</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Falling interrupt voltage</td>
<td>2.79</td>
<td>2.86</td>
<td>2.99</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{LVO2})</td>
<td>(LVIS1, LVIS0 = 0, 1) Rising release reset voltage</td>
<td>2.95</td>
<td>3.02</td>
<td>3.17</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Falling interrupt voltage</td>
<td>2.89</td>
<td>2.96</td>
<td>3.09</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{LVO3})</td>
<td>(LVIS1, LVIS0 = 0, 0) Rising release reset voltage</td>
<td>3.97</td>
<td>4.06</td>
<td>4.25</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Falling interrupt voltage</td>
<td>3.89</td>
<td>3.98</td>
<td>4.15</td>
<td>V</td>
</tr>
</tbody>
</table>

3.6.7 Supply voltage rise inclination characteristics

\((T_A = -40 \text{ to } +125^\circ C, V_{SS} = 0 \ V)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage rise</td>
<td>(SV_{DD})</td>
<td></td>
<td></td>
<td>54</td>
<td></td>
<td>V/ms</td>
</tr>
</tbody>
</table>

Caution  Keep the internal reset status by using the LVD circuit or an external reset signal until \(V_{DD}\) rises to within the operating voltage range shown in 33.4 AC Characteristics.

3.7 RAM Data Retention Characteristics

\((T_A = -40 \text{ to } +125^\circ C, V_{SS} = 0 \ V)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data retention supply voltage(\text{Note } 2)</td>
<td>(V_{DDDR})</td>
<td></td>
<td>1.47(\text{Note } 1)</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

Note  The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

Caution  When CPU is operated at the voltage of out of the operation voltage range, RAM data is not retained. Therefore, set STOP mode before the supplied voltage is below the operation voltage range.
3.8 Flash Memory Programming Characteristics

\((T_A = -40 \text{ to } +105^\circ\text{C}, 2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, V_{SS} = 0\text{ V})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU/peripheral hardware clock frequency</td>
<td>(f_{CLK})</td>
<td>(2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V})</td>
<td>1</td>
<td>32</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Number of code flash rewrites(^1, 2, 3)</td>
<td>(C_{\text{erw}})</td>
<td>Retained for 20 years, (T_A = 85^\circ\text{C})(^3, 4)</td>
<td>1,000</td>
<td></td>
<td></td>
<td>Times</td>
</tr>
<tr>
<td>Number of data flash rewrites(^1, 2, 3)</td>
<td></td>
<td>Retained for 1 year, (T_A = 25^\circ\text{C})(^3, 4)</td>
<td></td>
<td>1,000,000</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Retained for 5 years, (T_A = 85^\circ\text{C})(^3, 4)</td>
<td>100,000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Retained for 20 years, (T_A = 85^\circ\text{C})(^3, 4)</td>
<td>10,000</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes**
1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
2. When using flash memory programmer and Renesas Electronics self programming library
3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
4. These are the average temperature of during the retainment.

3.9 Dedicated Flash Memory Programmer Communication (UART)

\((T_A = -40 \text{ to } +105^\circ\text{C}, 2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, V_{SS} = 0\text{ V})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer rate</td>
<td></td>
<td>During serial programming</td>
<td>115.2 k</td>
<td>1 M</td>
<td></td>
<td>bps</td>
</tr>
</tbody>
</table>
3.10 Timing of Entry to Flash Memory Programming Modes

\[(T_A = -40 \text{ to } +125^\circ C, 2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, V_{SS} = 0 \text{ V})\]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>How long from when an external reset ends until the initial communication settings are specified</td>
<td>$t_{SUINIT}$</td>
<td>POR and LVD reset must end before the external reset ends.</td>
<td>100 ms</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>How long from when the TOOL0 pin is placed at the low level until an external reset ends</td>
<td>$t_{SU}$</td>
<td>POR and LVD reset must end before the external reset ends.</td>
<td>10 $\mu$s</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>How long the TOOL0 pin must be kept at the low level after a reset ends (except soft processing time)</td>
<td>$t_{HD}$</td>
<td>POR and LVD reset must end before the external reset ends.</td>
<td>1 ms</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- $t_{SUINIT}$: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.
- $t_{SU}$: How long from when the TOOL0 pin is placed at the low level until an external reset ends.
- $t_{HD}$: How long to keep the TOOL0 pin at the low level from when the external and internal resets end (except soft processing time).

Remark $t_{SUINIT}$: The low level is input to the TOOL0 pin.
$<1>$: The external reset ends (POR and LVD reset must end before the pin reset ends.).
$<2>$: The TOOL0 pin is set to the high level.
$<3>$: Complete the baud rate setting by UART reception.

Diagram: Timing of Entry to Flash Memory Programming Modes

- $t_{SU}$: How long from when the TOOL0 pin is placed at the low level until an external reset ends.
- $t_{SUINIT}$: How long from when an external reset ends until the initial communication settings are specified.
- 723 $\mu$s + processing time for setting mode.
- 1-byte data for setting mode.

Remark: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.
4. PACKAGE DRAWINGS

4.1 20-pin Products

R5F1076CGSP#V0, R5F1076CGSP#X0, R5F1076CMSP#V0, R5F1076CMSP#X0

<table>
<thead>
<tr>
<th>JEITA Package Code</th>
<th>RENESAS Code</th>
<th>Previous Code</th>
<th>MASS (TYP.) [g]</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-LSSOP20-4.4x6.5-0.65</td>
<td>PLSP0020JB-A</td>
<td>P20MA-65-NAA-1</td>
<td>0.1</td>
</tr>
</tbody>
</table>

NOTE
1. Dimensions “※1” and “※2” do not include mold flash.
2. Dimension “※3” does not include trim offset.

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4.2 30-pin Products

R5F107ACGSP#V0, R5F107AEGSP#V0, R5F107ACGSP#X0, R5F107AEGSP#X0, R5F107ACMSP#V0, R5F107ACMSP#X0, R5F107AEMSP#V0, R5F107ACMSP#X0, R5F107AEMSP#X0

<table>
<thead>
<tr>
<th>JEITA Package Code</th>
<th>RENESAS Code</th>
<th>Previous Code</th>
<th>MASS (TYP.) [g]</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-LSSOP30-0300-0.65</td>
<td>PLSP0030JB-B</td>
<td>S30MC-65-5A4-3</td>
<td>0.18</td>
</tr>
</tbody>
</table>

NOTE
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.
4.3 38-pin Products

R5F107DEGSP#V0, R5F107DEGSP#X0, R5F107DEMSP#V0, R5F107DEMSP#X0

<table>
<thead>
<tr>
<th>JEITA Package Code</th>
<th>RENESAS Code</th>
<th>Previous Code</th>
<th>MASS (TYP.) [g]</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-SSOP38-0300-0.65</td>
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NOTE
Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
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The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.
   Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.
   Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).

7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.
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(Rev.5.0-1 October 2020)

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