

RJU65F24DWA / RJU60F24DWS

650V - 50A - Fast Recovery Diode

Application: Inverter

R07DS1482EJ0201

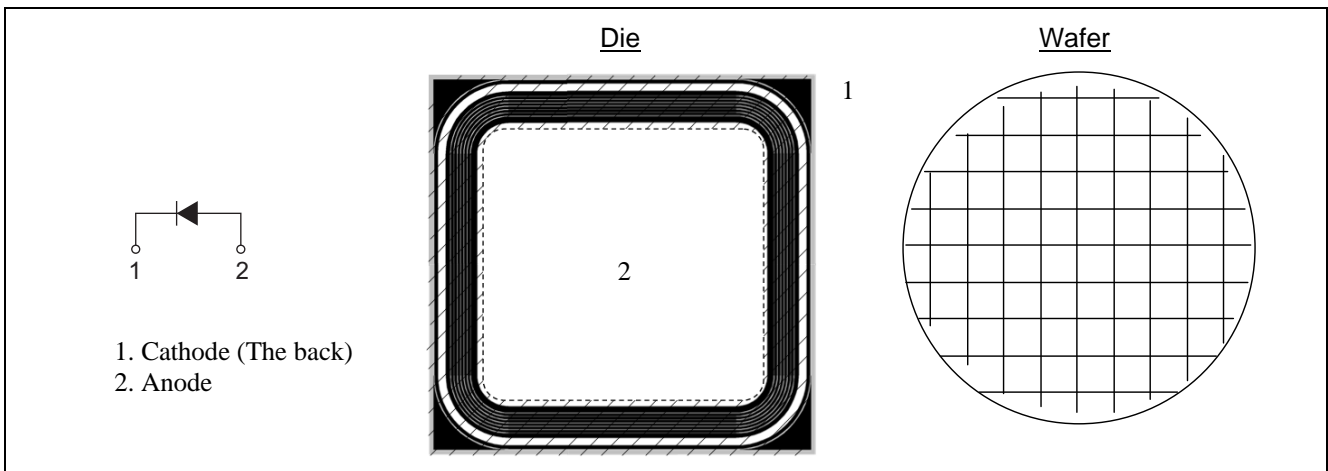
Rev.2.01

Apr.10.2020

Features

- Low forward voltage
 $V_F = 1.55 \text{ V typ. (at } I_F = 50 \text{ A, } T_c = 25^\circ\text{C)}$
- Fast recovery (soft recovery)
 $t_{rr} = 70 \text{ ns typ. (at } I_F = 50 \text{ A, } di/dt = 100 \text{ A}/\mu\text{s, } T_c = 25^\circ\text{C)}$

Outline



Absolute Maximum Ratings

($T_c = 25^\circ\text{C}$ unless otherwise noted)

Item	Symbol	Ratings	Unit	
Maximum reverse voltage	V_{RM}	650	V	
Forward current	$T_c = 25^\circ\text{C}$	I_F Notes1	100	A
	$T_c = 100^\circ\text{C}$	I_F Notes1	50	A
Junction temperature	T_j Notes2	175	$^\circ\text{C}$	

- Notes: 1. Depends on thermal properties of assembly.
 2. Please use this device in the thermal condition which the junction temperature does not exceed 175°C . IGBT Application Note is disclosed about reliability test and application condition up to $T_j = 175^\circ\text{C}$.
 3. Continuous heavy condition (e.g. high temperature/voltage/current or high variation of temperature) may affect a reliability even if it is within the absolute maximum ratings. Please consider derating condition for appropriate reliability in reference Renesas Semiconductor Reliability Handbook (Recommendation for Handling and Usage of Semiconductor Devices) and individual reliability data.

Electrical Characteristics (These data are an actual measurement value in a package.)

(Tc = 25°C unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Forward Voltage	V_F	—	1.55	2.0	V	$I_F = 50$ A Notes4, Notes5
Reverse current	I_R	—	—	2	μ A	$V_R = 650$ V Notes6
Reverse Recovery Time	t_{rr}	—	70	—	ns	$I_F = 50$ A, $di/dt = 100$ A/ μ s Notes5, Notes7

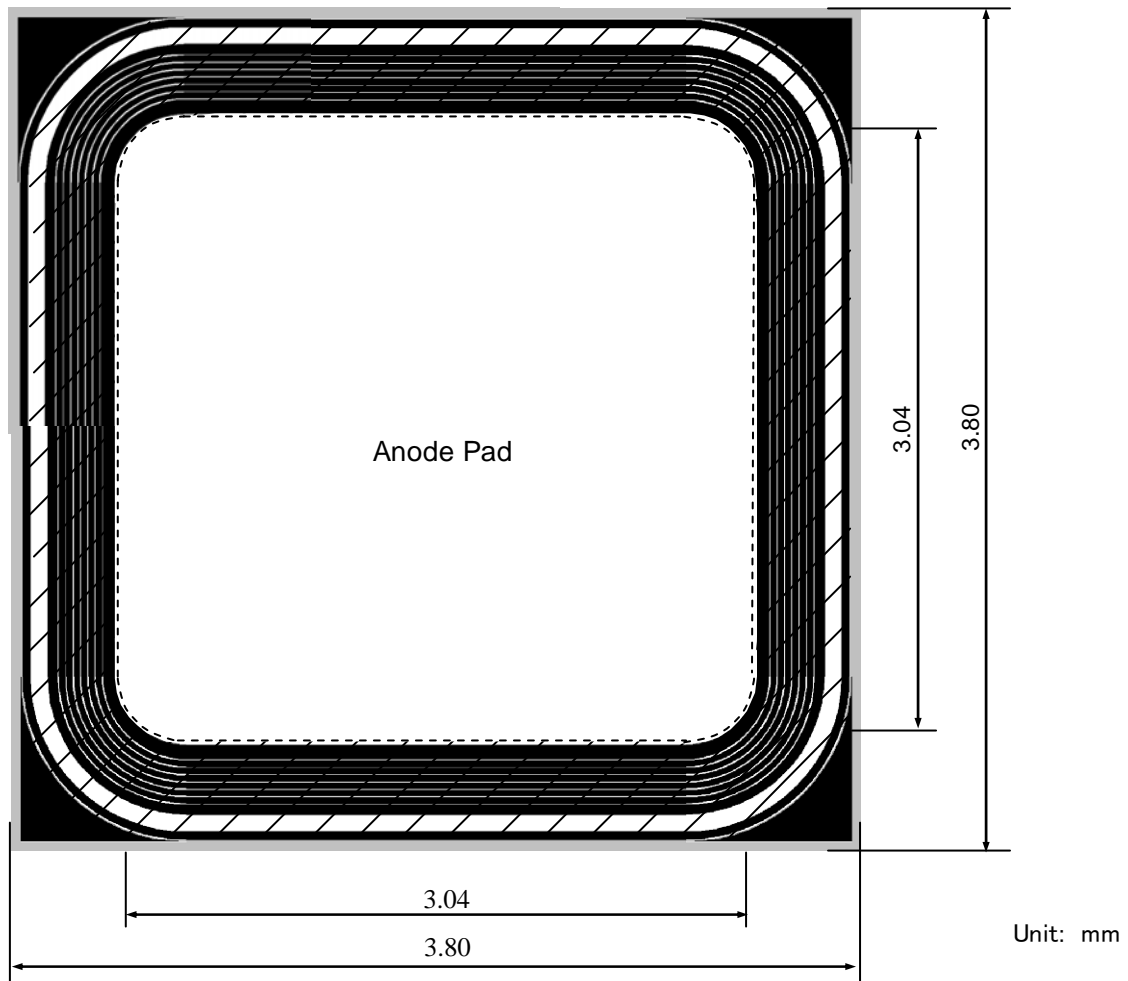
Notes: 4. Pulse test

5. Designed target value on Renesas measurement condition. (Not tested)

6. Tested on wafer

7. Tested to be mounted on Renesas single test vehicle.

Die Dimension



Note 1 :

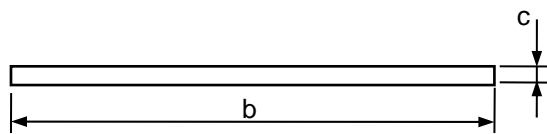
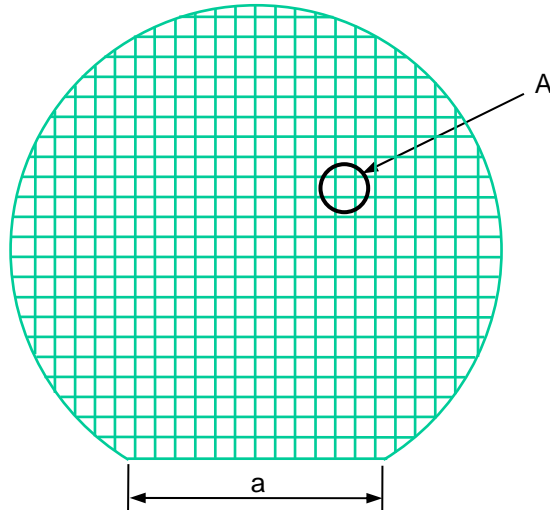
Illustration	Definition
Part of white	Al pattern
Part of dotted line	Bonding area
Part of hatching	Final passivation

Note 2 : The back of the chip is processed with Au evaporation.

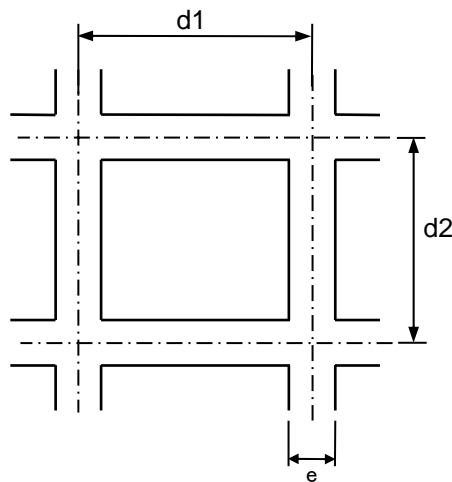
Note 3 : Recognition, target and any other patterns which are not related to FRD operation, may be changed without notice.

Wafer Dimension

Wafer dimension



A Enlargement



Item	Symbol	Dimensions (mm)
Orientation flat	a	(47.5)
Wafer diameter	b	150
Wafer thickness	c	0.07
Chip pitch	d1	3.80
	d2	3.80
Scribe grid	e	0.076

() : Reference

Ordering Information

Orderable Part Number	Shipment form
RJU65F24DWA-00#W0	Unsawn wafer
RJU65F24DWS-00#W0	Sawn wafer

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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