**RJK1056DPB**

100V, 25A, 14mΩ max.
Silicon N Channel Power MOS FET
Power Switching

**Features**
- High speed switching
- Low drive current
- Low on-resistance
  - \( R_{DS(\text{on})} = 11 \text{ mΩ typ. (at } V_{GS} = 10 \text{ V) } \)
- Pb-free
- Halogen-free
- High density mounting

**Outline**

RENESAS Package code: PTZZ0005DA-A
(Package name: LFPAK)

**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to source voltage</td>
<td>( V_{DSS} )</td>
<td>100</td>
<td>V</td>
</tr>
<tr>
<td>Gate to source voltage</td>
<td>( V_{GS} )</td>
<td>( \pm 20 )</td>
<td>V</td>
</tr>
<tr>
<td>Drain current</td>
<td>( I_D )</td>
<td>25</td>
<td>A</td>
</tr>
<tr>
<td>Drain peak current</td>
<td>( I_{D\text{(pulse)}} )</td>
<td>100</td>
<td>A</td>
</tr>
<tr>
<td>Body-drain diode reverse drain current</td>
<td>( I_{DR} )</td>
<td>25</td>
<td>A</td>
</tr>
<tr>
<td>Avalanche current</td>
<td>( I_{AP} )</td>
<td>25</td>
<td>A</td>
</tr>
<tr>
<td>Avalanche energy</td>
<td>( E_{AS} )</td>
<td>6.3</td>
<td>mJ</td>
</tr>
<tr>
<td>Channel dissipation</td>
<td>( P_{ch} )</td>
<td>65</td>
<td>W</td>
</tr>
<tr>
<td>Channel to Case Thermal Resistance</td>
<td>( \theta_{ch-C} )</td>
<td>1.92</td>
<td>°C/W</td>
</tr>
<tr>
<td>Channel temperature</td>
<td>( T_{ch} )</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>( T_{stg} )</td>
<td>–55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Notes:  
1. PW \( \leq 10 \) μs, duty cycle \( \leq 1\% \)
2. Value at L=10μH, \( T_{ch} = 25°C \), \( R_{g} \geq 50 \) Ω
3. \( T_c = 25°C \)
### Electrical Characteristics

(Ta = 25°C)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to source breakdown voltage</td>
<td>V_{BRDSS}</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>I_D = 10 mA, V_GS = 0 V</td>
</tr>
<tr>
<td>Gate to source leak current</td>
<td>I_{GSS}</td>
<td>—</td>
<td>—</td>
<td>±0.1</td>
<td>μA</td>
<td>V_{GS} = ±20 V, V_DS = 0 V</td>
</tr>
<tr>
<td>Zero gate voltage drain current</td>
<td>I_{DSS}</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>μA</td>
<td>V_{DS} = 100 V, V_GS = 0 V</td>
</tr>
<tr>
<td>Gate to source cutoff voltage</td>
<td>V_{GSOFF}</td>
<td>2.0</td>
<td>—</td>
<td>4.0</td>
<td>V</td>
<td>V_DS = 10 V, I_D = 1 mA</td>
</tr>
<tr>
<td>Static drain to source on state resistance</td>
<td>R_{DS(on)}</td>
<td>—</td>
<td>11</td>
<td>14</td>
<td>mΩ</td>
<td>I_D = 12.5 A, V_GS = 10 V</td>
</tr>
<tr>
<td>Forward transfer admittance</td>
<td></td>
<td>—</td>
<td>42</td>
<td>—</td>
<td>S</td>
<td>I_D = 12.5 A, V_DS = 10 V</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>C_{iss}</td>
<td>—</td>
<td>3000</td>
<td>—</td>
<td>pF</td>
<td>V_DS = 10 V, V_GS = 0 V, f = 1 MHz</td>
</tr>
<tr>
<td>Output capacitance</td>
<td></td>
<td>—</td>
<td>490</td>
<td>—</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Reverse transfer capacitance</td>
<td>C_{rss}</td>
<td>—</td>
<td>120</td>
<td>—</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Gate Resistance</td>
<td>R_g</td>
<td>—</td>
<td>0.5</td>
<td>—</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>Total gate charge</td>
<td>Q_g</td>
<td>—</td>
<td>41</td>
<td>—</td>
<td>nC</td>
<td>V_DD = 50 V, V_GS = 10 V, I_D = 25 A</td>
</tr>
<tr>
<td>Gate to source charge</td>
<td></td>
<td>—</td>
<td>13</td>
<td>—</td>
<td>nC</td>
<td></td>
</tr>
<tr>
<td>Gate to drain charge</td>
<td>Q_{gd}</td>
<td>—</td>
<td>7.5</td>
<td>—</td>
<td>nC</td>
<td></td>
</tr>
<tr>
<td>Turn-on delay time</td>
<td>t_{(on)}</td>
<td>—</td>
<td>16</td>
<td>—</td>
<td>ns</td>
<td>V_{GS} = 10 V, I_D = 12.5 A, V_DD ≥ 30 V, R_L = 2.4 Ω, R_g = 4.7 Ω</td>
</tr>
<tr>
<td>Rise time</td>
<td>t_r</td>
<td>—</td>
<td>4.5</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Turn-off delay time</td>
<td>t_{(off)}</td>
<td>—</td>
<td>36</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Fall time</td>
<td>t_f</td>
<td>—</td>
<td>6.5</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Body–drain diode forward voltage</td>
<td>V_{DF}</td>
<td>—</td>
<td>0.8</td>
<td>1.1</td>
<td>V</td>
<td>I_F = 25 A, V_GS = 0 V</td>
</tr>
<tr>
<td>Body–drain diode reverse recovery time</td>
<td>t_r</td>
<td>—</td>
<td>52</td>
<td>—</td>
<td>ns</td>
<td>I_F = 25 A, V_GS = 0 V, dI_F / dt = 100 A / μs</td>
</tr>
</tbody>
</table>

Notes: 4. Pulse test
Main Characteristics

Power vs. Temperature Derating

Maximum Safe Operation Area

Typical Output Characteristics

Typical Transfer Characteristics

Drain to Source Saturation Voltage vs. Gate to Source Voltage

Static Drain to Source on State Resistance vs. Drain Current
Static Drain to Source on State Resistance vs. Temperature

Dynamic Input Characteristics

Maximum Avalanche Energy vs. Channel Temperature Derating
Normalized Transient Thermal Impedance vs. Pulse Width

Avalanche Test Circuit

Avalanche Waveform

Switching Time Test Circuit

Switching Time Waveform

\[ E_{AS} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}} \]
Package Dimensions

<table>
<thead>
<tr>
<th>Package Name</th>
<th>JETTA Package Code</th>
<th>RENESAS Code</th>
<th>Previous Code</th>
<th>MASS (Typ.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPPAK</td>
<td>SC-105</td>
<td>P122005DA-A</td>
<td>LPPARV</td>
<td>0.080g</td>
</tr>
</tbody>
</table>

![Package Diagram]

(Ni/Pd/Au plating)

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Quantity</th>
<th>Shipping Container</th>
</tr>
</thead>
<tbody>
<tr>
<td>RJK1056DPB-00-J5</td>
<td>2500 pcs</td>
<td>Taping</td>
</tr>
</tbody>
</table>
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